

# Voltage Regulator - High Accuracy, Ultra Low Iq, Adjustable, Low Dropout

500 mA

## NCP3334

### Description

The NCP3334 is a high performance, low dropout regulator. With accuracy of  $\pm 0.9\%$  over line and load and ultra-low quiescent current and noise it encompasses all of the necessary features required by today's consumer electronics. This unique device is guaranteed to be stable without a minimum load current requirement and stable with any type of capacitor as small as 1.0  $\mu\text{F}$ . The NCP3334 offers reverse bias protection.

### Features

- High Accuracy Over Line and Load ( $\pm 0.9\%$  at  $25^\circ\text{C}$ )
- Ultra-Low Dropout Voltage
- Low Noise
- Low Shutdown Current (0.07  $\mu\text{A}$ )
- Reverse Bias Protected
- 2.6 V to 12 V Supply Range
- Thermal Shutdown Protection
- Current Limitation
- Requires Only 1.0  $\mu\text{F}$  Output Capacitance for Stability
- Stable with Any Type of Capacitor (including MLCC)
- No Minimum Output Current Required for Stability
- This is a Pb-Free Device

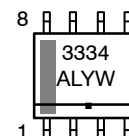
### Applications

- PCMCIA Card
- Cellular Phones
- Camcoders and Cameras
- Networking Systems, DSL/Cable Modems
- Cable Set-Top Box
- MP3/CD Players
- DSP Supply
- Displays and Monitors



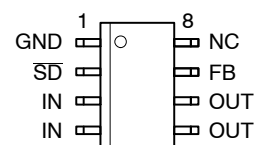
SOIC-8  
CASE 751

### MARKING DIAGRAM



- A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NOTE: Some of the device on this data sheet have been **DISCONTINUED**. Please refer to the table on page 7

# NCP3334

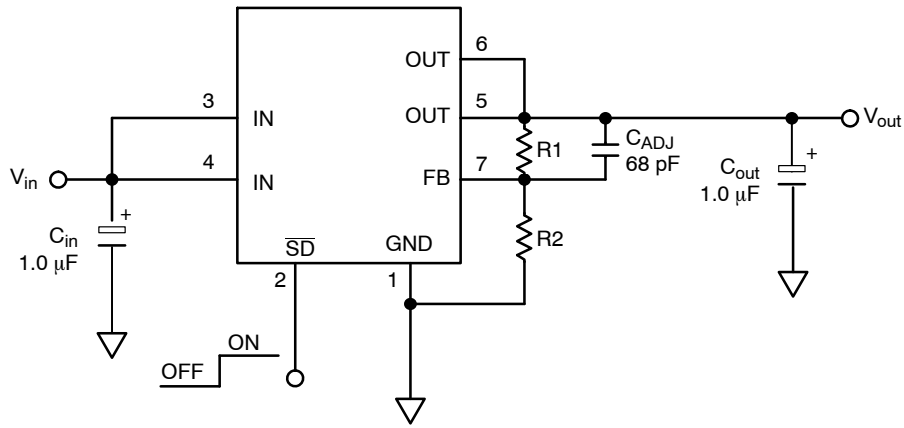


Figure 1. Typical Adjustable Version Application Schematic

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name        | Description                                                                   |
|---------|-----------------|-------------------------------------------------------------------------------|
| 1       | GND             | Power Supply Ground                                                           |
| 2       | $\overline{SD}$ | Shutdown pin. When not in use, this pin should be connected to the input pin. |
| 3, 4    | IN              | Power Supply Input Voltage                                                    |
| 5, 6    | OUT             | Regulated output voltage. Bypass to ground with $C_{out} \geq 1.0 \mu F$ .    |
| 7       | FB              | Feedback pin; reference voltage = 1.25 V.                                     |
| 8       | NC              | Not Connected                                                                 |

## MAXIMUM RATINGS

| Rating                                                         | Symbol          | Value                           | Unit |
|----------------------------------------------------------------|-----------------|---------------------------------|------|
| Input Voltage                                                  | $V_{in}$        | -0.3 to +16                     | V    |
| Output Voltage                                                 | $V_{out}$       | -0.3 to $V_{in} + 0.3$ or 10 V* | V    |
| Shutdown Pin Voltage                                           | $V_{sh}$        | -0.3 to +16                     | V    |
| Thermal Characteristics<br>Thermal Resistance, Junction-to-Air | $R_{\theta JA}$ | 238                             | °C/W |
| Operating Junction Temperature Range                           | $T_J$           | -40 to +150                     | °C   |
| Storage Temperature Range                                      | $T_{stg}$       | -50 to +150                     | °C   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) JESD 22-A114-B

Machine Model (MM) JESD 22-A115-A

\*Whichever is less. Reverse bias protection feature valid only if  $V_{out} - V_{in} \leq 7.0$  V.

# NCP3334

**ELECTRICAL CHARACTERISTICS** ( $V_{out} = 1.25\text{ V}$  ( $V_{ref}$ ) typical,  $V_{in} = 2.9\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted.)

| Characteristic                                                                                                                                                                                                                                                                  | Symbol                                               | Min            | Typ                                         | Max                                           | Unit                                            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|----------------|---------------------------------------------|-----------------------------------------------|-------------------------------------------------|
| Reference Voltage Accuracy<br>$V_{in} = 2.9\text{ V}$ to $V_{out} + 4.0\text{ V}$ , $I_L = 0.1\text{ mA}$ to $500\text{ mA}$ , $T_A = 25^\circ\text{C}$                                                                                                                         | $V_{REF}$                                            | -0.9%<br>1.239 | 1.25                                        | +0.9%<br>1.261                                | V                                               |
| Reference Voltage Accuracy<br>$V_{in} = 2.9\text{ V}$ to $V_{out} + 4.0\text{ V}$ , $I_L = 0.1\text{ mA}$ to $500\text{ mA}$ , $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$                                                                                                   | $V_{REF}$                                            | -1.4%<br>1.233 | 1.25                                        | +1.4%<br>1.268                                | V                                               |
| Reference Voltage Accuracy (Note 1)<br>$V_{in} = 2.9\text{ V}$ to $V_{out} + 4.0\text{ V}$ , $I_L = 0.1\text{ mA}$ to $500\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+150^\circ\text{C}$                                                                                       | $V_{REF}$                                            | -1.5%<br>1.231 | 1.25                                        | +1.5%<br>1.269                                | V                                               |
| Line Regulation<br>$V_{in} = 2.9\text{ V}$ to $12\text{ V}$ , $I_L = 0.1\text{ mA}$                                                                                                                                                                                             | $Line_{Reg}$                                         |                | 0.04                                        |                                               | mV/V                                            |
| Load Regulation<br>$V_{in} = 2.9\text{ V}$ , $I_L = 0.1\text{ mA}$ to $500\text{ mA}$                                                                                                                                                                                           | $Load_{Reg}$                                         |                | 0.04                                        |                                               | mV/mA                                           |
| Dropout Voltage, $V_{out} = 2.5\text{ V}$ to $10\text{ V}$<br>$I_L = 500\text{ mA}$ (Note 2)<br>$I_L = 300\text{ mA}$<br>$I_L = 50\text{ mA}$<br>$I_L = 0.1\text{ mA}$                                                                                                          | $V_{Drop}$                                           |                |                                             | 340<br>230<br>110<br>10                       | mV                                              |
| Peak Output Current (Notes 1 and 2) (See Figure 6)                                                                                                                                                                                                                              | $I_{pk}$                                             | 500            | 700                                         | 860                                           | mA                                              |
| Short Output Current (See Figure 6)<br>$V_{out} \leq 3.3\text{ V}$<br>$V_{out} > 3.3\text{ V}$                                                                                                                                                                                  | $I_{sc}$                                             |                | 990                                         | 900<br>1300                                   | mA                                              |
| Thermal Shutdown                                                                                                                                                                                                                                                                | $T_{JSD}$                                            |                | 160                                         |                                               | $^\circ\text{C}$                                |
| Ground Current<br>In Regulation<br>$I_L = 500\text{ mA}$ (Note 2)<br>$I_L = 300\text{ mA}$ (Note 2)<br>$I_L = 50\text{ mA}$<br>$I_L = 0.1\text{ mA}$<br><br>In Dropout<br>$V_{in} = V_{out} - 0.1\text{ V}$ , $I_L = 0.1\text{ mA}$<br><br>In Shutdown<br>$V_{SD} = 0\text{ V}$ | $I_{GND}$<br><br><br><br><br><br><br><br>$I_{GNDsh}$ |                | 9.0<br>4.6<br>0.8<br>–<br><br>–<br><br>0.07 | 14<br>7.5<br>2.5<br>190<br><br>500<br><br>1.0 | mA<br><br><br><br><br><br><br><br>$\mu\text{A}$ |
| Output Noise<br>$I_L = 500\text{ mA}$ , $f = 10\text{ Hz}$ to $100\text{ kHz}$ , $C_{out} = 10\text{ }\mu\text{F}$                                                                                                                                                              | $V_{noise}$                                          |                | 38                                          |                                               | $\mu\text{V}_{rms}$                             |
| Shutdown<br>Threshold Voltage ON<br>Threshold Voltage OFF                                                                                                                                                                                                                       | $V_{THSD}$                                           | 2.0            |                                             | 0.4                                           | V<br>V                                          |
| SD Input Current, $V_{SD} = 0\text{ V}$ to $0.4\text{ V}$ or $V_{SD} = 2.0\text{ V}$ to $V_{in}$<br>$V_{in} \leq 5.4\text{ V}$<br>$V_{in} > 5.4\text{ V}$                                                                                                                       | $I_{SD}$                                             |                | 0.07                                        | 1.0<br>5.0                                    | $\mu\text{A}$                                   |
| Output Current In Shutdown Mode, $V_{out} = 0\text{ V}$                                                                                                                                                                                                                         | $I_{OSD}$                                            |                | 0.07                                        | 1.0                                           | $\mu\text{A}$                                   |
| Reverse Bias Protection, Current Flowing from the Output Pin to GND<br>( $V_{in} = 0\text{ V}$ , $V_{out\_forced} = V_{out}(\text{nom}) \leq 7\text{ V}$ ) (Note 3)                                                                                                             | $I_{OUTR}$                                           |                | 1.0                                         |                                               | $\mu\text{A}$                                   |

## RECOMMENDED OPERATING CONDITIONS

|               |          |     |  |    |   |
|---------------|----------|-----|--|----|---|
| Input Voltage | $V_{IN}$ | 2.6 |  | 12 | V |
|---------------|----------|-----|--|----|---|

- For output current capability for  $T_J < 0^\circ\text{C}$ , please refer to Figure 8.
- $T_A$  must be greater than  $0^\circ\text{C}$ .
- Reverse bias protection feature valid only if  $V_{out} - V_{in} \leq 7.0\text{ V}$ .

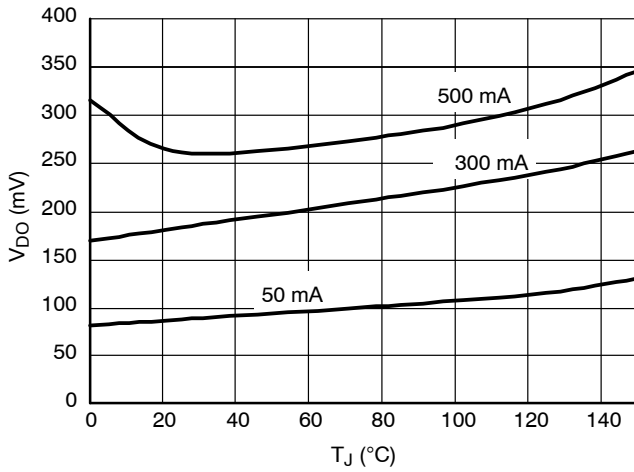


Figure 2. Dropout Voltage vs. Temperature

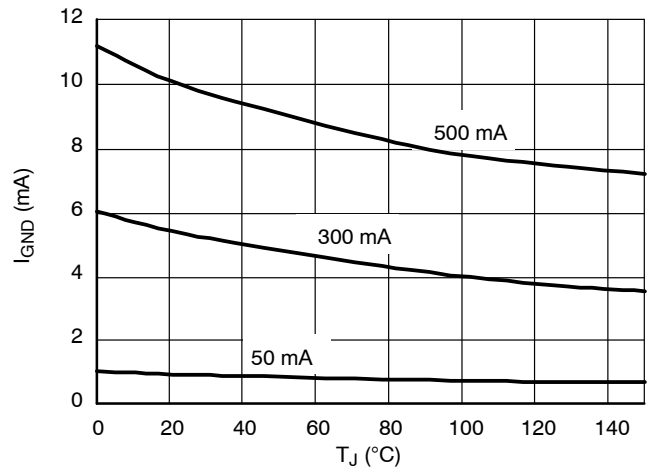


Figure 3. Ground Current vs. Temperature

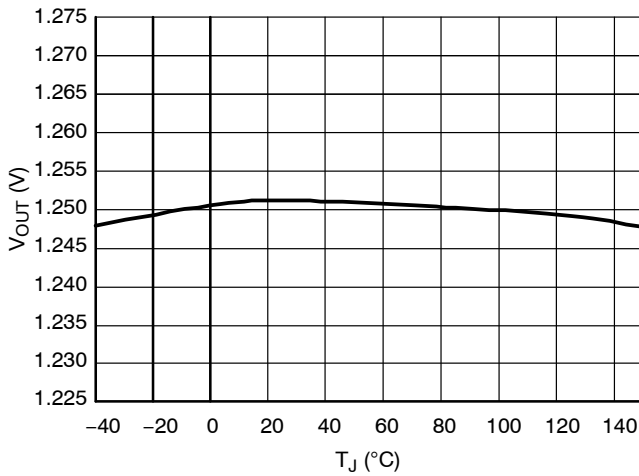


Figure 4. Output Voltage vs. Temperature

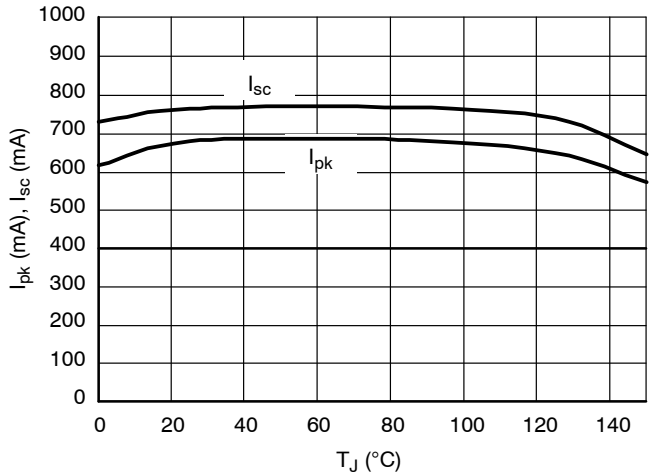


Figure 5. Peak and Short Current vs. Temperature

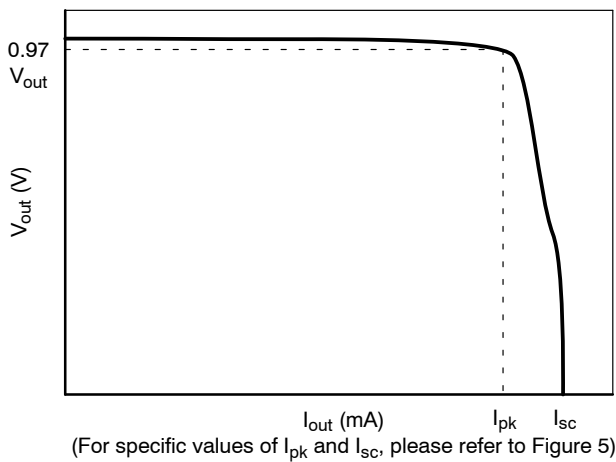


Figure 6. Output Voltage vs. Output Current

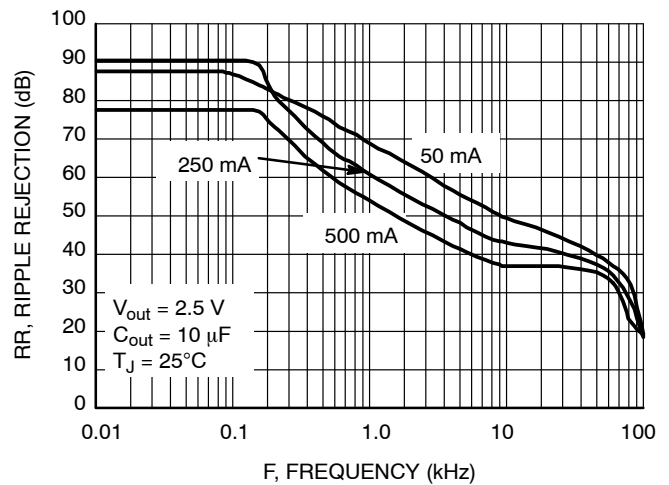
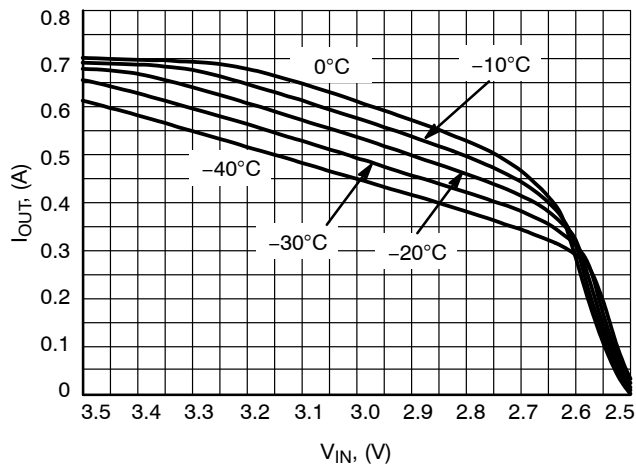
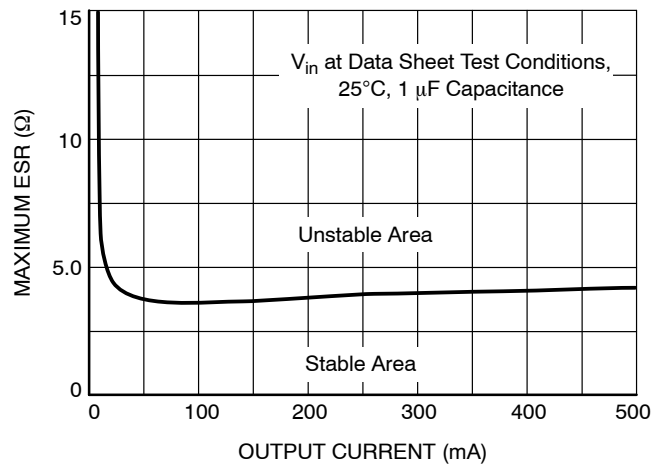


Figure 7. Ripple Rejection vs. Frequency



**Figure 8. Output Current Capability when set at 2.5 V  $V_{out}$**



**Figure 9. Stability with ESR vs.  $I_{out}$**

## APPLICATIONS INFORMATION

**Reverse Bias Protection**

Reverse bias is a condition caused when the input voltage goes to zero, but the output voltage is kept high either by a large output capacitor or another source in the application which feeds the output pin.

Normally in a bipolar LDO all the current will flow from the output pin to input pin through the PN junction with limited current capability and with the potential to destroy the IC.

Due to an improved architecture, the NCP3334 can withstand up to 7.0 V on the output pin with virtually no current flowing from output pin to input pin, and only negligible amount of current (tens of  $\mu\text{A}$ ) flowing from the output pin to ground for infinite duration.

Operation with output voltages in the range of 7 to 10 volts requires that the output to input voltage differential be less than 7 volts.

**Input Capacitor**

An input capacitor of at least 1.0  $\mu\text{F}$ , any type, is recommended to improve the transient response of the regulator and/or if the regulator is located more than a few inches from the power source. It will also reduce the circuit's sensitivity to the input line impedance at high frequencies. The capacitor should be mounted with the shortest possible track length directly across the regulator's input terminals.

**Output Capacitor**

The NCP3334 remains stable with any type of capacitor as long as it fulfills its 1.0  $\mu\text{F}$  requirement. There are no constraints on the minimum ESR and it will remain stable up to an ESR of 5.0  $\Omega$ . Larger capacitor values will improve the noise rejection and load transient response.

**Noise Reduction**

A 68 pF capacitor connected in parallel with R1 (see Figure 1) is recommended to reduce output noise and improve stability.

**Adjustable Operation**

The output voltage can be set by using a resistor divider as shown in Figure 1 with a range of 1.25 to 10 V. The appropriate resistor divider can be found by solving the equation below. The recommended current through the resistor divider is from 10  $\mu\text{A}$  to 100  $\mu\text{A}$ . This can be accomplished by selecting resistors in the  $\text{k}\Omega$  range. As result, the  $I_{\text{adj}} \cdot R_2$  becomes negligible in the equation and can be ignored.

$$V_{\text{out}} = 1.25 * \left(1 + \frac{R_1}{R_2}\right) + I_{\text{adj}} * R_2 \quad (\text{eq. 1})$$

Example:

For  $V_{\text{out}} = 2.9 \text{ V}$ , can use  $R_1 = 36 \text{ k}\Omega$  and  $R_2 = 27 \text{ k}\Omega$ .

$$1.25 * \left(1 + \frac{36 \text{ k}\Omega}{27 \text{ k}\Omega}\right) = 2.91 \text{ V} \quad (\text{eq. 2})$$

**Dropout Voltage**

The voltage dropout is measured at 97% of the nominal output voltage.

**Thermal Considerations**

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. This feature provides protection from a catastrophic device failure due to accidental overheating. This protection feature is not intended to be used as a substitute to heat sinking. The maximum power that can be dissipated, can be calculated with the equation below:

$$P_D = \frac{T_{J(\text{max})} - T_A}{R_{\theta JA}} \quad (\text{eq. 3})$$

For improved thermal performance, contact the factory for the DFN package option. The DFN package includes an exposed metal pad that is specifically designed to reduce the junction to air thermal resistance,  $R_{\theta JA}$ .

# NCP3334

## ORDERING INFORMATION

| Device         | Package           | Shipping†          |
|----------------|-------------------|--------------------|
| NCP3334DADJR2G | SO-8<br>(Pb-Free) | 2500 / Tape & Reel |

**Table 1. DISCONTINUED** (Note 4)

| Part Number  | Package           | Temperature Range |
|--------------|-------------------|-------------------|
| NCP3334DADJG | SO-8<br>(Pb-Free) | 98 Units / Rail   |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](http://www.onsemi.com).



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
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\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2                                                                                                                                                                         |

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**CASE 751-07**  
**ISSUE AK**

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|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

|                         |                    |                                                                                                                                                                                     |
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