

TERMINAL ASSIGNMENT

CMOS Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

High-Voltage Types (20-Volt Rating)

Features:

- Independence of power-supply sequence considerations— V_{CC} can exceed V_{DD} ; input signals can exceed both V_{CC} and V_{DD}
- Up and down level-shifting capability
- Shiftable input threshold for either CMOS or TTL compatibility
- Standardized symmetrical output characteristics
- 100% tested for quiescent current @ 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5 V, 10 V, and 15 V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

■ CD4504B hex voltage level-shifter consists of six circuits which shift input signals from the V_{CC} logic level to the V_{DD} logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the V_{CC} HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

The CD4504B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and MT suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

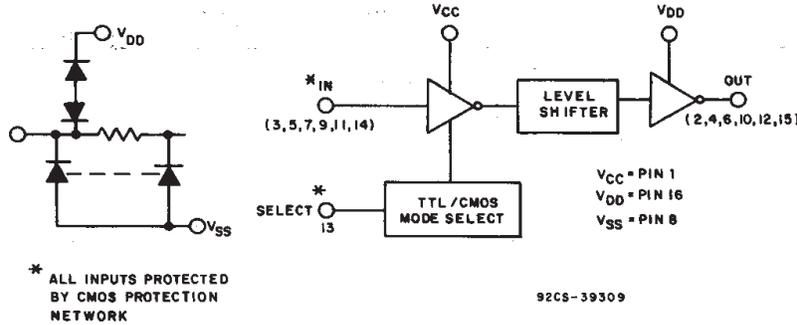


Fig. 1 - Functional diagram for CD4504B.

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|--|--|
| DC SUPPLY-VOLTAGE RANGE, (V_{DD}) | |
| Voltages referenced to V_{SS} Terminal | -0.5V to +20V |
| INPUT VOLTAGE RANGE, ALL INPUTS | |
| | -0.5V to $V_{CC} + 0.5V$ |
| DC INPUT CURRENT, ANY ONE INPUT | |
| | ± 10 mA |
| POWER DISSIPATION PER PACKAGE (P_D): | |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ | 500mW |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$: | Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR - | |
| FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T_A) | |
| | -55°C to $+125^\circ\text{C}$ |
| STORAGE TEMPERATURE RANGE (T_{stg}) | |
| | -85°C to $+150^\circ\text{C}$ |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max | +265°C |

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4504B Types

V_{GEN}

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS | |
|---|-----------------------|------------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|---|
| | V _O (V) | V _{IN} (V) | V _{CC} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | | |
| | | | | | | | | | MIN | TYP | MAX | | |
| Quiescent Device Current, I _{DD} Max and I _{CC} in CMOS-CMOS Mode | — | 0,5 | 5 | 5 | 1.5 | 1.5 | 1.5 | 1.5 | — | 0.02 | 1.5 | mA | |
| | — | 0,10 | 5 | 10 | 2 | 2 | 2 | 2 | — | 0.02 | 2 | | |
| | — | 0,15 | 5 | 15 | 4 | 4 | 120 | 120 | — | 0.02 | 4 | μA | |
| | — | 0,20 | 5 | 20 | 20 | 20 | 600 | 600 | — | 0.04 | 20 | | |
| Quiescent Device Current, I _{CC} Max TTL-CMOS Mode | — | 0,5 | 5 | 5 | 5 | 5 | 6 | 6 | — | 2.5 | 5 | mA | |
| | — | 0,10 | 5 | 10 | 5 | 5 | 6 | 6 | — | 2.5 | 5 | | |
| | — | 0,15 | 5 | 15 | 5 | 5 | 6 | 6 | — | 2.5 | 5 | | |
| Output Low (Sink) Current, I _{OL} Min | 0.4 | 0.5 | — | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | mA | |
| | 0.5 | 0,10 | — | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | | |
| | 1.5 | 0,15 | — | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | | |
| Output High (Source) Current, I _{OH} Min | 4.6 | 0,5 | — | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | mA | |
| | 2.5 | 0,5 | — | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | | |
| | 9.5 | 0,10 | — | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | | |
| | 13.5 | 0,15 | — | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | — | | |
| Output Voltage: Low-Level, V _{OL} Max | — | 0,5 | — | 5 | 0.05 | | | | — | 0 | 0.05 | V | |
| | — | 0,10 | — | 10 | 0.05 | | | | — | 0 | 0.05 | | |
| | — | 0,15 | — | 15 | 0.05 | | | | — | 0 | 0.05 | | |
| Output Voltage: High-Level, V _{OH} Min | — | 0,5 | — | 5 | 4.95 | | | | 4.95 | 5 | — | V | |
| | — | 0,10 | — | 10 | 9.95 | | | | 9.95 | 10 | — | | |
| | — | 0,15 | — | 15 | 14.95 | | | | 14.95 | 15 | — | | |
| Input Low Voltage, V _{IL} Max Note 1 | TTL-CMOS | 1 | — | 5 | 10 | 0.8 | | | | — | — | 0.8 | V |
| | TTL-CMOS | 1 | — | 5 | 15 | 0.8 | | | | — | — | 0.8 | |
| | CMOS-CMOS | 1 | — | 5 | 10 | 1.5 | | | | — | — | 1.5 | |
| | CMOS-CMOS | 1.5 | — | 5 | 15 | 1.5 | | | | — | — | 1.5 | |
| | CMOS-CMOS | 1.5 | — | 10 | 15 | 3 | | | | — | — | 3 | |
| Input High Voltage, V _{IH} Min Note 1 | TTL-CMOS | 9 | — | 5 | 10 | 2 | | | | 2 | — | — | V |
| | TTL-CMOS | 13.5 | — | 5 | 15 | 2 | | | | 2 | — | — | |
| | CMOS-CMOS | 9 | — | 5 | 10 | 3.5 | | | | 3.5 | — | — | |
| | CMOS-CMOS | 13.5 | — | 5 | 15 | 3.5 | | | | 3.5 | — | — | |
| | CMOS-CMOS | 13.5 | — | 10 | 15 | 7 | | | | 7 | — | — | |
| Input Current, I _{IN} Max | — | 0,18 | — | 18 | ±0.1 | ±0.1 | ±1 | ±1 | — | ±10 ⁻⁵ | ±0.1 | μA | |

Note 1: Applies to the 6 input signals. For mode control (P13), only the CMOS-CMOS ratings apply.

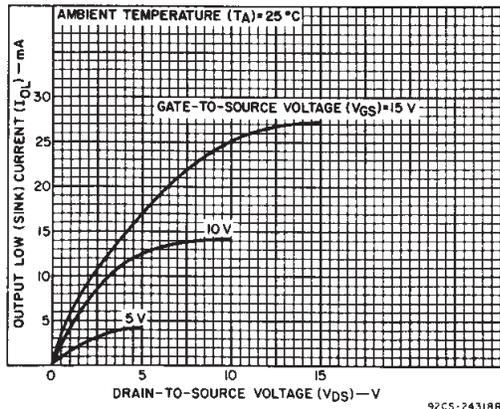


Fig. 2 - Typical output low (sink) current characteristics.

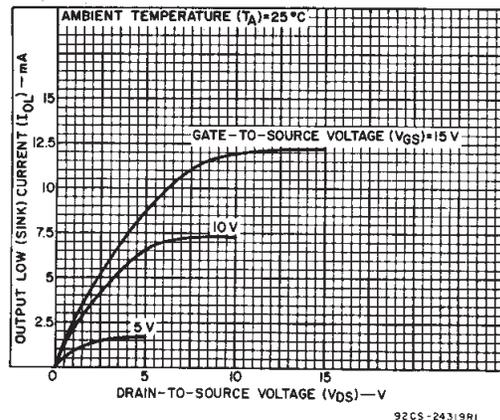
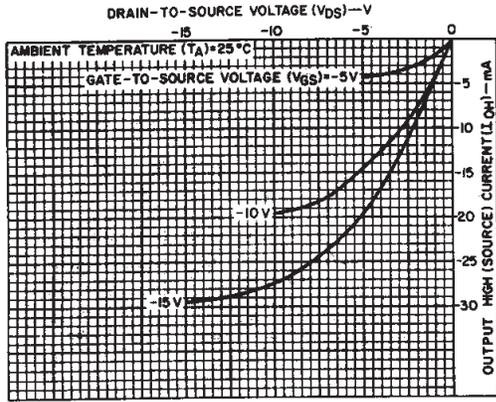


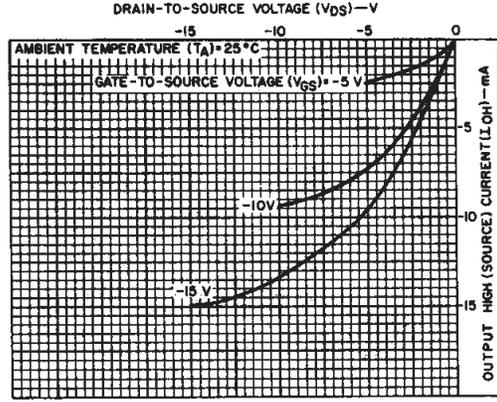
Fig. 3 - Minimum output low (sink) current characteristics.

CD4504B Types



92CS-24320R3

Fig. 4 - Typical output high (source) current characteristics.



92CS-24321R2

Fig. 5 - Minimum output high (source) current characteristics.

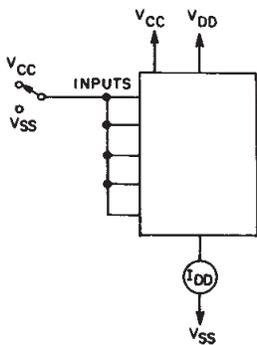
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V _{DD} (V) | LIMITS | | UNITS |
|--|---------------------|--------|------|-------|
| | | Min. | Max. | |
| Supply-Voltage Range (For T _A = Full Package-Temperature Range) | — | 5 | 18 | V |

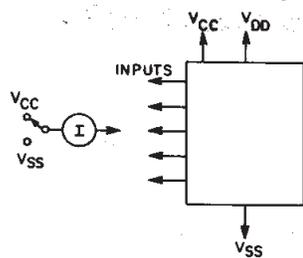
DYNAMIC ELECTRICAL CHARACTERISTICS, At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 Ω

| CHARACTERISTIC | SHIFTING MODE | V _{CC} (V) | V _{DD} (V) | LIMITS | | UNITS |
|--|---|---------------------|---------------------|--------|------|-------|
| | | | | TYP. | MAX. | |
| Propagation Delay: High-to-Low, t _{PHL} | TTL to CMOS V _{DD} > V _{CC} | 5 | 10 | 140 | 280 | ns |
| | CMOS to CMOS V _{DD} > V _{CC} | 5 | 15 | 140 | 280 | |
| | CMOS to CMOS V _{CC} > V _{DD} | 5 | 10 | 120 | 240 | |
| | | 5 | 15 | 120 | 240 | |
| | | 10 | 15 | 70 | 140 | |
| | | 10 | 5 | 275 | 550 | |
| | | 15 | 5 | 275 | 550 | |
| | | 15 | 10 | 70 | 140 | |
| Low-to-High, t _{PLH} | TTL to CMOS V _{DD} > V _{CC} | 5 | 10 | 140 | 280 | ns |
| | CMOS to CMOS V _{DD} > V _{CC} | 5 | 15 | 140 | 280 | |
| | CMOS to CMOS V _{CC} > V _{DD} | 5 | 10 | 120 | 240 | |
| | | 5 | 15 | 120 | 240 | |
| | | 10 | 15 | 70 | 140 | |
| | | 10 | 5 | 200 | 400 | |
| | | 15 | 5 | 200 | 400 | |
| | | 15 | 10 | 60 | 120 | |
| Transition Time, t _{THL} , t _{TLH} | All Modes | | 5 | 100 | 200 | ns |
| | | | 10 | 50 | 100 | |
| | | | 15 | 40 | 80 | |
| Input Capacitance, C _{IN} | Any Input | | | 5 | 7.5 | pF |



92CS-29452

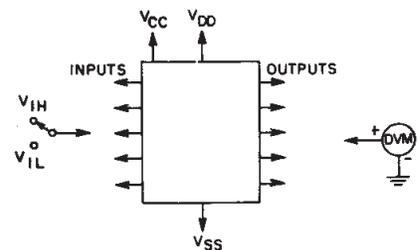
Fig. 6 - Quiescent device current.



92CS-29454

Fig. 7 - Input current.

NOTE:
MEASURE INPUTS
SEQUENTIALLY,
TO BOTH V_{DD} AND V_{VSS}.
CONNECT ALL UNUSED
INPUTS TO EITHER
V_{CC} OR V_{VSS}.



92CS-29453

Fig. 8 - Input voltage.

NOTE:
TEST ANY COMBINATION
OF INPUTS

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4504B Types

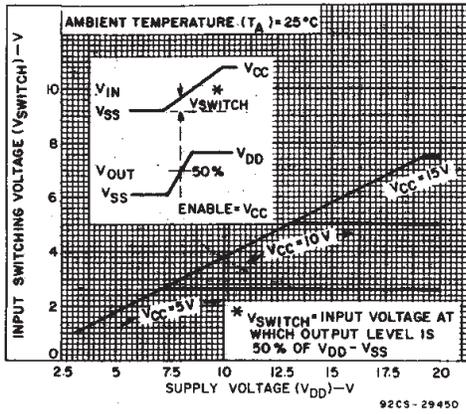


Fig. 9 - Typical input switching as a function of high-level supply voltage. (SELECT at V_{CC} -CMOS mode).

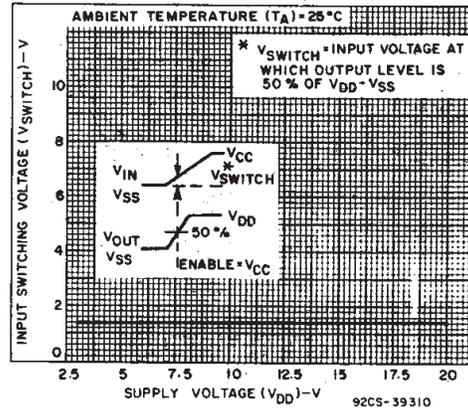


Fig. 10 - Typical input switching as a function of high-level supply voltage (SELECT at V_{SS} -TTL mode).

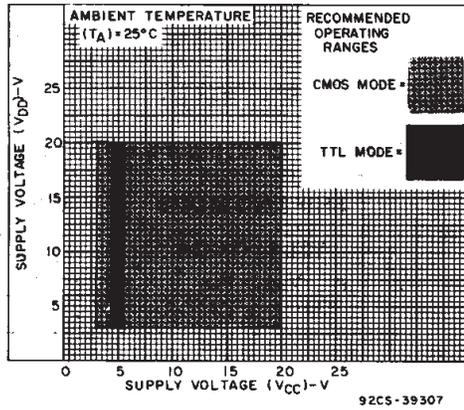
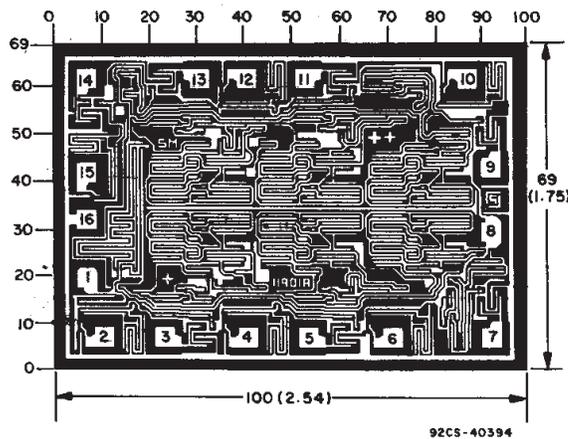


Fig. 11 - High-level supply voltage vs. low-level supply voltage.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD4504BH.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CD4504BE | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4504BE |
| CD4504BE.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4504BE |
| CD4504BEE4 | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4504BE |
| CD4504BF3A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4504BF3A |
| CD4504BF3A.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4504BF3A |
| CD4504BM | Active | Production | SOIC (D) 16 | 40 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4504BM |
| CD4504BM.A | Active | Production | SOIC (D) 16 | 40 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4504BM |
| CD4504BM96 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4504BM |
| CD4504BM96.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4504BM |
| CD4504BM96E4 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4504BM |
| CD4504BME4 | Active | Production | SOIC (D) 16 | 40 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4504BM |
| CD4504BMG4 | Active | Production | SOIC (D) 16 | 40 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4504BM |
| CD4504BMT | Active | Production | SOIC (D) 16 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4504BM |
| CD4504BMT.A | Active | Production | SOIC (D) 16 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4504BM |
| CD4504BPW | Active | Production | TSSOP (PW) 16 | 90 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM504B |
| CD4504BPW.A | Active | Production | TSSOP (PW) 16 | 90 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM504B |
| CD4504BPWE4 | Active | Production | TSSOP (PW) 16 | 90 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM504B |
| CD4504BPWR | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM504B |
| CD4504BPWR.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM504B |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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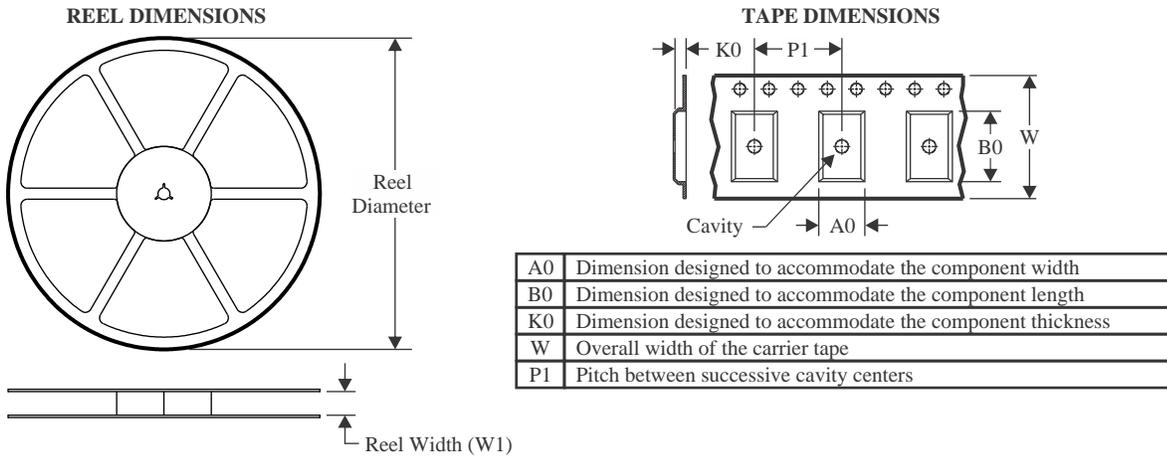
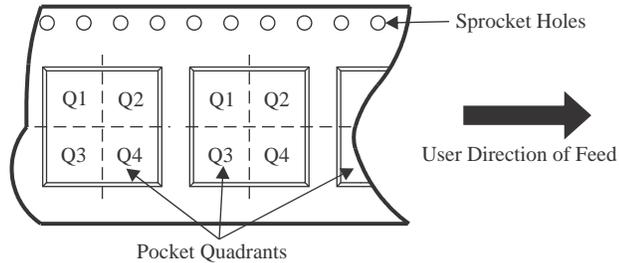
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OTHER QUALIFIED VERSIONS OF CD4504B, CD4504B-MIL :

- Catalog : [CD4504B](#)
- Enhanced Product : [CD4504B-EP](#), [CD4504B-EP](#)
- Military : [CD4504B-MIL](#)

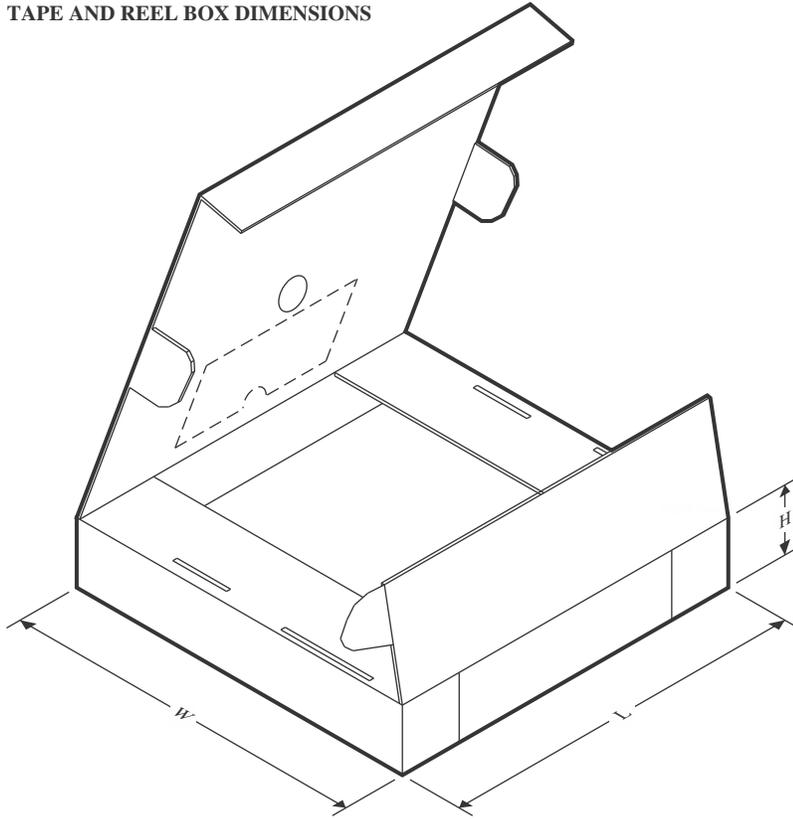
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


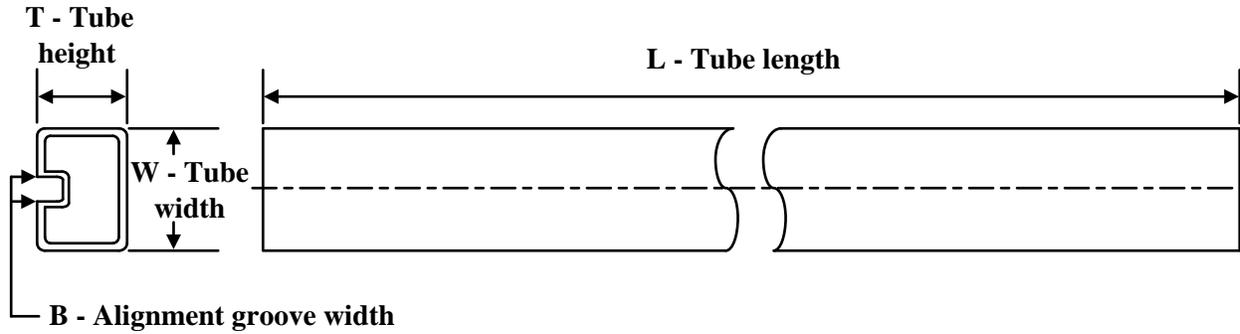
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4504BM96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4504BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4504BM96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD4504BPWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

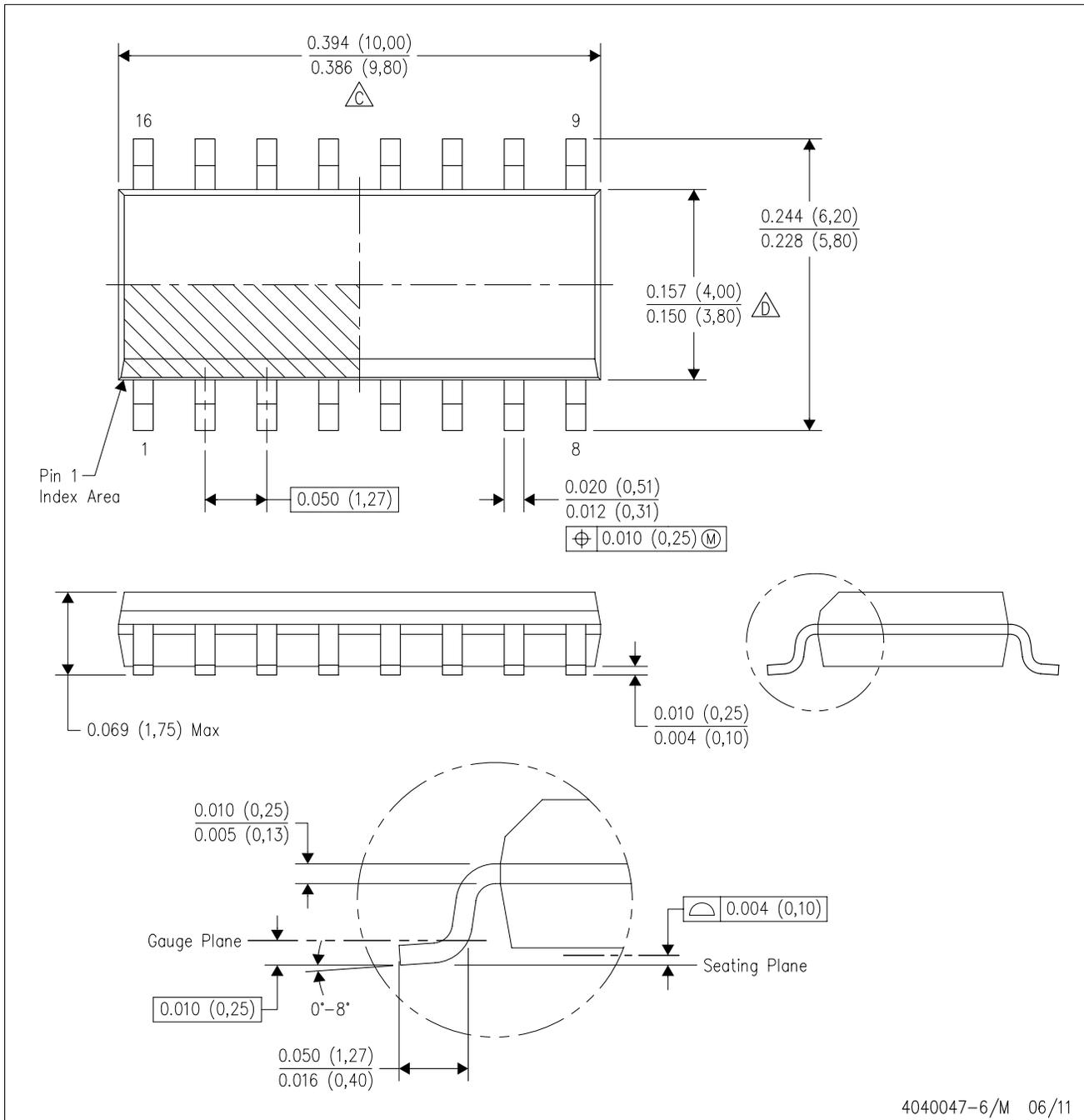
TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD4504BE | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4504BE | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4504BE.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4504BE.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4504BEE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4504BEE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4504BM | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| CD4504BM.A | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| CD4504BME4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| CD4504BMG4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| CD4504BPW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| CD4504BPW.A | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| CD4504BPWE4 | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |

D (R-PDSO-G16)

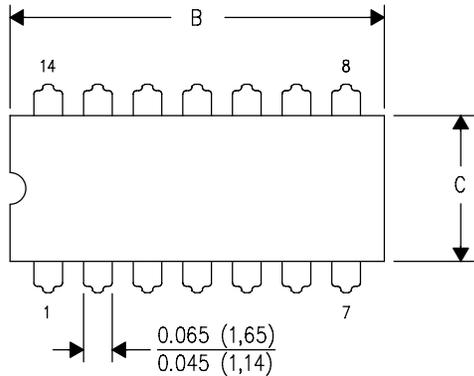
PLASTIC SMALL OUTLINE



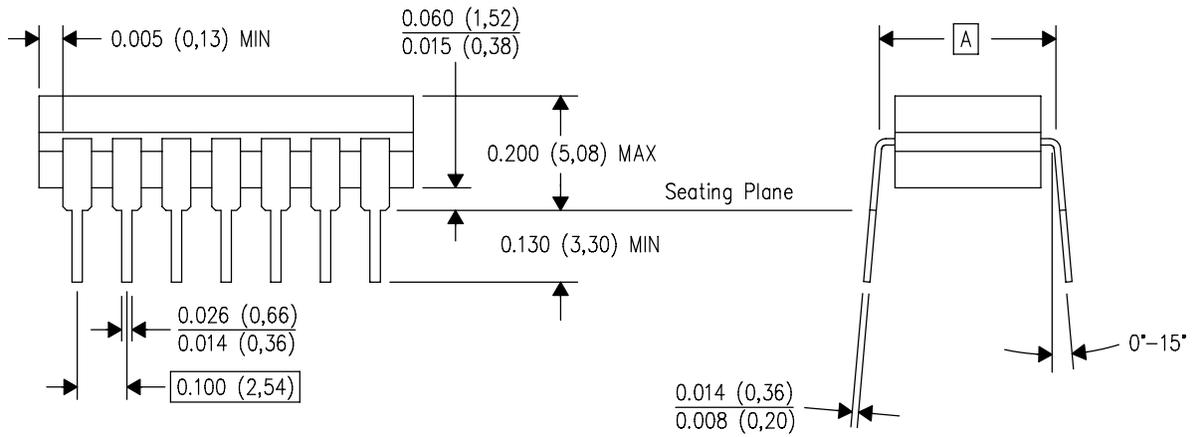
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

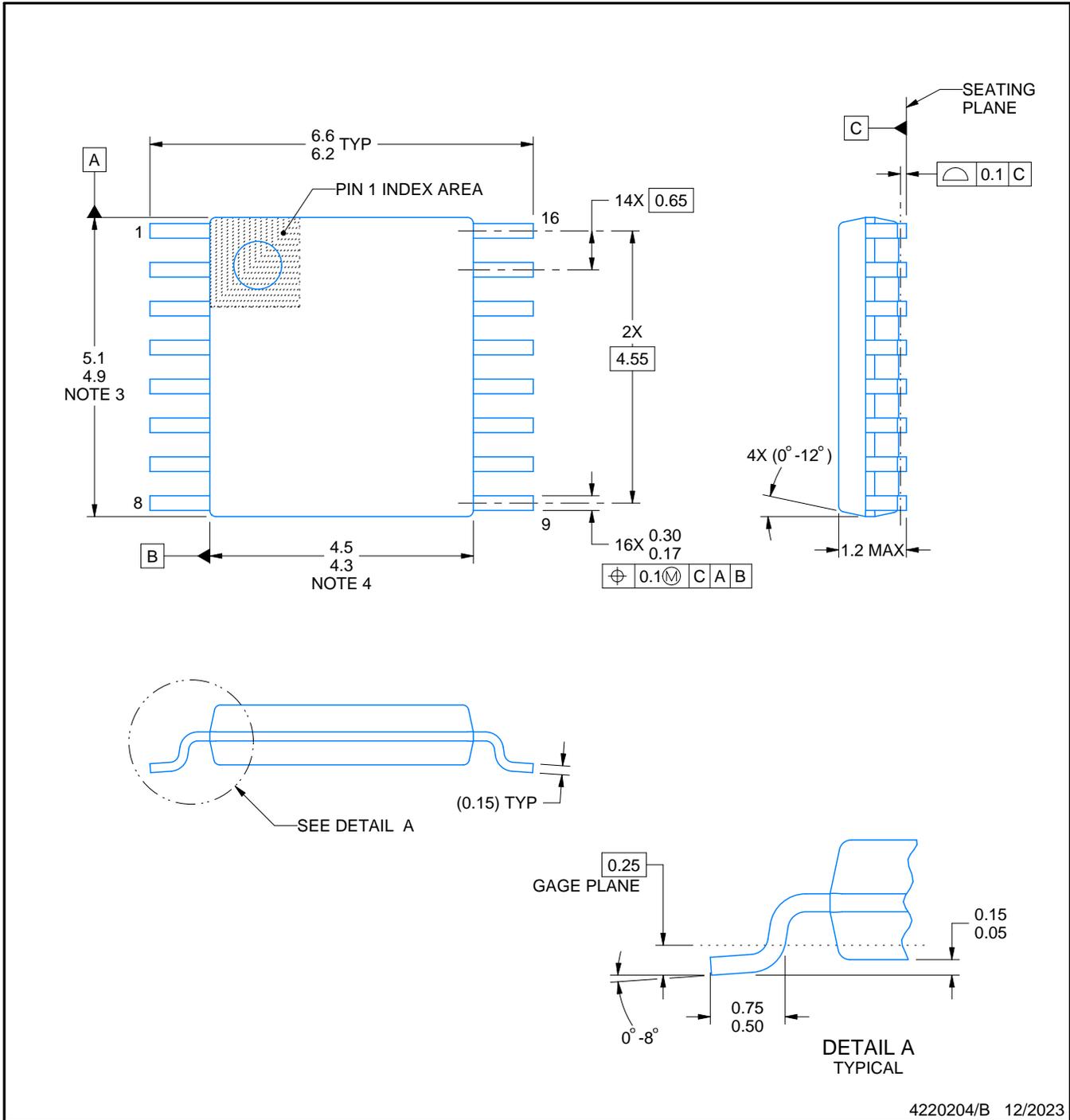


| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



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NOTES:

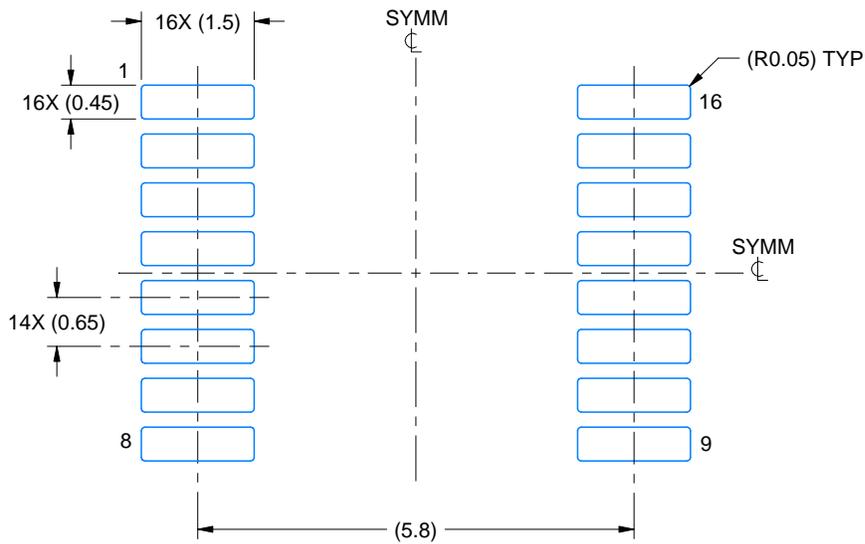
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

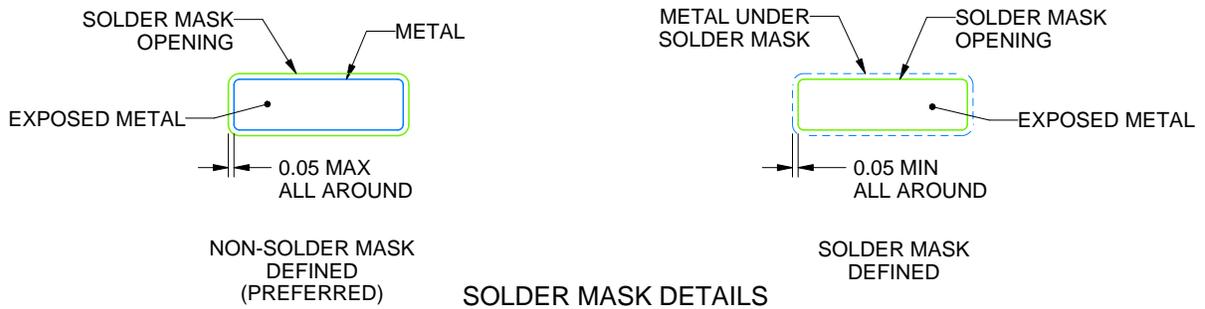
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

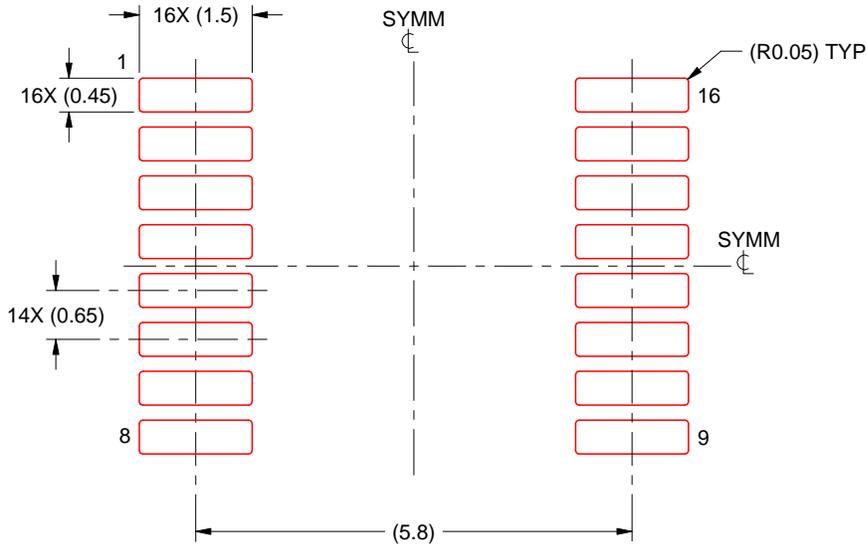
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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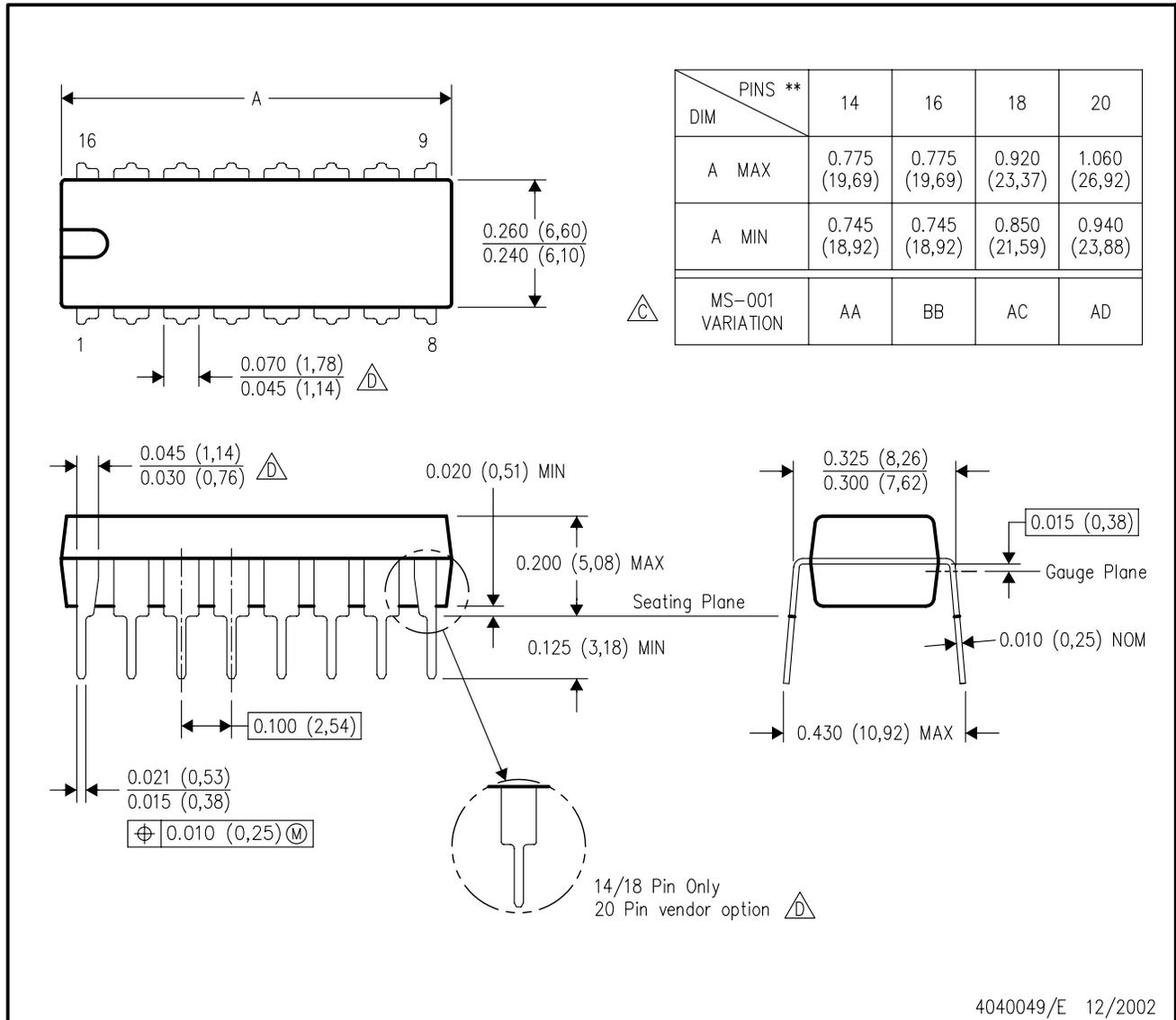
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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