CD74HC93, CD74HCT93 High-Speed CMOS Logic 4-Bit Binary Ripple Counter

1 Features

- Can be configured to divide by 2, 8, and 16
- Asynchronous reset
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range: – 55°C to 125°C
- Balances propagation delay and transition times
- Signigicant power reduction compared to LSTTL logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V (max), V_{IH} = 2 V (min)
  - CMOS input compatibility, $I_I \leq 1$ µA at V_{OL}, V_{OH}

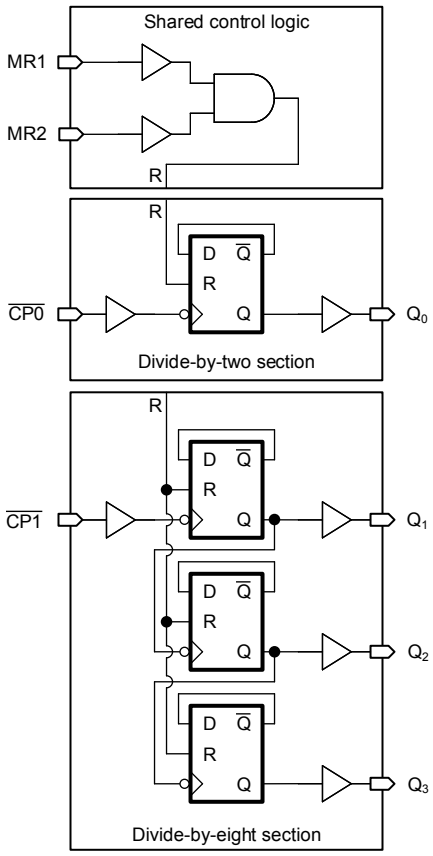
2 Description

The CD74HC93 and CD74HCT93 are high-speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL). These 4-bit binary ripple counters consist of four flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP0}$ and $\overline{CP1}$) to initiate state changes of the counter on the HIGH to LOW clock transition. State changes of the Q_n outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD74HC93M	SOIC (14)	8.65 mm × 3.90 mm
CD74HC93E	PDIP (14)	19.31 mm × 6.35 mm
CD74HCT93E	PDIP (14)	19.31 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

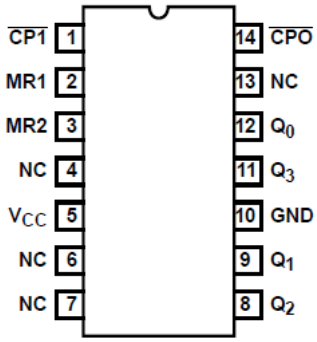
Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2003) to Revision D (March 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the doucment to reflect modern data sheet standards	1

4 Pin Configuration and Functions



N or D package
14-Pin PDIP or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input diode current(2)	(V_I < – 0.5 V or V_I > V_{CC} + 0.5 V)		±20	mA
I_{OK}	Output diode current(2)	(V_O < – 0.5 V or V_O > V_{CC} + 0.5 V)		±20	mA
I_O	Output source or sink current per output pin	(V_O > – 0.5 V or V_O < V_{CC} + 0.5 V)		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	HC types	2		6	V
		HCT types	4.5		5.5	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
t_t	Input transition rise/fall time	2 V			1000	ns
		4.5 V			500	
		6 V			400	
T_A	Operating free-air temperature		– 55		125	°C

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 14 PINS	N (PDIP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	86	80	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS(1)	V_{CC} (V)	T_A = 25°C			– 40°C to 85°C		– 55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	V
V_{OH}	High-level output voltage	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		V
		I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		V
V_{OL}	Low-level output voltage	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1		10.1		0.1	V
		I_{OL} = 20 µA	6			0.1		0.1		0.1	V
		I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} or GND	6			±0.1		±1		±1	nA
I_{CC}	Supply current	V_{CC} or GND	6			8		80		160	µA
I_{CC}	Supply-current change	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}	5.5		1.4	2.4		2.9			mA
C_i	Input capacitance		4.5 to 5.5		3	10		10			pF
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level Output Voltage	I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
		I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
V_{OL}	Low level output voltage	I_{OH} = 20 µA	4.5			0.1		0.1		0.1	V
		I_{OH} = 4 mA	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} or GND	5.5			±0.1		±1		±1	µA
I_{CC}	Supply current	V_{CC} or GND	5.5			8		80		160	µA
ΔI_{CC} (2) (3)	Additional supply current per input pin	$\overline{CP0}$,$\overline{CP1}$	4.5 to 5.5		100	216		270		294	µA
		CLR1, CLR2	4.5 to 5.5		100	144		180		196	µA

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.
(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specifications is 1.8 mA.
(3) Inputs held at V_{CC} – 2.1.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V_{CC} (V)	25°C		– 40°C to 85°C		– 55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
f_{MAX}	Maximum clock frequency	2	6		5		4		MHz
		4.5	30		24		20		MHz
		6	35		28		24		MHz
t_W	Clock pulse width $\overline{CP0}$, $\overline{CP1}$	2	80		100		120		ns
		4.5	16		20		24		ns
		6	14		17		20		ns
t_w	Reset pulse width	2	80		100		120		ns
		4.5	16		20		24		ns
		6	14		17		20		ns
t_{REM}	Reset removal time	2	50		65		75		ns
		4.5	10		13		15		ns
		6	9		11		13		ns
HCT TYPES									
f_{MAX}	Maximum clock frequency	4.5	30		24		20		MHz
t_W	Clock pulse width $\overline{CP0}$, $\overline{CP1}$	4.5	16		20		24		ns
t_W	Reset pulse width	4.5	16		20		24		ns
t_{REM}	Reset removal time	4.5	10		13		15		ns

5.6 Switching Characteristics

Input t_r, t_f = 6ns. C_L = 50pF unless otherwise noted

PARAMETER		V_{CC} (V)	25°C			– 40°C to 85°C		– 55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t_{PLH}, t_{PHL}	$\overline{CP0}$ to Q0	2			125		155		190	ns
		4.5		10[1]	25		31		38	ns
		6			21		26		32	ns
t_{PLH}, t_{PHL}	$\overline{CP1}$ to Q1	2			135		170		205	ns
		4.5			27		34		41	ns
		6			23		29		35	ns
t_{PLH}, t_{PHL}	$\overline{CP1}$ to Q2	2			185		230		280	ns
		4.5			37		46		56	ns
		6			31		39		48	ns
t_{PLH}, t_{PHL}	$\overline{CP1}$ to Q3	2			245		305		370	ns
		4.5		21[1]	49		61		74	ns
		6			42		52		63	ns
t_{PLH}, t_{PHL}	MR1, MR2 to Qn	2			155		195		235	ns
		4.5		13[1]	31		39		47	ns
		6			26		33		40	ns
t_{TLH}, t_{THL}	Output transition time	2			75		95		110	ns
		4.5			15		19		22	ns
		6			13		16		19	ns
C_{IN}	Input capacitance				10		10		10	pF

5.6 Switching Characteristics (continued)

Input t_r, t_f = 6ns. C_L = 50pF unless otherwise noted

PARAMETER		V_{CC} (V)	25°C			– 40°C to 85°C		– 55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C_{PD}	Power dissipation capacitance			25			10		19	pF
HCT TYPES										
t_{PLH}, t_{PHL}	$\overline{CP0}$ to Q0	4.5		14[1]	34		43		51	ns
t_{PLH}, t_{PHL}	$\overline{CP1}$ to Q1	4.5			34		43		51	ns
t_{PLH}, t_{PHL}	$\overline{CP1}$ to Q2	4.5			46		58		69	ns
t_{PLH}, t_{PHL}	$\overline{CP1}$ to Q3	4.5		24[1]	58		73		87	ns
t_{PLH}, t_{PHL}	MR1, MR2 to Qn	4.5		13[1]	33		41		50	ns
t_{TLH}, t_{THL}	Output Transition time	4.5			15		19		22	ns
C_{IN}	Input Capacitance				10		10		10	pF
C_{PD}	Power dissipation capacitance			25						pF

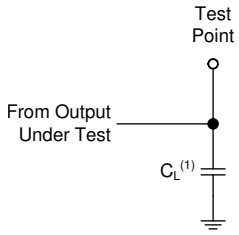
(1) C_L = 15pF. V_{CC} = 5.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

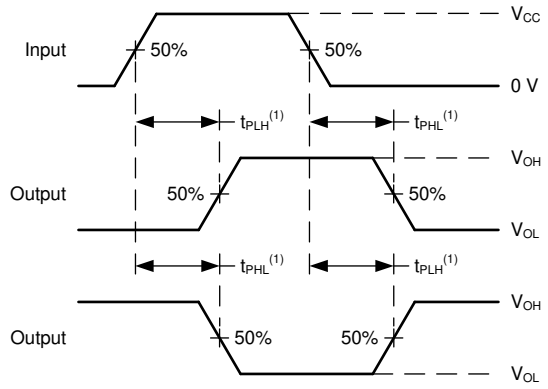
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



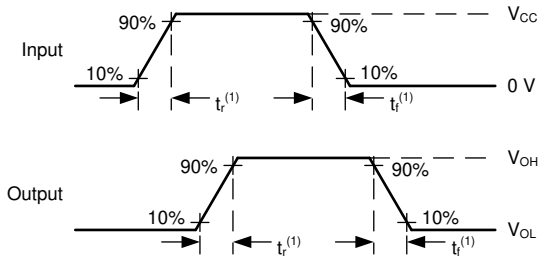
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



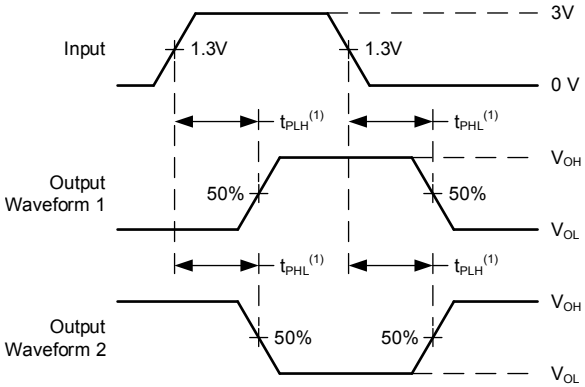
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

7.1 Overview

The CD74HC93 and CD74HCT93 are high-speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL). These 4-bit binary ripple counters consist of four flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP0}$ and $\overline{CP1}$) to initiate state changes of the counter on the HIGH to LOW clock transition. State changes of the Q_n outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous reset (MR1 and MR2) is provided which overrides both clocks and resets (clears) all flip-flops.

Because the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

In a 4-bit ripple counter the output Q0 must be connected externally to input $\overline{CP1}$. The input count pulses are applied to clock input $\overline{CP0}$. Simultaneous frequency divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP1}$.

Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, Q_3 outputs. Independent use of the first flipflop is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

7.2 Functional Block Diagram

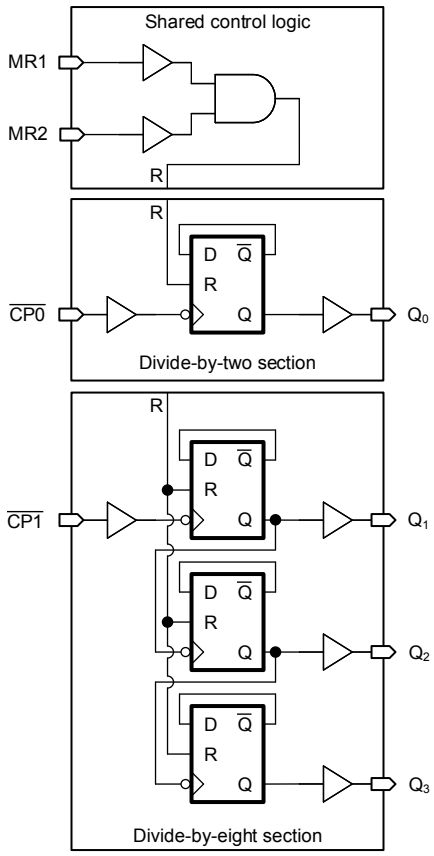


Figure 7-1. Functional Block Diagram

7.3 Device Functional Modes

Truth Table

COUNT	OUTPUTS(1)			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

(1) H = High voltage level, L = Low voltage level.

Table 7-1. Mode Selection

RESET OUTPUTS		OUTPUTS(1)			
MR1	MR2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count	Count	Count	Count
H	L				
L	L				

(1) H = High voltage level, L = Low voltage level.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC93E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC93E
CD74HC93E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC93E
CD74HC93EE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC93E
CD74HC93M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC93M
CD74HC93M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC93M
CD74HC93M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC93M
CD74HC93MT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC93M
CD74HCT93E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT93E
CD74HCT93E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT93E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

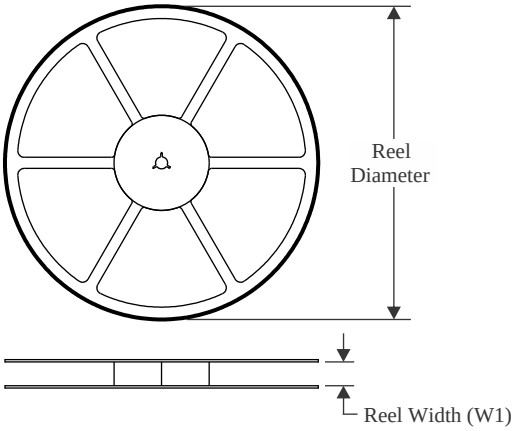
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

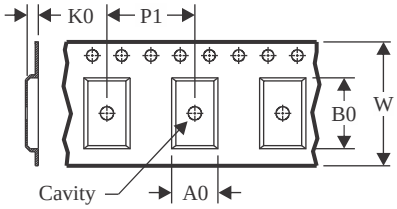
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

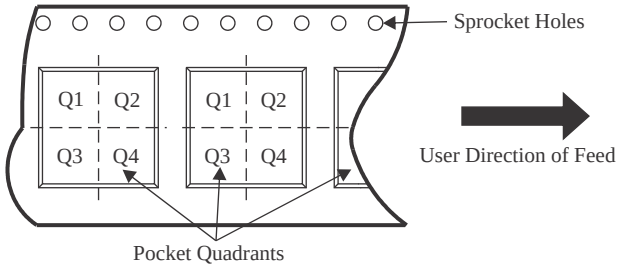


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

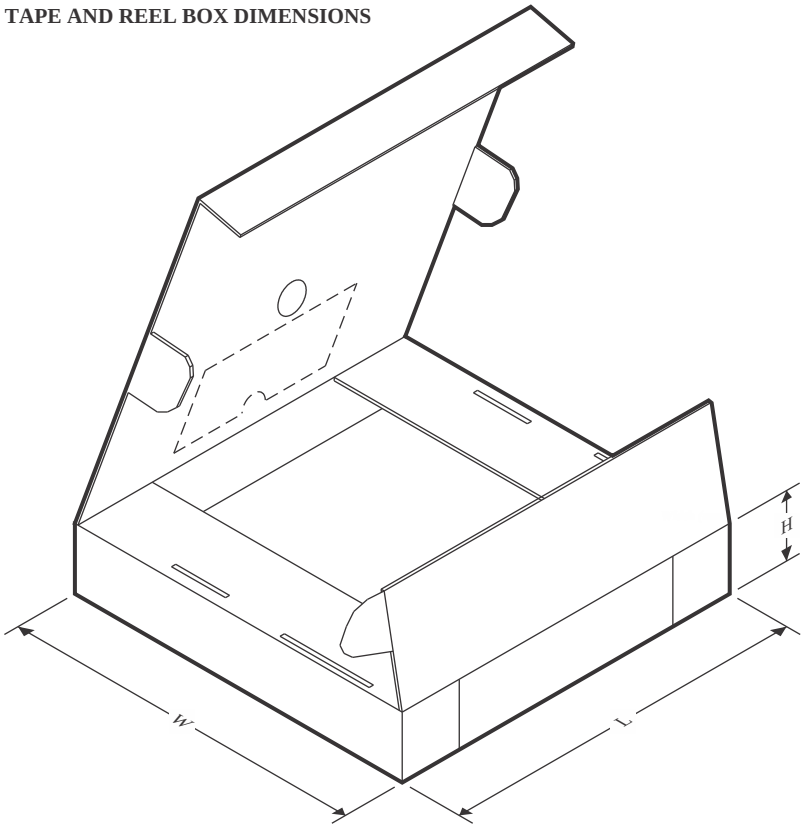
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC93M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

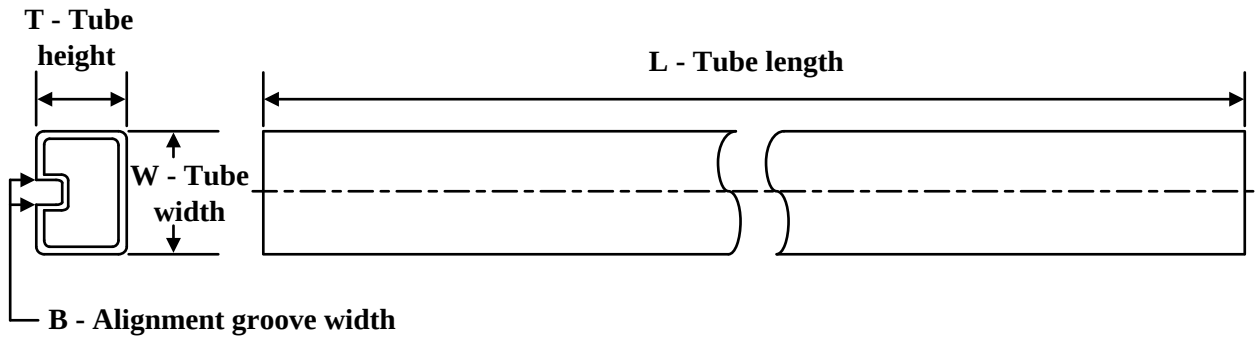
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC93M96	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



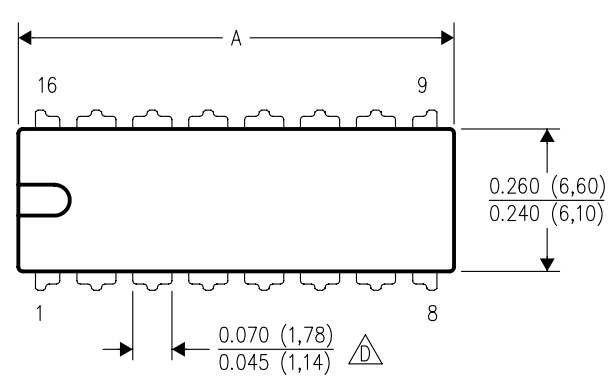
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC93E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC93E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC93E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC93E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC93EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC93EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT93E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT93E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT93E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT93E.A	N	PDIP	14	25	506	13.97	11230	4.32

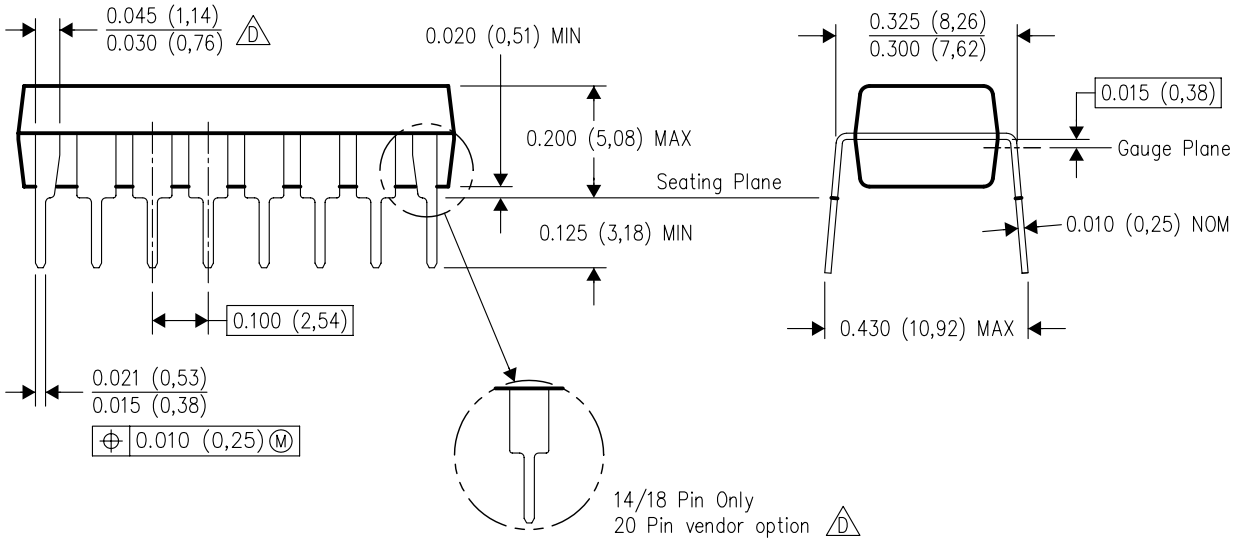
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

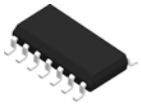


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

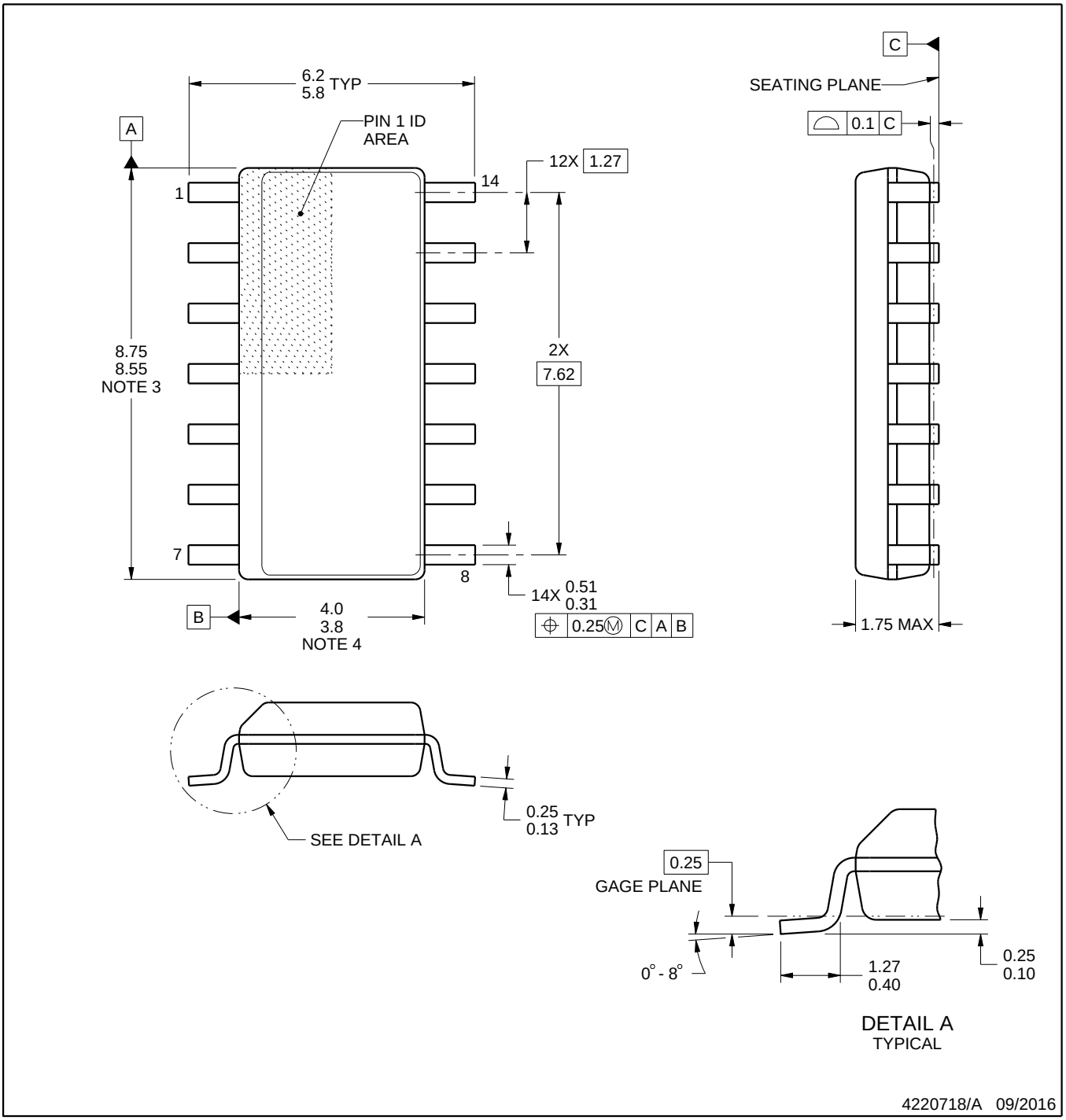


PACKAGE OUTLINE

D0014A

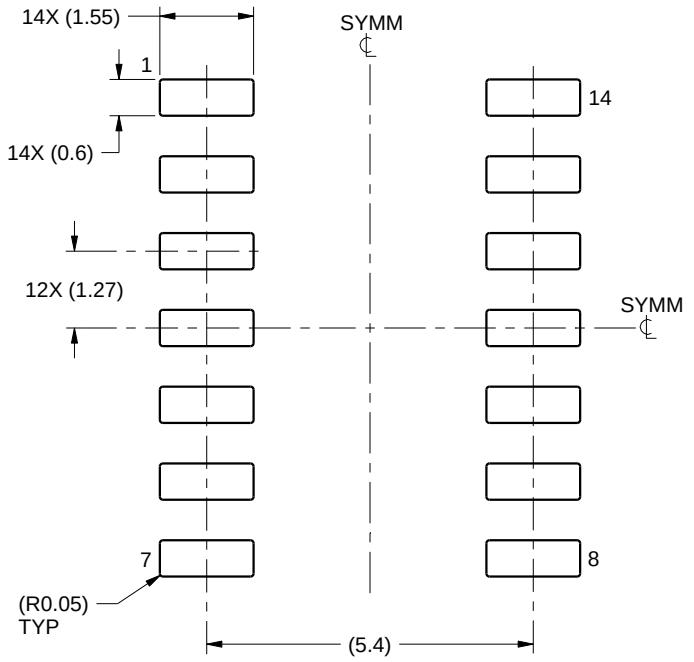
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

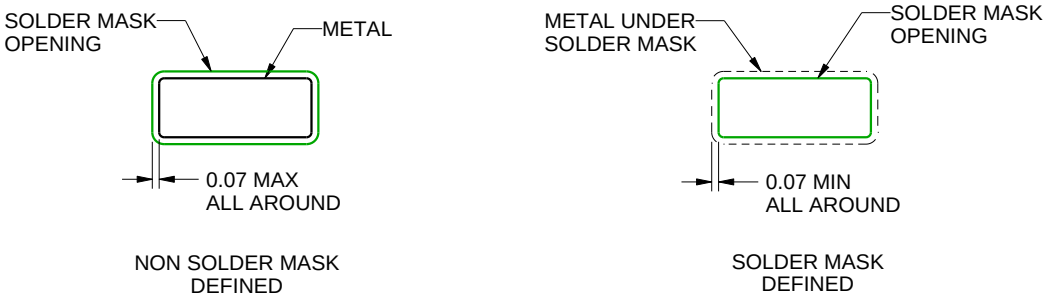


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

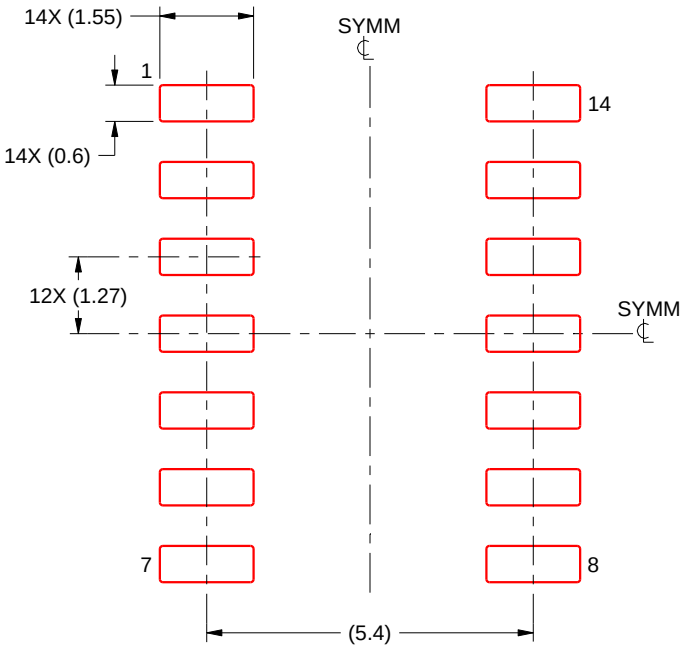
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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