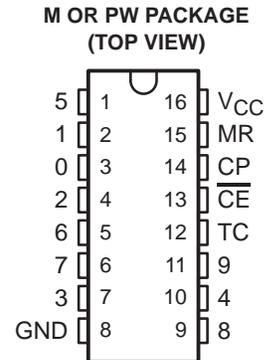# CD74HC4017-EP
HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER
WITH 10 DECODED OUTPUTS

SCLS550 – DECEMBER 2003

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Fully Static Operation**
- **Buffered Inputs**
- **Common Reset**
- **Positive Edge Clocking**
- **Typical f_{max} = 60 MHz at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . 15 LSTTL Loads**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **V_{CC} Voltage = 2 V to 6 V**
- **High Noise Immunity N_{IL} or N_{IH} = 30% of V_{CC}, V_{CC} = 5 V**

M OR PW PACKAGE
(TOP VIEW)

5	1	16	V_{CC}
1	2	15	MR
0	3	14	CP
2	4	13	$\overline{CE}$
6	5	12	TC
7	6	11	9
3	7	10	4
GND	8	9	8

description/ordering information

The CD74HC4017 is a high-speed silicon-gate CMOS 5-stage Johnson counter with ten decoded outputs. Each of the decoded outputs normally is low and sequentially goes high on the low-to-high transition clock period of the ten-clock-period cycle. The carry (TC) output transitions low to high after output 9 goes from high to low and can be used in conjunction with the clock enable ($\overline{CE}$) input to cascade several stages. $\overline{CE}$ disables counting when in the high state. A master reset (MR) input also is provided that, when taken high, sets all the decoded outputs, except output 0, to low.

The device can drive up to ten low-power Schottky equivalent loads.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC4017QM96EP	HC4017E
	TSSOP – PW	Tape and reel	CD74HC4017QPWREP	HC4017E

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE

INPUTS			OUTPUT STATE†
CP	$\overline{CE}$	MR	
L	X	L	No change
X	H	L	No change
X	X	H	0 = H, 1–9 = L
↑	L	L	Increments counter
↓	X	L	No change
X	↑	L	No change
H	↓	L	Increments counter

NOTE: H = high voltage level, L = low voltage level,
X = don't care, ↑ = transition from low to high
level, ↓ = transition from high to low level
† If n < 5, TC = H, otherwise TC = L

logic diagram (positive logic)
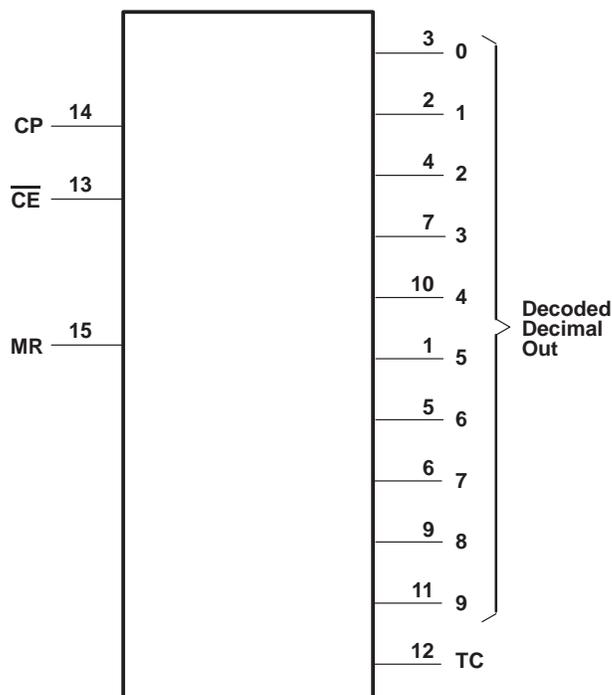
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 7 V

Input clamp current, I_{IK} (V_I < –0.5 V or V_I > V_{CC} + 0.5 V) . . . . ±20 mA

Output clamp current, I_{OK} (V_O < –0.5 V or V_O > V_{CC} + 0.5 V) . . . . ±20 mA

Source or sink current per output pin, I_O (V_O > –0.5 V or V_O < V_{CC} + 0.5 V) . . . . ±25 mA

Continuous current through V_{CC} or GND . . . . ±50 mA

Package thermal impedance, θ_{JA} (see Note 2): M package . . . . 73°C/W

PW package . . . . 108°C/W

Maximum junction temperature, T_J . . . . 150°C

Lead temperature (during soldering):

At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . 300°C

Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to GND unless otherwise specified.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6 V	0	400	
T_A	Operating free-air temperature		–40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report,
Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	$T_A = 25°C$		MIN MAX	UNIT
					MIN	MAX		
V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	–0.02	2 V	1.9		1.9	V
			–0.02	4.5 V	4.4		4.4	
			–0.02	6 V	5.9		5.9	
		TTL loads	–4	4.5 V	3.98		3.7	
			–5.2	6 V	5.48		5.2	
V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	2 V		0.1	0.1	V
			0.02	4.5 V		0.1	0.1	
			0.02	6 V		0.1	0.1	
		TTL loads	4	4.5 V		0.26	0.4	
			5.2	6 V		0.26	0.4	
I_I	$V_I = V_{CC}$ or GND			6 V		±0.1	±1	µA
I_{CC}	$V_I = V_{CC}$ or GND		0	6 V		8	160	µA
C_{IN}	$C_L = 50$ pF					10	10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			V_{CC}	$T_A = 25°C$		MIN MAX	UNIT
				MIN	MAX		
f_{max}	Maximum clock frequency		2 V	6		4	MHz
			4.5 V	30		20	
			6 V	35		23	
t_w	Pulse duration	CP	2 V	80		120	ns
			4.5 V	16		24	
			6 V	14		20	
		MR	2 V	80		120	
			4.5 V	16		24	
			6 V	14		20	
t_{su}	Setup time	$\overline{CE}$ to CP	2 V	75		110	ns
			4.5 V	15		22	
			6 V	13		19	
		MR inactive	2 V	5		5	
			4.5 V	5		5	
			6 V	5		5	
t_h	Hold time, $\overline{CE}$ to CP		2 V	0		0	ns
			4.5 V	0		0	
			6 V	0		0	

![Texas Instruments logo]

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	$T_A = 25°C$ MIN	TYP	MAX	MIN	MAX	UNIT
t_{pd}	CP	Decade out	C_L = 50 pF	2 V			230		345	ns
				4.5 V			46		69	
				6 V			39		59	
			C_L = 15 pF	5 V		19				
		TC	C_L = 50 pF	2 V			230		345	
				4.5 V			46		69	
				6 V			39		59	
			C_L = 15 pF	5 V		19				
	$\overline{CE}$	Decade out	C_L = 50 pF	2 V			250		375	
				4.5 V			50		75	
				6 V			43		64	
			C_L = 15 pF	5 V		21				
		TC	C_L = 50 pF	2 V			250		375	
				4.5 V			50		75	
				6 V			43		64	
			C_L = 15 pF	5 V		21				
	MR	Decade out	C_L = 50 pF	2 V			230		345	
				4.5 V			46		69	
				6 V			39		59	
			C_L = 15 pF	5 V		19				
		TC	C_L = 50 pF	2 V			230		345	
				4.5 V			46		69	
				6 V			39		59	
			C_L = 15 pF	5 V		19				
t_t		TC, Decade out	C_L = 50 pF	2 V		75			110	ns
				4.5 V		15			22	
				6 V		13			19	
f_{max}	CP		C_L = 15 pF	5 V		60				MHz

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns, C_L = 15 pF

	PARAMETER	TYP	UNIT
C_{pd}	Power dissipation capacitance (see Note 4)	39	pF

NOTE 4: C_{pd} is used to determine the dynamic power consumption per package.
$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_O)$
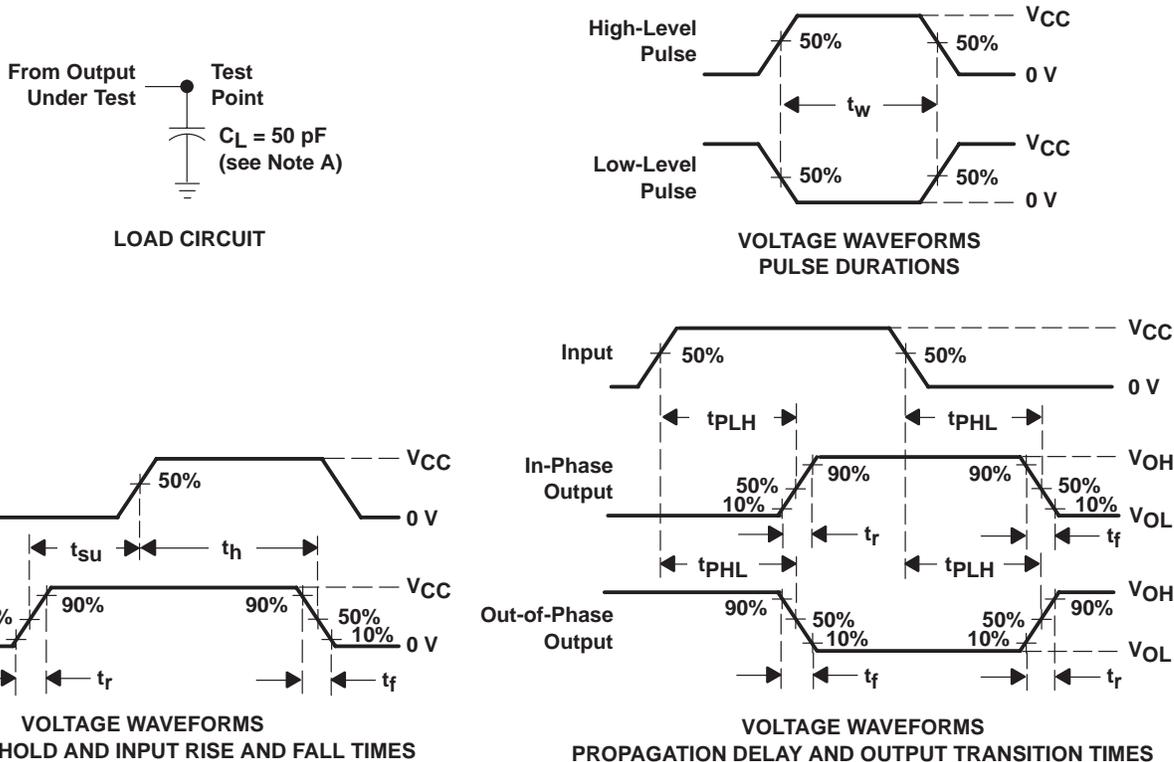f_I = input frequency
f_O = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, $Z_O = 50\ \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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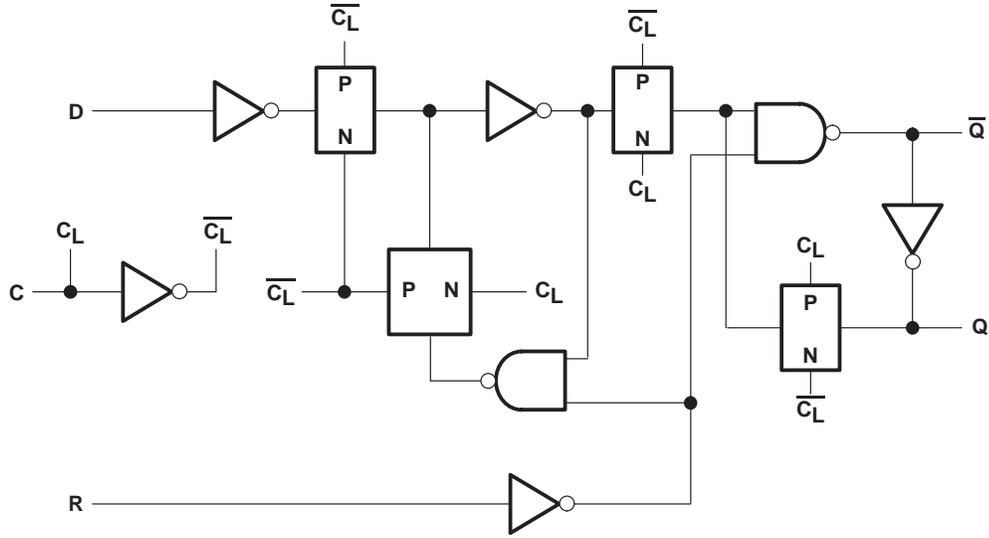
Figure 2. Flip-Flop Detail
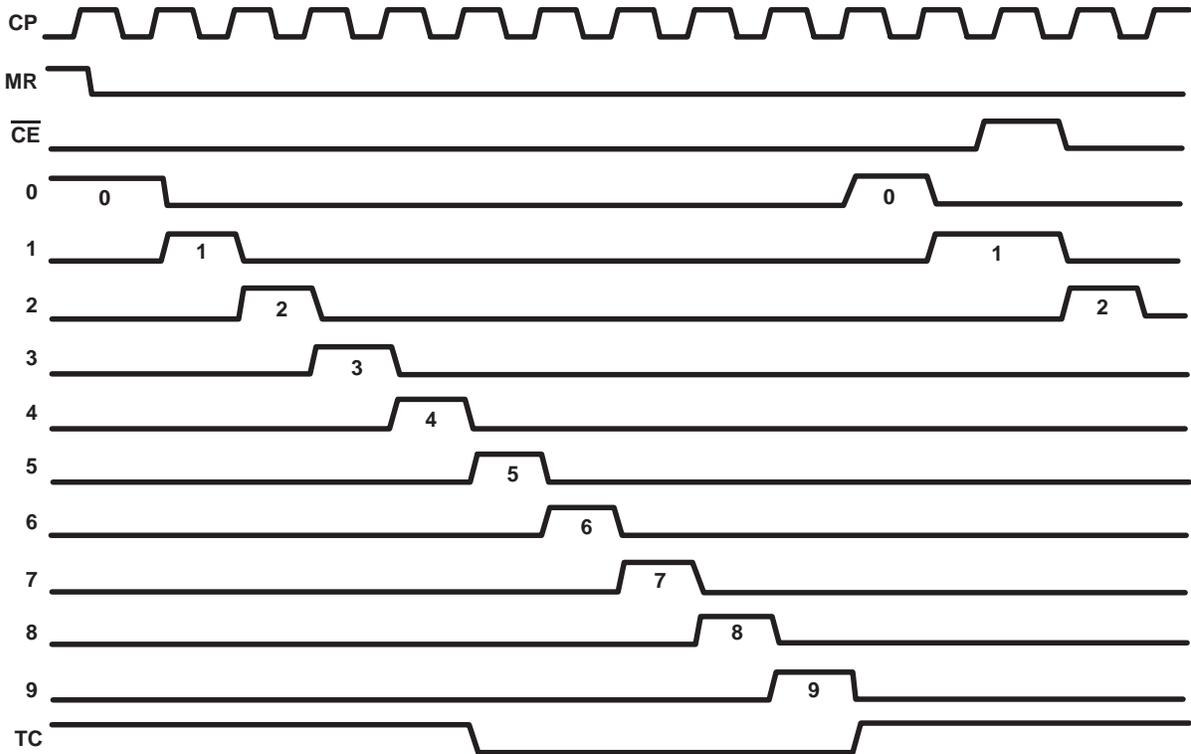
Figure 3. Timing Diagram

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4017QM96EP	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4017E
CD74HC4017QM96EP.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4017E
CD74HC4017QPWREP	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4017E
CD74HC4017QPWREP.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4017E
V62/04703-01XE	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4017E
V62/04703-01YE	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4017E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE OPTION ADDENDUM

OTHER QUALIFIED VERSIONS OF CD74HC4017-EP :

● Catalog : CD74HC4017

● Automotive : CD74HC4017-Q1

● Military : CD54HC4017

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4017QM96EP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
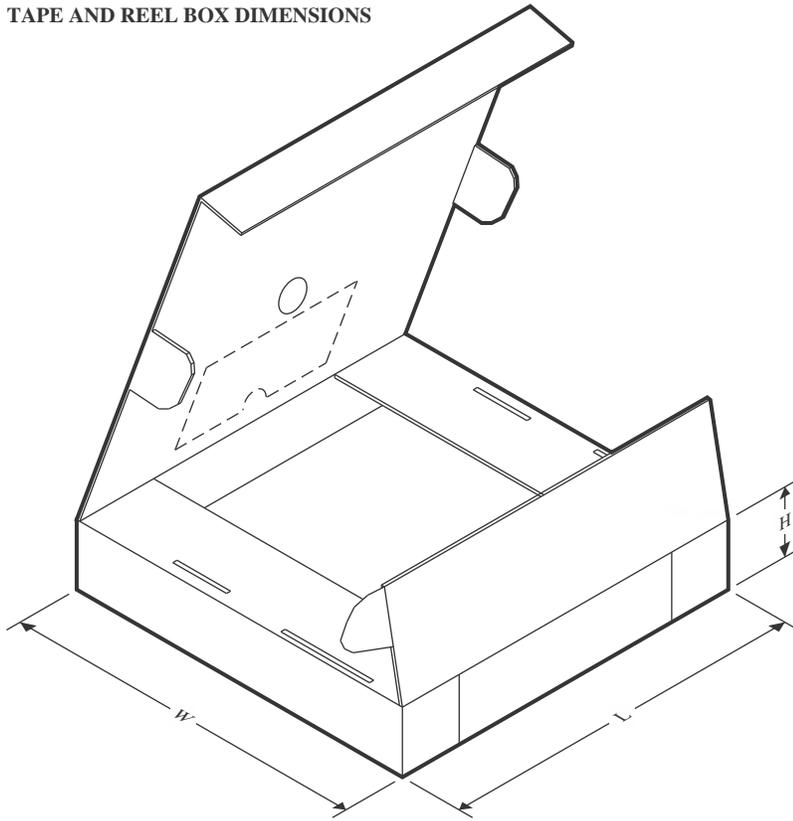
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4017QM96EP	SOIC	D	16	2500	353.0	353.0	32.0

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
△C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11
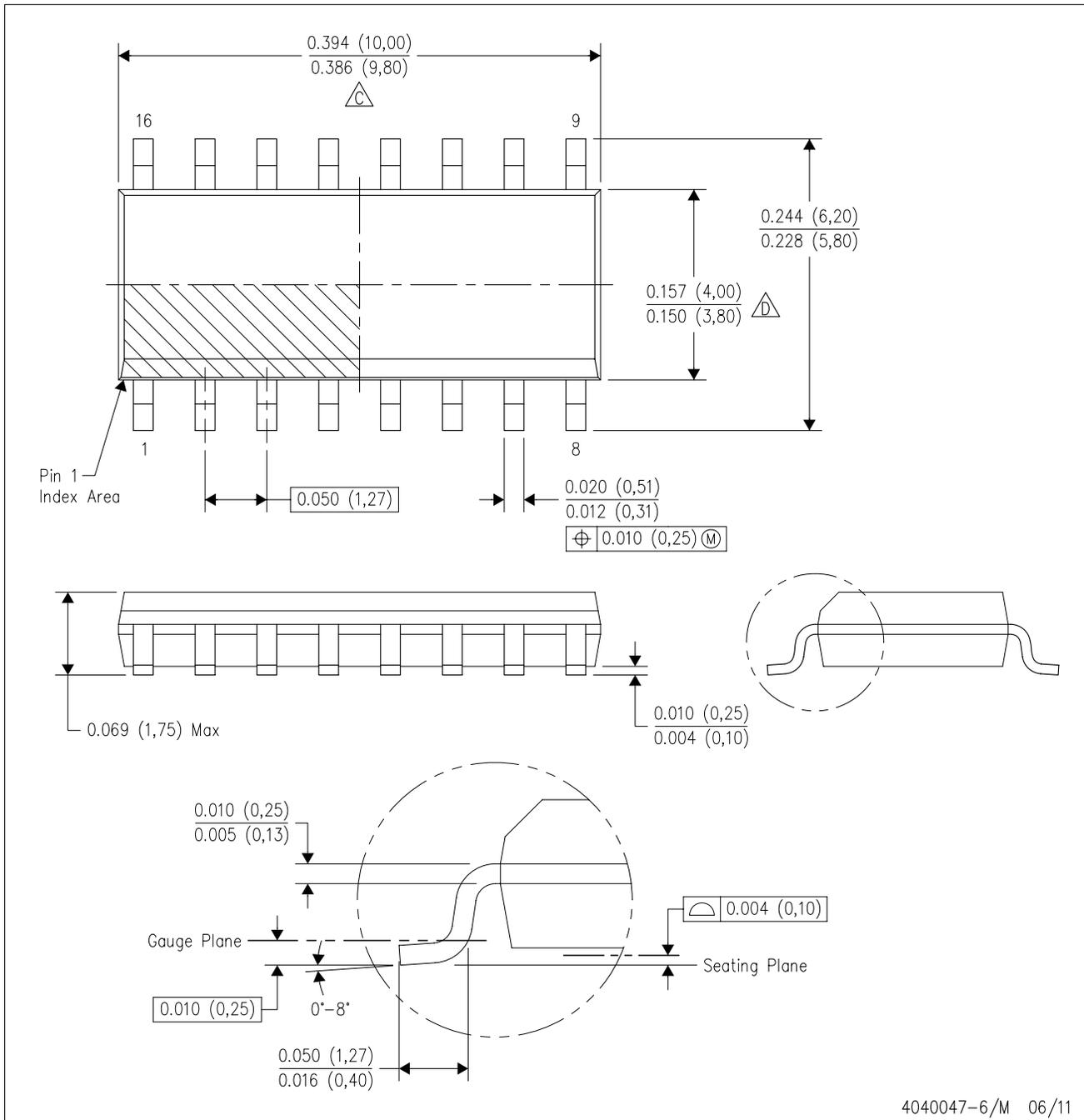
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
      △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0.006 (0,15) each side.
      △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
        E. Reference JEDEC MS−012 variation AC.

TEXAS
INSTRUMENTS
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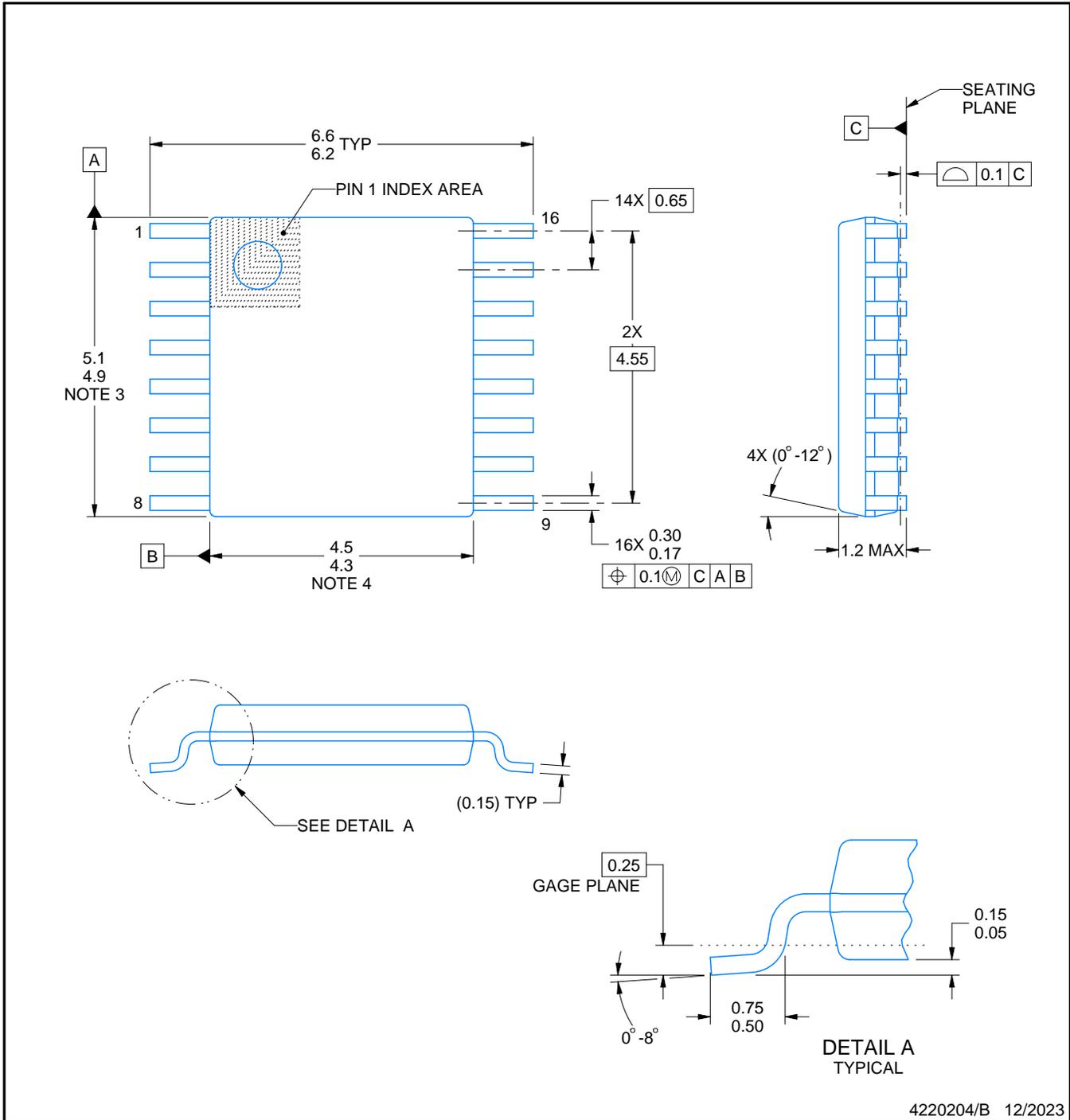
4220204/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

(R0.05) TYP

1

16X (0.45)

16

SYMM

14X (0.65)

8

9

(5.8)
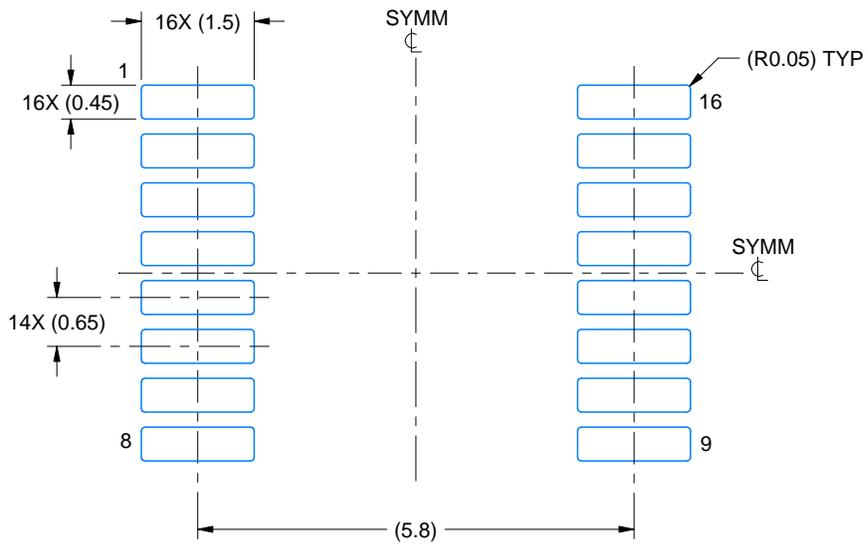
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
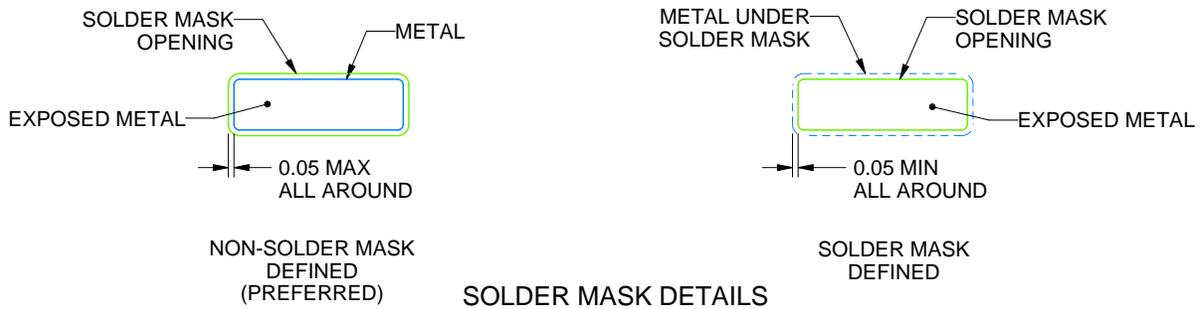
SOLDER MASK DETAILS

4220204/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

16

(R0.05) TYP

SYMM

14X (0.65)

8

9

(5.8)
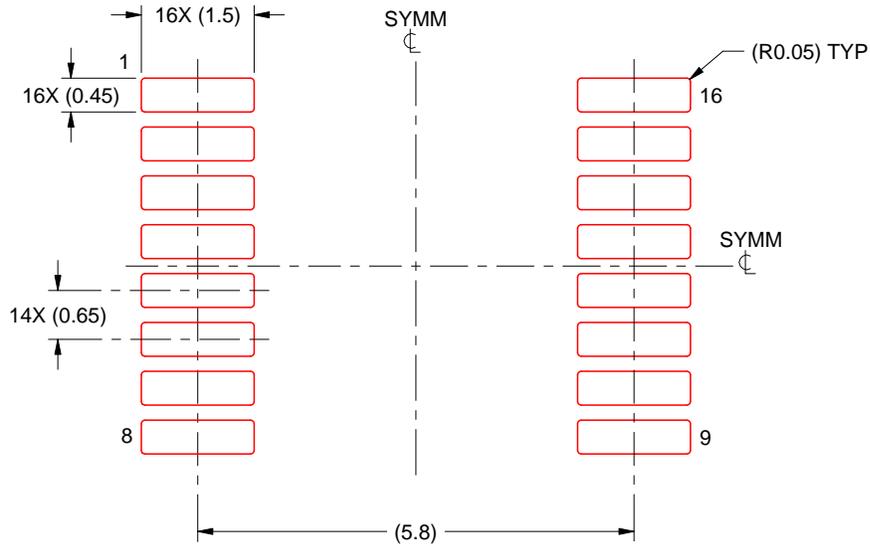
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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