

Quad D-Type Flip-Flop

74VHC175

General Description

The VHC175 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

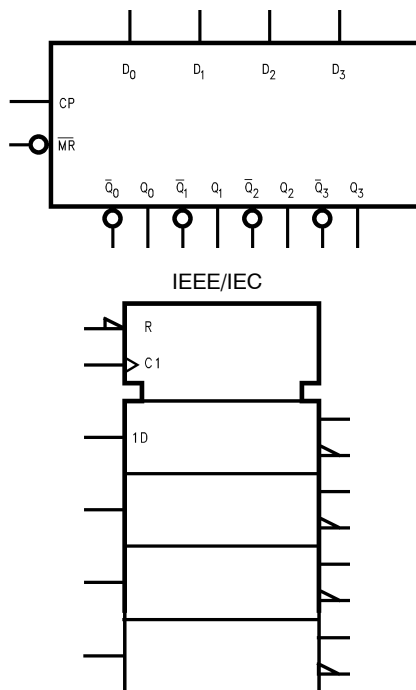
The VHC175 is a high-speed quad D-type flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flipflops, independent of the Clock or D inputs, when LOW.

An input protection circuit insures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

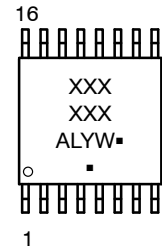
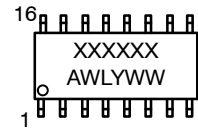
Features

- High Speed: $f_{MAX} = 210$ MHz (Typ.) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max.) at $T_A = 25$ °C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (Min.)
- Power Down Protection is Provided On All Inputs
- Low Noise: $V_{OLP} = 0.8$ V (Max.)
- Pin and Function Compatible with 74HC157
- This Device is Halide Free and Pb-Free

LOGIC SYMBOLS



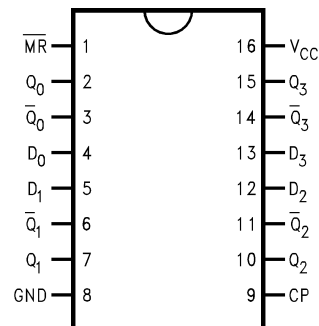
MARKING DIAGRAMS



A = Assembly Location
 WL, L = Wafer Lot
 Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

Pins	Function
D ₀ -D ₃	Data Inputs
CP	Clock Pulse Input
MR	Master Reset Input
Q ₀ -Q ₃	True Outputs
$\bar{Q}_0$ - $\bar{Q}_3$	Complement Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

74VHC175

Functional Description

The VHC175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\bar{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\bar{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\bar{Q}$ outputs HIGH independent of Clock or Data inputs. The VHC175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs @ t_n , MR = H	Outputs @ t_{n+1}	
D_n	Q_n	$\bar{Q}_n$
L	L	H
H	H	L

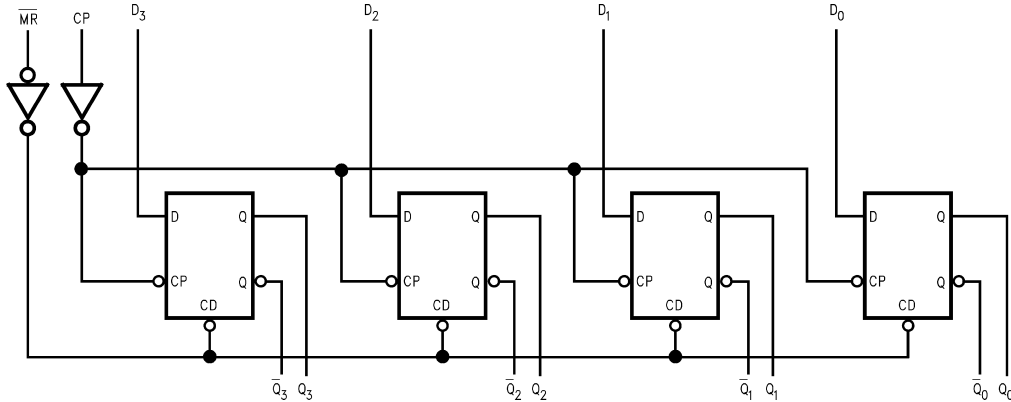
H = HIGH Voltage Level

L = LOW Voltage Level

t_n = Bit Time Before Clock Pulse

t_{n+1} = Bit Time After Clock Pulse

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage	−0.5 to +6.5	V	
V _{IN}	DC Input Voltage	−0.5 to +6.5	V	
V _{OUT}	DC Output Voltage	−0.5 to V _{CC} +0.5	V	
I _{IN}	DC Input Current, per Pin	±20	mA	
I _{OUT}	DC Output Current, per Pin	±25	mA	
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA	
I _{IK}	Input Clamp Current	−20	mA	
I _{OK}	Output Clamp Current	±20	mA	
T _{STG}	Storage Temperature Range	−65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C	
T _J	Junction Temperature Under Bias	+150	°C	
θ _{JA}	Thermal Resistance (Note 2)	SOIC-16 TSSOP-16	126 159	°C/W
P _D	Power Dissipation in Still Air at 25 °C	SOIC-16 TSSOP-16	995 787	mW
MSL	Moisture Sensitivity	Level 1	–	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.139 in	–
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage (Note 4)	0	5.5	V
V _{OUT}	DC Output Voltage (Note 4)	0	V _{CC}	V
T _A	Operating Temperature	−40	+85	°C
t _r , t _{fc}	Input Rise or Fall Rate	V _{CC} = 3.0 V to 3.6 V V _{CC} = 4.5 V to 55 V		ns/V
		0	100 20	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V _{CC} (V)	T _A = 25 °C			T _A = -40 °C to +85 °C		Unit
					Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage			2.0 3.0 – 5.5	1.50 0.7 x V _{CC}	–	–	1.50 0.7 x V _{CC}	–	V
V _{IL}	LOW Level Input Voltage			2.0 3.0 – 5.5	–	–	0.50 0.3 x V _{CC}	–	0.50 0.3 x V _{CC}	V
V _{OH}	HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	– – –	1.9 2.9 4.4	– – –	V
			I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94	– –		2.48 3.80	– –	V
V _{OL}	LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 µA	2.0 3.0 4.5	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I _{OH} = 4 mA I _{OH} = 8 mA	3.0 4.5	– –	– –	0.36 0.36	– –	0.44 0.44	V
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND		0 – 5.5	–	–	±0.1	–	±1.0	µA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND		5.5	–	–	4.0	–	40.0	µA

NOISE CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C		Unit
				Typ	Limits	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL} (Note 5)	CL = 50 pF	5.0	0.4	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL} (Note 5)	CL = 50 pF	5.0	-0.4	-0.8	V
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage (Note 5)	CL = 50 pF	5.0	–	3.5	V
V _{ILD}	Maximum LOW Level Dynamic Input Voltage (Note 5)	CL = 50 pF	5.0	–	1.5	V

5. Parameter guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = -40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	C _L = 15 pF	3.3 ± 0.3	90	140	–	75	–	MHz
		C _L = 50 pF		50	75	–	45	–	
		C _L = 15 pF	5.0 ± 0.5	150	210	–	125	–	MHz
		C _L = 50 pF		85	115	–	75	–	

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = -40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay Time, (CP to Q _n or Q _n)	C _L = 15 pF	3.3 ± 0.3	–	7.5	11.5	1.0	13.5	ns
		C _L = 50 pF		–	10.0	15.0	1.0	17.0	
		C _L = 15 pF	5.0 ± 0.5	–	4.8	7.3	1.0	8.5	ns
		C _L = 50 pF		–	6.3	9.3	1.0	10.5	
t _{PLH} , t _{PHL}	Propagation Delay Time, (MR to Q _n or Q _n)	C _L = 15 pF	3.3 ± 0.3	–	6.3	10.1	1.0	12.0	ns
		C _L = 50 pF		–	8.8	13.6	1.0	15.5	
		C _L = 15 pF	5.0 ± 0.5	–	4.3	6.4	1.0	7.5	ns
		C _L = 50 pF		–	5.8	8.4	1.0	9.5	
t _{OSLH} , t _{OSHL}	Output to Output Skew (Note 6)	C _L = 50 pF	3.3 ± 0.3	–	–	1.5	–	1.5	
		C _L = 50 pF	5.0 ± 0.5	–	–	1.0	–	1.0	
C _{IN}	Input Capacitance	V _{CC} = Open		–	4	10	–	10	pF
C _{PD}	Power Dissipation Capacitance (Note 7)			–	44	–	–	–	pF

6. Parameter guaranteed by design. t_{OSLH} = |t_{PLH} max – t_{PLH} min|; t_{OSHL} = |t_{PHL} max – t_{PHL} min|

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} · V_{CC} · f_{IN} + I_{CC}/4 (per F/F), and the total C_{PD} when n pcs of the Flip-Flop operate can be calculated by the following equation: C_{PD} (total) = 30 + 14 · n

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} (V) (Note 8)	T _A = 25 °C		T _A = −40 °C to +85 °C	Unit
			Typ	Guaranteed Minimum		
t _W (L), t _W (H)	Minimum Pulse Width (CP)	3.3	–	5.0	5.0	ns
		5.0	–	5.0	5.0	
t _W (L)	Minimum Pulse Width (MR)	3.3	–	5.0	5.0	ns
		5.0	–	5.0	5.0	
t _S	Minimum Setup Time (Dn to CP)	3.3	–	5.0	5.0	ns
		5.0	–	4.0	4.0	
t _H	Minimum Hold Time (Dn to CP)	3.3	–	1.0	1.0	ns
		5.0	–	1.0	1.0	
t _{REC}	Minimum Removal Time (MR)	3.3	–	5.0	5.0	ns
		5.0	–	5.0	5.0	

8. V_{CC} is 3.3 ± 0.3 V or 5.0 ± 0.5 V

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
74VHC175MX	VHC175G	SOIC-16	2500 Units / Tape & Reel
74VHC175MTCX	VHC175	TSSOP-16	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

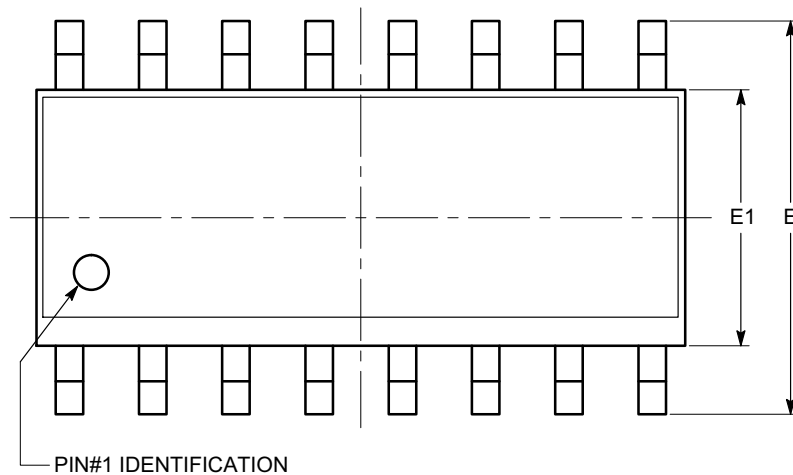
REVISION HISTORY

Revision	Description of Changes	Date
1	Converted the Data Sheet to onsemi format with the updates in Ordering Information Table, Recommended Operating Table, Maximum Rating Table.	9/23/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

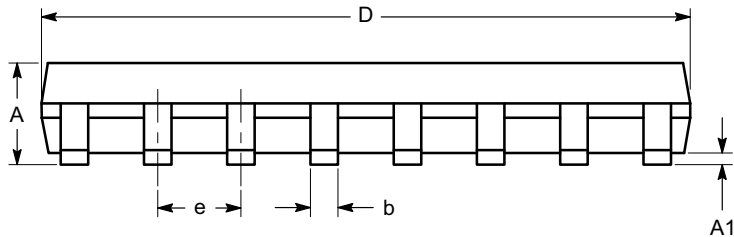
SOIC-16, 150 mils
CASE 751BG
ISSUE O

DATE 19 DEC 2008

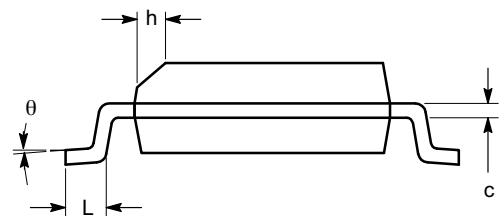


SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

Notes:

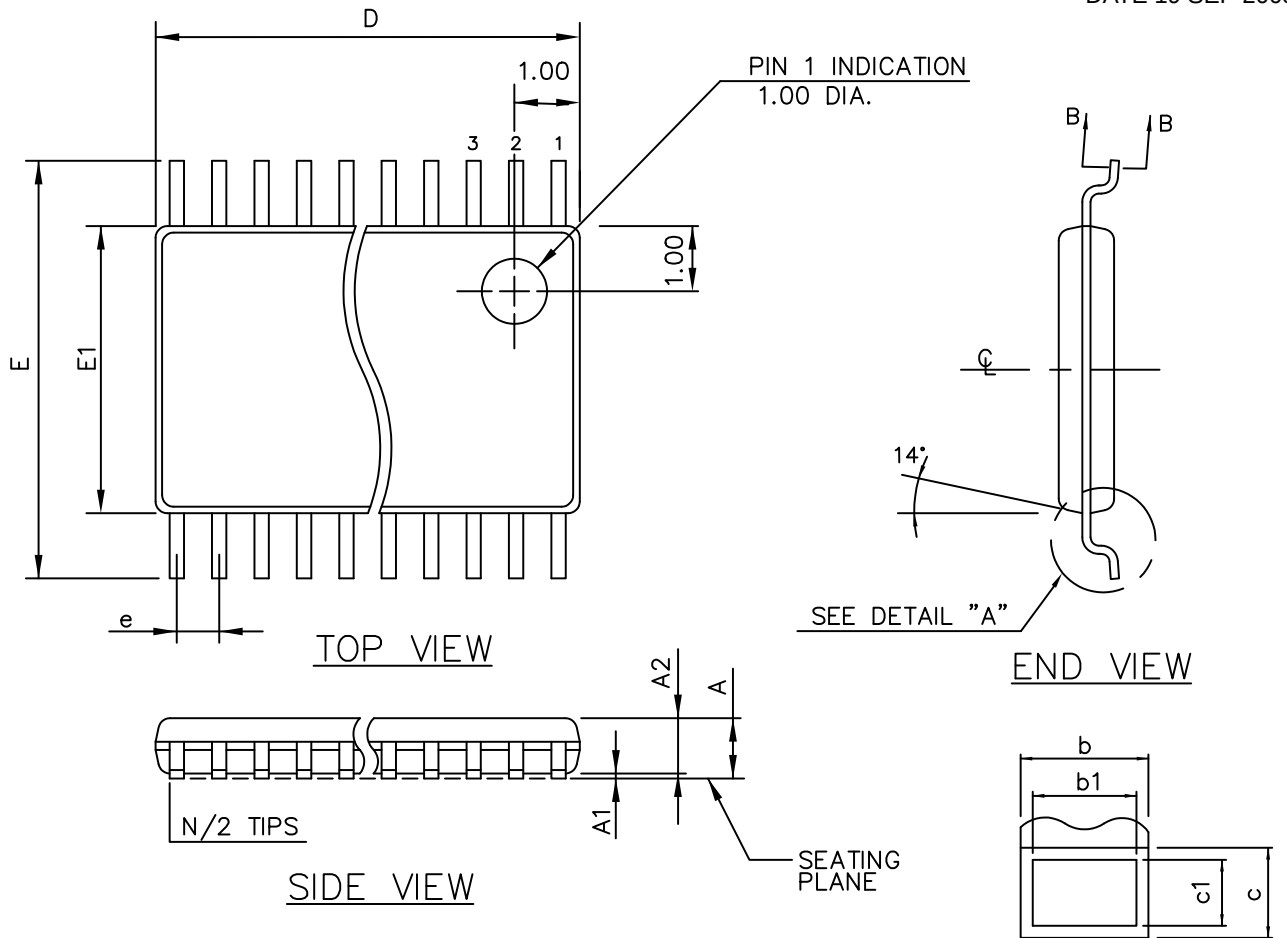
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

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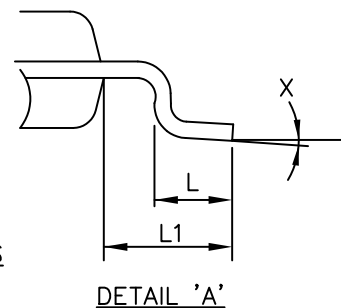


THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	D	N
	MIN.	NOM.	MAX.			
A	—	—	1.10	AA/AAT	3.00 BSC	8
A ₁	0.05	—	0.15	AB-1/ABT	5.00 BSC	14
A ₂	0.85	0.90	0.95	AB/ABT	5.00 BSC	16
b	0.19	—	0.30	AD/ADT	7.80 BSC	24
b ₁	0.19	0.22	0.25			
c	0.09	—	0.20			
c ₁	0.09	0.127	0.16			
D	SEE VARIATIONS					
E ₁	4.30	4.40	4.50			
e	0.65 BSC					
E	6.40 BSC					
L	0.50	0.60	0.70			
L ₁	1.00 REF					
N	SEE VARIATIONS					
X	0°	—	8°			

ALL DIMENSIONS IN MILLIMETERS

SECTION "B-B"



MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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