

# CMOS Strobed Hex Inverter/Buffer

High-Voltage Types (20-Volt Rating)

■ CD4502B consists of six inverter/buffers with 3-state outputs. A logic "1" on the OUTPUT DISABLE input produces a high-impedance state in all six outputs. This feature permits common bussing of the outputs, thus simplifying system design. A Logic "1" on the INHIBIT input switches all six outputs to logic "0" if the OUTPUT DISABLE input is a logic "0". This device is capable of driving two standard TTL loads, which is equivalent to six times the JEDEC "B"-series I<sub>OL</sub> standard.

The CD4502B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )	.....	-0.5V to +20V
Voltages referenced to V <sub>SS</sub> Terminal	.....	
INPUT VOLTAGE RANGE, ALL INPUTS	.....	-0.5V to V <sub>DD</sub> +0.5V
DC INPUT CURRENT, ANY ONE INPUT	.....	±10mA
POWER DISSIPATION PER PACKAGE (P <sub>D</sub> ):		
For T <sub>A</sub> = -55°C to +100°C	.....	500mW
For T <sub>A</sub> = +100°C to +125°C	.....	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	.....	100mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )	.....	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	.....	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	.....	+265°C

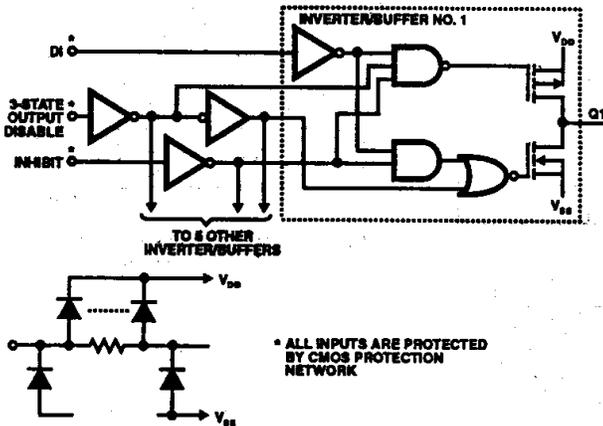
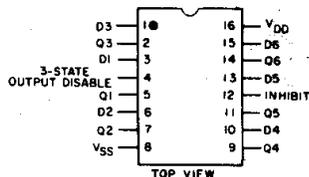


Fig. 1 – Logic diagram of 1 of 6 identical inverter/buffers.



**TERMINAL ASSIGNMENT**

**Features:**

- 2 TTL-load output drive capability
- 3-state outputs
- Common output-disable control
- Inhibit control
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Noise margin (full package-temperature range) =

- 1 V at V<sub>DD</sub> = 5 V
- 2 V at V<sub>DD</sub> = 10 V
- 2.5 V at V<sub>DD</sub> = 15 V

**Applications:**

- 3-state hex inverter for interfacing IC's with data buses
- COS/MOS to TTL hex buffer

# CD4502B Types

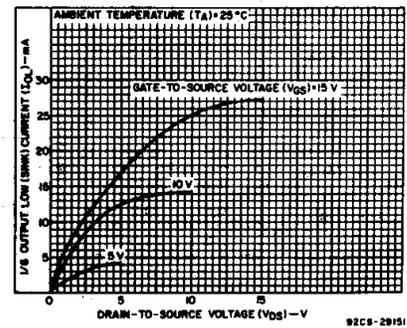
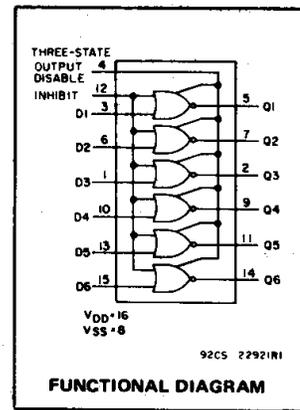


Fig. 2 – Typical output low (sink) current characteristics.

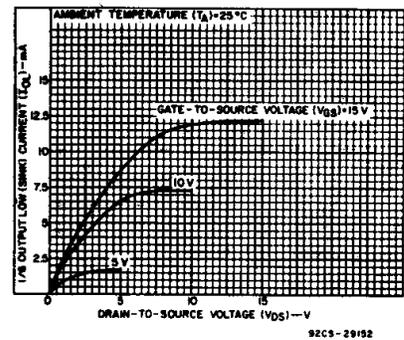


Fig. 3 – Minimum output low (sink) current characteristics.

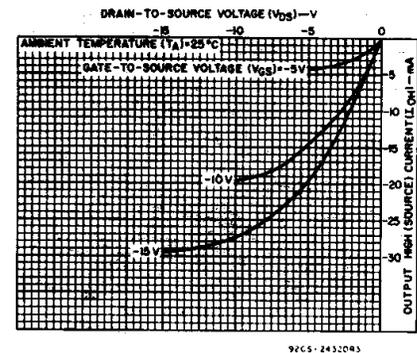


Fig. 4 – Typical output high (source) current characteristics.

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# CD4502B Types

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range)	3	18	V

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, $I_{DD}$ Max.	-	0.5	5	1	1	30	30	-	0.02	1	$\mu$ A
	-	0.10	10	2	2	60	60	-	0.02	2	
	-	0.15	15	4	4	120	120	-	0.02	4	
	-	0.20	20	20	20	600	600	-	0.04	20	
Output Low (Sink) Current $I_{OL}$ Min.	0.4	0.5	5	3.84	3.66	2.52	2.16	3.06	6	-	mA
	0.5	0.10	10	9.6	9	6.6	5.4	7.8	15.6	-	
	1.5	0.15	15	25.2	24	16.8	14.4	20.4	40.8	-	
Output High (Source) Current, $I_{OH}$ Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, $V_{OL}$ Max.	-	0.5	5	0.05				-	0	0.05	V
	-	0.10	10	0.05				-	0	0.05	
	-	0.15	15	0.05				-	0	0.05	
Output Voltage: High-Level, $V_{OH}$ Min.	-	0.5	5	4.95				4.95	5	-	V
	-	0.10	10	9.95				9.95	10	-	
	-	0.15	15	14.95				14.95	15	-	
Input Low Voltage, $V_{IL}$ Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	15, 13.5	-	15	4				-	-	4	
Input High Voltage, $V_{IH}$ Min.	4.5	-	5	3.5				3.5	-	-	V
	9	-	10	7				7	-	-	
	13.5	-	15	11				11	-	-	
Input Current $I_{IN}$ Max.		0.18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu$ A
3-State Output Leakage Current $I_{OUT}$ Max.	0.18	0.18	18	$\pm 0.4$	$\pm 0.4$	$\pm 12$	$\pm 12$	-	$\pm 10^{-4}$	$\pm 0.4$	$\mu$ A

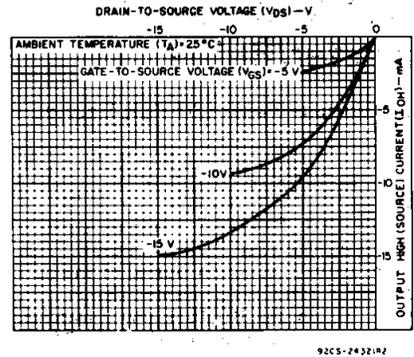


Fig. 5 - Minimum output high (source) current characteristics.

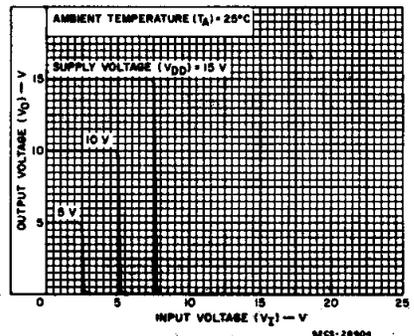


Fig. 6 - Typical voltage transfer characteristics.

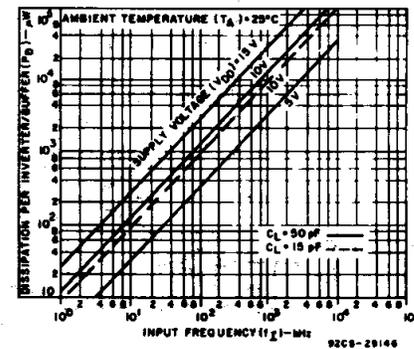


Fig. 7 - Typical power dissipation as a function of input frequency.

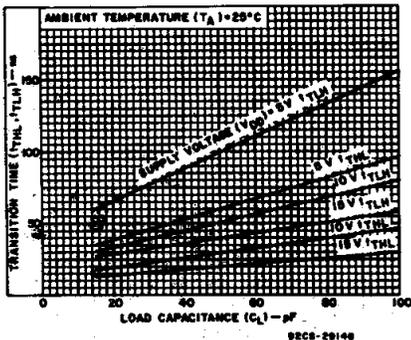


Fig. 8 - Typical transition time as a function of load capacitance.

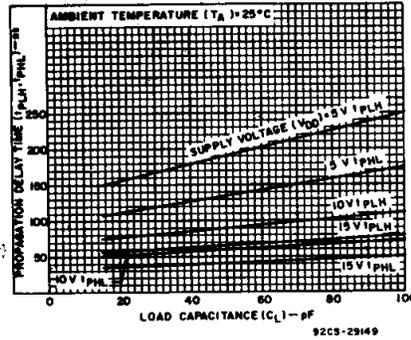


Fig. 9 - Typical propagation delay time as a function of load capacitance.

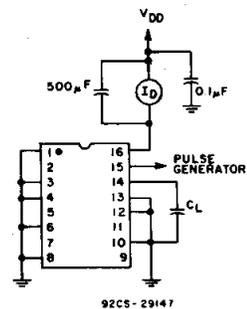


Fig. 10 - Power dissipation test circuit.

# CD4502B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ K}\Omega$  Unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		V <sub>DD</sub> (V)	TYP		MAX
Data or Inhibit Delay Times: High to Low, $t_{PHL}$		5	135	270	ns
		10	60	120	
		15	40	80	
Low to High, $t_{PLH}$		5	190	380	ns
		10	90	180	
		15	65	130	
Disable Delay Times: $R_L = 1 \text{ K}\Omega$ Output High to High Impedance, $t_{PHZ}$		5	60	120	ns
		10	40	80	
		15	30	60	
High-Impedance to Output High, $t_{PZH}$	See Fig. 14	5	110	220	ns
		10	50	100	
		15	40	80	
Output Low to High Impedance, $t_{PLZ}$		5	125	250	ns
		10	65	130	
		15	55	110	
High Impedance to Output Low, $t_{PZL}$		5	125	250	ns
		10	55	110	
		15	40	80	
Transition Times: Low to High, $t_{TLH}$		5	100	200	ns
		10	50	100	
		15	40	80	
High to Low, $t_{THL}$		5	60	120	ns
		10	30	60	
		15	20	40	
Input Capacitance, $C_{IN}$	Any Input	5	7.5	pF	
Output Capacitance, $C_{OUT}$		7-8	15	pF	

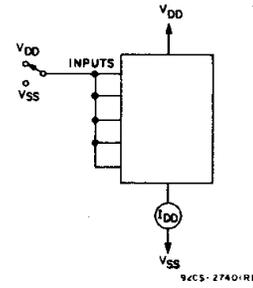


Fig. 11 - Quiescent-device-current test circuit.

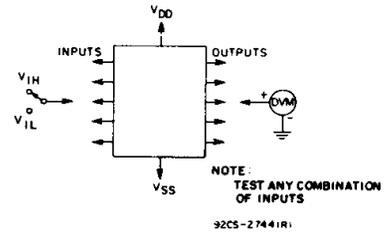


Fig. 12 - Input-voltage test circuit.

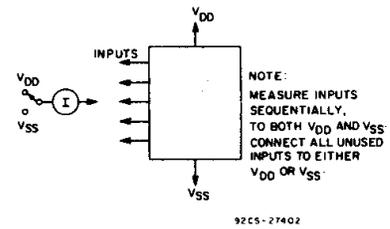


Fig. 13 - Input leakage current test circuit.

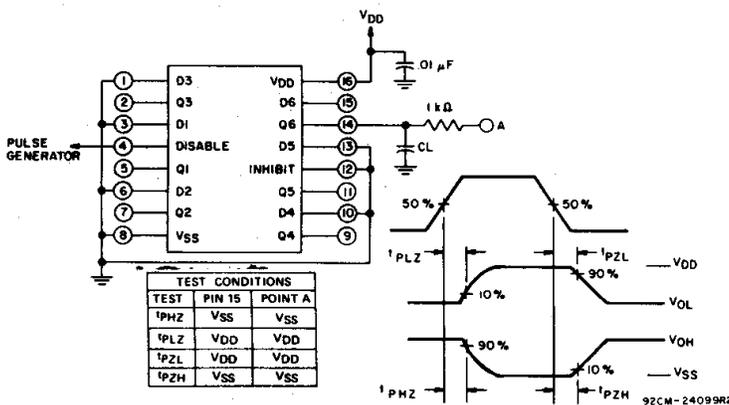
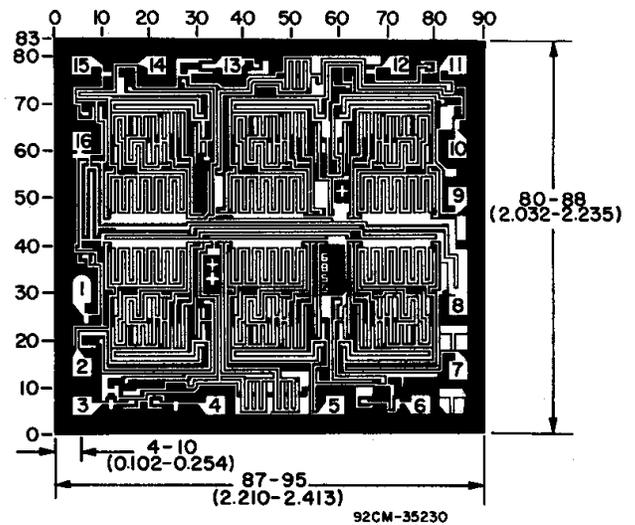


Fig. 14 - Disable delay times test circuit and waveforms.



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**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">7702002EA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7702002EA CD4502BF3A
<a href="#">CD4502BE</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4502BE
CD4502BE.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4502BE
CD4502BEE4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4502BE
<a href="#">CD4502BF3A</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7702002EA CD4502BF3A
CD4502BF3A.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7702002EA CD4502BF3A
<a href="#">CD4502BM</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-55 to 125	CD4502BM
<a href="#">CD4502BM96</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4502BM
CD4502BM96.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4502BM
<a href="#">CD4502BNSR</a>	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4502B
CD4502BNSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4502B
<a href="#">CD4502BPW</a>	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM502B
CD4502BPW.A	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM502B
<a href="#">JM38510/17403BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 17403BEA
JM38510/17403BEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 17403BEA
<a href="#">M38510/17403BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 17403BEA

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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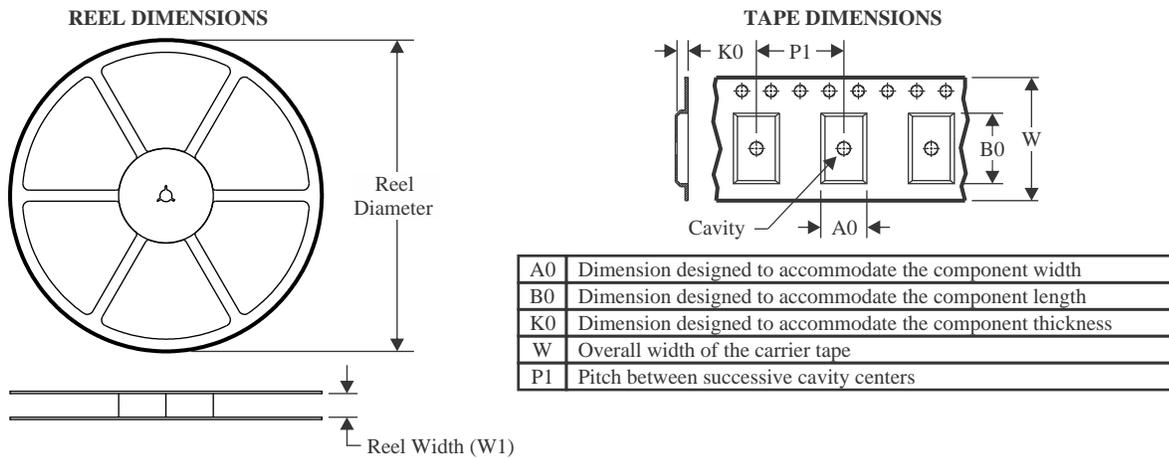
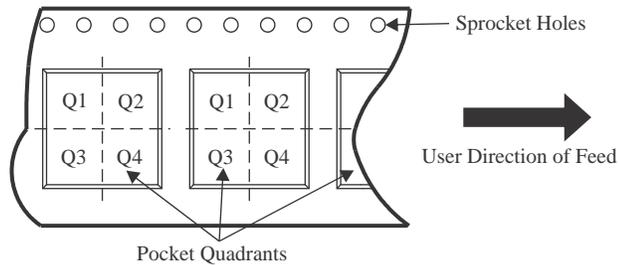
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4502B, CD4502B-MIL :**

- Catalog : [CD4502B](#)
- Military : [CD4502B-MIL](#)

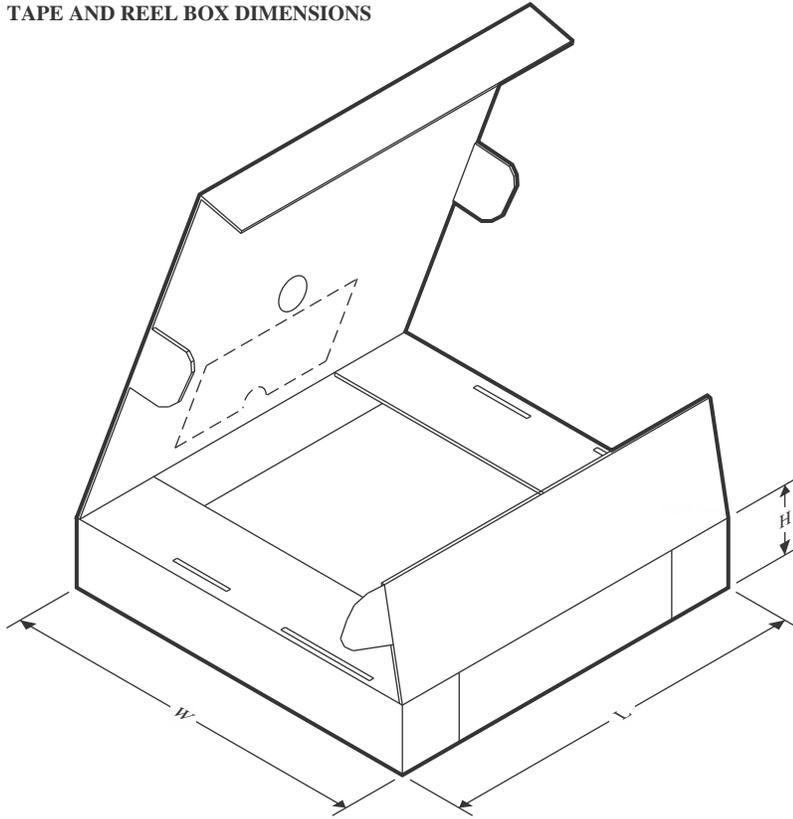
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


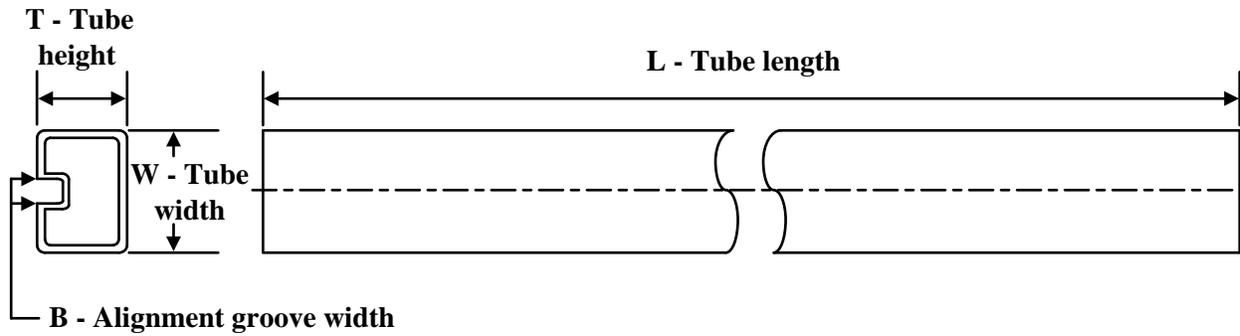
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4502BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4502BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4502BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4502BNSR	SOP	NS	16	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4502BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4502BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4502BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4502BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4502BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4502BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4502BPW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4502BPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5

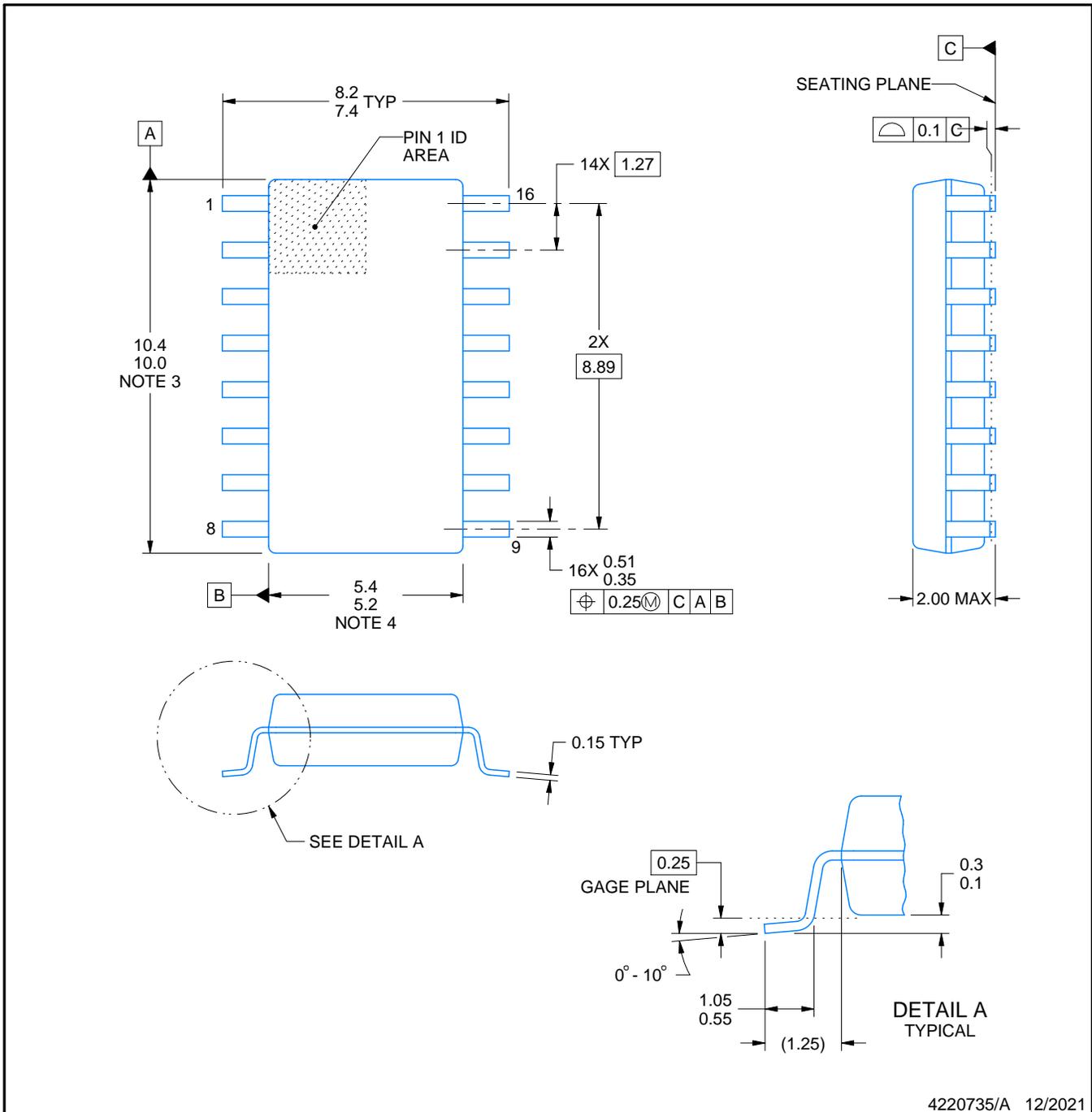


# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



#### NOTES:

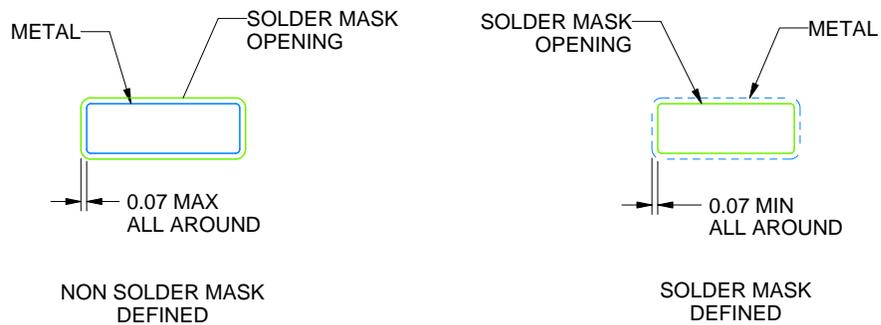
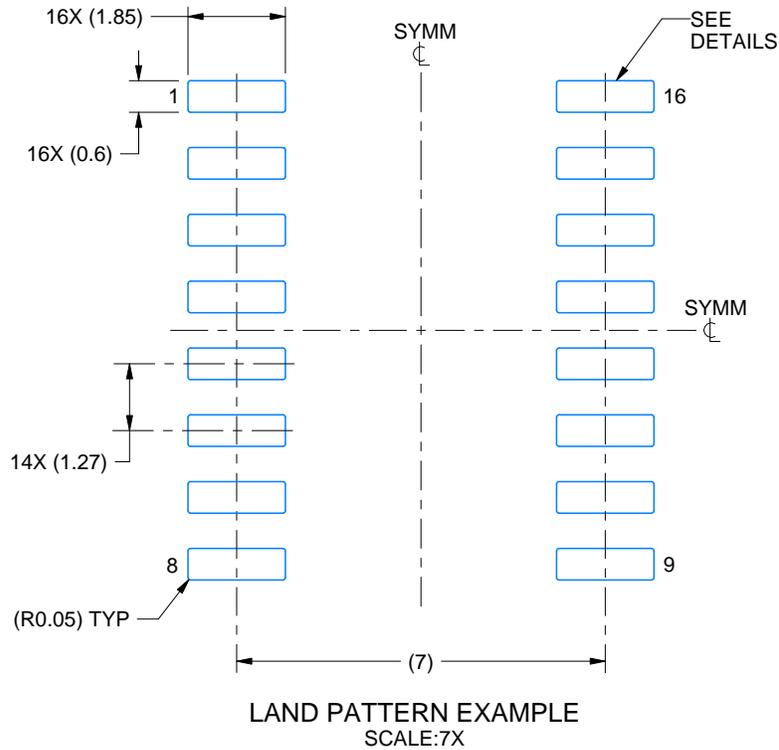
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

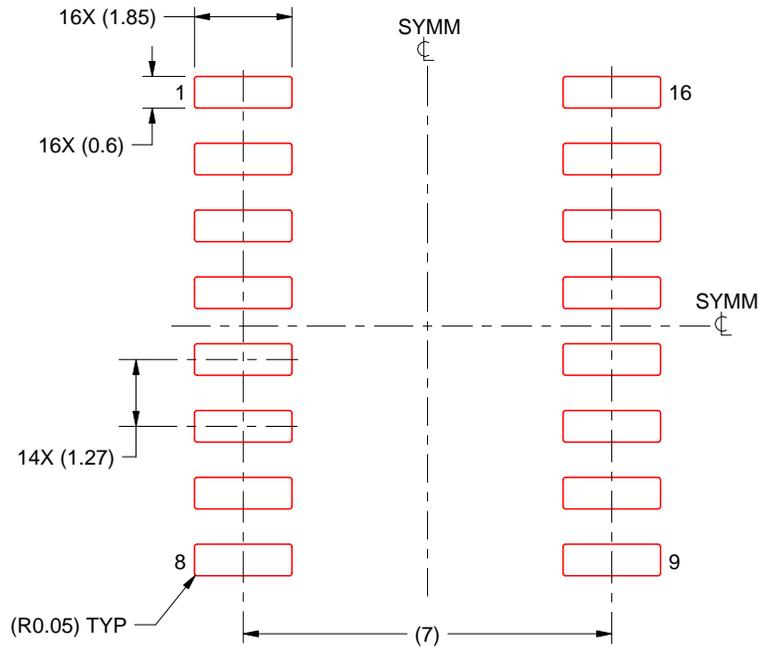
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

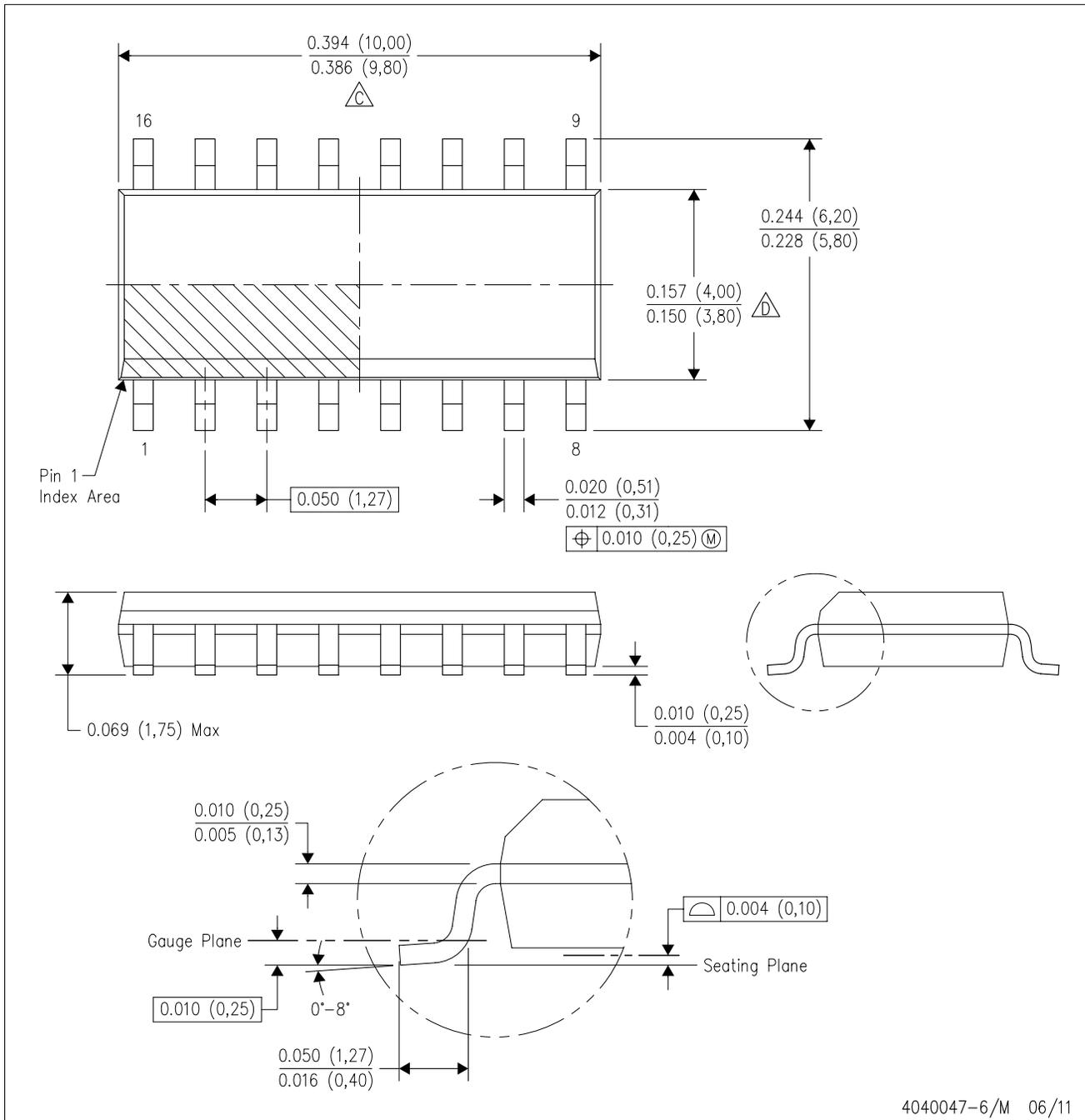
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



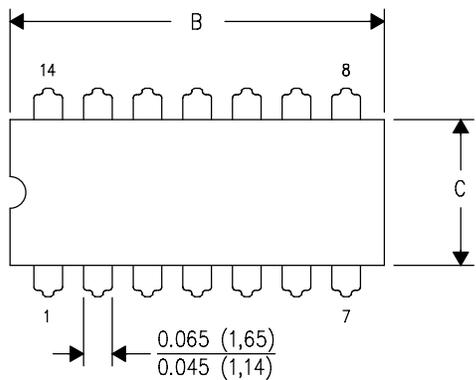
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- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

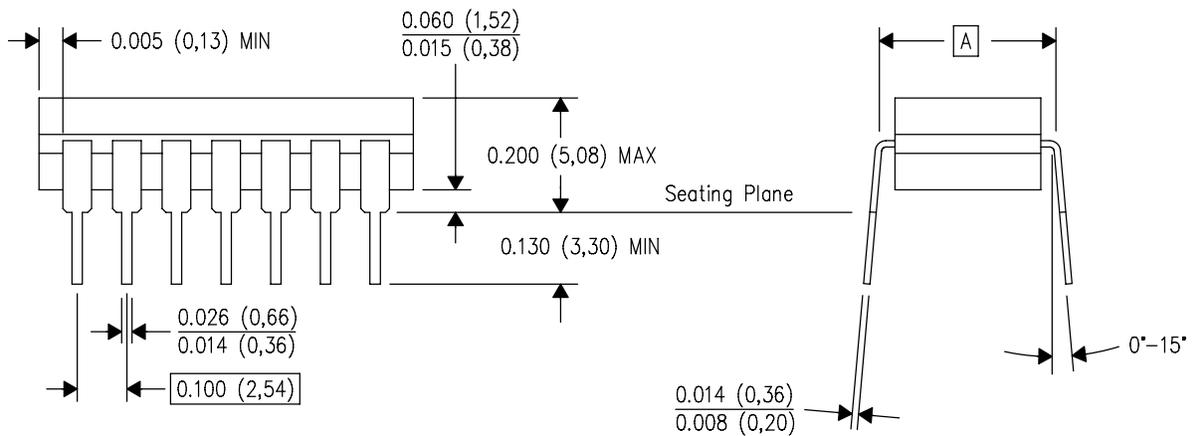
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14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

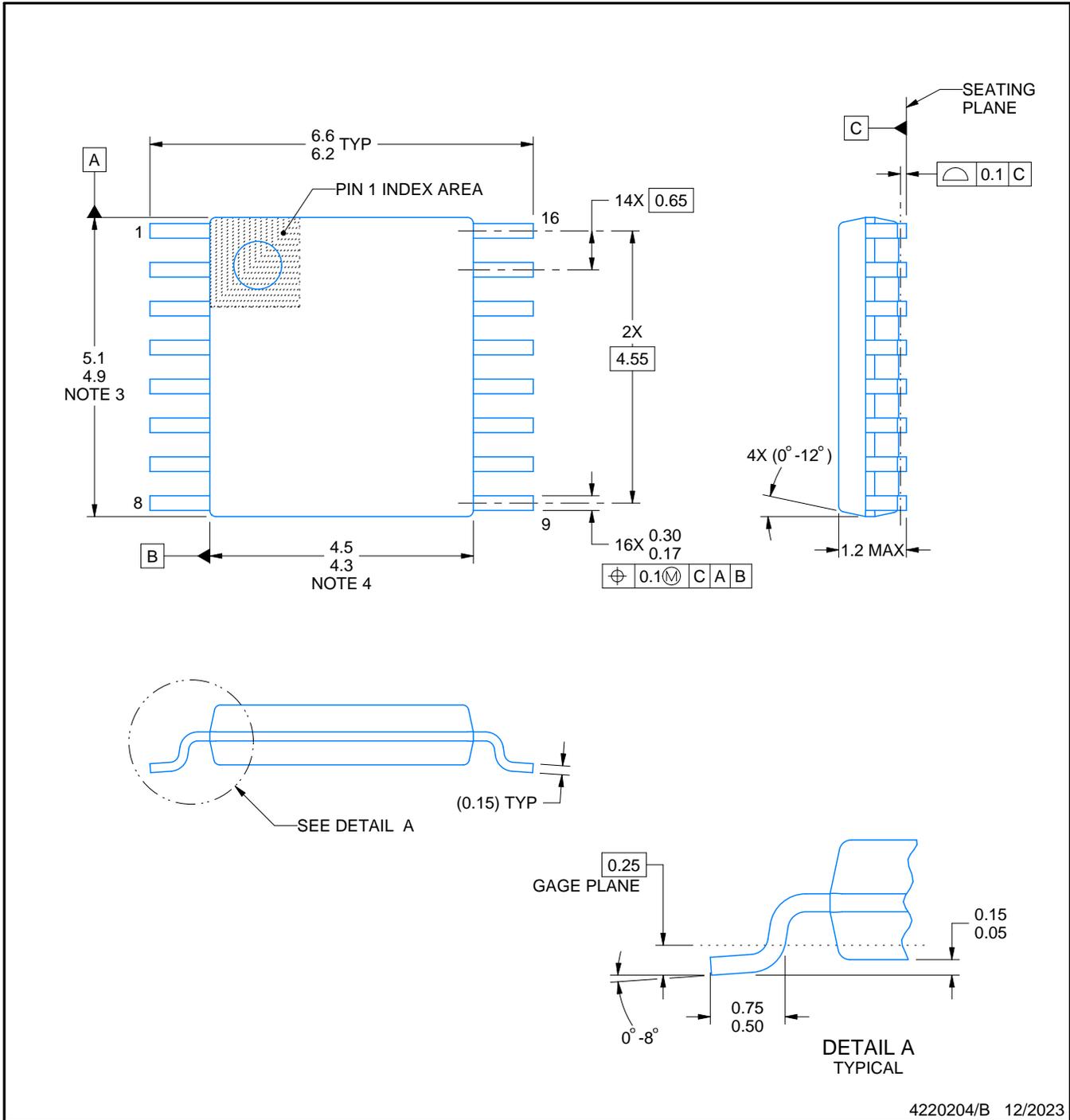


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



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NOTES:

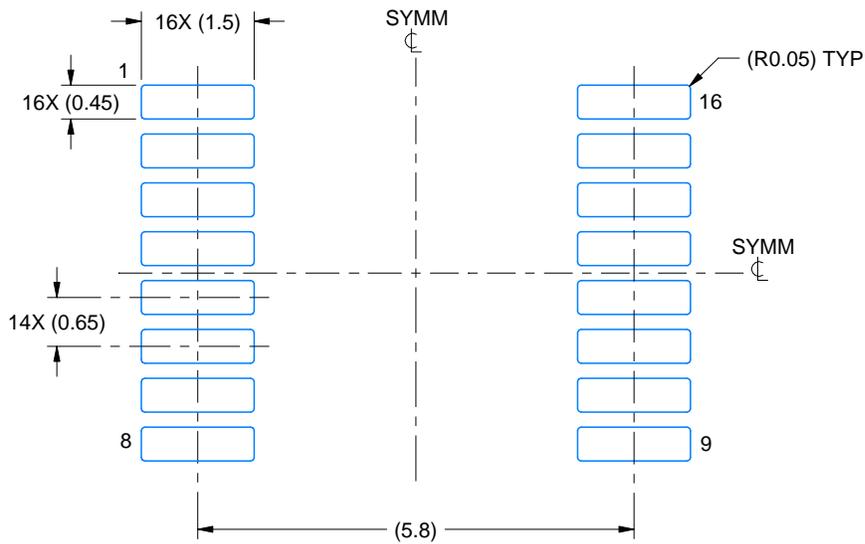
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

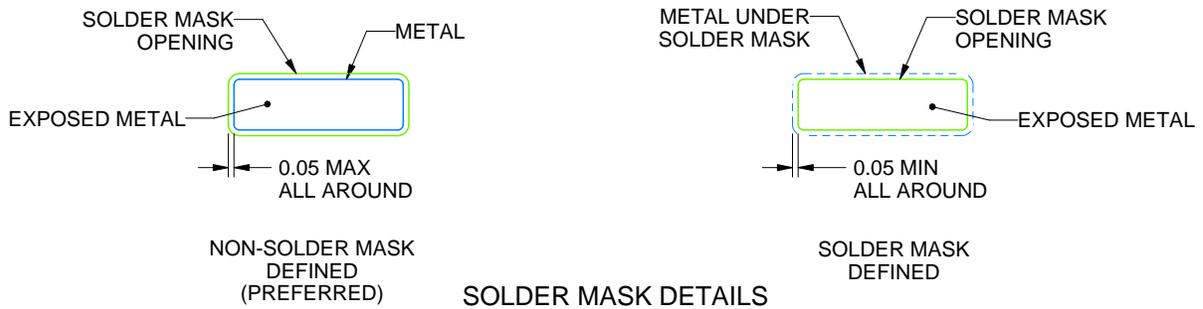
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

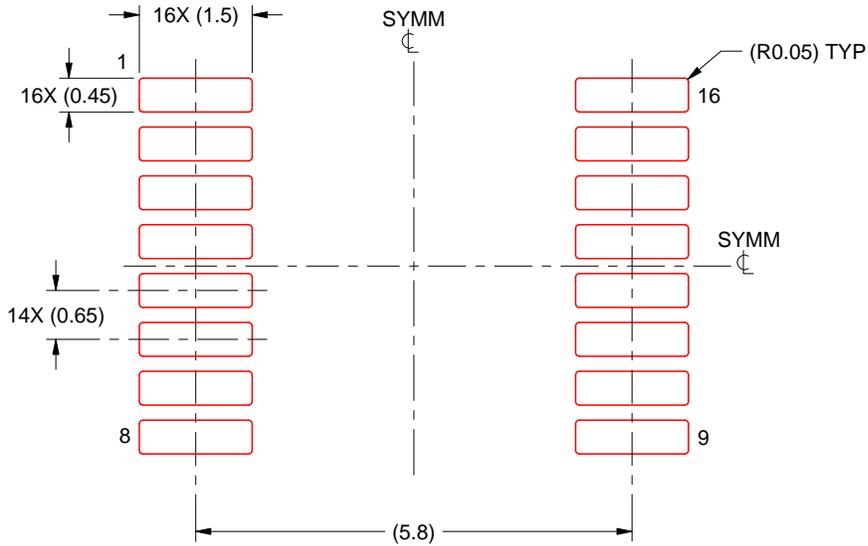
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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