

# B-Suffix Series CMOS Gates

MC14001B, MC14011B, MC14023B,  
MC14025B, MC14071B, MC14073B,  
MC14081B, MC14082B

## MC14001B Series

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

### Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

| Symbol            | Parameter                                                                          | Value                  | Unit |
|-------------------|------------------------------------------------------------------------------------|------------------------|------|
| $V_{DD}$          | DC Supply Voltage Range                                                            | -0.5 to +18.0          | V    |
| $V_{in}, V_{out}$ | Input or Output Voltage Range (DC or Transient)                                    | -0.5 to $V_{DD} + 0.5$ | V    |
| $I_{in}, I_{out}$ | Input or Output Current (DC or Transient) per Pin                                  | $\pm 10$               | mA   |
| $P_D$             | Power Dissipation, per Package (Note 1)                                            | 500                    | mW   |
| $T_A$             | Ambient Temperature Range                                                          | -55 to +125            | °C   |
| $T_{stg}$         | Storage Temperature Range                                                          | -65 to +150            | °C   |
| $T_L$             | Lead Temperature (8-Second Soldering)                                              | 260                    | °C   |
| $V_{ESD}$         | ESD Withstand Voltage<br>Human Body Model<br>Machine Model<br>Charged Device Model | > 3000<br>> 300<br>N/A | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65 °C to 125 °C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

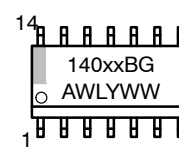


SOIC-14  
D SUFFIX  
CASE 751A

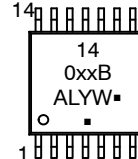


TSSOP-14  
DT SUFFIX  
CASE 948G

### MARKING DIAGRAMS



SOIC-14



TSSOP-14

xx = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### DEVICE INFORMATION

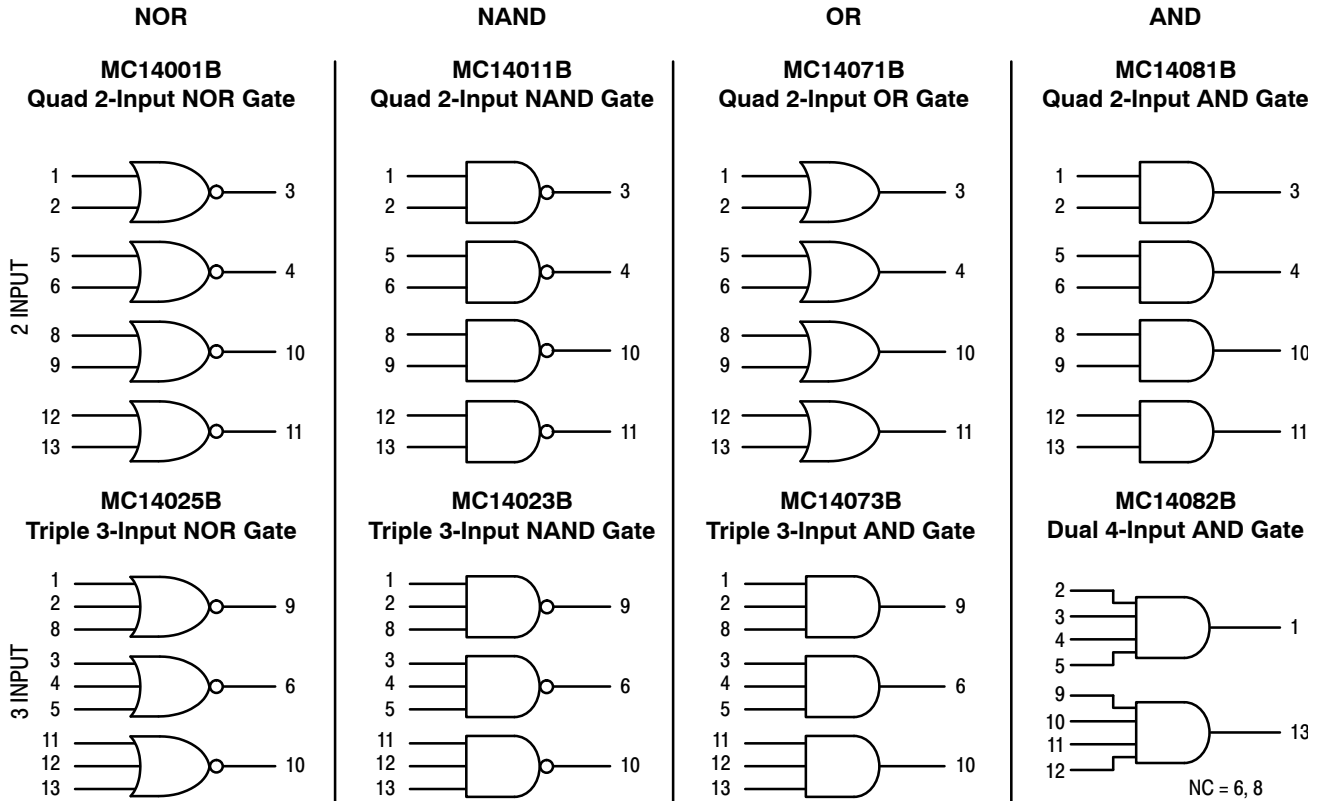
| Device   | Description              |
|----------|--------------------------|
| MC14001B | Quad 2-Input NOR Gate    |
| MC14011B | Quad 2-Input NAND Gate   |
| MC14023B | Triple 3-Input NAND Gate |
| MC14025B | Triple 3-Input NOR Gate  |
| MC14071B | Quad 2-Input OR Gate     |
| MC14073B | Triple 3-Input AND Gate  |
| MC14081B | Quad 2-Input AND Gate    |
| MC14082B | Dual 4-Input AND Gate    |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

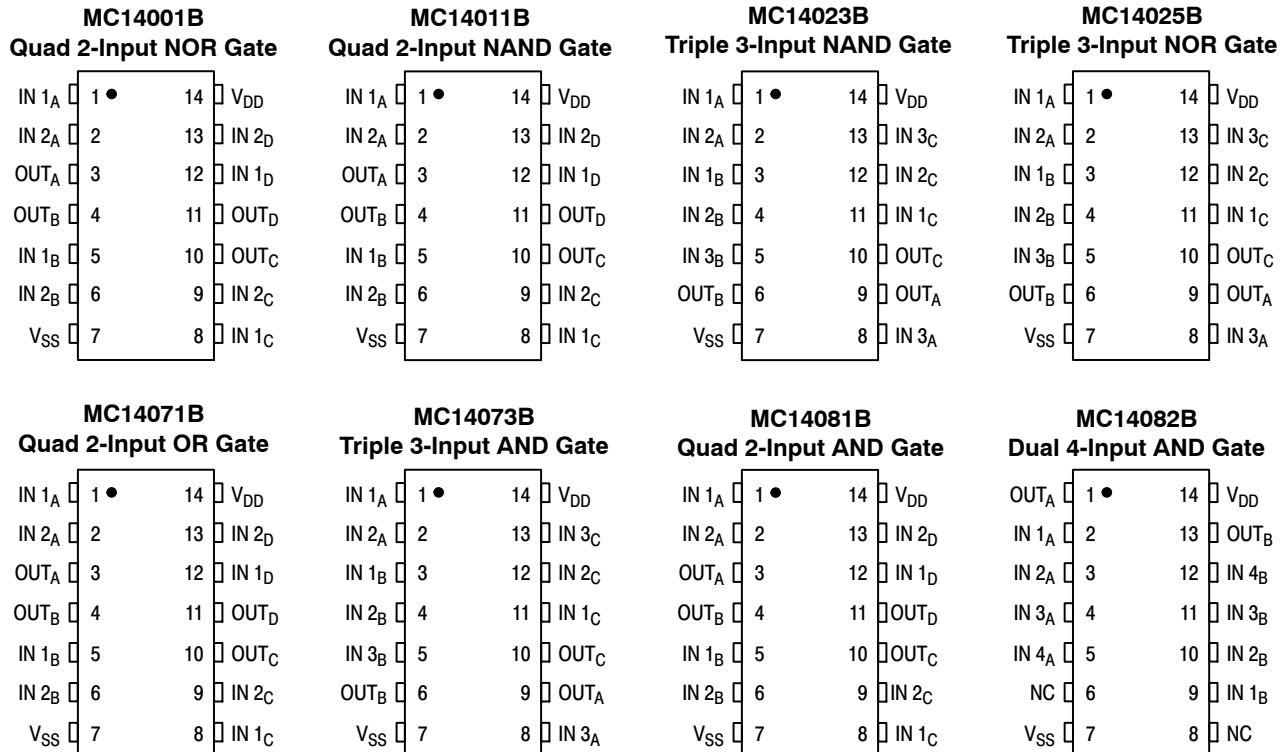
# MC14001B Series

## LOGIC DIAGRAMS



$V_{DD}$  = PIN 14  
 $V_{SS}$  = PIN 7  
 FOR ALL DEVICES

## PIN ASSIGNMENTS



NC = NO CONNECTION

# MC14001B Series

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

| Characteristic                                                                                                                                           | Symbol          | V <sub>DD</sub><br>Vdc | -55 °C                                                                                                                                                               |                      | 25 °C                         |                                |                      | 125 °C                        |                      | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-------------------------------|--------------------------------|----------------------|-------------------------------|----------------------|------|
|                                                                                                                                                          |                 |                        | Min                                                                                                                                                                  | Max                  | Min                           | Typ<br>(Note 2)                | Max                  | Min                           | Max                  |      |
| Output Voltage "0" Level<br>V <sub>in</sub> = V <sub>DD</sub> or 0                                                                                       | V <sub>OL</sub> | 5.0<br>10<br>15        | –<br>–<br>–                                                                                                                                                          | 0.05<br>0.05<br>0.05 | –<br>–<br>–                   | 0<br>0<br>0                    | 0.05<br>0.05<br>0.05 | –<br>–<br>–                   | 0.05<br>0.05<br>0.05 | Vdc  |
| V <sub>in</sub> = 0 or V <sub>DD</sub> "1" Level                                                                                                         | V <sub>OH</sub> | 5.0<br>10<br>15        | 4.95<br>9.95<br>14.95                                                                                                                                                | –<br>–<br>–          | 4.95<br>9.95<br>14.95         | 5.0<br>10<br>15                | –<br>–<br>–          | 4.95<br>9.95<br>14.95         | –<br>–<br>–          | Vdc  |
| Input Voltage "0" Level<br>(V <sub>O</sub> = 4.5 or 0.5 Vdc)<br>(V <sub>O</sub> = 9.0 or 1.0 Vdc)<br>(V <sub>O</sub> = 13.5 or 1.5 Vdc)                  | V <sub>IL</sub> | 5.0<br>10<br>15        | –<br>–<br>–                                                                                                                                                          | 1.5<br>3.0<br>4.0    | –<br>–<br>–                   | 2.25<br>4.50<br>6.75           | 1.5<br>3.0<br>4.0    | –<br>–<br>–                   | 1.5<br>3.0<br>4.0    | Vdc  |
| "1" Level<br>(V <sub>O</sub> = 0.5 or 4.5 Vdc)<br>(V <sub>O</sub> = 1.0 or 9.0 Vdc)<br>(V <sub>O</sub> = 1.5 or 13.5 Vdc)                                | V <sub>IH</sub> | 5.0<br>10<br>15        | 3.5<br>7.0<br>11                                                                                                                                                     | –<br>–<br>–          | 3.5<br>7.0<br>11              | 2.75<br>5.50<br>8.25           | –<br>–<br>–          | 3.5<br>7.0<br>11              | –<br>–<br>–          | Vdc  |
| Output Drive Current<br>(V <sub>OH</sub> = 2.5 Vdc) Source<br>(V <sub>OH</sub> = 4.6 Vdc)<br>(V <sub>OH</sub> = 9.5 Vdc)<br>(V <sub>OH</sub> = 13.5 Vdc) | I <sub>OH</sub> | 5.0<br>5.0<br>10<br>15 | –3.0<br>–0.64<br>–1.6<br>–4.2                                                                                                                                        | –<br>–<br>–<br>–     | –2.4<br>–0.51<br>–1.3<br>–3.4 | –4.2<br>–0.88<br>–2.25<br>–8.8 | –<br>–<br>–<br>–     | –1.7<br>–0.36<br>–0.9<br>–2.4 | –<br>–<br>–<br>–     | mAdc |
| (V <sub>OL</sub> = 0.4 Vdc) Sink<br>(V <sub>OL</sub> = 0.5 Vdc)<br>(V <sub>OL</sub> = 1.5 Vdc)                                                           | I <sub>OL</sub> | 5.0<br>10<br>15        | 0.64<br>1.6<br>4.2                                                                                                                                                   | –<br>–<br>–          | 0.51<br>1.3<br>3.4            | 0.88<br>2.25<br>8.8            | –<br>–<br>–          | 0.36<br>0.9<br>2.4            | –<br>–<br>–          | mAdc |
| Input Current                                                                                                                                            | I <sub>in</sub> | 15                     | –                                                                                                                                                                    | ±0.1                 | –                             | ±0.00001                       | ±0.1                 | –                             | ±1.0                 | μAdc |
| Input Capacitance<br>(V <sub>in</sub> = 0)                                                                                                               | C <sub>in</sub> | –                      | –                                                                                                                                                                    | –                    | –                             | 5.0                            | 7.5                  | –                             | –                    | pF   |
| Quiescent Current<br>(Per Package)                                                                                                                       | I <sub>DD</sub> | 5.0<br>10<br>15        | –<br>–<br>–                                                                                                                                                          | 0.25<br>0.5<br>1.0   | –<br>–<br>–                   | 0.0005<br>0.0010<br>0.0015     | 0.25<br>0.5<br>1.0   | –<br>–<br>–                   | 7.5<br>15<br>30      | μAdc |
| Total Supply Current (Notes 3, 4)<br>(Dynamic plus Quiescent,<br>Per Gate, C <sub>L</sub> = 50 pF)                                                       | I <sub>T</sub>  | 5.0<br>10<br>15        | I <sub>T</sub> = (0.3 μA/kHz) f + I <sub>DD</sub> /N<br>I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub> /N<br>I <sub>T</sub> = (0.9 μA/kHz) f + I <sub>DD</sub> /N |                      |                               |                                |                      |                               |                      | μAdc |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25 °C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> – V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

# MC14001B Series

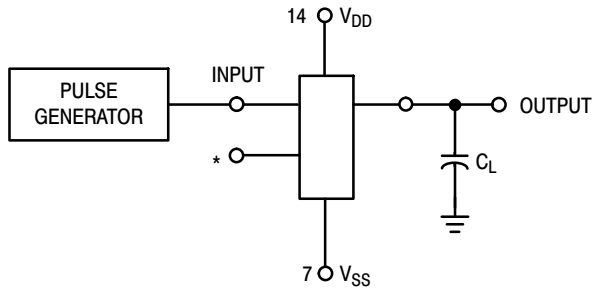
## B-SERIES GATE SWITCHING TIMES

### SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ \text{C}$ )

| Characteristic                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Symbol             | $V_{DD}$<br>Vdc                                               | Min                                               | Typ<br>(Note 6)                                               | Max                                                                | Unit |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------------------------------------------------------|---------------------------------------------------|---------------------------------------------------------------|--------------------------------------------------------------------|------|
| Output Rise Time, All B-Series Gates<br>$t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$<br>$t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$<br>$t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | $t_{TLH}$          | 5.0<br>10<br>15                                               | —<br>—<br>—                                       | 100<br>50<br>40                                               | 200<br>100<br>80                                                   | ns   |
| Output Fall Time, All B-Series Gates<br>$t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$<br>$t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$<br>$t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | $t_{THL}$          | 5.0<br>10<br>15                                               | —<br>—<br>—                                       | 100<br>50<br>40                                               | 200<br>100<br>80                                                   | ns   |
| Propagation Delay Time<br>MC14001B, MC14011B only<br>$t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 80 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 32 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 27 \text{ ns}$<br>All Other 2, 3, and 4 Input Gates<br>$t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 115 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 47 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 37 \text{ ns}$<br>8-Input Gates (MC14068B, MC14078B)<br>$t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 155 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 62 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$ | $t_{PLH}, t_{PHL}$ | 5.0<br>10<br>15<br><br>5.0<br>10<br>15<br><br>5.0<br>10<br>15 | —<br>—<br>—<br><br>—<br>—<br>—<br><br>—<br>—<br>— | 125<br>50<br>40<br><br>160<br>65<br>50<br><br>200<br>80<br>60 | 250<br>100<br>80<br><br>300<br>130<br>100<br><br>350<br>150<br>110 | ns   |

5. The formulas given are for the typical characteristics only at  $25^\circ \text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



\* All unused inputs of AND, NAND gates must be connected to  $V_{DD}$ .  
All unused inputs of OR, NOR gates must be connected to  $V_{SS}$ .

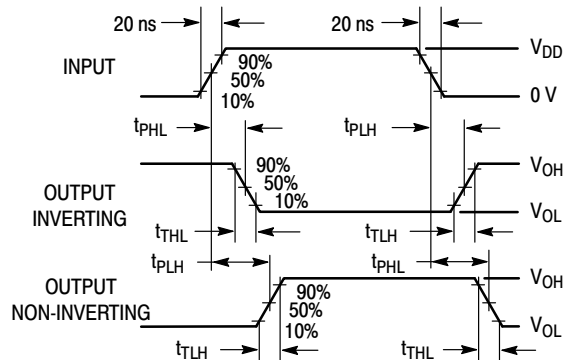
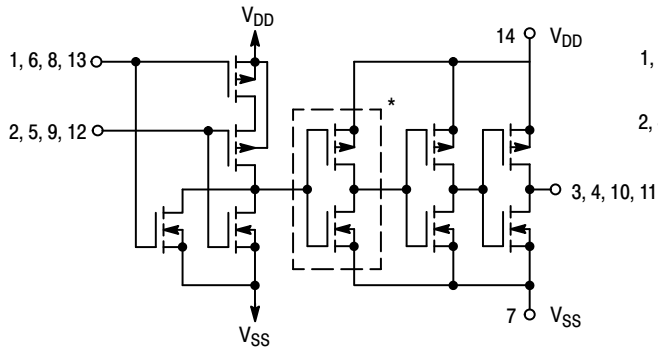


Figure 1. Switching Time Test Circuit and Waveforms

## MC14001B Series

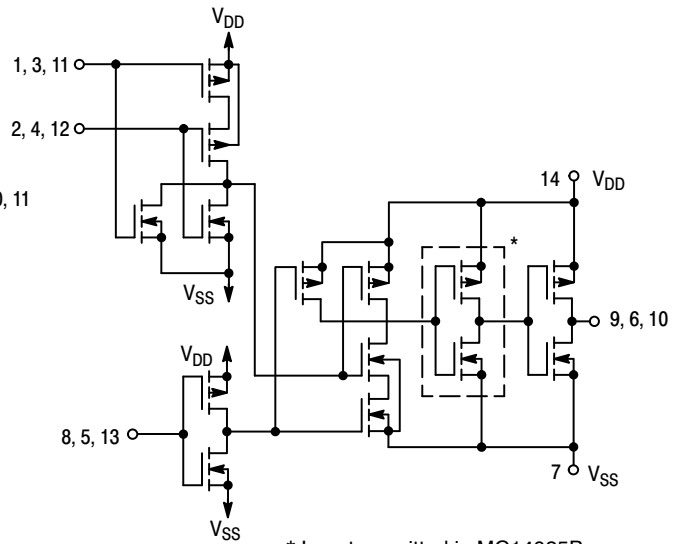
### CIRCUIT SCHEMATIC NOR, OR GATES

**MC14001B, MC14071B**  
One of Four Gates Shown



\* Inverter omitted in MC14001B

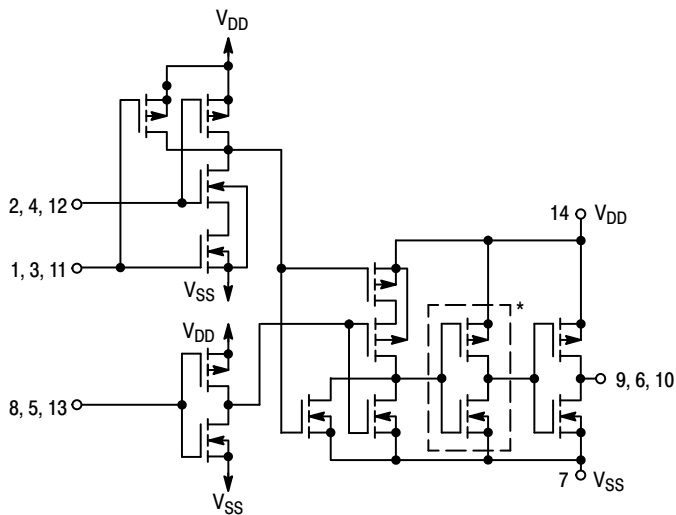
**MC14025B**  
One of Three Gates Shown



\* Inverter omitted in MC14025B

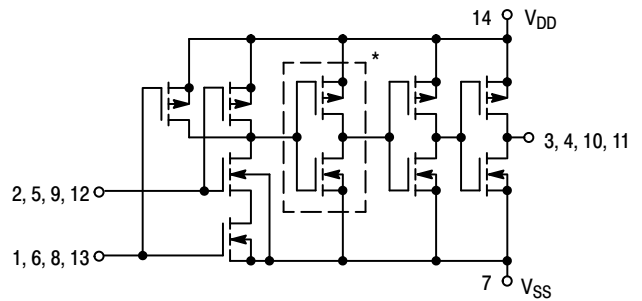
### CIRCUIT SCHEMATIC NAND, AND GATES

**MC14023B, MC14073B**  
One of Three Gates Shown



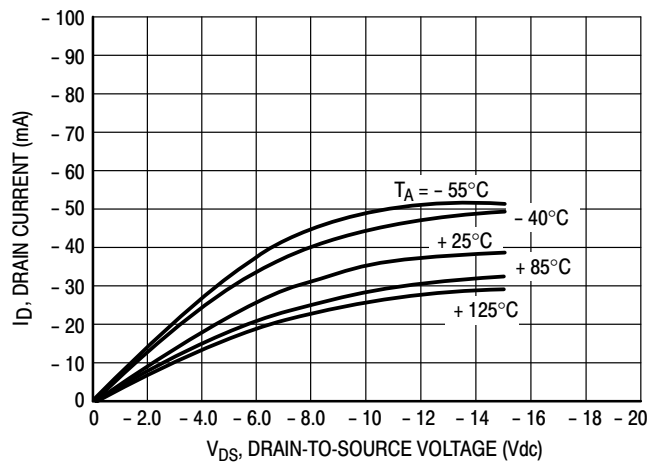
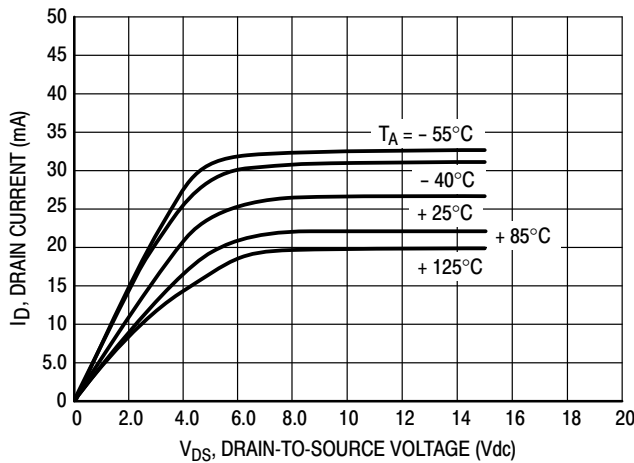
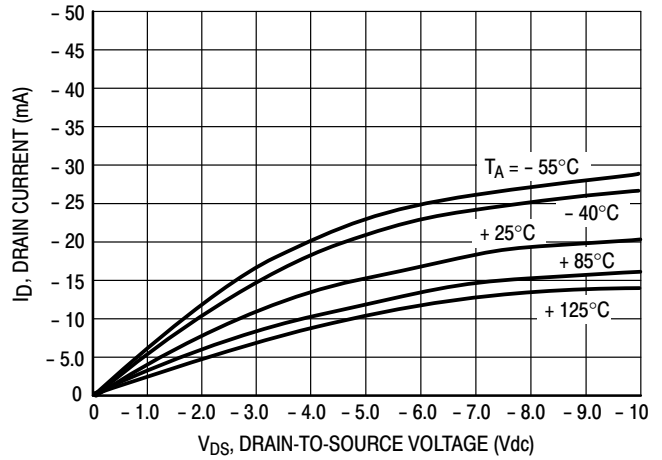
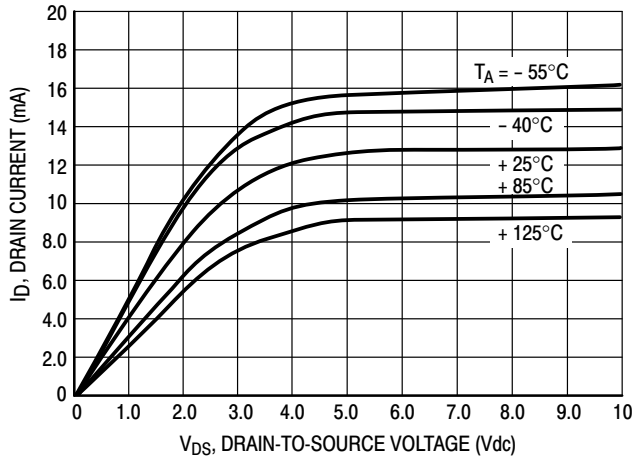
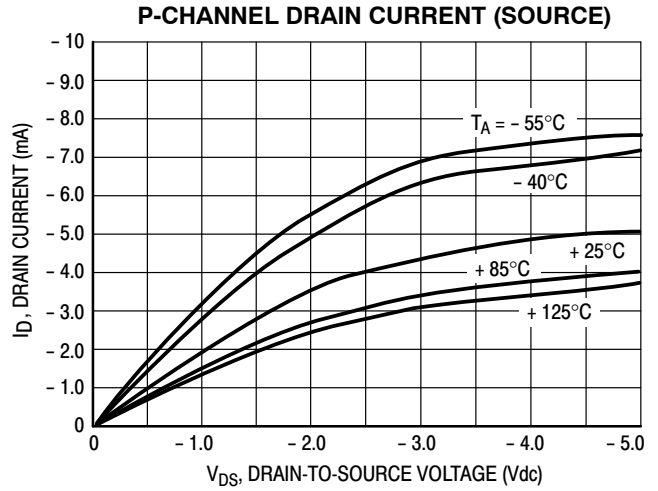
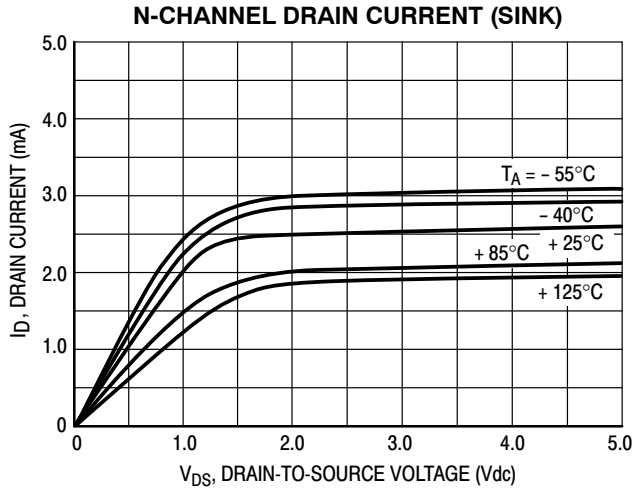
\* Inverter omitted in MC14023B

**MC14011B, MC14081B**  
One of Four Gates Shown



\* Inverter omitted in MC14011B

TYPICAL B-SERIES GATE CHARACTERISTICS



These typical curves are not guarantees, but are design aids.  
Caution: The maximum rating for output current is 10 mA per pin.

# MC14001B Series

## TYPICAL B-SERIES GATE CHARACTERISTICS (CONT'D)

### VOLTAGE TRANSFER CHARACTERISTICS

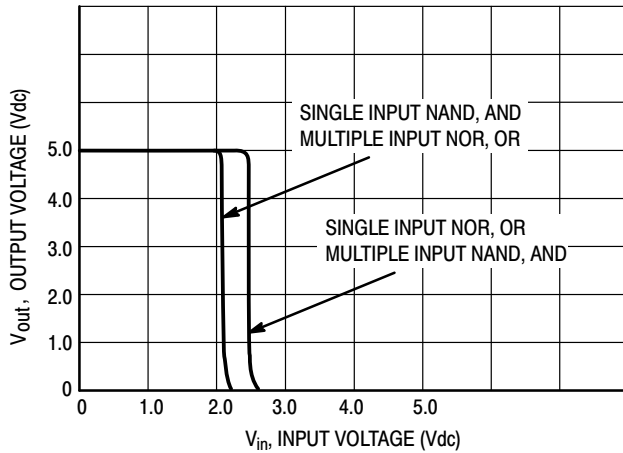


Figure 8.  $V_{DD} = 5.0 \text{ Vdc}$

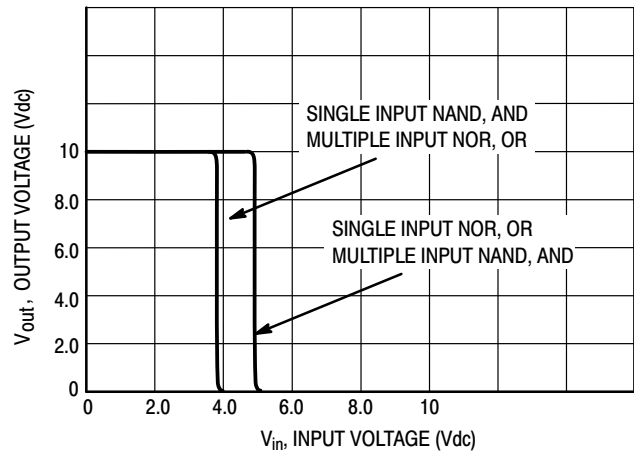


Figure 9.  $V_{DD} = 10 \text{ Vdc}$

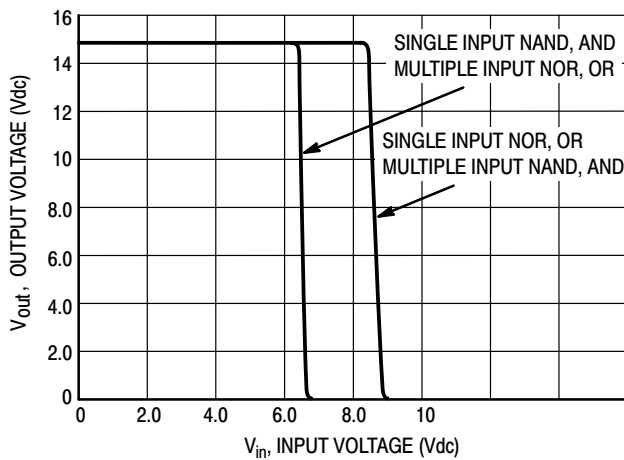


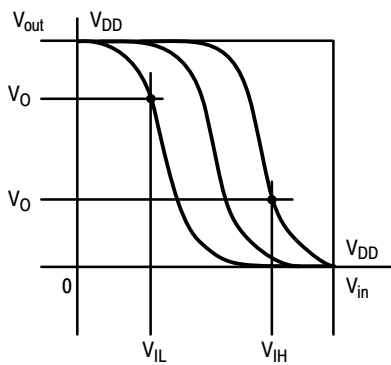
Figure 10.  $V_{DD} = 15 \text{ Vdc}$

### DC NOISE MARGIN

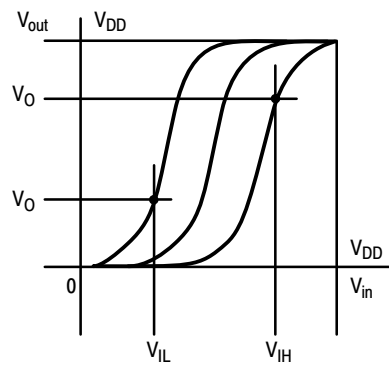
The DC noise margin is defined as the input voltage range from an ideal “1” or “0” input level which does not produce output state change(s). The typical and guaranteed limit values of the input values  $V_{IL}$  and  $V_{IH}$  for the output(s) to be at a fixed voltage  $V_O$  are given in the Electrical Characteristics table.  $V_{IL}$  and  $V_{IH}$  are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the “1” and “0” levels =

- 1.0 V with a 5.0 V supply
- 2.0 V with a 10.0 V supply
- 2.5 V with a 15.0 V supply



(a) Inverting Function



(b) Non-Inverting Function

Figure 11. DC Noise Immunity

## MC14001B Series

### ORDERING INFORMATION

| Device          | Package                | Shipping <sup>†</sup>    |
|-----------------|------------------------|--------------------------|
| MC14001BDG      | SOIC-14<br>(Pb-Free)   | 55 Units / Rail          |
| NLV14001BDG*    |                        |                          |
| MC14001BDR2G    | SOIC-14<br>(Pb-Free)   | 2500 Units / Tape & Reel |
| NLV14001BDR2G*  |                        |                          |
| MC14001BDTR2G   | TSSOP-14<br>(Pb-Free)  |                          |
| NLV14001BDTR2G* |                        |                          |
| MC14001BFELG    | SOEIAJ-14<br>(Pb-Free) | 2000 Units / Tape & Reel |

|                 |                        |                          |
|-----------------|------------------------|--------------------------|
| MC14011BDG      | SOIC-14<br>(Pb-Free)   | 55 Units / Rail          |
| NLV14011BDG*    |                        |                          |
| MC14011BDR2G    | SOIC-14<br>(Pb-Free)   | 2500 Units / Tape & Reel |
| NLV14011BDR2G*  |                        |                          |
| MC14011BDTR2G   | TSSOP-14<br>(Pb-Free)  |                          |
| NLV14011BDTR2G* |                        |                          |
| MC14011BFG      | SOEIAJ-14<br>(Pb-Free) | 50 Units / Rail          |
| MC14011BFELG    |                        | 2000 Units / Tape & Reel |

|                |                        |                          |
|----------------|------------------------|--------------------------|
| MC14023BDG     | SOIC-14<br>(Pb-Free)   | 55 Units / Rail          |
| MC14023BDR2G   | SOIC-14<br>(Pb-Free)   | 2500 Units / Tape & Reel |
| NLV14023BDR2G* |                        |                          |
| MC14023BFELG   | SOEIAJ-14<br>(Pb-Free) | 2000 Units / Tape & Reel |

|                |                      |                          |
|----------------|----------------------|--------------------------|
| MC14025BDG     | SOIC-14<br>(Pb-Free) | 55 Units / Rail          |
| NLV14025BDG*   |                      |                          |
| MC14025BDR2G   | SOIC-14<br>(Pb-Free) | 2500 Units / Tape & Reel |
| NLV14025BDR2G* |                      |                          |

|                 |                       |                          |
|-----------------|-----------------------|--------------------------|
| MC14071BDG      | SOIC-14<br>(Pb-Free)  | 55 Units / Rail          |
| NLV14071BDG*    |                       |                          |
| MC14071BDR2G    | SOIC-14<br>(Pb-Free)  | 2500 Units / Tape & Reel |
| NLV14071BDR2G*  |                       |                          |
| MC14071BDTG     | TSSOP-14<br>(Pb-Free) | 96 Units per Rail        |
| MC14071BDTR2G   |                       | 2500 Units / Tape & Reel |
| NLV14071BDTR2G* |                       |                          |

|              |                      |                          |
|--------------|----------------------|--------------------------|
| MC14073BDG   | SOIC-14<br>(Pb-Free) | 55 Units / Rail          |
| MC14073BDR2G | SOIC-14<br>(Pb-Free) | 2500 Units / Tape & Reel |



## MC14001B Series

### ORDERING INFORMATION (continued)

| Device          | Package               | Shipping <sup>†</sup>    |
|-----------------|-----------------------|--------------------------|
| MC14081BDG      | SOIC-14<br>(Pb-Free)  | 55 Units / Rail          |
| NLV14081BDG*    |                       |                          |
| MC14081BDR2G    | SOIC-14<br>(Pb-Free)  | 2500 Units / Tape & Reel |
| NLV14081BDR2G*  |                       |                          |
| MC14081BDTR2G   | TSSOP-14<br>(Pb-Free) |                          |
| NLV14081BDTR2G* |                       |                          |

|                |                      |                          |
|----------------|----------------------|--------------------------|
| MC14082BDG     | SOIC-14<br>(Pb-Free) | 55 Units / Rail          |
| NLV14082BDG*   |                      |                          |
| MC14082BDR2G   |                      | 2500 Units / Tape & Reel |
| NLV14082BDR2G* |                      |                          |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

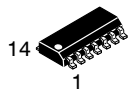
\* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

## MC14001B Series

### REVISION HISTORY

| Revision | Description of Changes                                       | Date       |
|----------|--------------------------------------------------------------|------------|
| 13       | Adding NLV14082BDR2G device into Ordering Information table. | 11/14/2025 |

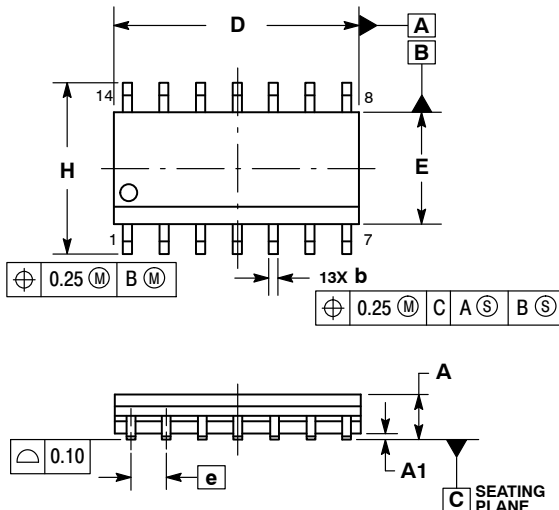
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

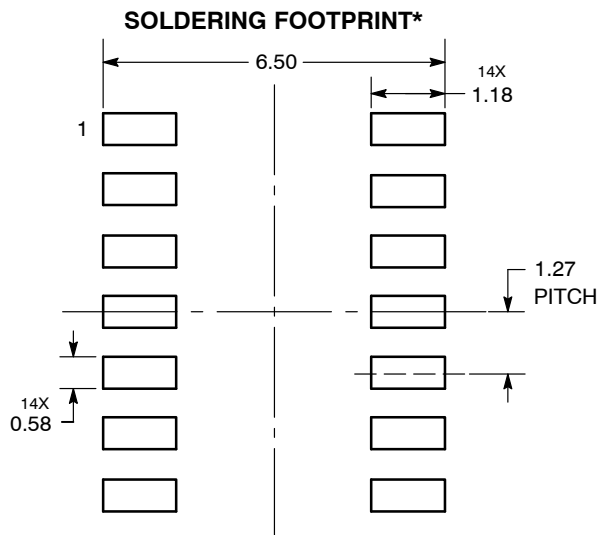
DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

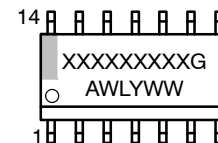
| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42565B | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-14 NB  | PAGE 1 OF 2                                                                                                                                                                         |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

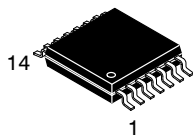
STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

|                         |                    |                                                                                                                                                                                     |
|-------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42565B</b> | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-14 NB</b>  | <b>PAGE 2 OF 2</b>                                                                                                                                                                  |

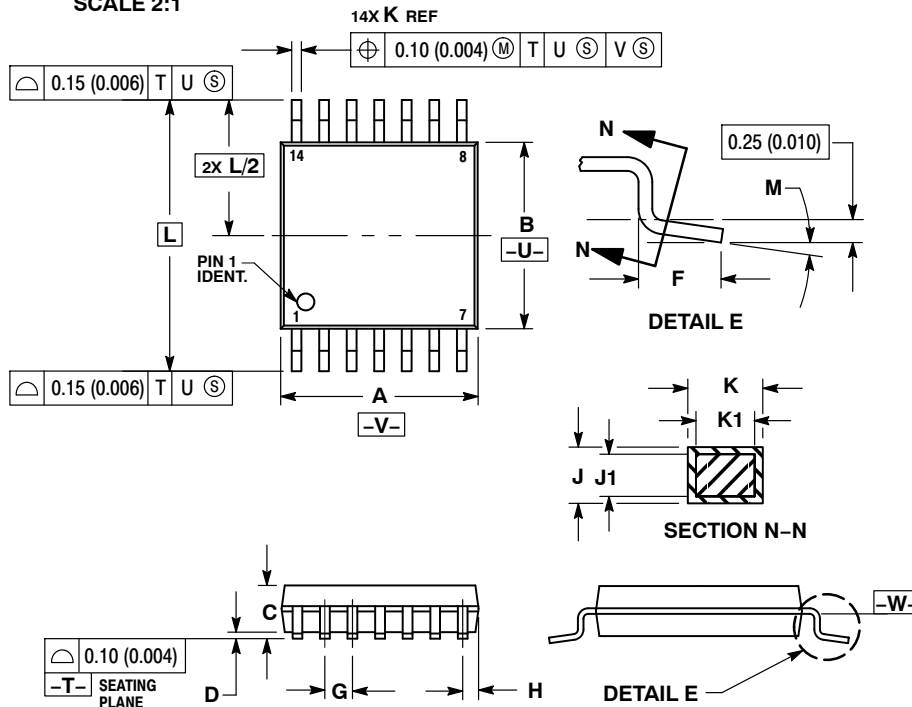
**onsemi** and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



TSSOP-14 WB  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

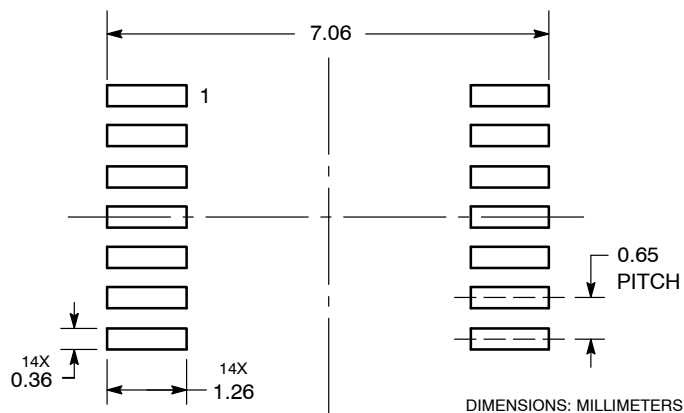


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

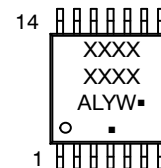
| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

RECOMMENDED  
SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER: 98ASH70246A

Electronic versions are uncontrolled except when accessed directly from the Document Repository.  
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: TSSOP-14 WB

PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)