

### DESCRIPTION

The MPM3683-20 is an easy-to-use, fully integrated, step-down DC/DC power module. The MPM3683-20 offers a complete power solution that achieves up to 20A of peak current. It integrates a DC/DC converter, power inductor, and passive components. The MPM3683-20 can deliver the output current ( $I_{OUT}$ ) across a wide input voltage ( $V_{IN}$ ) supply range, with excellent load and line regulation.

The MPM3683-20 uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization.

The operating switching frequency ( $f_{SW}$ ) can be set to 600kHz, 800kHz, or 1000kHz with the MODE pin. This allows  $f_{SW}$  to remain constant, regardless of  $V_{IN}$  or the output voltage ( $V_{OUT}$ ).

The MPM3683-20 features a configurable soft-start time ( $t_{SS}$ ) with one capacitor. An open-drain power good (PG) signal indicates whether  $V_{OUT}$  is within the nominal voltage range.

The MPM3683-20 has fully integrated, non-latch protection features including over-current protection (OCP), over-voltage protection (OVP), and over-temperature protection (OTP).

The MPM3683-20 is available in a compact FCM LGA-29 (7mmx7mmx4.4mm) package.

### FEATURES

- Wide Input Voltage ( $V_{IN}$ ) Range:
  - 2.7V to 16V with External 3.3V  $V_{CC}$
  - 4V to 16V with Internal or External  $V_{CC}$
- Output Voltage ( $V_{OUT}$ ) Range: 0.6V to 5.5V
- 15A Continuous Output Current ( $I_{OUT}$ ) with a 20A Peak <sup>(1)</sup>
- Differential  $V_{OUT}$  Remote Sense
- Adaptive Constant-On-Time (COT) for Ultra-Fast Transient Response
- Selectable Pulse-Skip Mode (PSM) or Forced Continuous Conduction Mode (FCCM)
- $V_{OUT}$  Tracking
- PG Active-Clamped to Low Level during Power Failure
- Configurable Soft-Start Time ( $t_{SS}$ )
- Pre-Biased Start-Up
- Selectable Switching Frequency ( $f_{SW}$ ) from 600kHz, 800kHz, and 1000kHz
- Non-Latch Over-Current Protection (OCP), Under-Voltage Lockout (UVLO), Over-Temperature Protection (OTP), and Over-Voltage Protection (OVP)
- Available in an FCM LGA-29 (7mmx7mmx4.4mm) Package

### APPLICATIONS

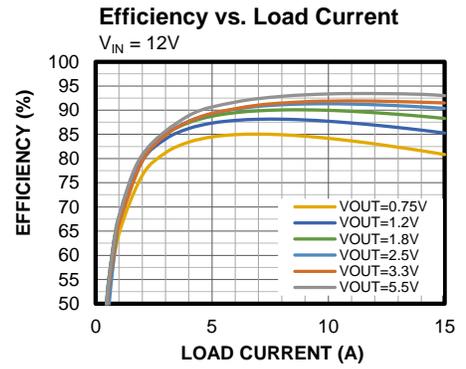
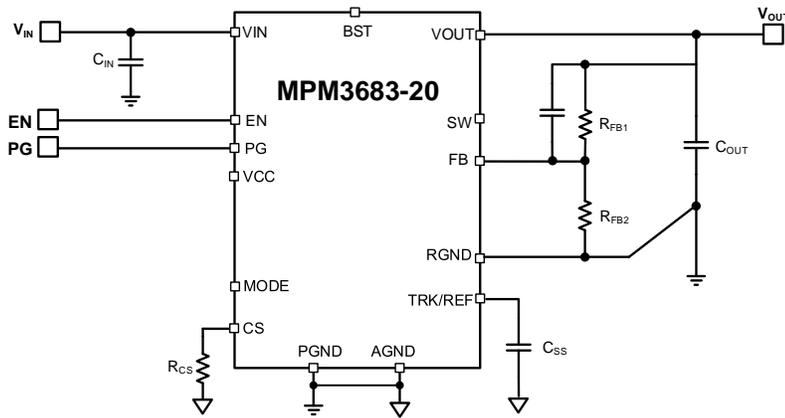
- Telecom and Networking Systems
- Base Stations
- Industrial Systems
- Servers and Storage
- FPGA and ASIC Cards

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**Note:**

- 1) It is recommended that the maximum continuous output current ( $I_{OUT}$ ) be kept below 10A when  $V_{OUT}$  exceeds 3.3V.

### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3683GMN-20	LGA-29 (7mmx7mmx4.4mm)	See Below	3

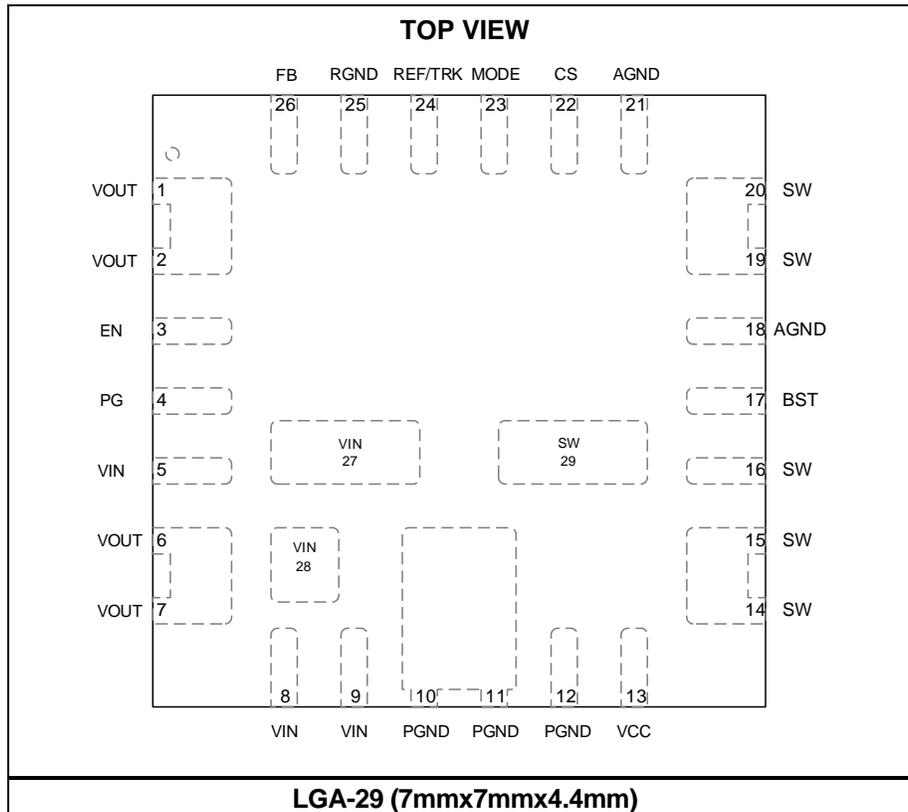
\* For tray, add suffix -T (e.g. MPM3683GMN-20-T).

### TOP MARKING

**MPS YYWW**  
**MP3683-20**  
**LLLLLLLLLL**  
**M**

MPS: MPS prefix  
 YY: Year code  
 WW: Week code  
 MP3683-20: Part number  
 LLLLLLLLLL: Lot number  
 M: Module

### PACKAGE REFERENCE



**PIN FUNCTIONS**

Pin #	Name	Description
1, 2, 6, 7	VOUT	<b>Module voltage output node.</b>
3	EN	<b>Enable.</b> The EN pin is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistor divider for automatic start-up. Do not float EN.
4	PG	<b>Power good output.</b> PG is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate a logic high signal if the output voltage ( $V_{OUT}$ ) is within regulation. There is a delay of about 0.9ms between the time $V_{FB} > 92.5\%V_{REF}$ and PG pulling high.
5, 8, 9, 27, 28	VIN	<b>Input voltage.</b> The VIN pin supplies power for the internal MOSFET and regulator. Place input capacitors at VIN to decouple the input rail. Use wide PCB traces to make the VIN connection.
10, 11, 12	PGND	<b>System ground.</b> The PGND pin is the reference ground of the regulated output voltage, and requires careful consideration during the PCB layout. Use wide PCB traces to make the PGND connection.
13	VCC	<b>Internal 3.3V LDO output.</b> The driver and control circuits are powered from the VCC pin's voltage. The module integrates a 1 $\mu$ F capacitor, and does not require an additional external capacitor.
14, 15, 16, 19, 20, 29	SW	<b>Switch output.</b> It is recommended to place a large copper plane on SW to improve thermal performance.
17	BST	<b>Bootstrap.</b> There is an internal, integrated bootstrap capacitor between the BST pin and SW pin, and does not require an external connection.
18, 21	AGND	<b>Analog ground.</b> Select AGND as the control circuit reference point.
22	CS	<b>Current limit.</b> Connect a resistor from CS to ground to set the current limit tripping point. The module integrates a 24.9k $\Omega$ resistor from CS to AGND.
23	MODE	<b>Operation mode selection.</b> Configure the MODE pin to select forced continuous conduction mode (FCCM), pulse-skip mode (PSM), and set the operating switching frequency. See Table 1 on page 15 for more details.
24	TRK/REF	<b>External tracking voltage input.</b> The output voltage tracks the TRK/REF input signal. Decouple TRK/REF with a ceramic capacitor, placed as close to TRK/REF as possible. The capacitance of this capacitor determines the soft-start time ( $t_{SS}$ ). See the Soft Start (SS) section on page 15 for more details.
25	RGND	<b>Differential remote sense negative input.</b> Directly connect RGND to the negative side of the voltage sense point. Short RGND to GND if the remote sense function is not used.
26	FB	<b>Feedback (differential remote sense positive input).</b> An external resistor divider from the output to RGND (tapped to FB) sets $V_{OUT}$ . It is recommended to place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.

**ABSOLUTE MAXIMUM RATINGS** <sup>(2)</sup>

Supply voltage ( $V_{IN}$ to GND) .....	-0.3V to +18V
$V_{SW}$ to GND (DC) .....	-0.3V to $V_{IN} + 0.3V$
$V_{SW}$ to GND (25ns).....	-5V to +25V
$V_{CC}$ .....	4.5V
$V_{OUT}$ .....	6V
All other pins .....	-0.3V to +4.3V
Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(7)</sup>	9.25W
Junction temperature .....	170°C
Lead temperature .....	260°C
Storage temperature .....	-55°C to +170°C

**ESD Ratings**

Human body model (HBM) .....	±2kV
Charged device model (CDM) .....	±2kV

**Recommended Operating Conditions** <sup>(3)</sup>

Supply input voltage ( $V_{IN}$ ) .....	4V to 16V
$V_{IN}$ (DC) - $V_{SW}$ (DC) .....	-0.3V to $V_{IN} + 0.3V$
$V_{SW}$ (DC) .....	-0.3V to $V_{IN} + 0.3V$
Output voltage ( $V_{OUT}$ ).....	0.6V to 5.5V
External VCC bias ( $V_{CC\_EXT}$ ).....	3.12V to 3.6V
EN voltage <sup>(4)</sup> ( $V_{EN}$ ).....	3.6V
Operating junction temp ( $T_J$ )....	-40°C to +125°C

**Thermal Resistance** <sup>(5) (6) (7) (8) (9)</sup>

LGA-29 (7mmx7mmx4.4mm)	
$\theta_{JA}$ .....	15.67°C/W
$\theta_{JC\_TOP}$ .....	3.11°C/W
$\theta_{JB}$ .....	7.7°C/W

**Notes:**

- 2) Exceeding these ratings may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) The EN pin has an embedded Zener diode to clamp the voltage at 3.6V. See the EN Configuration section on page 17 for the current limit.
- 5)  $\theta_{JA}$  is the junction-to-ambient thermal resistance,  $\theta_{JC\_TOP}$  is the junction-to-case top thermal characterization parameter, and  $\theta_{JB}$  is the junction-to-board thermal characterization parameter.
- 6) The thermal parameter is based on tests on MPS's evaluation board (EVM3683-20-MN-00B) under no airflow cooling conditions in a standard enclosure. The board size is 6.1cmx6.1cm, 6-layer.
- 7) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature.
- 8) The junction-to-case top thermal characterization parameter,  $\theta_{JC\_TOP}$ , estimates the junction temperature in the real system, based on the equation  $T_J = \theta_{JC\_TOP} \times P_{LOSS} + T_{CASE\_TOP}$ . Where  $P_{LOSS}$  is the module's entire power loss in a real application, and  $T_{CASE\_TOP}$  is the case top temperature.
- 9) The junction-to-board thermal characterization parameter,  $\theta_{JB}$ , estimates the junction temperature in the real system, based on equation  $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$ . Where  $P_{LOSS}$  is the module's entire power loss in a real application, and  $T_{BOARD}$  is the board temperature.

## ELECTRICAL CHARACTERISTICS

Typical value is tested at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 1.2\text{V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  <sup>(10)</sup>, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Supply Current</b>						
Supply current (shutdown)	$I_S$	$V_{EN} = 0\text{V}$		10	20	$\mu\text{A}$
Supply current (quiescent)	$I_Q$	$V_{EN} = 2\text{V}$ , $V_{FB} = 0.62\text{V}$		650	850	$\mu\text{A}$
<b>MOSFET</b>						
Switch leakage	$SW_{LKG\_HS}$	$V_{EN} = 0\text{V}$ , $V_{SW} = 0\text{V}$		0	10	$\mu\text{A}$
	$SW_{LKG\_LS}$	$V_{EN} = 0\text{V}$ , $V_{SW} = 12\text{V}$		0	30	
High-side (HS) on resistance	$R_{DS\_ON\_HS}$	$V_{EN} = 2\text{V}$ at $25^\circ\text{C}$		8.6		$\text{m}\Omega$
Low-side (LS) on resistance	$R_{DS\_ON\_LS}$	$V_{EN} = 2\text{V}$ at $25^\circ\text{C}$		2.5		$\text{m}\Omega$
<b>Current Limit</b>						
Current limit threshold	$V_{LIM}$		1.15	1.2	1.25	V
$I_{CS}$ to $I_{OUT}$ ratio	$I_{CS}/I_{OUT}$	$I_{OUT} \geq 2\text{A}$	9	10	11	$\mu\text{A}/\text{A}$
Low-side negative current limit	$I_{LIM\_NEG}$			-18		A
Negative current limit timeout <sup>(11)</sup>	$t_{NCL\_TIMER}$			200		ns
<b>Switching Frequency</b>						
Switching frequency <sup>(10)</sup>	$f_{SW}$	MODE = GND, $I_{OUT} = 0\text{A}$ , $V_{OUT} = 1\text{V}$	480	600	720	kHz
		MODE = $34.8\text{k}\Omega$ , $I_{OUT} = 0\text{A}$ , $V_{OUT} = 1\text{V}$	680	800	920	kHz
		MODE = $80.6\text{k}\Omega$ , $I_{OUT} = 0\text{A}$ , $V_{OUT} = 1\text{V}$	850	1000	1150	kHz
Minimum on time <sup>(10)</sup>	$t_{ON\_MIN}$	$V_{FB} = 500\text{mV}$			65	ns
Minimum off time <sup>(10)</sup>	$t_{OFF\_MIN}$	$V_{FB} = 500\text{mV}$			190	ns
<b>Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)</b>						
OVP threshold	$V_{OVP}$		113%	116%	119%	$V_{REF}$
UVP threshold	$V_{UVP}$		77%	80%	83%	$V_{REF}$
<b>Feedback Voltage and Soft Start</b>						
Feedback voltage	$V_{REF}$	$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	594	600	606	mV
		$T_J = 0^\circ\text{C}$ to $70^\circ\text{C}$	597	600	603	mV
TRK/REF sourcing current	$I_{TRACK\_SOURCE}$	$V_{TRK/REF} = 0\text{V}$		42		$\mu\text{A}$
TRK/REF sinking current	$I_{TRACK\_SINK}$	$V_{TRK/REF} = 1\text{V}$		12		$\mu\text{A}$
Soft-start time	$t_{SS}$	$T_J = 25^\circ\text{C}$		1.6		ms
<b>Error Amplifier (EA)</b>						
EA offset	$V_{OS}$		-3	0	+3	mV
Feedback current	$I_{FB}$	$V_{FB} = V_{REF}$		10	100	nA

**ELECTRICAL CHARACTERISTICS (continued)**

Typical value is tested at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 1.2\text{V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  <sup>(10)</sup>, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Enable and Under-Voltage Lockout (UVLO)</b>						
Enable input rising threshold	$V_{IHEN}$		1.17	1.22	1.27	V
Enable hysteresis	$V_{EN-HYS}$			200		mV
Enable input current	$I_{EN}$	$V_{EN} = 2\text{V}$		0		$\mu\text{A}$
<b><math>V_{IN}</math> UVLO</b>						
$V_{IN}$ UVLO threshold rising	$V_{INVT_{H\_RISE}}$	$V_{CC} = 3.3\text{V}$	2.1	2.4	2.7	V
$V_{IN}$ UVLO threshold falling	$V_{INVT_{H\_FALL}}$		1.55	1.85	2.15	
<b>VCC Regulator</b>						
$V_{CC}$ UVLO threshold rising	$V_{CCVT_{H\_RISE}}$		2.65	2.8	2.95	V
$V_{CC}$ UVLO threshold falling	$V_{CCVT_{H\_FALL}}$		2.35	2.5	2.65	V
VCC regulator	$V_{CC}$		2.88	3	3.12	V
VCC load regulation		$I_{CC} = 25\text{mA}$		0.5		%
<b>Power Good (PG)</b>						
PG high threshold	$PG_{VTH\_HI\_RISE}$	FB from low to high	89.5%	92.5%	95.5%	$V_{REF}$
PG low threshold	$PG_{VTH\_LO\_RISE}$	FB from low to high	113%	116%	119%	$V_{REF}$
	$PG_{VTH\_LO\_FALL}$	FB from high to low	77%	80%	83%	$V_{REF}$
PG low-to-high delay	$PG_{TD}$	$T_J = 25^\circ\text{C}$	0.63	0.9	1.17	ms
PG sink current capability	$V_{PG}$	$I_{PG} = 10\text{mA}$			0.5	V
PG leakage current	$I_{PG\_LEAK}$	$V_{PG} = 3.3\text{V}$			3	$\mu\text{A}$
PG low-level output voltage	$V_{OL\_100}$	$V_{IN} = 0\text{V}$ , pull PGOOD up to 3.3V through a 100k $\Omega$ resistor at 25 $^\circ\text{C}$		650	800	mV
	$V_{OL\_10}$	$V_{IN} = 0\text{V}$ , pull PGOOD up to 3.3V through a 10k $\Omega$ resistor at 25 $^\circ\text{C}$		750	900	mV
<b>Thermal Protection</b>						
Thermal shutdown <sup>(11)</sup>	$T_{SD}$			160		$^\circ\text{C}$
Thermal shutdown hysteresis <sup>(11)</sup>				30		$^\circ\text{C}$

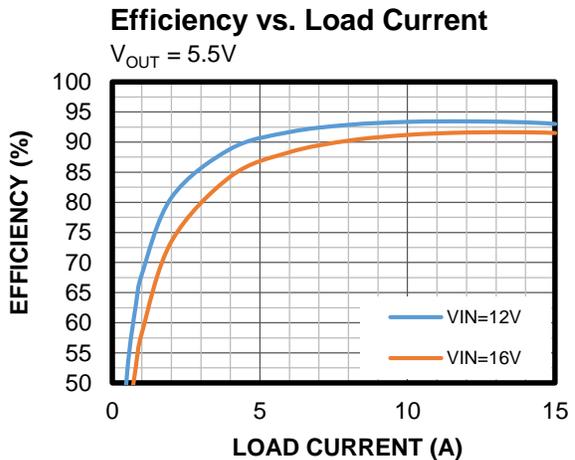
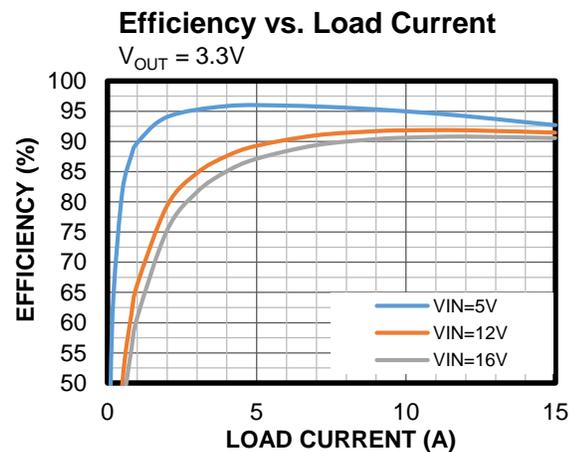
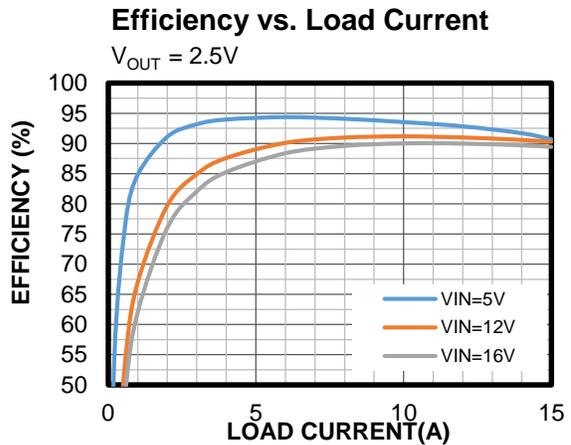
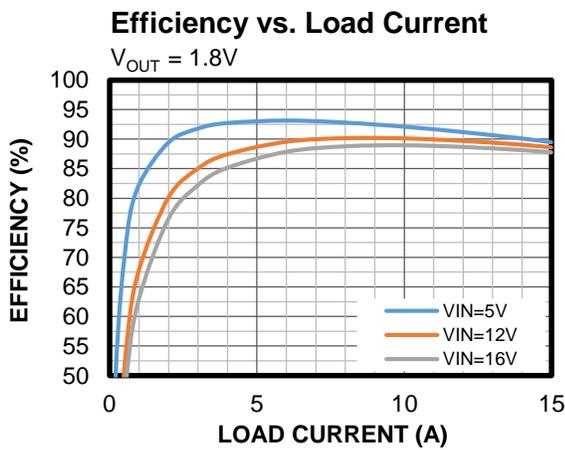
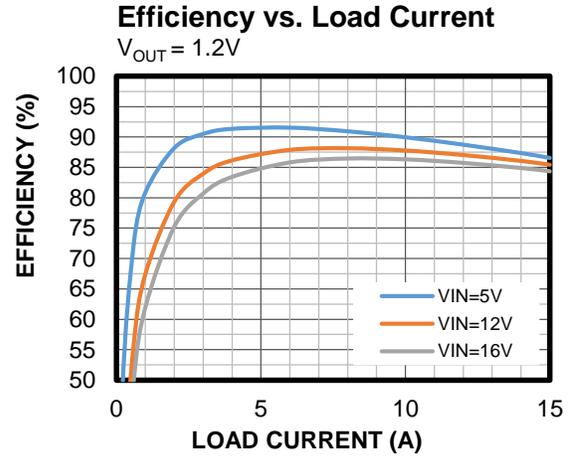
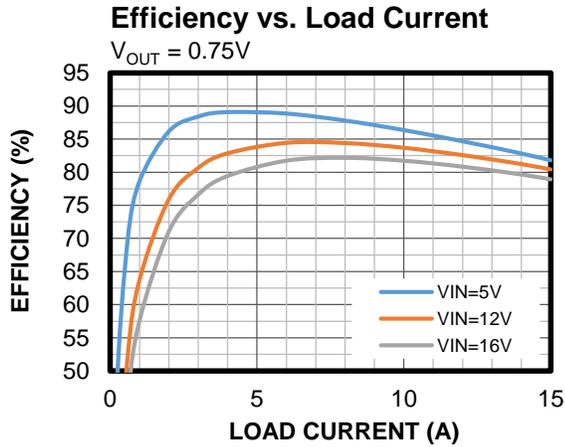
**Notes:**

10) Guaranteed by over-temperature (OT) correlation. Not tested in production.

11) Guaranteed by sample characterization. Not tested in production.

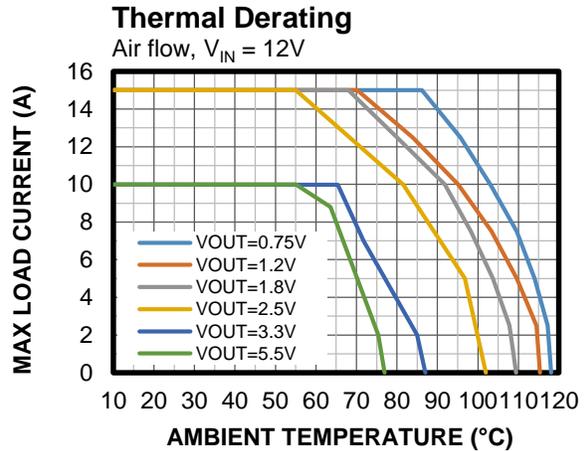
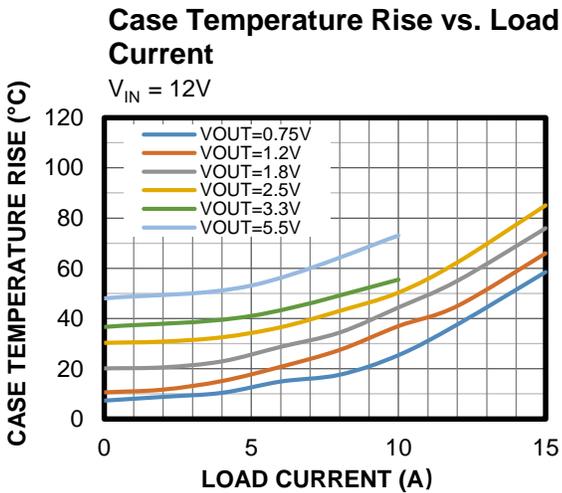
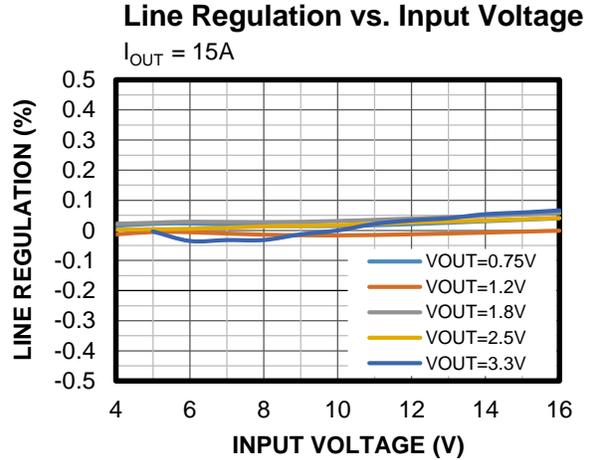
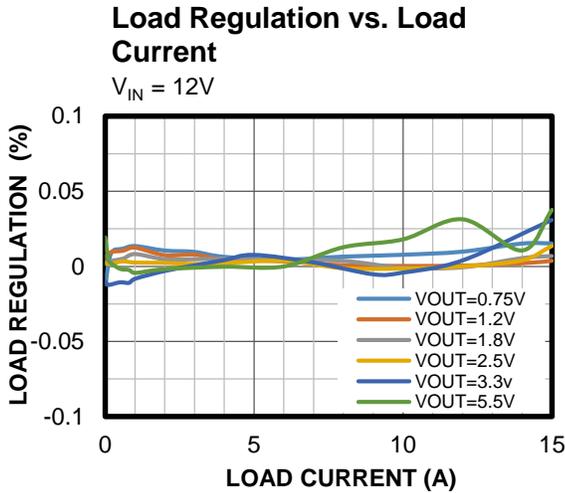
## TYPICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 10 \times 47\mu F$  ceramic +  $220\mu F$  electrolytic, FCCM,  $f_{sw} = 1000kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



**TYPICAL CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 10 \times 47\mu F$  ceramic +  $220\mu F$  electrolytic, FCCM,  $f_{sw} = 1000kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

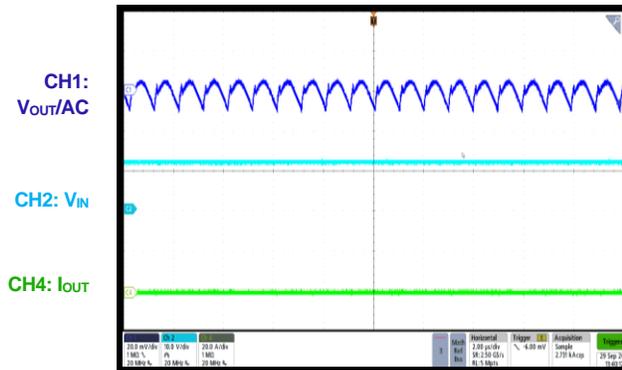


## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 10 \times 47\mu F$  ceramic +  $220\mu F$  electrolytic, FCCM,  $f_{sw} = 1000kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

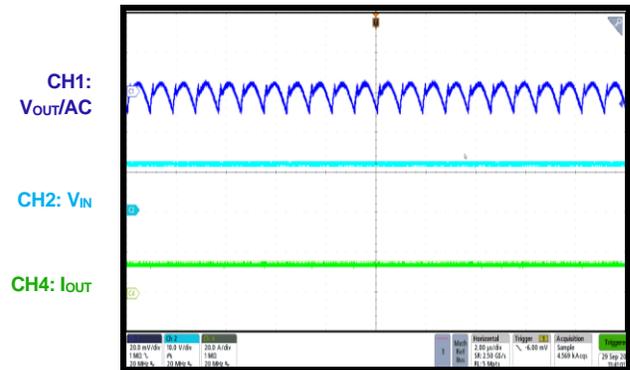
### Ripple

$I_{OUT} = 0A$



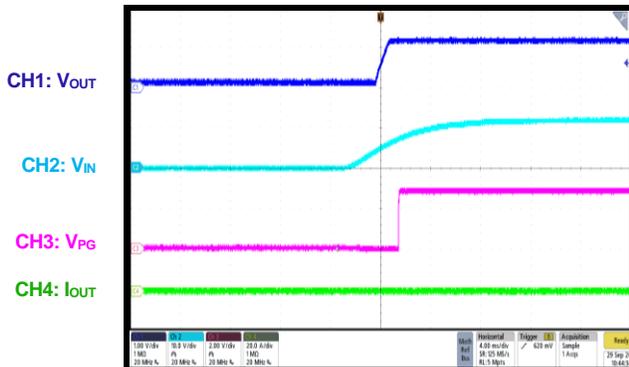
### Ripple

$I_{OUT} = 15A$



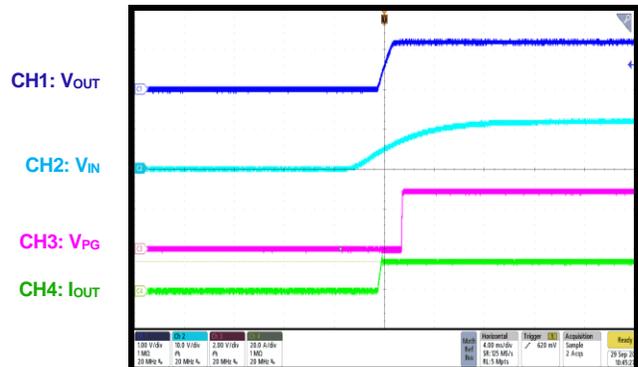
### Start-Up through VIN

$I_{OUT} = 0A$



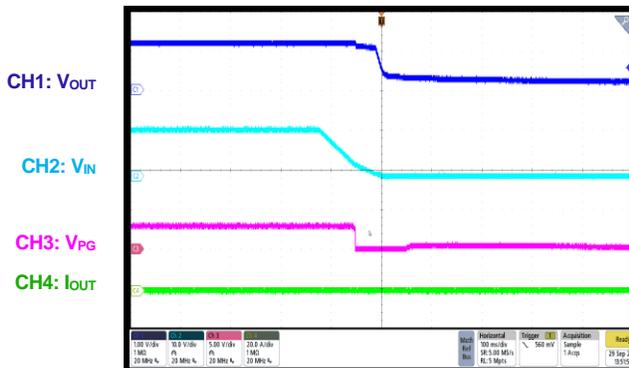
### Start-Up through VIN

$I_{OUT} = 15A$



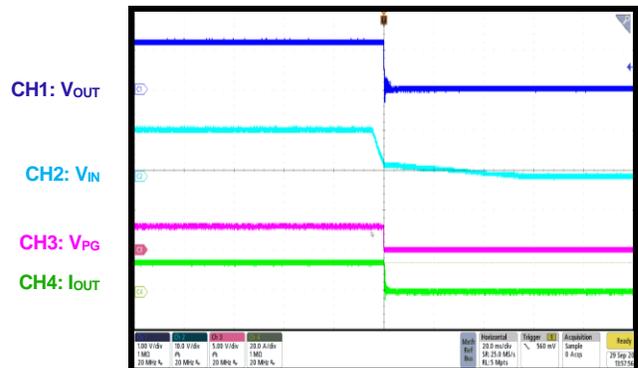
### Shutdown through VIN

$I_{OUT} = 0A$



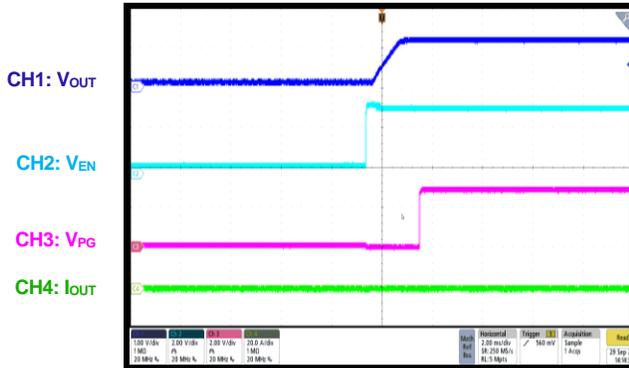
### Shutdown through VIN

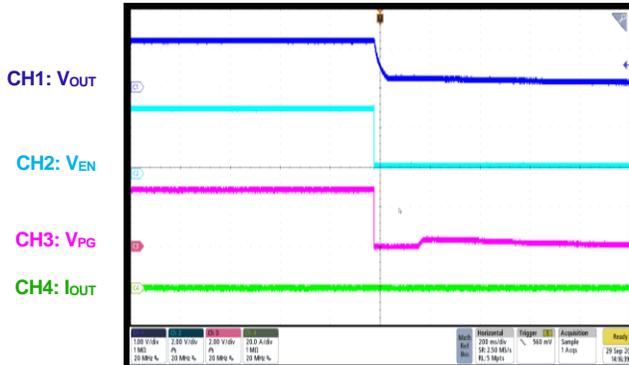
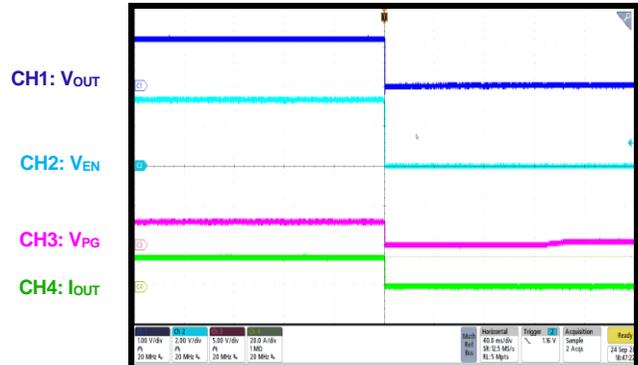
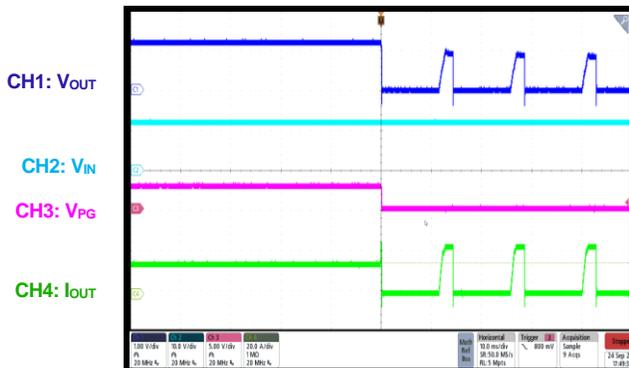
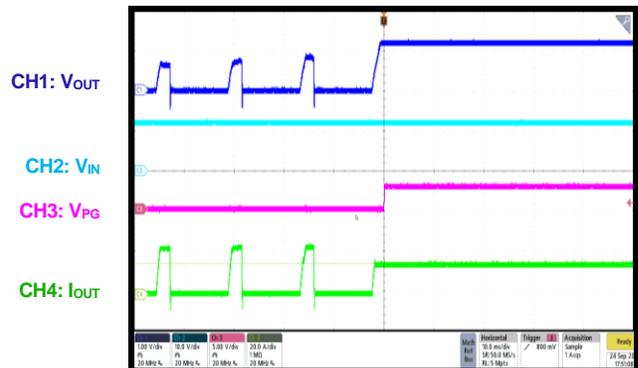
$I_{OUT} = 15A$



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{OUT} = 1.2V$ ,  $C_{OUT} = 10 \times 47\mu F$  ceramic +  $220\mu F$  electrolytic, FCCM,  $f_{sw} = 1000kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Start-Up through EN**
 $I_{OUT} = 0A$ 

**Start-Up through EN**
 $I_{OUT} = 15A$ 

**Shutdown through EN**
 $I_{OUT} = 0A$ 

**Shutdown through EN**
 $I_{OUT} = 15A$ 

**SCP Entry**
 $I_{OUT} = 15A$ 

**SCP Recovery**
 $I_{OUT} = 15A$ 




### FUNCTIONAL BLOCK DIAGRAM

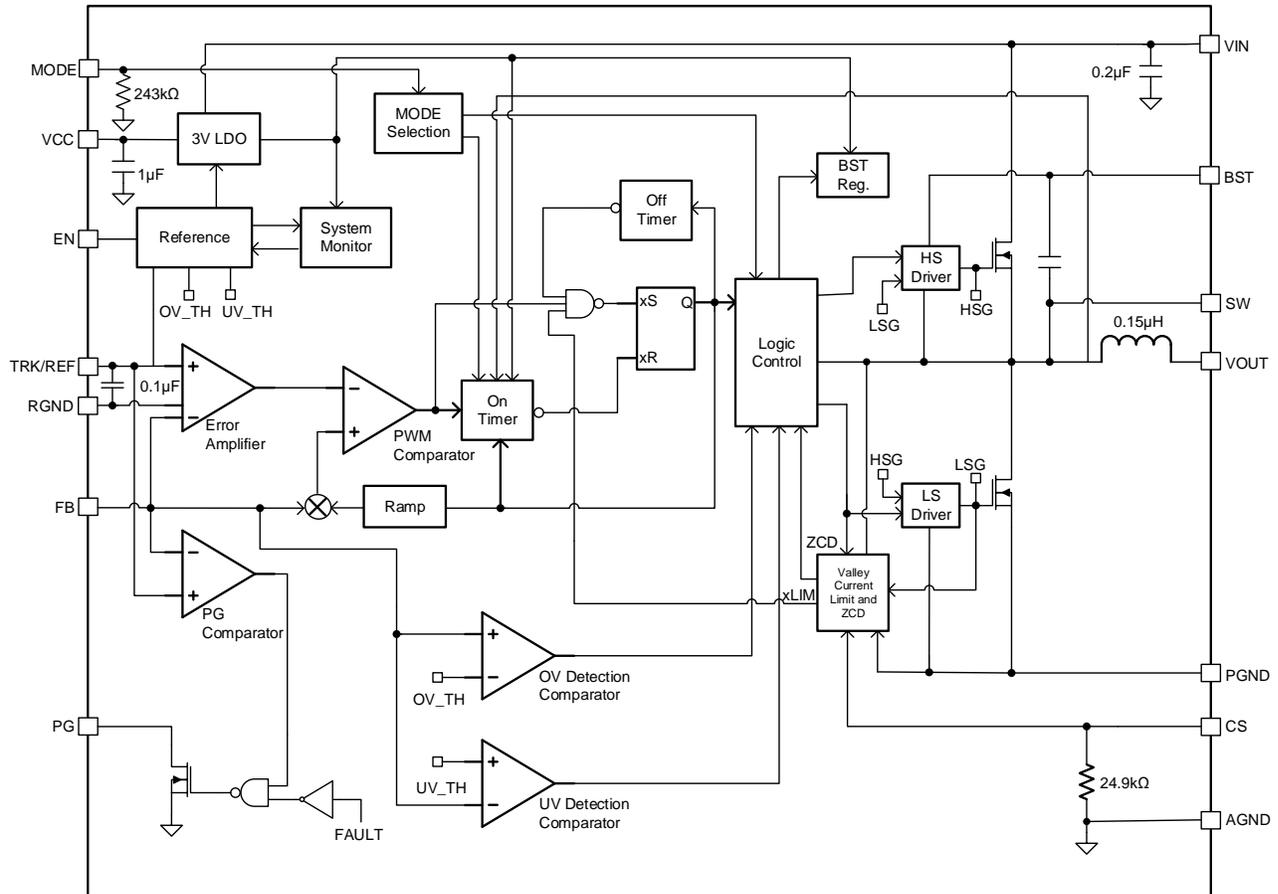
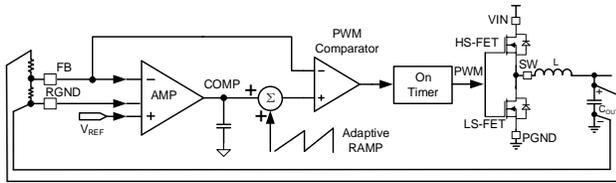


Figure 1: Functional Block Diagram

## OPERATION

### Constant-On-Time (COT) Control

The MPM3683-20 employs constant-on-time (COT) control to achieve a fast load transient response (see Figure 2).



**Figure 2: COT Control**

The operational amplifier (op amp) corrects any voltage error between the FB pin and the reference voltage ( $V_{REF}$ ). By working with the op amp, the MPM3683-20 can provide excellent load regulation across the entire load range, regardless of whether it is operating in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM).

The dedicated RGND pin helps to provide feedback remote GND sensing. The pair of remote sense traces should be kept at a low impedance to optimize performance.

The MPM3683-20 uses internal ramp compensation to support low-ESR, MLCC output capacitor solutions. The adaptive, internal ramp is optimized so that the MPM3683-20 is stable across the entire operating input voltage ( $V_{IN}$ ) and output voltage ( $V_{OUT}$ ) ranges, provided the proper design of the output filter.

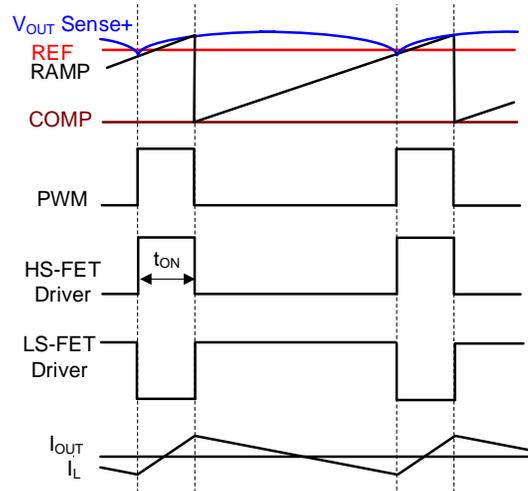
### Pulse-Width Modulation (PWM) Operation

Figure 3 shows how the pulse-width modulation (PWM) is generated under heavy loads.

The op amp corrects any error between FB and REF, and generates a fairly smooth DC voltage ( $V_{COMP}$ ). The internal ramp is superimposed onto  $V_{COMP}$ , then the superimposed  $V_{COMP}$  is compared with the FB signal.

When the FB voltage ( $V_{FB}$ ) drops below the superimposed  $V_{COMP}$ , the integrated high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed on time, which is determined by  $V_{IN}$ ,  $V_{OUT}$ , and the selected switching frequency ( $f_{SW}$ ). After the on period elapses, the HS-FET turns off. It turns on again when  $V_{FB}$  drops below the superimposed  $V_{COMP}$ .

By repeating this operation, the MPM3683-20 regulates  $V_{OUT}$ .



**Figure 3: Heavy-Load Operation (PWM)**

The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. If the HS-FET and LS-FET are turned on simultaneously, then a dead short occurs between  $V_{IN}$  and PGND; this is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period, or vice versa.

### Continuous Conduction Mode (CCM)

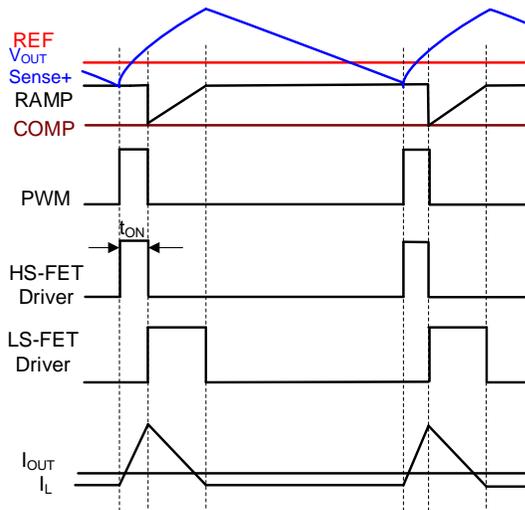
Continuous conduction mode (CCM) occurs when the output current ( $I_{OUT}$ ) is high and the inductor current ( $I_L$ ) remains above 0A. The MPM3683-20 can also be configured to operate in FCCM when  $I_{OUT}$  is low (see the Mode Selection section on page 15 for more details).

In CCM,  $f_{SW}$  is fairly constant (PWM mode), so the output ripple remains almost constant across the entire load range.

### Pulse-Skip Mode (PSM)

Under light-load conditions, the MPM3683-20 can be configured to work in pulse-skip mode (PSM) to optimize efficiency. When the load decreases,  $I_L$  also decreases. Once  $I_L$  reaches 0A, the MPM3683-20 transitions from CCM to PSM, provided that it has been configured accordingly (see the Mode Selection section on page 15 for more details).

Figure 4 shows PSM operation under light-loads.



**Figure 4: PSM Under Light Loads**

When  $V_{FB}$  drops below the superimposed  $V_{COMP}$ , the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until  $I_L$  reaches 0A. In PSM,  $V_{FB}$  does not reach the superimposed  $V_{COMP}$  while  $I_L$  is approaching 0A.

The LS-FET driver enters tri-state (Hi-Z) when  $I_L$  reaches 0A. A current modulator takes over control of the LS-FET and limits  $I_L$  below -1mA. Therefore, the output capacitor ( $C_{OUT}$ ) discharges slowly to PGND through the LS-FET. Under light-load conditions, the HS-FET does not turn on as frequently in PSM compared to FCCM. As a result, efficiency in PSM is significantly improved when compared to FCCM.

As  $I_{OUT}$  increases under light-load conditions, the current modulator regulation period becomes shorter, the HS-FET turns on more frequently, and  $f_{SW}$  increases accordingly.  $I_{OUT}$  reaches its critical level when the current modulator time is 0s. The  $I_{OUT}$  critical level ( $I_{OUT\_CRITICAL}$ ) can be calculated using Equation (1):

$$I_{OUT\_CRITICAL} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

Where  $f_{SW}$  is the switching frequency, and  $L = 0.15\mu\text{H}$  represents the inductance of the integrated inductor.

The MPM3683-20 enters PWM mode once  $I_{OUT}$  exceeds its critical level. Afterward,  $f_{SW}$  remains fairly constant across the  $I_{OUT}$  range.

The MPM3683-20 can be configured to operate in FCCM even under light-load conditions (see Table 1).

### Mode Selection

The MPM3683-20 provides both FCCM and PSM for light-load conditions. The MPM3683-20 has three options for  $f_{SW}$  selection: 600kHz, 800kHz, and 1000kHz. Select the operation mode for light-load conditions and  $f_{SW}$  by choosing the value of the resistor placed between MODE and AGND or VCC (see Table 1).

**Table 1: MODE Selection**

MODE	Light-Load Mode	$f_{sw}$
VCC	PSM	600kHz
Float	PSM	800kHz
243k $\Omega$ ( $\pm 20\%$ ) to GND	PSM	1000kHz
GND	FCCM	600kHz
34.8k $\Omega$ ( $\pm 20\%$ ) to GND	FCCM	800kHz
80.6k $\Omega$ ( $\pm 20\%$ ) to GND	FCCM	1000kHz

### Soft Start (SS)

With the integrated 100nF soft-start capacitor, the minimum soft-start time ( $t_{SS}$ ) is limited to 1.6ms.  $t_{SS}$  can be increased by adding an external capacitor between TRK/REF and AGND.

The soft-start capacitor ( $C_{SS}$ ) can be estimated with Equation (2):

$$C_{SS} (\text{nF}) = \frac{t_{SS} (\text{ms}) \times 36\mu\text{A}}{0.6\text{V}} - 100\text{nF} \quad (2)$$

### Output Voltage ( $V_{OUT}$ ) Tracking and Reference

The MPM3683-20 provides an analog input pin (TRK/REF) to track another power supply or accept an external reference. When an external voltage signal is connected to TRK/REF, it acts as a reference for the MPM3683-20's  $V_{OUT}$ .  $V_{FB}$  follows this external voltage signal exactly, and the SS settings are ignored. The TRK/REF input signal is between 0.3V and 1.4V.

During initial start-up, the TRK/REF voltage must first reach or exceed 600mV to ensure proper operation. Afterward, the voltage can be any value between 0.3V and 1.4V.

### Pre-Biased Start-Up

The MPM3683-20 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables the HS-FET and LS-FET switching until the voltage on the TRK/REF pin exceeds the sensed output voltage at the FB pin.

Before the TRK/REF voltage reaches the pre-biased FB level, if the BST voltage (from BST to SW) is below 2.3V, the LS-FET turns on to allow the BST voltage to be charged through VCC. The LS-FET turns on for very narrow pulses, so the drop-in pre-biased level is negligible.

### Current Sense (CS) and Over-Current Protection (OCP)

The MPM3683-20 features on-die current sensing and a configurable over-current protection (OCP) threshold for the inductor valley current.

OCP is active when the MPM3683-20 is enabled. When the LS-FET is on,  $I_L$  is sensed and mirrored on the CS pin with the current-sense gain ( $G_{CS}$ ) ratio. By connecting a resistor ( $R_{CS}$ ) between the CS and AGND pins, a voltage ( $V_{CS}$ ) that is proportional to the cycle-by-cycle  $I_L$  is generated. The HS-FET can only turn on when  $V_{CS}$  is below the internal OVP threshold ( $V_{OCP}$ ) (during the LS-FET on state) to limit the inductor valley current cycle by cycle. The MPM3683-20 integrates a 24.9k $\Omega$  current-sense resistor between the CS and AGND pins.

The OCP threshold for the inductor valley current can be calculated with Equation (3):

$$I_{VALLEY} = \frac{V_{OCP}}{R_{CS}(\text{M}\Omega) // 0.0249 \times G_{CS}} \quad (3)$$

Estimate the value of  $R_{CS}$  for the target output current limit ( $I_{LIM}$ ) with Equation (4):

$$R_{CS}(\text{M}\Omega) // 0.0249 = \frac{V_{OCP}}{G_{CS} \times \left( I_{LIM} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L(\mu\text{H}) \times f_{SW}(\text{MHz})} \right)} \quad (4)$$

Where  $V_{OCP} = 1.2\text{V}$ ,  $G_{CS} = 10\mu\text{A/A}$ ,  $L = 0.15\mu\text{H}$ , and  $I_{LIM}$  is the target output current limit (in A).

Note that the MPM3683-20 provides accurate cycle-by-cycle OCP for the inductor valley current. However, the conversion between the inductor valley current and  $I_{OUT}$  may involve an error that is introduced by the tolerance of the integrated inductor and  $f_{SW}$  variation due to COT operation.

OCP hiccup mode is active 3ms after the MPM3683-20 is enabled. Once OCP hiccup mode is active, if the MPM3683-20 detects an OC condition for 31 consecutive cycles, it enters hiccup mode.

In hiccup mode, the MPM3683-20 latches off the HS-FET immediately and latches off the LS-FET after zero-current detection (ZCD). Meanwhile, the TRK/REF capacitor discharges. After about 11ms, the MPM3683-20 attempts to soft start automatically. If the OC condition still remains after 3ms, the MPM3683-20 repeats this operation until the OC condition is removed. Then  $V_{OUT}$  rises back to the regulation level smoothly.

### Negative Inductor Current Limit

When the LS-FET detects a -18A (typical) current, the MPM3683-20 turns off the LS-FET for 200ns to limit the negative current.

### Over-Voltage Protection (OVP)

The MPM3683-20 monitors  $V_{OUT}$  by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage (OV) condition. The device provides OVP with hiccup mode.

If  $V_{FB}$  exceeds 116% of  $V_{REF}$ , OVP is triggered. The PG pin pulls down until it reaches the low-side negative current limit (NOCP). Then the LS-FET turns off for 200ns. The HS-FET turns on during this period. After 200ns, the LS-FET turns on again. The MPM3683-20 repeats this operation to discharge any OV condition on the output.

The MPM3683-20 exits OVP discharge mode when  $V_{FB}$  drops below 105% of  $V_{REF}$ .

### Over-Temperature Protection (OTP)

The MPM3683-20 features over-temperature protection (OTP).

The MPM3683-20 monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off and discharges the TRK/REF capacitors. OTP is a non-latch protection. There is a hysteresis of about 30°C. Once the junction temperature drops to about 130°C, a soft start initiates.

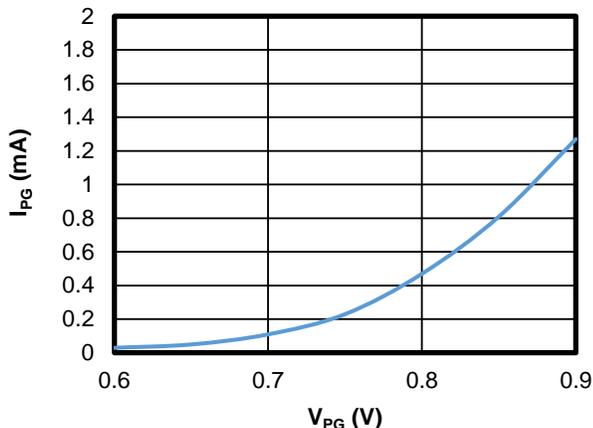
OTP is effective once the MPM3683-20 is enabled.

### Power Good (PG)

The MPM3683-20 has a power good (PG) output. PG is the open drain of a MOSFET. Connect PG to VCC or another external voltage source (below 3.6V) through a pull-up resistor (typically 10kΩ). After applying  $V_{IN}$ , the MOSFET turns on, and PG pulls to GND before TRK/REF is ready. Once  $V_{FB}$  reaches 92.5% of  $V_{REF}$ , PG pulls high after a 0.9ms delay.

When  $V_{FB}$  drops to 80% of  $V_{REF}$  or exceeds 116% of the nominal  $V_{REF}$ , PG pulls low. PG pulls high again after the FB voltage rises to 92.5% of  $V_{REF}$  or drops to 101% of  $V_{REF}$ .

If the input supply fails to power the MPM3683-20, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. Figure 5 shows the relationship between the PG voltage and the pull-up current.



**Figure 5: PG Clamped Voltage vs. Pull-Up Current**

### EN Configuration

The MPM3683-20 turns on when EN goes high. The MPM3683-20 turns off when EN goes low. EN cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable or disable the MPM3683-20.

The MPM3683-20 provides accurate EN thresholds. A resistor divider can be connected from  $V_{IN}$  to AGND to configure the  $V_{IN}$  at which the MPM3683-20 is enabled. This is highly recommended for applications where there is no dedicated EN control logic signal because it can prevent under-voltage lockout (UVLO) bouncing during start-up and shutdown.

The resistor divider values can be calculated with Equation (5):

$$V_{IN\_START} (V) = V_{IH\_EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (5)$$

Where  $V_{IH\_EN}$  is typically 1.22V.

Select  $R_{UP}$  and  $R_{DOWN}$  such that the EN voltage does not exceed 3.6V when  $V_{IN}$  reaches its maximum value.

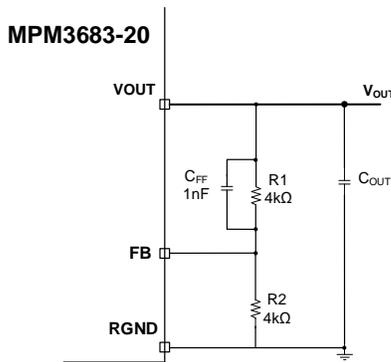
EN can also be directly connected to  $V_{IN}$  through a pull-up resistor ( $R_{UP}$ ). Select  $R_{UP}$  such that the maximum current going into EN is 50μA.  $R_{UP}$  can be estimated with Equation (6):

$$R_{UP} (k\Omega) = \frac{V_{IN\_MAX} (V)}{0.05 (mA)} \quad (6)$$

## APPLICATION INFORMATION

### Setting the Output Voltage ( $V_{OUT}$ )

Figure 6 shows the circuit connection for  $V_{OUT}$ .



**Figure 6: Circuit Connection**

$R_2$  can be calculated with Equation (7):

$$R_2(\text{k}\Omega) = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_1(\text{k}\Omega) \quad (7)$$

Where  $V_{REF} = 0.6\text{V}$ .

To optimize the load transient response, it is recommended to place a feed-forward capacitor ( $C_{FF}$ ) in parallel with  $R_1$ .  $R_1$  and  $C_{FF}$  add an extra zero ( $f_z$ ) to the system, which improves loop response.  $R_1$  and  $C_{FF}$  are selected such that the zero formed by  $R_1$  and  $C_{FF}$  is between 20kHz and 60kHz. Estimate  $f_z$  with Equation (8):

$$f_z = \frac{1}{2\pi \times R_1 \times C_{FF}} \quad (8)$$

Table 3 shows the values of feedback resistors and feed-forward capacitor for common output voltages.

**Table 3: Setting Common Output Voltages**

$V_{OUT}$ (V)	$C_{FF}$ (nF)	$R_1$ (kΩ)	$R_2$ (kΩ)
0.75	1	4	16
1.2	1	4	4
1.8	1	4	2
2.5	1	6.3	2
3.3	0.068	9	2
5.5	0.068	10.2	1.24

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use ceramic capacitors

for the best performance. During the layout, place the input capacitors as close to  $V_{IN}$  as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable across a wide temperature range and offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Calculate the input ripple current with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (9)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , estimated with Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current. The input capacitor value determines the converter's input voltage ripple. If the system has an input voltage ripple requirement, select an input capacitor that meets the specification.

Calculate the input voltage ripple with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , estimated with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (12)$$

### Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors. Calculate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (13)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple can be calculated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (15)$$

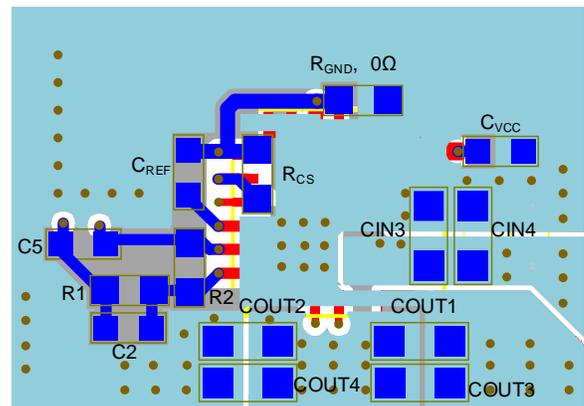
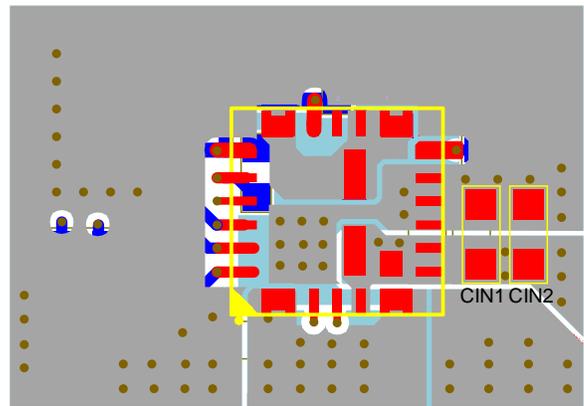
Where L is fixed at 0.15μH internally.

### PCB Layout Guidelines

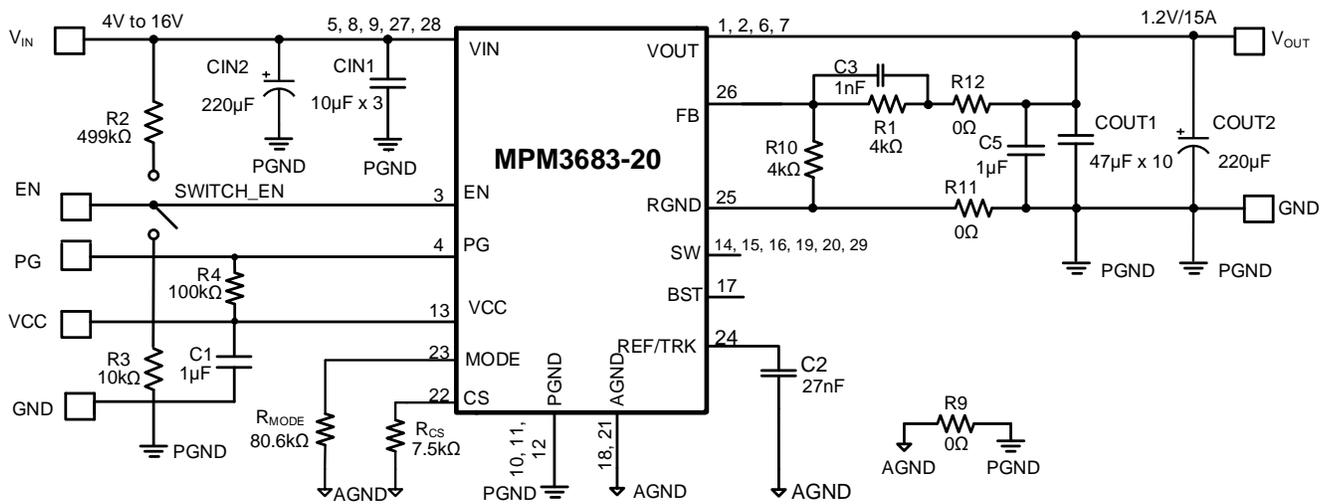
Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 7 and follow the guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Place the major MLCC capacitors on the same layer as the MPM3683-20.
3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
4. Ensure that the high-current paths (PGND, VIN, and VOUT) have short, direct, and wide traces.
5. Place as many PGND vias as possible as close to PGND as possible to minimize both parasitic impedance and thermal resistance.
6. Place the external feedback resistors next to FB.
7. Route the feedback network away from the switching node.

- Top Layer Line and Pad
- Bottom Layer Line and Pad
- Top Layer Copper
- Bottom Layer Copper
- Via

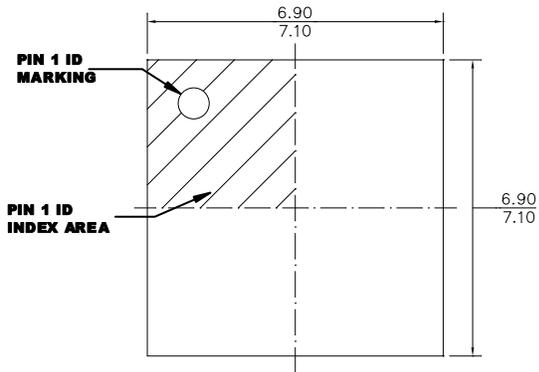


**Figure 7: Recommended PCB Layout**

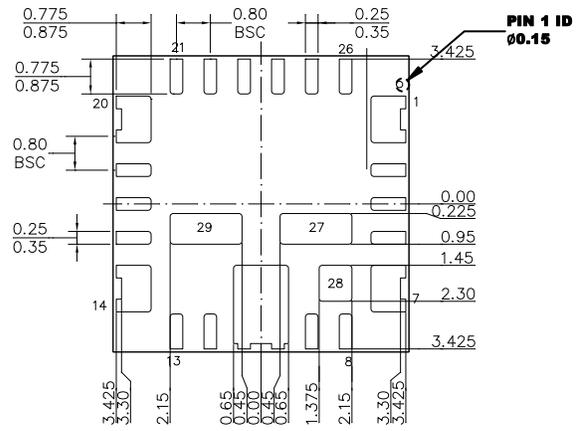
**TYPICAL APPLICATION CIRCUIT**

**Figure 8: Typical Application Circuit ( $V_{IN} = 12V$ , 1.2V/15A Output, FCCM, 100kHz)**

PACKAGE INFORMATION

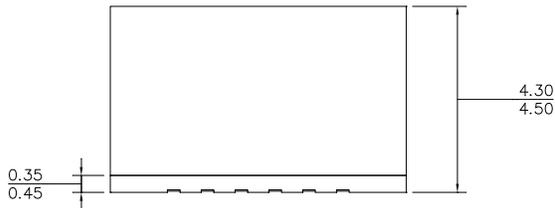
LGA-29 (7mmx7mmx4.4mm)



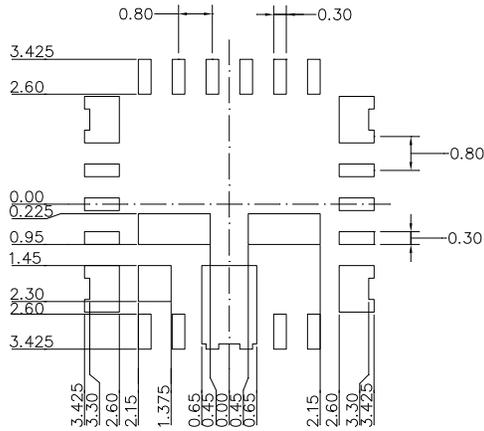
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

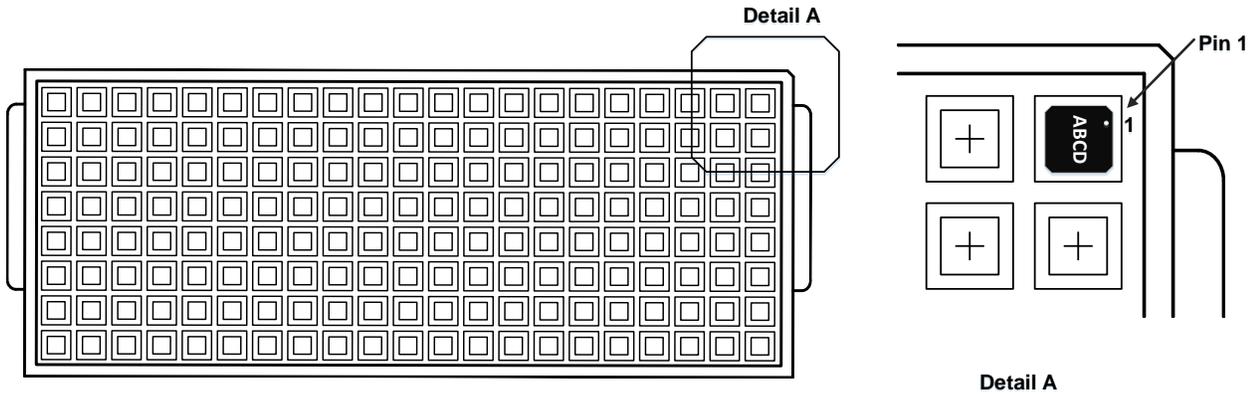


**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-303.
- 4) DRAWING IS NOT TO SCALE.

### CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3683GMN-20-T	LGA-29 (7mmx7mmx4.4mm)	N/A	N/A	260	N/A	N/A	N/A

**Note:**

12) This is a schematic of the tray. Different packages correspond to different trays, with a different length, width, and height.

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/1/2023	Initial Release	-

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