

JFET Switching Transistors

N-Channel

MMBF4391L, MMBF4392L, MMBF4393L

Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

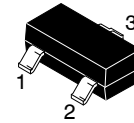
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	50	mAdc

THERMAL CHARACTERISTICS

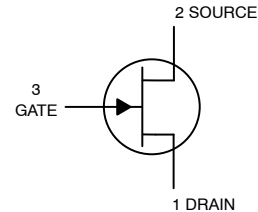
Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 1) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

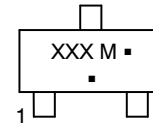
1. FR-5 = $1.0 \times 0.75 \times 0.062$ in.



SOT-23
CASE 318
STYLE 10



MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

- * Date Code orientation and/or overbar may vary depending upon manufacturing location.

MARKING & ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

MMBF4391L, MMBF4392L, MMBF4393L

ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage ($I_G = 1.0\text{ }\mu\text{Adc}$, $V_{DS} = 0$)	$V_{(BR)GSS}$	30	–	Vdc
Gate Reverse Current ($V_{GS} = 15\text{ Vdc}$, $V_{DS} = 0$, $T_A = 25\text{ }^{\circ}\text{C}$) ($V_{GS} = 15\text{ Vdc}$, $V_{DS} = 0$, $T_A = 100\text{ }^{\circ}\text{C}$)	I_{GSS}	– –	1.0 0.20	nAdc μAdc
Gate-Source Cutoff Voltage ($V_{DS} = 15\text{ Vdc}$, $I_D = 10\text{ nAdc}$) MMBF4391LT1 MMBF4392LT1 MMBF4393LT1	$V_{GS(off)}$	–4.0 –2.0 –0.5	–10 –5.0 –3.0	Vdc
Off-State Drain Current ($V_{DS} = 15\text{ Vdc}$, $V_{GS} = -12\text{ Vdc}$) ($V_{DS} = 15\text{ Vdc}$, $V_{GS} = -12\text{ Vdc}$, $T_A = 100\text{ }^{\circ}\text{C}$)	$I_{D(off)}$	– –	1.0 1.0	nAdc μAdc

ON CHARACTERISTICS

Zero-Gate-Voltage Drain Current ($V_{DS} = 15\text{ Vdc}$, $V_{GS} = 0$) MMBF4391LT1 MMBF4392LT1 MMBF4393LT1	I_{DSS}	50 25 5.0	150 75 30	mAdc
Drain-Source On-Voltage ($I_D = 12\text{ mAdc}$, $V_{GS} = 0$) MMBF4391LT1 ($I_D = 6.0\text{ mAdc}$, $V_{GS} = 0$) MMBF4392LT1 ($I_D = 3.0\text{ mAdc}$, $V_{GS} = 0$) MMBF4393LT1	$V_{DS(on)}$	– – –	0.4 0.4 0.4	Vdc
Static Drain-Source On-Resistance ($I_D = 1.0\text{ mAdc}$, $V_{GS} = 0$) MMBF4391LT1 MMBF4392LT1 MMBF4393LT1	$r_{DS(on)}$	– – –	30 60 100	Ω

SMALL-SIGNAL CHARACTERISTICS

Input Capacitance ($V_{DS} = 0\text{ Vdc}$, $V_{GS} = -15\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{iss}	–	14	pF
Reverse Transfer Capacitance ($V_{DS} = 0\text{ Vdc}$, $V_{GS} = -12\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{rss}	–	3.5	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MMBF4391LT1G	6J	SOT-23 (Pb-Free)	3,000 / Tape & Reel
SMMBF4391LT1G*	6J		
MMBF4392LT1G	6K		
MMBF4393LT1G	M6G		
SMMBF4393LT1G*	M6G		

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

TYPICAL CHARACTERISTICS

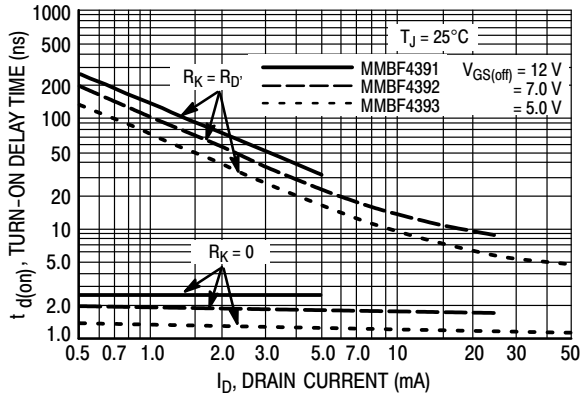


Figure 1. Turn-On Delay Time

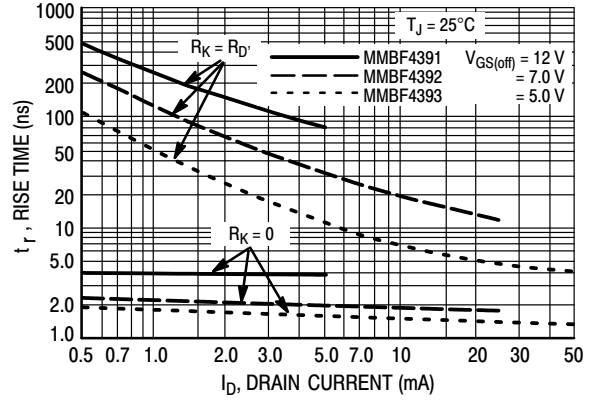


Figure 2. Rise Time

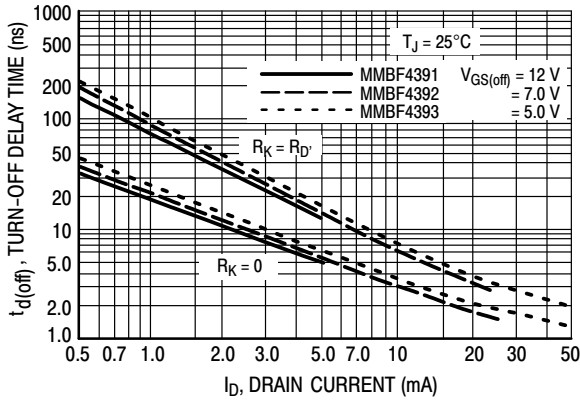


Figure 3. Turn-Off Delay Time

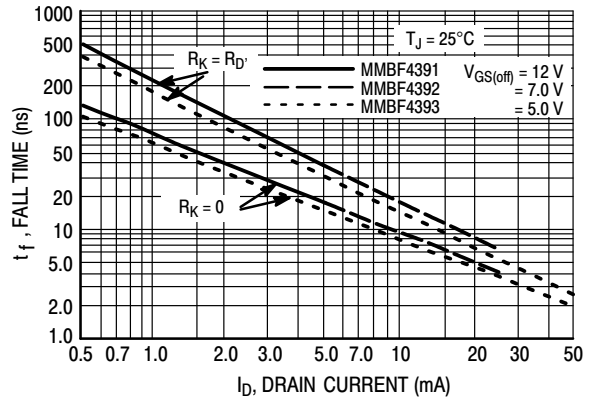


Figure 4. Fall Time

NOTE 1

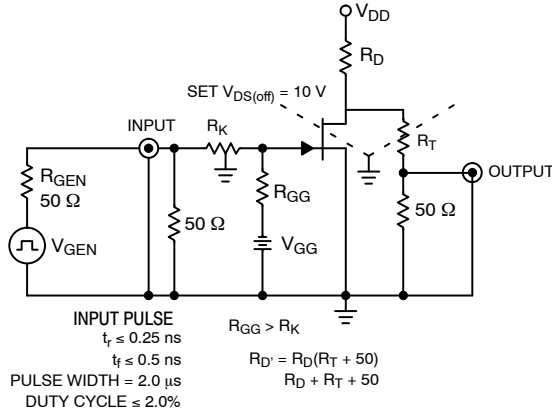


Figure 5. Switching Time Test Circuit

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain-Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) of Gate-Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn-on interval, Gate-Source Capacitance (C_{gs}) discharges through the series combination of R_{Gen} and R_K . C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain-Source Resistance (r_{DS}). During the turn-off, this charge flow is reversed.

Predicting turn-on time is somewhat difficult as the channel resistance r_{DS} is a function of the gate-source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{DS} decreases. Since C_{gd} discharges through r_{DS} , turn-on time is non-linear. During turn-off, the situation is reversed with r_{DS} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to R_D , which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

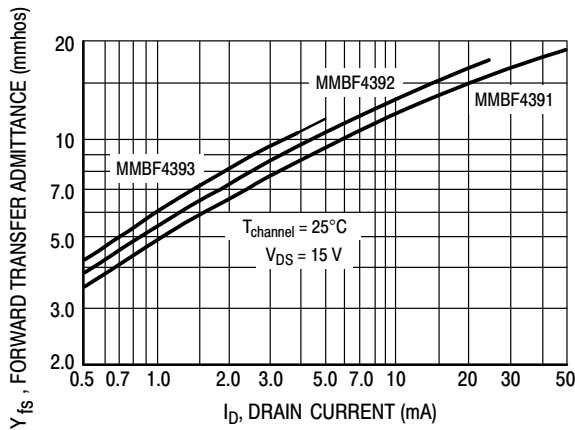


Figure 6. Typical Forward Transfer Admittance

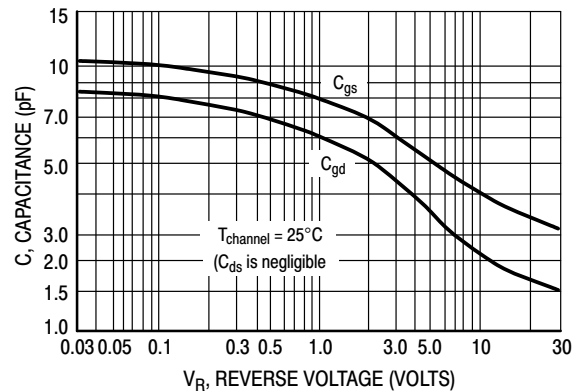


Figure 7. Typical Capacitance

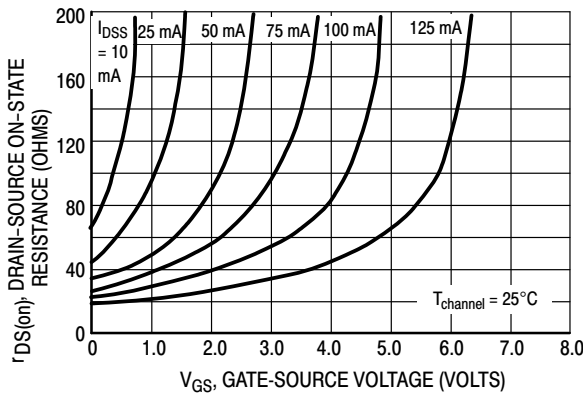


Figure 8. Effect of Gate-Source Voltage on Drain-Source Resistance

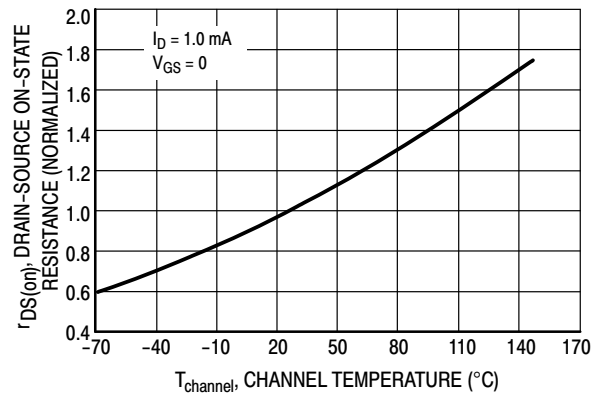


Figure 9. Effect of Temperature on Drain-Source On-State Resistance

NOTE 2

The Zero-Gate-Voltage Drain Current (I_{DSS}) is the principle determinant of other J-FET characteristics. Figure 10 shows the relationship of Gate-Source Off Voltage ($V_{GS(off)}$) and Drain-Source On Resistance ($r_{DS(on)}$) to I_{DSS} . Most of the devices will be within $\pm 10\%$ of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

The electrical characteristics table indicates that an MMBF4392 has an I_{DSS} range of 25 to 75 mA. Figure 10 shows $r_{DS(on)} = 52\ \Omega$ for $I_{DSS} = 25\text{ mA}$ and $30\ \Omega$ for $I_{DSS} = 75\text{ mA}$. The corresponding V_{GS} values are 2.2 V and 4.8 V.

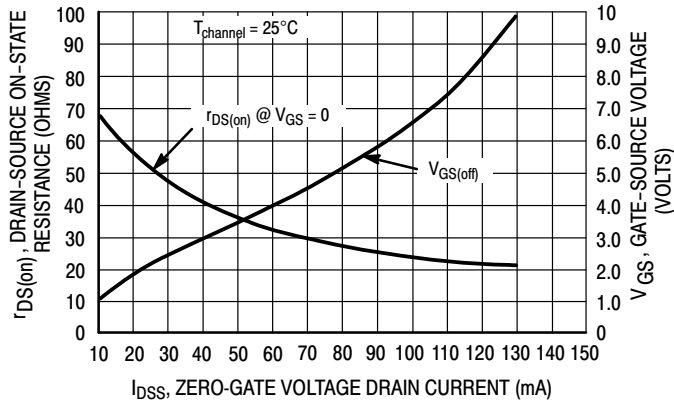


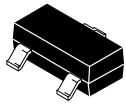
Figure 10. Effect of I_{DSS} on Drain-Source Resistance and Gate-Source Voltage

MMBF4391L, MMBF4392L, MMBF4393L

REVISION HISTORY

Revision	Description of Changes	Date
14	The Y-axis label in Figure 6 has been corrected. Removed missing information of NOTE 2.	07/03/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

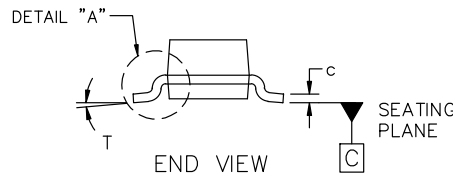
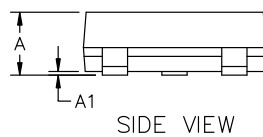
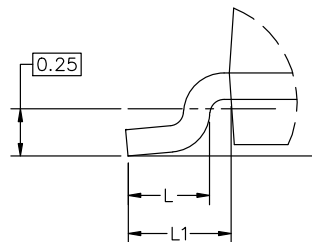
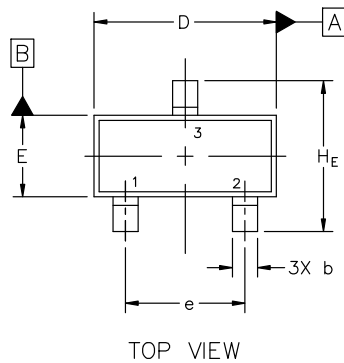


SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P

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ISSUE AU

DATE 14 AUG 2024

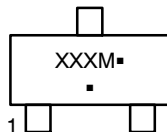


MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

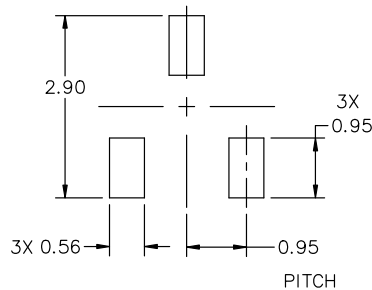
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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