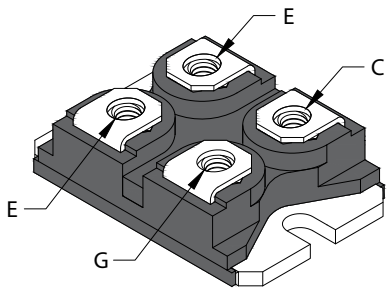
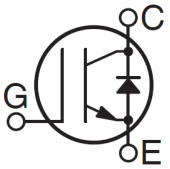
1200 V, 75 A Power MOS 7™ PT IGBT with DQ Diode

APT75GP120JDQ3

Product Overview

1200 V, 60 A at 10 kHz Power MOS 7 punch-through (PT) IGBT with co-packaged anti-parallel DQ diode, SOT-227





G—Gate
C—Collector
E—Emitter

Features

- Low conduction loss and saturation voltage
- Low gate charge
- Ultrafast tail current shutoff
- Soft recovery
- High operating frequency
- Reverse-bias safe operating area (RBSOA) rated
- RoHS compliant
- Isolated voltage to 2500 V, UL certified file E145592

1. Device Specifications: IGBT

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{CES}	Collector-emitter voltage	1200	V
V_{GE}	Gate-emitter voltage	±20	
I_{C1}	Continuous collector current at T_C = 25 °C	128	A
I_{C2}	Continuous collector current at T_C = 110 °C	57	
I_{CM}	Pulsed collector current[1] at T_C = 150 °C	300	
RBSOA	Reverse-bias safe operating area at T_J = 150 °C and 960 V	300	A
P_D	Total power dissipation T_C = 25 °C	543	W

Note:

1. Repetitive rating: Pulse width and case temperature limited by the maximum junction temperature.

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$R_{\Theta JC}$	Junction-to-case thermal resistance (IGBT)		0.16	0.23	°C/W
$R_{\Theta JC}$	Junction-to-case thermal resistance (diode)		0.39	0.56	
T_J, T_{STG}	Operating and storage junction temperature range	–55		150	°C
$V_{ISOLATION}$	RMS voltage (50 Hz–60 Hz sinusoidal waveform from terminals to mounting base for 1 minute)	2500			V
τ_M	Mounting torque, M3 screw for heat sink attachment (requires 2, not included)		0.8		N·m
τ_T	Terminal screw torque, M4 screw (4 included)			1.1	
Wt	Package weight		29.2		g

ESD practices should comply with JESD-625.

1.2 Electrical Performance

The following table shows the static characteristics of this device. T_J = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{CE} = 0 V, I_G = 1250 µA	1200			V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 2.5 mA	3	4.5	6	
$V_{CE(ON)}$	Collector-emitter on voltage	V_{GE} = 15 V, I_C = 75 A		3.3	3.9	
		V_{GE} = 15 V, I_C = 75 A, T_J = 125 °C		3.0		
I_{CES}	Collector cut-off current[1]	V_{CE} = 1200 V, V_{GE} = 0 V			1250	µA
		V_{CE} = 1200 V, V_{GE} = 0 V, T_J = 125 °C			6000	
I_{GES}	Gate-emitter leakage current	V_{GE} = ±20 V			±100	nA

Note:

1. I_{CES} includes both IGBT and FRED leakages.

The following table shows the dynamic characteristics of this device. T_J = 25 °C unless otherwise specified.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	V_{GE} = 0 V		7035		pF
C_{res}	Reverse transfer capacitance	V_{CE} = 25 V		80		
C_{oes}	Output capacitance	ƒ = 1 MHz		460		
V_{GEP}	Gate-to-emitter plateau voltage	Gate charge		7.5		V
Q_G	Total gate charge[1]	V_{GE} = 15 V		320		nC
Q_{GE}	Gate-emitter charge	V_{CE} = 600 V		50		
Q_{GC}	Gate-collector ("Miller") charge	I_C = 75 A		140		
RBSOA	Reverse-bias safe operating area	T_J = 150 °C R_G = 5 Ω V_{GE} = 15 V V_{CE} = 960 V L = 100 µH	300			A
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V		20		ns
t_r	Current rise time	V_{GE} =15 V		40		
$t_{d(off)}$	Turn-off delay time	I_C = 75 A		165		
t_f	Current fall time	R_G = 5 Ω		55		
E_{on1}	Turn-on switching energy[2]	T_J = 25 °C		1620		µJ
E_{on2}	Turn-on switching energy (diode)[3]			4100		
E_{off}	Turn-off switching energy[4]			2500		
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V		20		ns
t_r	Current rise time	V_{GE} = 15 V		40		
$t_{d(off)}$	Turn-off delay time	I_C = 75 A		245		
t_f	Current fall time	R_G = 5 Ω		115		
E_{on1}	Turn-on switching energy[2]	T_J = 125 °C		1620		µJ
E_{on2}	Turn-on switching energy (diode)[3]			5850		
E_{off}	Turn-off switching energy[4]			4820		

Notes:

1. See MIL-STD-750 Method 3471.
2. E_{on1} is the clamped inductive turn-on-energy of the IGBT only, without the effect of a commutating diode reverse recovery current adding to the IGBT turn-on loss. (See Figure 1-25.)
3. E_{on2} is the clamped inductive turn-on energy that includes a commutating diode reverse recovery current in the IGBT turn-on switching loss. (See Figures 1-22, 1-23.)
4. E_{off} is the clamped inductive turn-off energy measured in accordance with JEDEC standard JESD24-1. (See Figures 1-22, 1-24.)

1.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Output Characteristics

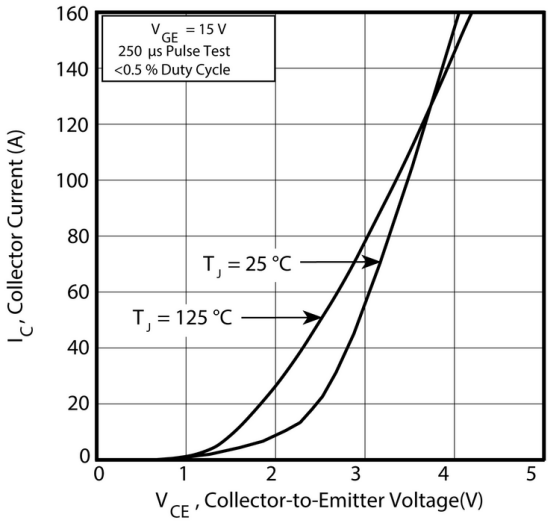


Figure 1-2. Output Characteristics

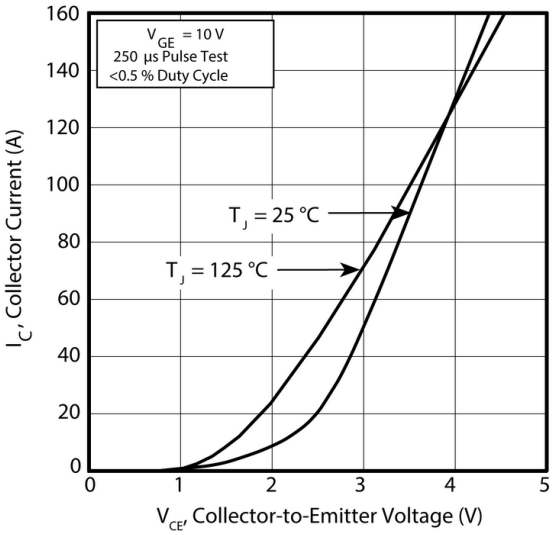


Figure 1-3. Transfer Characteristics

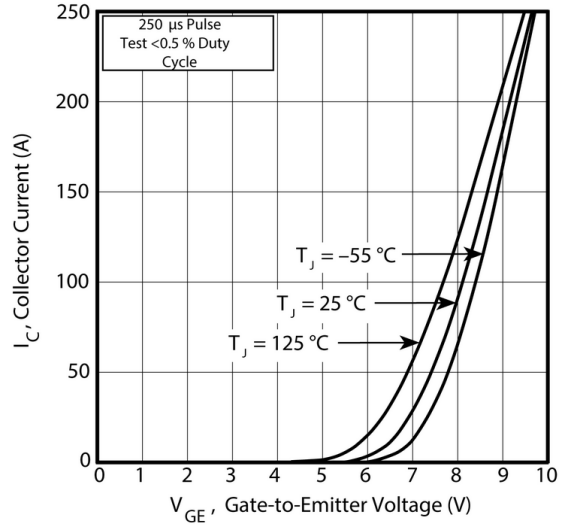


Figure 1-4. Gate Charge

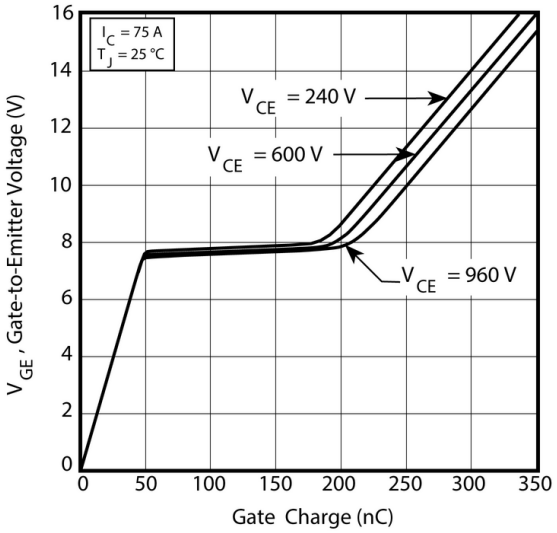


Figure 1-5. On-State Voltage vs. Gate-to- Emitter Voltage

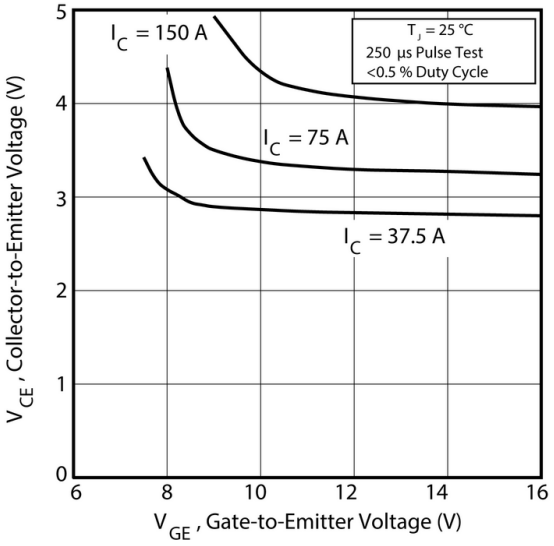


Figure 1-6. On-State Voltage vs. Junction Temperature

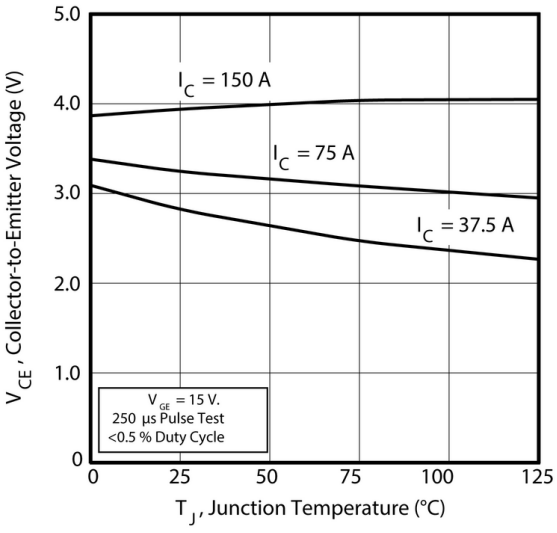


Figure 1-7. Breakdown Voltage vs. Junction Temperature

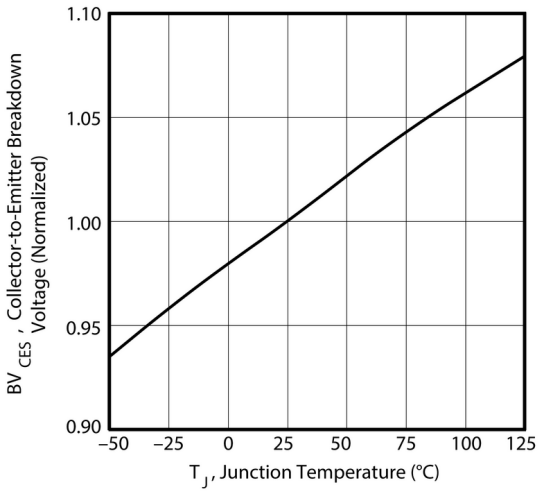


Figure 1-8. DC Collector Current vs. Case Temperature

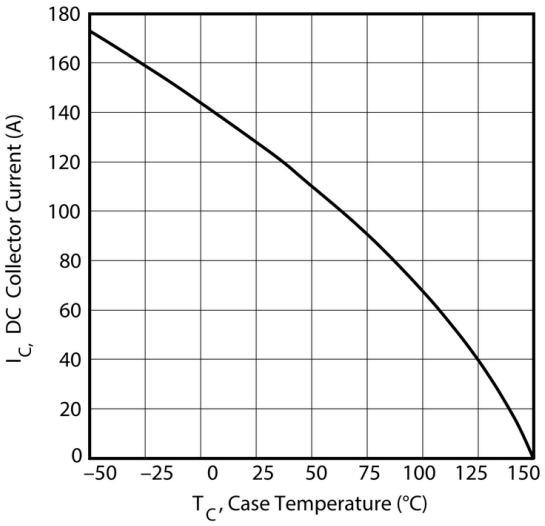


Figure 1-9. Turn-On Delay Time vs. Collector Current

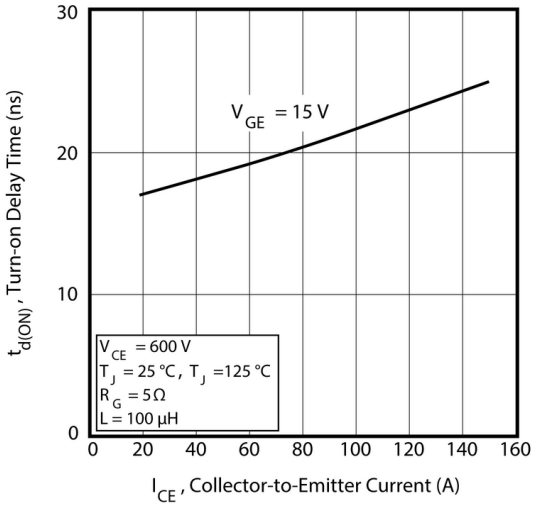


Figure 1-10. Turn-Off Delay Time vs. Collector Current

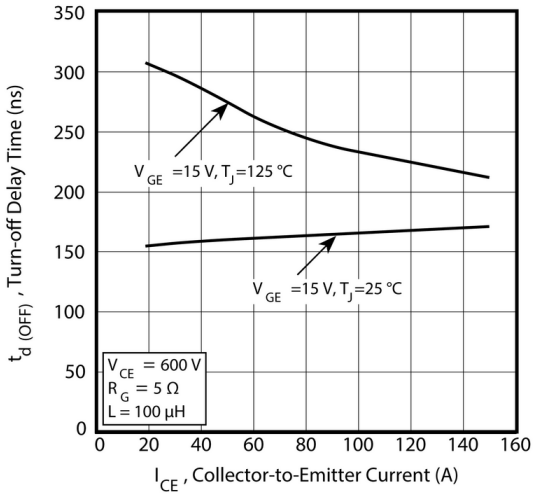


Figure 1-11. Current Rise Time vs. Collector Current

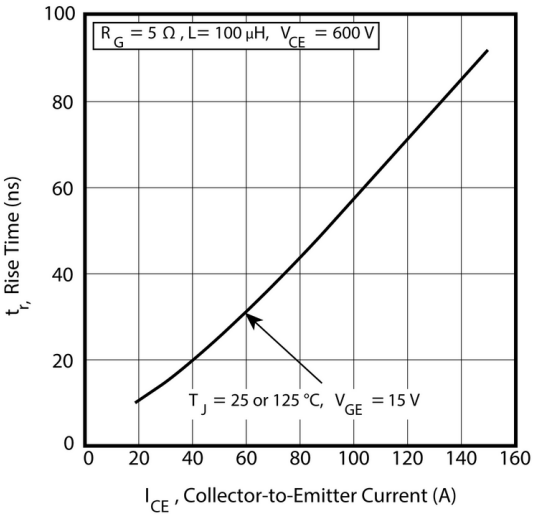


Figure 1-12. Current Rise Time vs. Collector Current

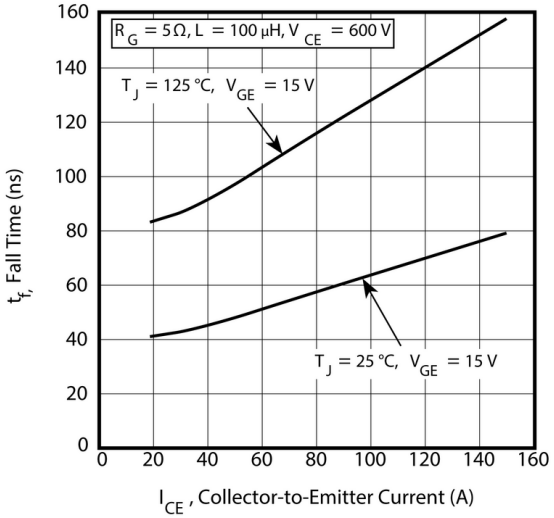


Figure 1-13. Turn-On Energy Loss vs. Collector Current

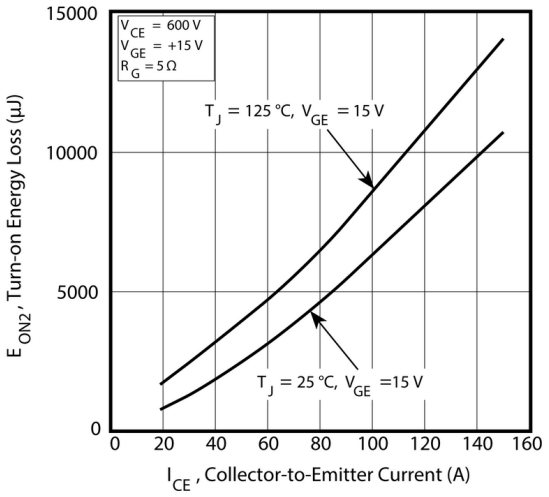


Figure 1-14. Turn-Off Energy Loss vs. Collector Current

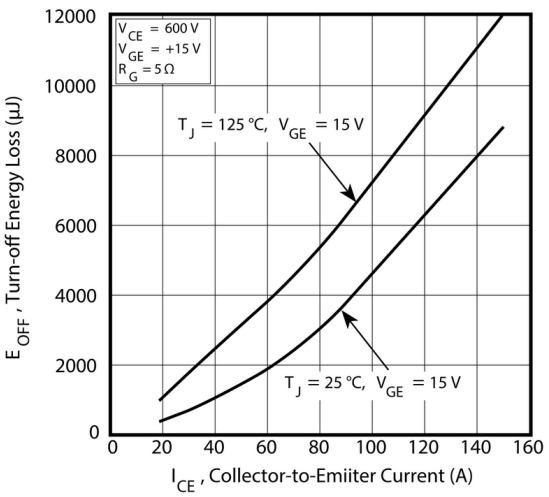


Figure 1-15. Switching Energy Losses vs. Gate Resistance

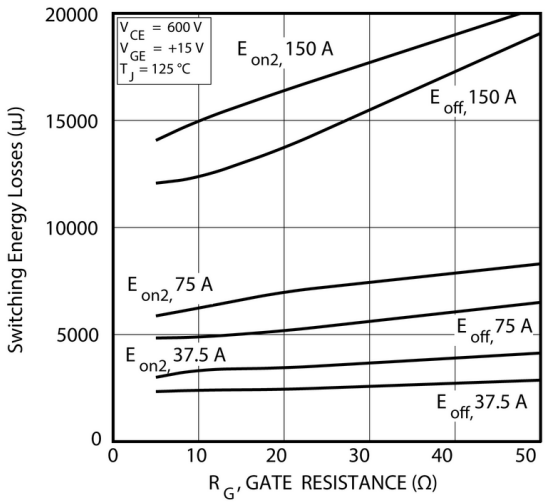


Figure 1-16. Switching Energy Losses vs. Junction Temperature

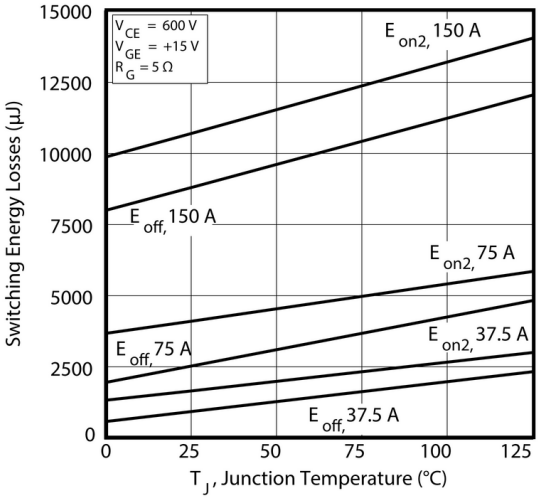


Figure 1-17. Capacitance vs. Collector-To-Emitter Voltage

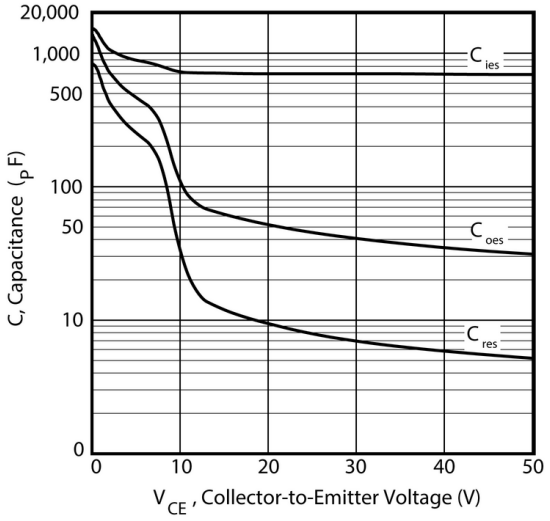


Figure 1-18. Reverse-bias Safe Operating Area

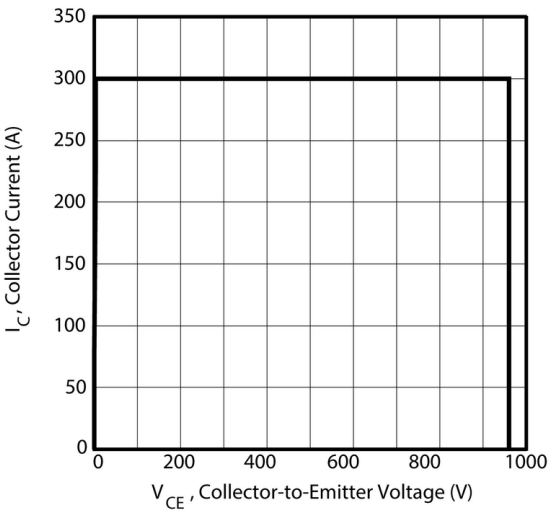


Figure 1-19. Maximum Transient Thermal Impedance

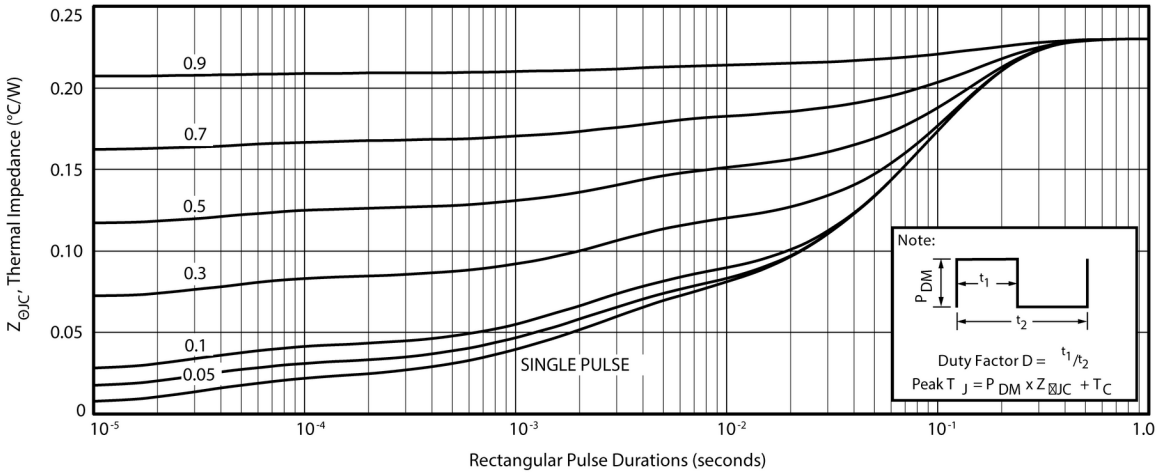


Figure 1-20. Transient Thermal Impedance Model

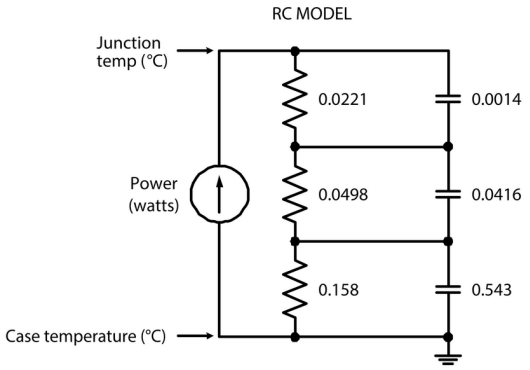


Figure 1-21. Operating Frequency vs. Collector Current

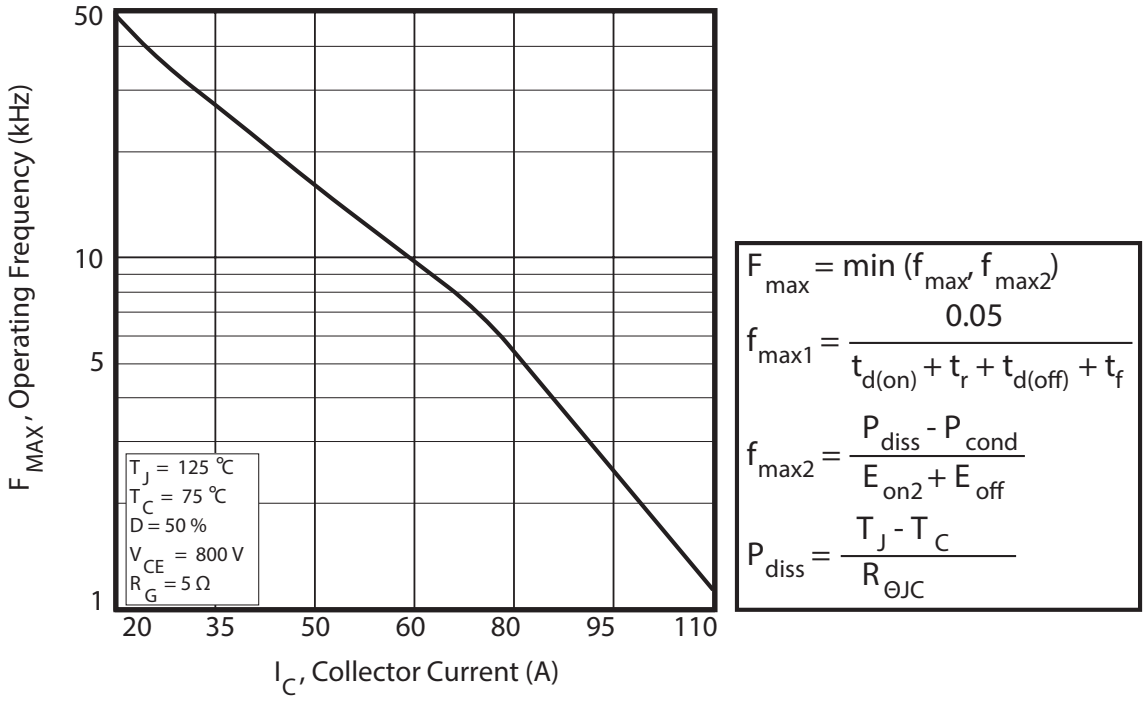


Figure 1-22. Inductive Switching Test Circuit

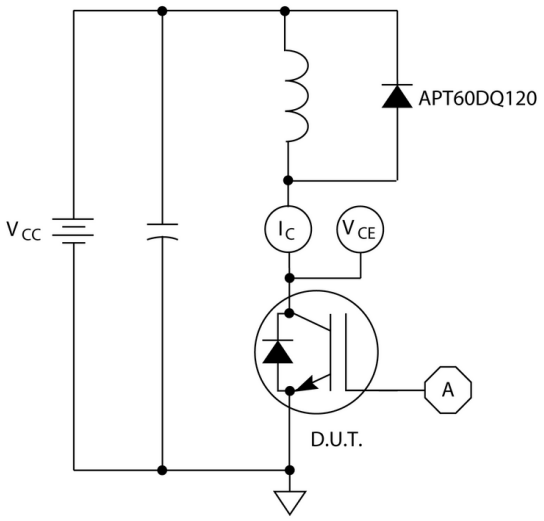


Figure 1-23. Turn-on Switching Waveforms and Definitions

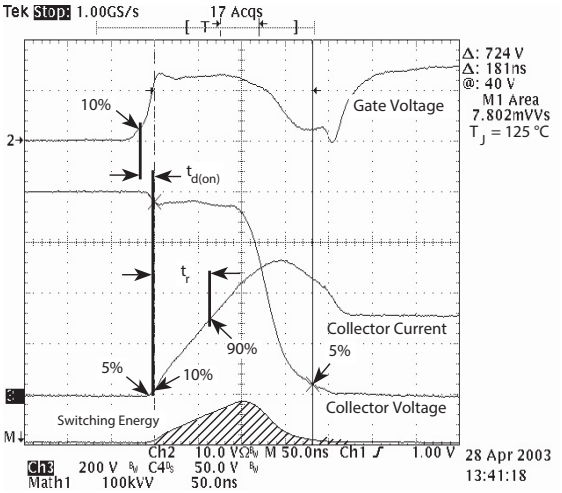


Figure 1-24. Turn-off Switching Waveforms and Definitions

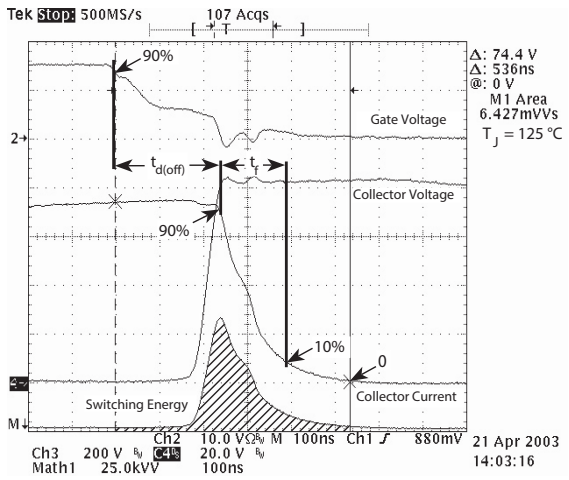
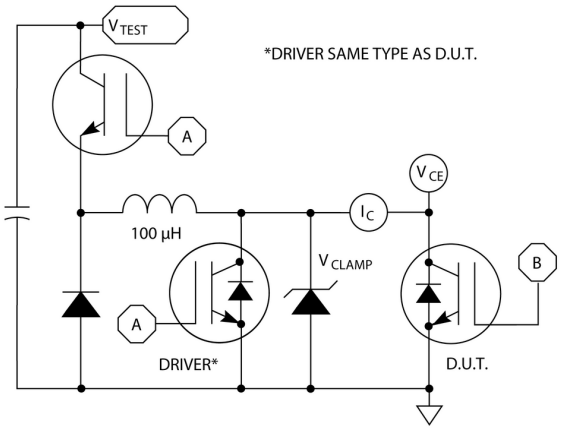


Figure 1-25. E_{on1} Test Circuit



2. Device Specifications: Ultrafast Soft Recovery Anti-Parallel Diode

This section shows the specifications of the Ultrafast Soft Recovery Anti-Parallel Diode.

2.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the anti-parallel diode.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
$I_F(AV)$	Maximum average forward current (T_C = 105 °C, Duty Cycle = 0.5)	60	A
$I_F(RMS)$	RMS forward current (square wave, 50% duty)	88	
I_{FSM}	Non-repetitive forward surge current (T_J = 45 °C, 8.3 ms)	540	

2.2 Electrical Performance

The following table shows the static characteristics of the anti-parallel diode. T_J = 25 °C unless otherwise specified.

Table 2-2. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
V_F	Forward voltage	I_F = 75 A		2.8		V
		I_F = 150 A		3.5		
		I_F = 75 A, T_J = 125 °C		2.2		

The following table shows the dynamic characteristics of the anti-parallel diode. T_J = 25 °C unless otherwise specified.

Table 2-3. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	I_F = 1 A di_F/dt = –100 A/µs V_R = 30 V		60		ns
t_{rr}	Reverse recovery time	I_F = 60 A		265		
Q_{rr}	Reverse recovery charge	di_F/dt = –200 A/µs		560		nC
I_{RRM}	Maximum reverse recovery current	V_R = 800 V		5		A
t_{rr}	Reverse recovery time	I_F = 60 A		350		ns
Q_{rr}	Reverse recovery charge	di_F/dt = –200 A/µs		2890		nC
I_{RRM}	Maximum reverse recovery current	V_R = 800 V T_C = 125 °C		13		A
t_{rr}	Reverse recovery time	I_F = 60 A		150		ns
Q_{rr}	Reverse recovery charge	di_F/dt = –1000 A/µs		4720		nC
I_{RRM}	Maximum reverse recovery current	V_R = 800 V T_C = 125 °C		40		A

2.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 2-1. Maximum Transient Thermal Impedance

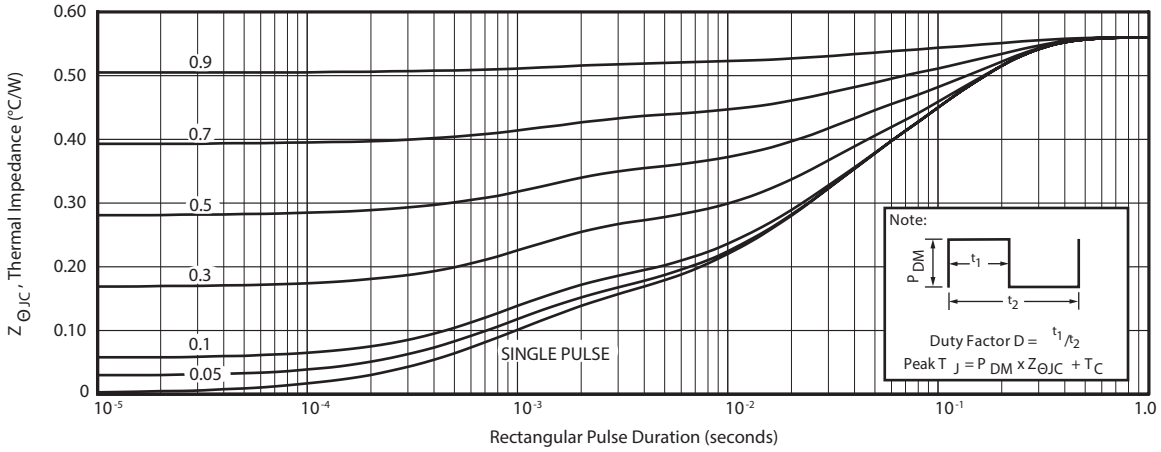


Figure 2-2. Transient Thermal Impedance Model

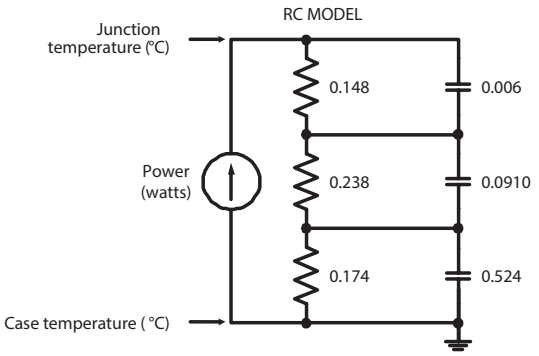


Figure 2-3. Forward Current vs. Forward Voltage

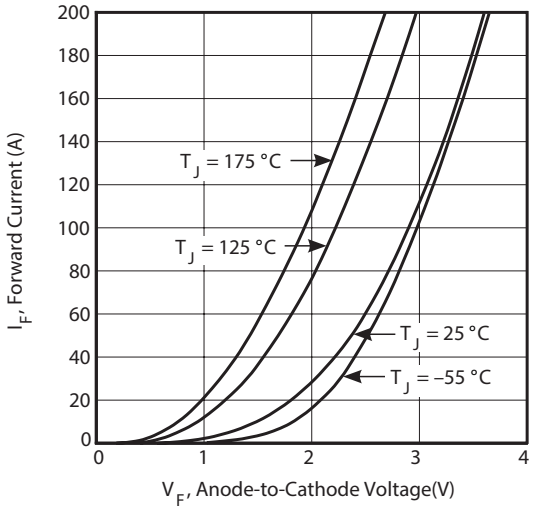


Figure 2-4. Reverse Recovery Time vs. Current Rate of Change

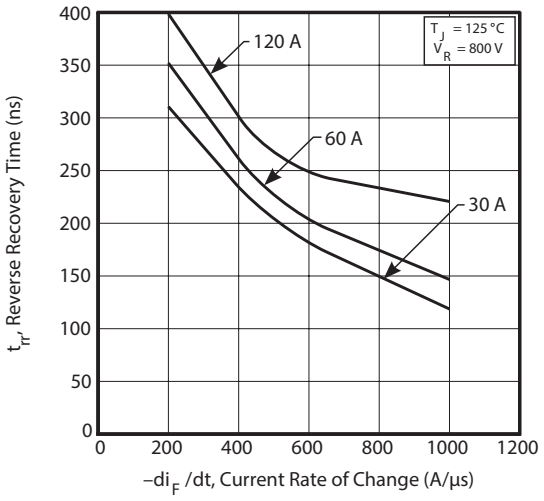


Figure 2-5. Reverse Recovery Charge vs. Current Rate of Change

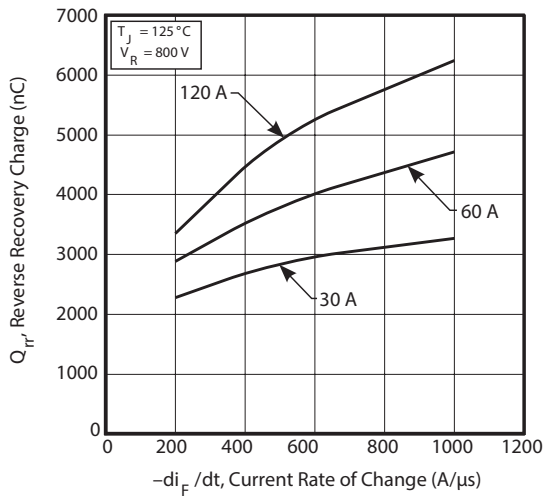


Figure 2-6. Reverse Recovery Current vs. Current Rate of Change

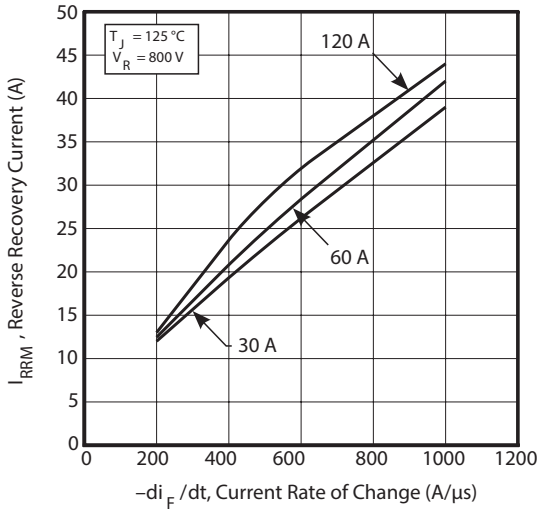


Figure 2-7. Dynamic Parameters vs. Junction Temperature

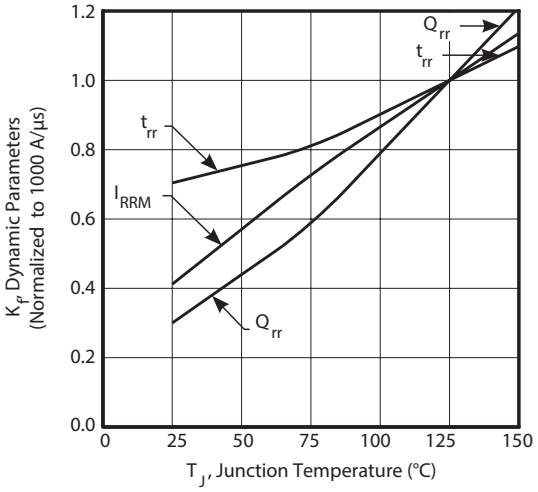


Figure 2-8. Maximum Average Forward Current vs. Case Temperature

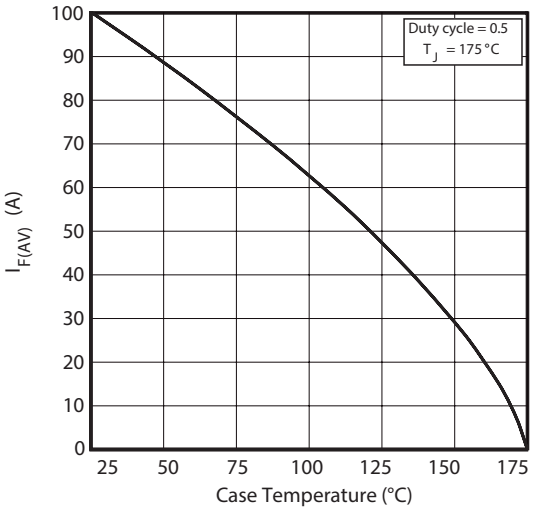
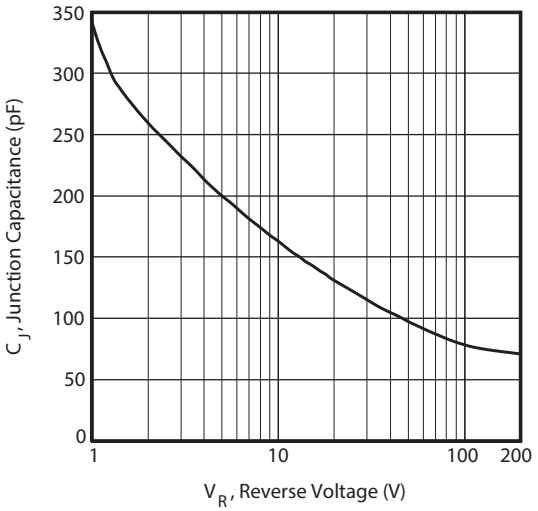


Figure 2-9. Junction Capacitance vs. Reverse Voltage



The following figure shows the diode test circuit of this device.

Figure 2-10. Diode Test Circuit

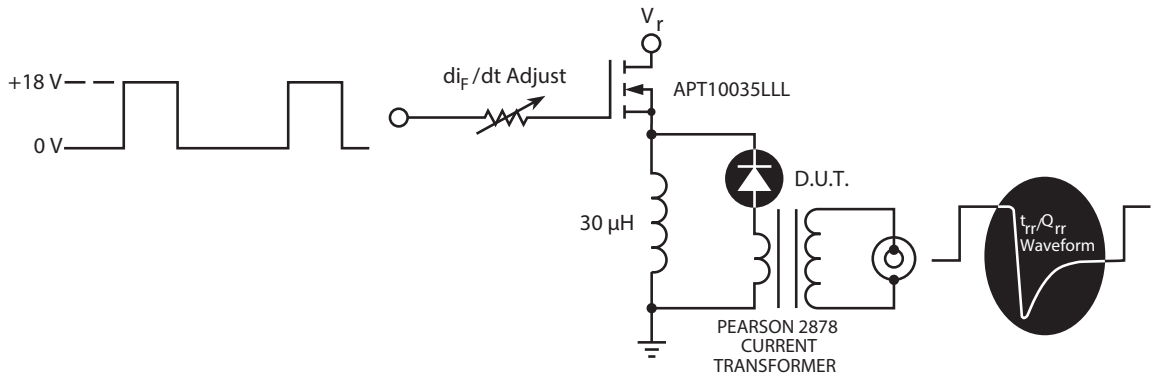
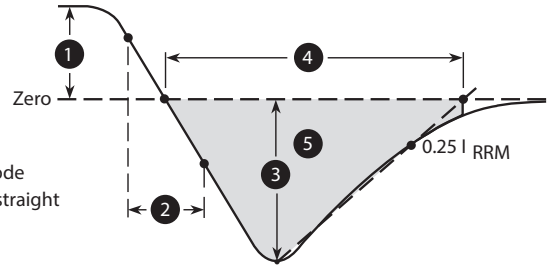


Figure 2-11. Diode Reverse Recovery Waveform and Definitions

1. I_F — Forward Conduction Current
2. di_F/dt — Rate of Diode Current Change Through Zero Crossing.
3. I_{RRM} — Maximum Reverse Recovery Current.
4. t_{rr} — Reverse Recovery Time, measured from zero crossing where diode current goes from positive to negative, to the point at which the straight line through I_{RRM} and 0.25 • I_{RRM} passes through zero.
5. Q_{rr} — Area Under the Curve Defined by I_{RRM} and t_{rr}.



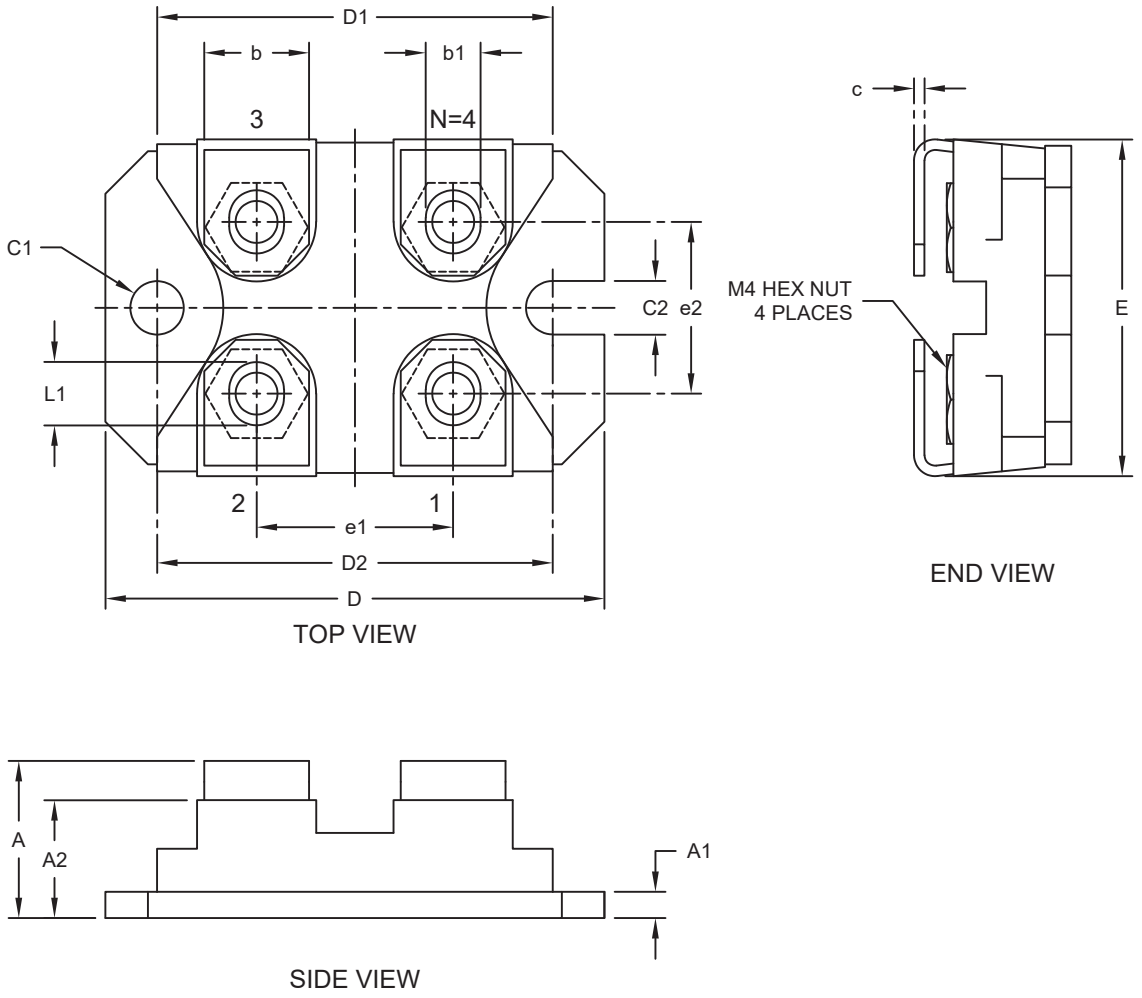
3. Package Specification

This section shows the package specification of this device.

3.1 Package Outline Drawing

The following figure illustrates the SOT-227 package outline of this device.

Figure 3-1. Package Outline Drawing



The following table shows the SOT-227 dimensions and should be used in conjunction with the package outline drawing.

Table 3-1. SOT-227 Dimensions

Dimension Limits		Dimensions (millimeters)	
		Min.	Max.
Number of terminals	N	4	
Terminal pitch	e1	14.9	15.1
Terminal pitch	e2	12.6	12.8
Overall height	A	11.8	12.2
Base plate thickness	A1	1.95	2.14

.....continued			
Dimension Limits		Dimensions (millimeters)	
		Min.	Max.
Molded package thickness	A2	8.9	9.6
Overall length	D	38.0	38.2
Molded package length	D1	31.5	31.7
Mounting centers	D2	30.1	30.3
Overal width	E	25.2	25.4
Terminal width	b	7.8	8.2
Terminal thickness	c	0.75	0.85
Terminal slot width	b1	4.1	4.3
Terminal slot length	L1	4.8	4.9
Mounting hole diameter	C1	4.0	4.2
Mounting slot width	C2	4.0	4.2

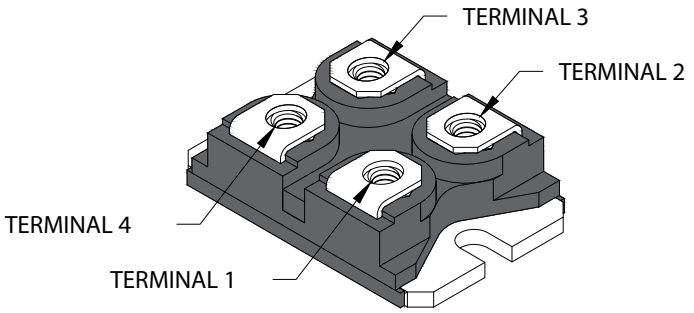
Note:

1. Dimensioning and tolerancing per ASME Y14.5M.

3.2 Terminal Pinout

The following figure illustrates the terminal pinout of this device.

Figure 3-2. Terminal Pinout



The following table shows the electrical signal terminal pinout of this device.

Table 3-2. Electrical Signal Terminal Pinout

Terminal	Definition
TERMINAL 1	Gate
TERMINAL 2	Collector, Cathode
TERMINAL 3	Emitter, Anode
TERMINAL 4	Emitter, Anode

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	05/2024	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00005343A, which replaces the previous Microsemi literature number 050-7458.
Initial release (Microsemi Revision A)	10/2005	Initial release.

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