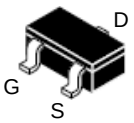
# Field Effect Transistor - N-Channel, Logic Level, Enhancement Mode

# NDS355AN




**SOT−23/SUPERSOT−23, 3 LEAD, 1.4x2.9**
**CASE 527AG**

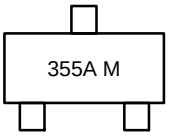
## General Description

SuperSOT™−3 N−Channel logic level enhancement mode power field effect transistors are produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on−state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in−line power loss are needed in a very small outline surface mount package.

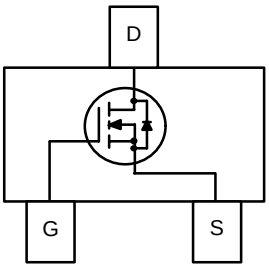
## Features

- 1.7 A, 30 V
  - $R_{DS(on)}$ = 0.125 Ω @ $V_{GS}$ = 4.5 V
  - $R_{DS(on)}$ = 0.085 Ω @ $V_{GS}$ = 10 V
- Industry Standard Outline SOT−23 Surface Mount Package Using Proprietary SUPERSOT−3 Design for Superior Thermal and Electrical Capabilities
- High Density Cell Design for Extremely Low $R_{DS(on)}$
- Exceptional On−Resistance and Maximum DC Current Capability
- Compact Industry Standard SOT−23 Surface Mount Package
- This is a Pb−Free Device

## MARKING DIAGRAM




355A = Specific Device Code
M = Date Code




**N−Channel**

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C, unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain−Source Voltage | 40 | V |
| $V_{GSS}$ | Gate−Source Voltage − Continuous | ±20 | V |
| $I_D$ | Maximum Drain Current<br>− Continuous (Note 1a)<br>− Pulsed | <br>1.7<br>10 | A |
| $P_D$ | Power Dissipation<br>(Note 1a)<br>(Note 1b) | <br>0.5<br>0.46 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS ($T_A$ = 25°C, unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 1a) | 250 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case (Note 1) | 75 | °C/W |

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NDS355AN | SOT−23−3/ SUPERSOT−23 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 30 | – | – | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| | | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V, $T_J$ = 125°C | – | – | 10 | |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | – | – | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | $V_{GS}$ = −20 V, $V_{DS}$ = 0 V | – | – | −100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | 1.6 | 2 | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA, $T_J$ = 125°C | 0.5 | 1.2 | 1.5 | |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 1.7 A | – | 0.105 | 0.125 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 1.7 A, $T_J$ = 125°C | – | 0.16 | 0.23 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 1.9 A | – | 0.065 | 0.085 | |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = 4.5 V, $V_{DS}$ = 5 V | 6 | – | – | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 1.7 A | – | 3.5 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | – | 195 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 135 | – | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 48 | – | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 10 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 10 | 20 | ns |
| $t_r$ | Turn–On Rise Time | | – | 13 | 25 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | – | 13 | 25 | ns |
| $t_f$ | Turn–Off Fall Time | | – | 4 | 10 | ns |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 5 V, $I_D$ = 1 A, $V_{GS}$ = 4.5V, $R_{GEN}$ = 6 Ω | – | 10 | 20 | ns |
| $t_r$ | Turn–On Rise Time | | – | 32 | 60 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | – | 10 | 20 | ns |
| $t_f$ | Turn–Off Fall Time | | – | 5 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 10 V, $I_D$ = 1.7 A, $V_{GS}$ = 5 V | – | 3.5 | 5 | nC |
| $Q_{gs}$ | Gate–Source Charge | | – | 0.8 | – | nC |
| $Q_{gd}$ | Gate–Drain Charge | | – | 1.7 | – | nC |
| **DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain−Source Diode Forward Current | | – | – | 0.42 | A |
| $I_{SM}$ | Maximum Pulsed Drain−Source Diode Forward Current | | – | – | 10 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 0.42 A (Note 2) | – | 0.8 | 1.2 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x 5" FR−4 PCB in a still air environment:

a) 250°C/W when mounted on a 0.02 $in^2$ pad of 2oz copper.

b) 270°C/W when mounted on a 0.001 $in^2$ pad of 2oz copper.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL ELECTRICAL CHARACTERISTICS

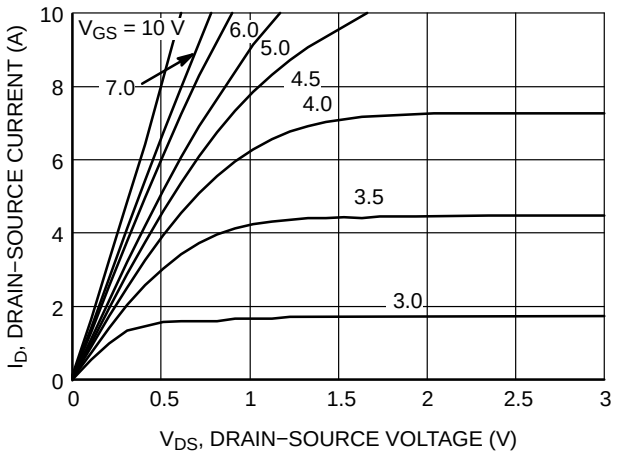



**Figure 1. On−Region Characteristics**

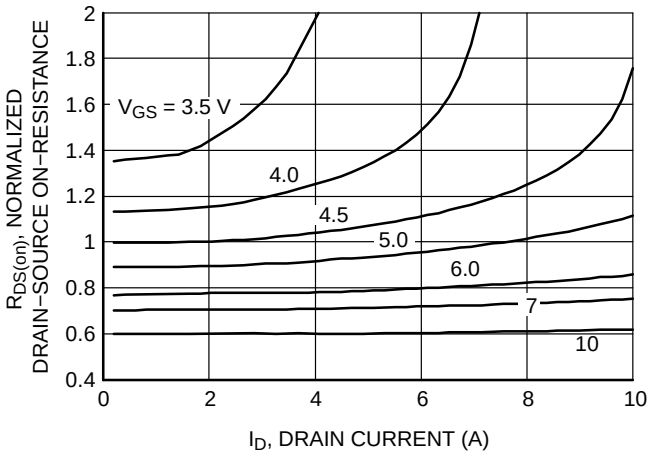



**Figure 2. On−Resistance Variation with Drain Current and Gate Voltage**

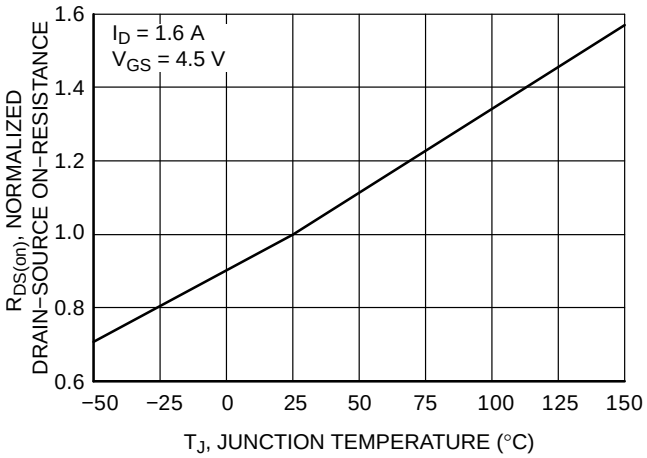



**Figure 3. On−Resistance Variation with Temperature**

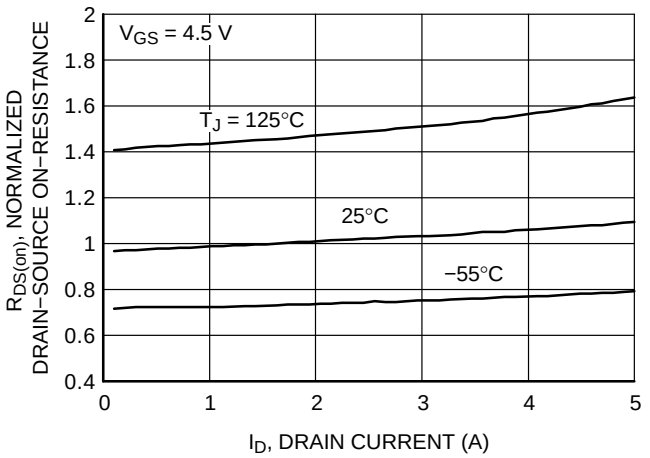



**Figure 4. On−Resistance Variation with Drain Current and Temperature**

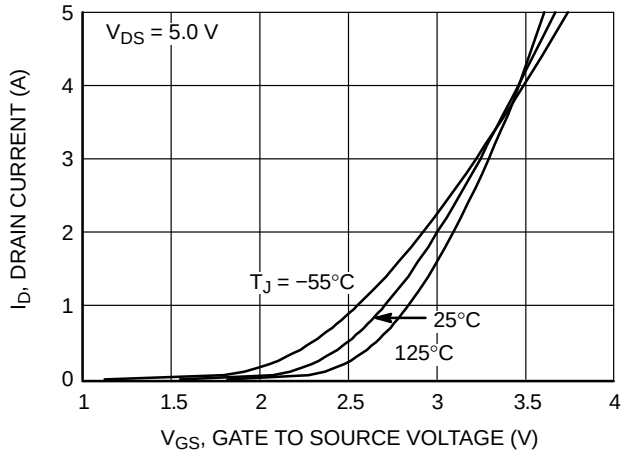



**Figure 5. Transfer Characteristics**

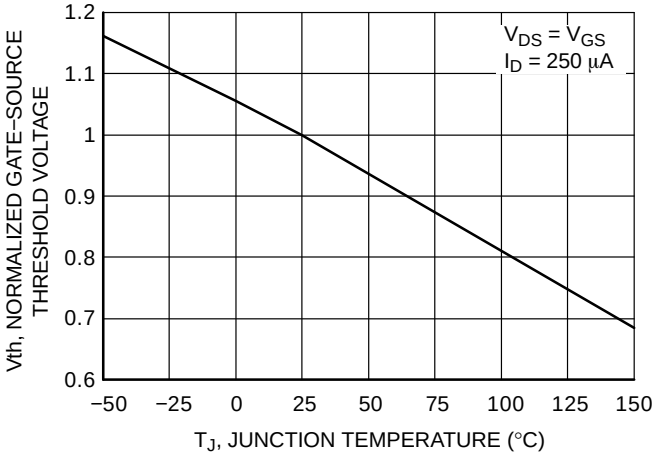



**Figure 6. Gate Threshold Variation with Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS (CONTINUED)

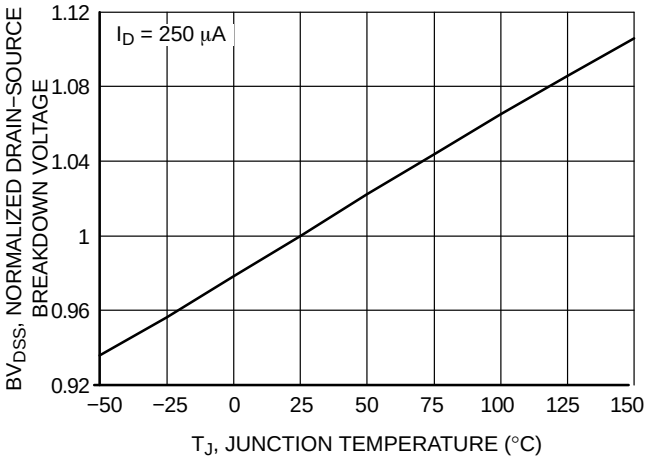



**Figure 7. Breakdown Voltage Variation with Temperature**

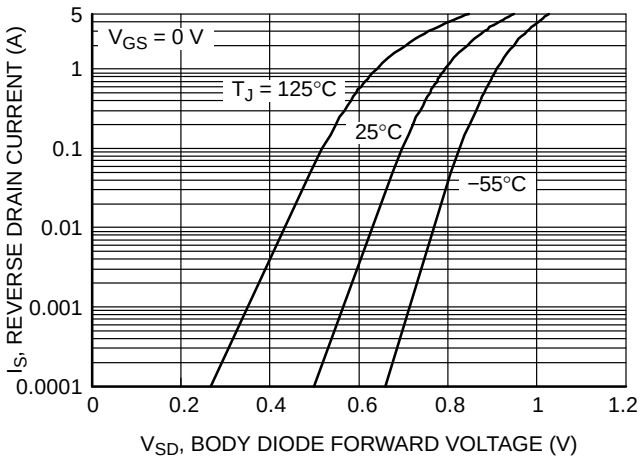



**Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature**

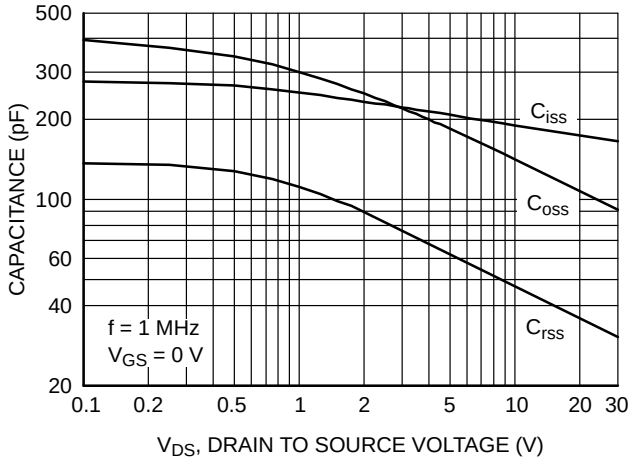



**Figure 9. Capacitance Characteristics**

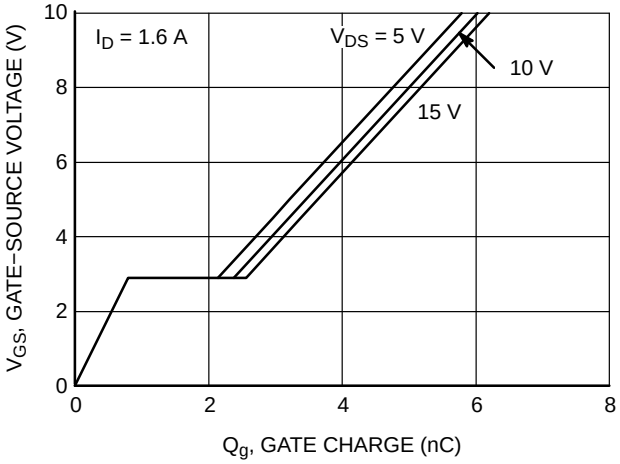



**Figure 10. Gate Charge Characteristics**

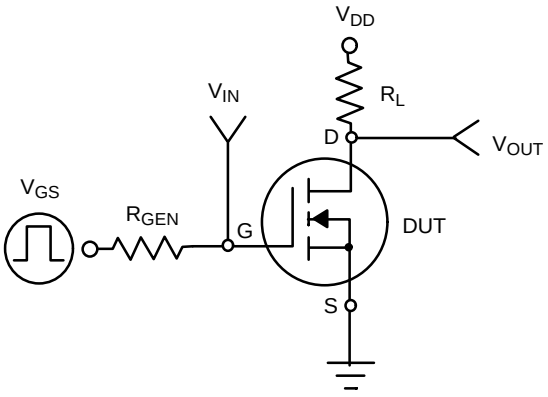



**Figure 11. Switching Test Circuit**

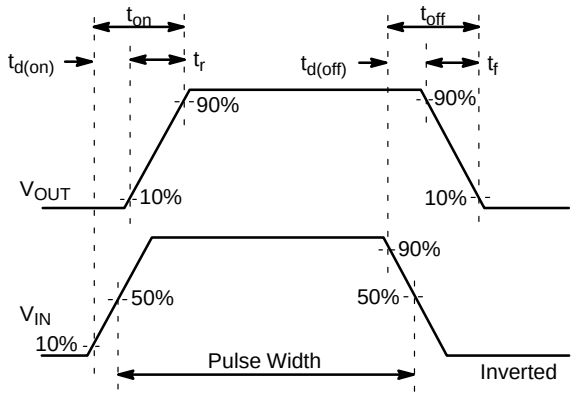



**Figure 12. Switching Waveforms**

## TYPICAL ELECTRICAL CHARACTERISTICS (CONTINUED)

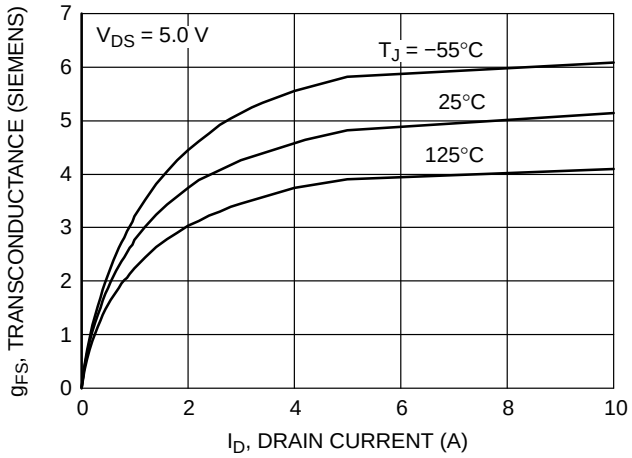



**Figure 13. Transconductance Variation with Drain Current and Temperature**

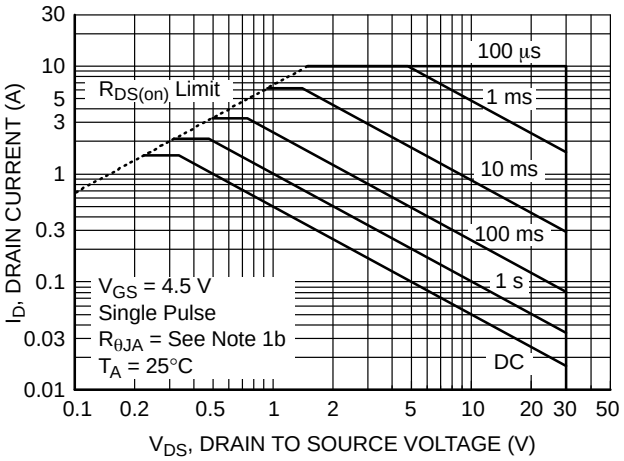



**Figure 14. Maximum Safe Operating Area**

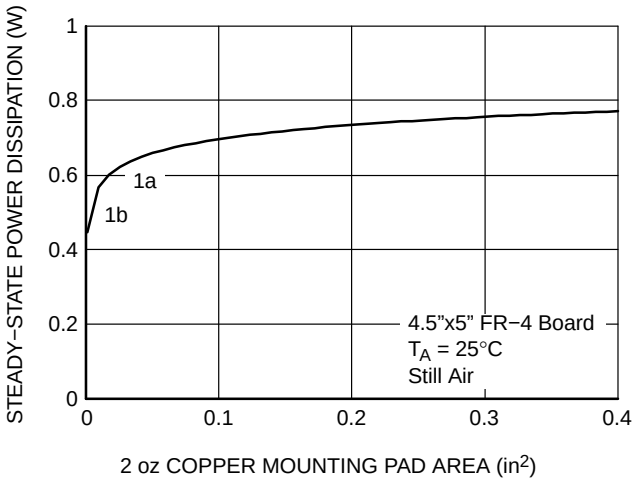



**Figure 15. SUPERSOT−3 Maximum Steady−State Power Dissipation vs. Copper Mounting Pad Area**

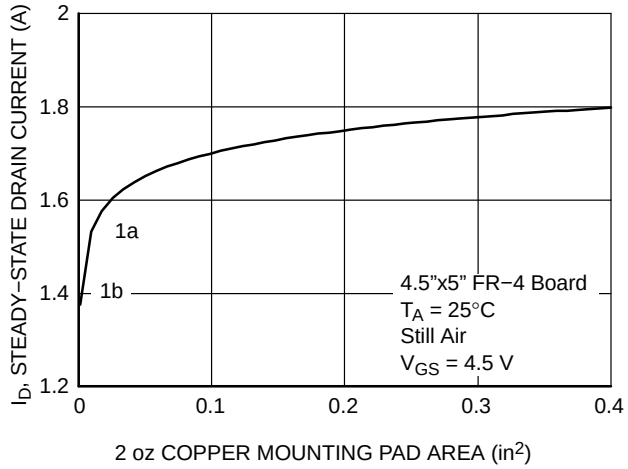



**Figure 16. Maximum Steady−State Drain Current vs. Copper Mounting Pad Area**

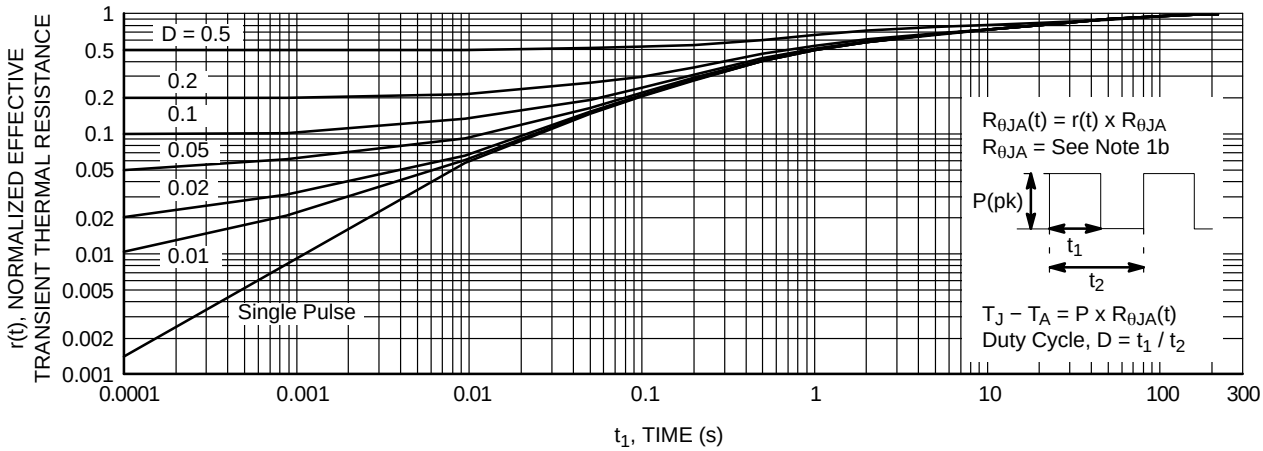
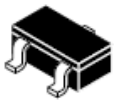


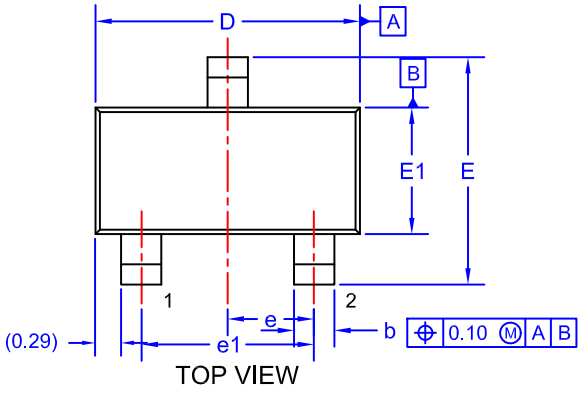

**Figure 17. Transient Thermal Response Curve**

NOTE: Characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.



**SOT−23/SUPERSOT™ −23, 3 LEAD, 1.4x2.9**
CASE 527AG
ISSUE A

DATE 09 DEC 2019

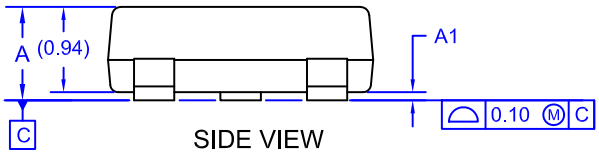


TOP VIEW

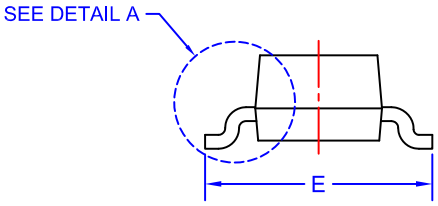
NOTES: UNLESS OTHERWISE SPECIFIED

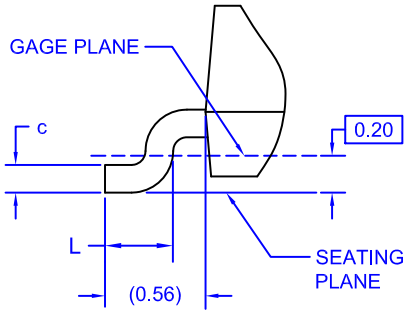
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

| DIM | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.85 | 0.95 | 1.12 |
| A1 | 0.00 | 0.05 | 0.10 |
| b | 0.370 | 0.435 | 0.508 |
| c | 0.085 | 0.150 | 0.180 |
| D | 2.80 | 2.92 | 3.04 |
| E | 2.31 | 2.51 | 2.71 |
| E1 | 1.20 | 1.40 | 1.52 |
| e | 0.95 BSC | | |
| e1 | 1.90 BSC | | |
| L | 0.33 | 0.38 | 0.43 |

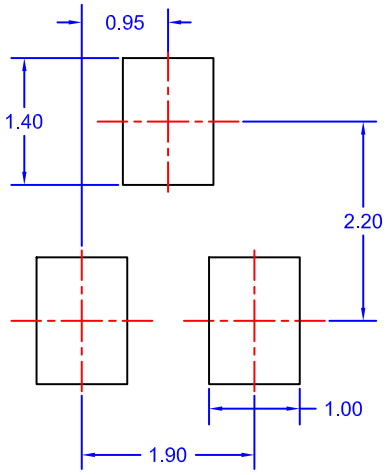


SIDE VIEW



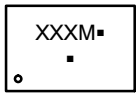
DETAIL A



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON34319E** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **SOT−23/SUPERSOT−23, 3 LEAD, 1.4X2.9** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales