FINAL DATA SHEET

Si823x 0.5 and 4.0 Amp ISOdrivers (2.5 and 5 kVRMS)

The Si823x isolated driver family combines two independent, isolated drivers into a single package. The Si8230/1/3/4 are high-side/low-side drivers, while the Si8232/5/7/8 are dual drivers. Versions with peak output currents of 0.5 A (Si8230/1/2/7) and 4.0 A (Si8233/4/5/8) are available. All drivers operate with a maximum supply voltage of 24 V.

The Si823x drivers utilize Skyworks' proprietary silicon isolation technology, which provides up to 5 kVRMS withstand voltage per UL1577 and fast 45 ns propagation times. Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage. The TTL level compatible inputs with >400 mV hysteresis are available in individual control input (Si8230/2/3/5/7/8) or PWM input (Si8231/4) configurations. High integration, low propagation delay, small installed size, flexibility, and cost-effectiveness make the Si823x family ideal for a wide range of isolated MOSFET/IGBT gate drive applications.

Automotive Grade is available for certain part numbers. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Industrial Applications

- Power delivery systems
- Motor control systems
- Isolated dc-dc power supplies
- Lighting control systems
- Plasma displays
- Solar and industrial inverters

Automotive Applications

- Onboard chargers
- Battery management systems
- Charging stations
- Traction inverters
- Hybrid Electric Vehicles
- Battery Electric Vehicles

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 5000 V_{RMS} for one minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
  - 60601-1 (2 MOPP)
- VDE certification conformity
  - 60747-17 (basic insulation)
- CQC certification approval
  - GB4943.1 (reinforced insulation)

Key Features

- Two completely isolated drivers in one package
  - Up to 5 kV_{RMS} input-to-output isolation
  - Up to 1500 V_{DC} peak driver-to-driver differential voltage
- HS/LS and dual driver versions
- Up to 8 MHz switching frequency
- 0.5 A peak output (Si8230/1/2/7)
- 4.0 A peak output (Si8233/4/5/8)
- High electromagnetic immunity
- RoHS-compliant packages:
  - SOIC-14/16 wide body
  - SOIC-16 narrow body
  - LGA-14
- AEC-Q100 qualification
- Automotive-grade OPNs available
  - AIAG compliant PPAP documentation support
  - IMDS and CAMDS listing support

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

1. Ordering Guide

Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an "-I" in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an "-A" in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 1. Si823x Ordering Guide [1,2,3]

Ordering Part Number (OPN)[4]	Automotive OPN[5,6]	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Package Type
Wide Body (WB) 5 kV Packages with 16- and 14-Pin Options							
Si8230BD-D-IS	Si8230BD-AS	VIA, VIB	High Side/Low Side	0.5 A	8 V	5.0 kVrms	SOIC-16 Wide Body
Si8231BD-D-IS	Si8231BD-AS	PWM	High Side/Low Side	0.5 A	8 V	5.0 kVrms	
Si8232BD-D-IS	Si8232BD-AS	VIA, VIB	Dual Driver	0.5 A	8 V	5.0 kVrms	
Si8233BD-D-IS	Si8233BD-AS	VIA, VIB	High Side/Low Side	4.0 A	8 V	5.0 kVrms	
Si8234BD-D-IS	Si8234BD-AS	PWM	High Side/Low Side	4.0 A	8 V	5.0 kVrms	
Si8235BD-D-IS	Si8235BD-AS	VIA, VIB	Dual Driver	4.0 A	8 V	5.0 kVrms	
Si8230AD-D-IS	Si8230AD-AS	VIA, VIB	High Side/Low Side	0.5 A	5 V	5.0 kVrms	
Si8231AD-D-IS	Si8231AD-AS	PWM	High Side/Low Side	0.5 A	5 V	5.0 kVrms	
Si8232AD-D-IS	Si8232AD-AS	VIA, VIB	Dual Driver	0.5 A	5 V	5.0 kVrms	
Si8233AD-D-IS	Si8233AD-AS	VIA, VIB	High Side/Low Side	4.0 A	5 V	5.0 kVrms	
Si8234AD-D-IS	Si8234AD-AS	PWM	High Side/Low Side	4.0 A	5 V	5.0 kVrms	
Si8235AD-D-IS	Si8235AD-AS	VIA, VIB	Dual Driver	4.0 A	5 V	5.0 kVrms	
Si8230AD-D-IS3	Si8230AD-AS3	VIA, VIB	High Side/Low Side	0.5 A	5 V	5.0 kVrms	SOIC-14 Wide Body with increased creepage
Si8230BD-D-IS3	Si8230BD-AS3	VIA, VIB	High Side/Low Side	0.5 A	8 V	5.0 kVrms	
Si8233AD-D-IS3	Si8233AD-AS3	VIA, VIB	High Side/Low Side	4.0 A	5 V	5.0 kVrms	
Si8233BD-D-IS3	Si8233BD-AS3	VIA, VIB	High Side/Low Side	4.0 A	8 V	5.0 kVrms	
Si8235AD-D-IS3	Si8235AD-AS3	VIA, VIB	Dual Driver	4.0 A	5 V	5.0 kVrms	
Si8235BD-D-IS3	Si8235BD-AS3	VIA, VIB	Dual Driver	4.0 A	8 V	5.0 kVrms	

Table 1. Si823x Ordering Guide (Continued)[1,2,3]

Ordering Part Number (OPN)[4]	Automotive OPN[5,6]	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Package Type
Wide Body (WB) 2.5 kV Packages							
Si8230BB-D-IS	Si8230BB-AS	VIA, VIB	High Side/Low Side	0.5 A	8 V	2.5 kVrms	SOIC-16 Wide Body
Si8231BB-D-IS	Si8231BB-AS	PWM	High Side/Low Side	0.5 A	8 V	2.5 kVrms	
Si8232BB-D-IS	Si8232BB-AS	VIA, VIB	Dual Driver	0.5 A	8 V	2.5 kVrms	
Si8234CB-D-IS	Si8234CB-AS	PWM	High Side/Low Side	4.0 A	10 V	2.5 kVrms	
Si8233BB-D-IS	Si8233BB-AS	VIA, VIB	High Side/Low Side	4.0 A	8 V	2.5 kVrms	
Si8234BB-D-IS	Si8234BB-AS	PWM	High Side/Low Side	4.0 A	8 V	2.5 kVrms	
Si8235BB-D-IS	Si8235BB-AS	VIA, VIB	Dual Driver	4.0 A	8 V	2.5 kVrms	
Si8230AB-D-IS	Si8230AB-AS	VIA, VIB	High Side/Low Side	0.5 A	5 V	2.5 kVrms	
Si8231AB-D-IS	Si8231AB-AS	PWM	High Side/Low Side	0.5 A	5 V	2.5 kVrms	
Si8232AB-D-IS	Si8232AB-AS	VIA, VIB	Dual Driver	0.5 A	5 V	2.5 kVrms	
Si8233AB-D-IS	Si8233AB-AS	VIA, VIB	High Side/Low Side	4.0 A	5 V	2.5 kVrms	
Si8234AB-D-IS	Si8234AB-AS	PWM	High Side/Low Side	4.0 A	5 V	2.5 kVrms	
Si8235AB-D-IS	Si8235AB-AS	VIA, VIB	Dual Driver	4.0 A	5 V	2.5 kVrms	
Narrow Body (NB) Packages with 1, 2.5, and 3.75 kV Options							
Si8230BB-D-IS1	Si8230BB-AS1	VIA, VIB	High Side/Low Side	0.5 A	8 V	2.5 kVrms	SOIC-16 Narrow Body
Si8231BB-D-IS1	Si8231BB-AS1	PWM	High Side/Low Side	0.5 A	8 V	2.5 kVrms	
Si8232BB-D-IS1	Si8232BB-AS1	VIA, VIB	Dual Driver	0.5 A	8 V	2.5 kVrms	
Si8233BB-D-IS1	Si8233BB-AS1	VIA, VIB	High Side/Low Side	4.0 A	8 V	2.5 kVrms	
Si8234BB-D-IS1	Si8234BB-AS1	PWM	High Side/Low Side	4.0 A	8 V	2.5 kVrms	
Si8235BB-D-IS1	Si8235BB-AS1	VIA, VIB	Dual Driver	4.0 A	8 V	2.5 kVrms	
Si8235BA-D-IS1	Si8235BA-AS1	VIA, VIB	Dual Driver	4.0 A	8 V	1.0 kVrms	
Si8230AB-D-IS1	Si8230AB-AS1	VIA, VIB	High Side/Low Side	0.5 A	5 V	2.5 kVrms	
Si8231AB-D-IS1	Si8231AB-AS1	PWM	High Side/Low Side	0.5 A	5 V	2.5 kVrms	
Si8232AB-D-IS1	Si8232AB-AS1	VIA, VIB	Dual Driver	0.5 A	5 V	2.5 kVrms	
Si8233AB-D-IS1	Si8233AB-AS1	VIA, VIB	High Side/Low Side	4.0 A	5 V	2.5 kVrms	
Si8234AB-D-IS1	Si8234AB-AS1	PWM	High Side/Low Side	4.0 A	5 V	2.5 kVrms	
Si8235AB-D-IS1	Si8235AB-AS1	VIA, VIB	Dual Driver	4.0 A	5 V	2.5 kVrms	
Si8230BC-D-IS1	Si8230BC-AS1	VIA, VIB	High Side/Low Side	0.5 A	8 V	3.75 kVrms	
Si8231BC-D-IS1	Si8231BC-AS1	PWM	High Side/Low Side	0.5 A	8 V	3.75 kVrms	
Si8232BC-D-IS1	Si8232BC-AS1	VIA, VIB	Dual Driver	0.5 A	8 V	3.75 kVrms	
Si8233BC-D-IS1	Si8233BC-AS1	VIA, VIB	High Side/Low Side	4.0 A	8 V	3.75 kVrms	
Si8234BC-D-IS1	Si8234BC-AS1	PWM	High Side/Low Side	4.0 A	8 V	3.75 kVrms	
Si8235BC-D-IS1	Si8235BC-AS1	VIA, VIB	Dual Driver	4.0 A	8 V	3.75 kVrms	

Table 1. Si823x Ordering Guide (Continued)[1,2,3]

Ordering Part Number (OPN)[4]	Automotive OPN[5,6]	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Package Type
Si8230AC-D-IS1	Si8230AC-AS1	VIA, VIB	High Side/Low Side	0.5 A	5 V	3.75 kVrms	SOIC-16 Narrow Body
Si8231AC-D-IS1	Si8231AC-AS1	PWM	High Side/Low Side	0.5 A	5 V	3.75 kVrms	
Si8232AC-D-IS1	Si8232AC-AS1	VIA, VIB	Dual Driver	0.5 A	5 V	3.75 kVrms	
Si8233AC-D-IS1	Si8233AC-AS1	VIA, VIB	High Side/Low Side	4.0 A	5 V	3.75 kVrms	
Si8234AC-D-IS1	Si8234AC-AS1	PWM	High Side/Low Side	4.0 A	5 V	3.75 kVrms	
Si8235AC-D-IS1	Si8235AC-AS1	VIA, VIB	Dual Driver	4.0 A	5 V	3.75 kVrms	
LGA Packages							
Si8233CB-D-IM	Si8233CB-AM	VIA, VIB	High Side/Low Side	4.0 A	10 V	2.5 kVrms	LGA-14 5x5 mm
Si8233BB-D-IM	Si8233BB-AM	VIA, VIB	High Side/Low Side	4.0 A	8 V	2.5 kVrms	
Si8233AB-D-IM	Si8233AB-AM	VIA, VIB	High Side/Low Side	4.0 A	5 V	2.5 kVrms	
Si8234BB-D-IM	Si8234BB-AM	PWM	High Side/Low Side	4.0 A	8 V	2.5 kVrms	
Si8234AB-D-IM	Si8234AB-AM	PWM	High Side/Low Side	4.0 A	5 V	2.5 kVrms	
Si8235BB-D-IM	Si8235BB-AM	VIA, VIB	Dual Driver	4.0 A	8 V	2.5 kVrms	
Si8235AB-D-IM	Si8235AB-AM	VIA, VIB	Dual Driver	4.0 A	5 V	2.5 kVrms	
3 V Expanded VDDI Option in Multiple Packages							
Si8237AB-D-IS1	Si8237AB-AS1	VIA, VIB	Dual Driver	0.5 A	5 V	2.5 kVrms	SOIC-16 Narrow Body
Si8237BB-D-IS1	Si8237BB-AS1	VIA, VIB	Dual Driver	0.5 A	8 V	2.5 kVrms	
Si8238AB-D-IS1	Si8238AB-AS1	VIA, VIB	Dual Driver	4.0 A	5 V	2.5 kVrms	
Si8238BB-D-IS1	Si8238BB-AS1	VIA, VIB	Dual Driver	4.0 A	8 V	2.5 kVrms	
Si8237AC-D-IS1	Si8237AC-AS1	VIA, VIB	Dual Driver	0.5 A	5 V	3.75 kVrms	
Si8237BC-D-IS1	Si8237BC-AS1	VIA, VIB	Dual Driver	0.5 A	8 V	3.75 kVrms	
Si8238AC-D-IS1	Si8238AC-AS1	VIA, VIB	Dual Driver	4.0 A	5 V	3.75 kVrms	
Si8238BC-D-IS1	Si8238BC-AS1	VIA, VIB	Dual Driver	4.0 A	8 V	3.75 kVrms	
Si8237AD-D-IS	Si8237AD-AS	VIA, VIB	Dual Driver	0.5 A	5 V	5.0 kVrms	SOIC-16 Wide Body
Si8237BD-D-IS	Si8237BD-AS	VIA, VIB	Dual Driver	0.5 A	8 V	5.0 kVrms	
Si8238AD-D-IS	Si8238AD-AS	VIA, VIB	Dual Driver	4.0 A	5 V	5.0 kVrms	
Si8238BD-D-IS	Si8238BD-AS	VIA, VIB	Dual Driver	4.0 A	8 V	5.0 kVrms	
Si8238AD-D-IS3	Si8238AD-AS3	VIA, VIB	Dual Driver	4.0 A	5 V	5.0 kVrms	SOIC-14 Wide Body with increased creepage
Si8238BD-D-IS3	Si8238BD-AS3	VIA, VIB	Dual Driver	4.0 A	8 V	5.0 kVrms	

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. The temperature ranges is –40 to +125 °C.
4. An “R” at the end of the part number denotes tape and reel packaging option.
5. Automotive-Grade devices (with an “–A” suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with an "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In the top markings of each device, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

2. System Overview

2.1. Top Level Block Diagrams

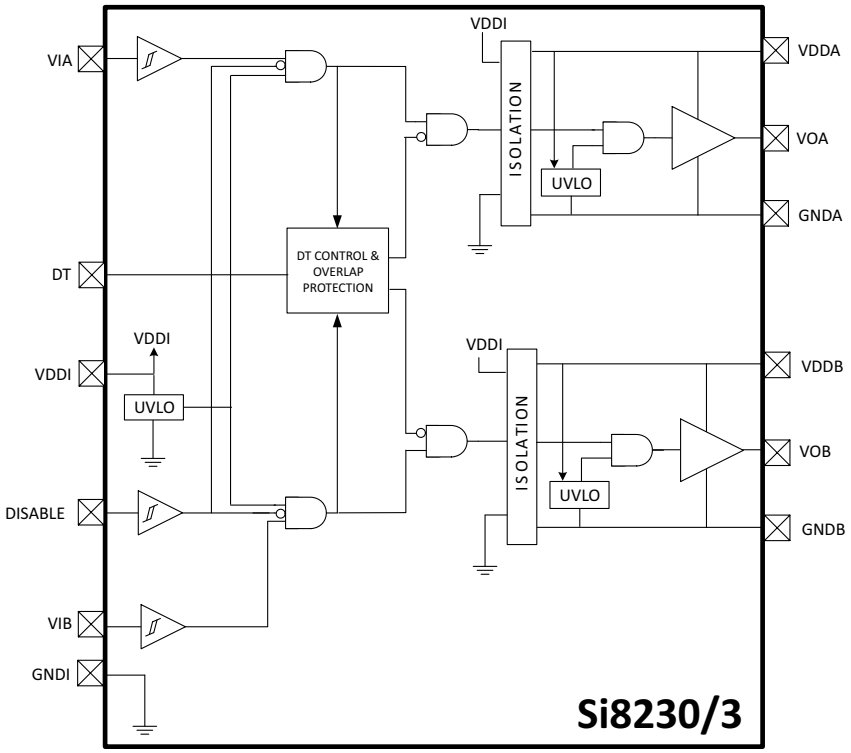


Figure 1. Si8230/3 Two-Input High-Side/Low-Side Isolated Drivers

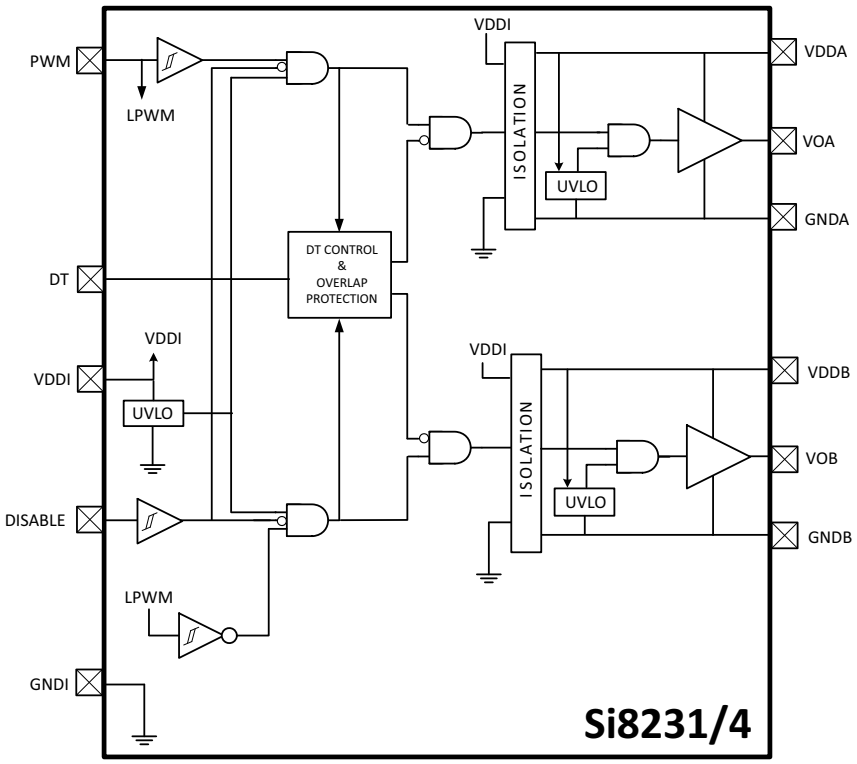


Figure 2. Si8231/4 Single-Input High-Side/Low-Side Isolated Drivers

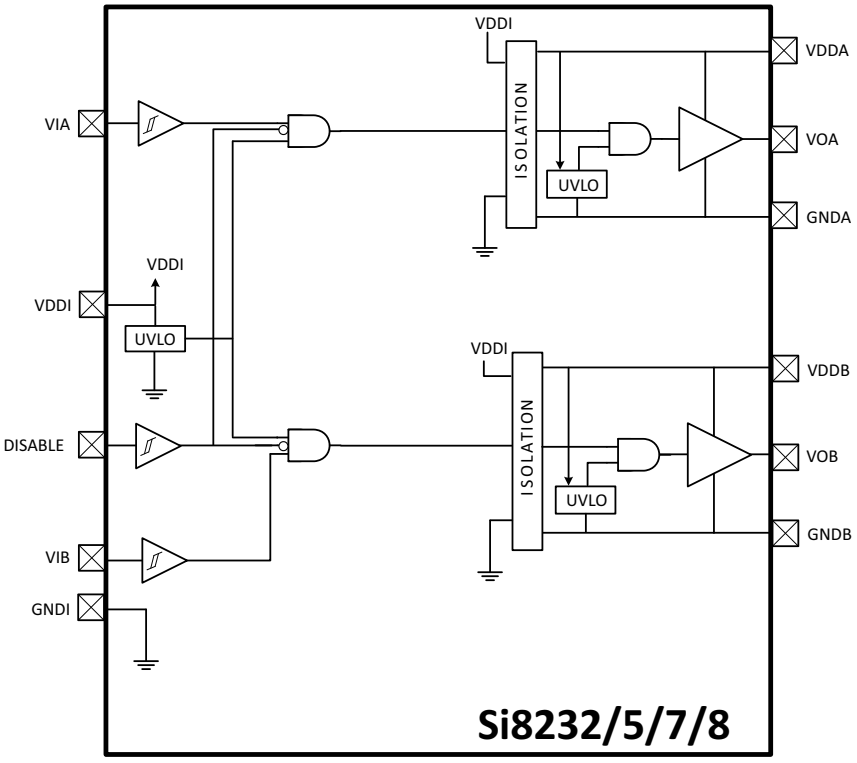


Figure 3. Si8232/5/7/8 Dual Isolated Drivers

2.2. Functional Description

The operation of an Si823x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si823x channel is shown in the figure below.

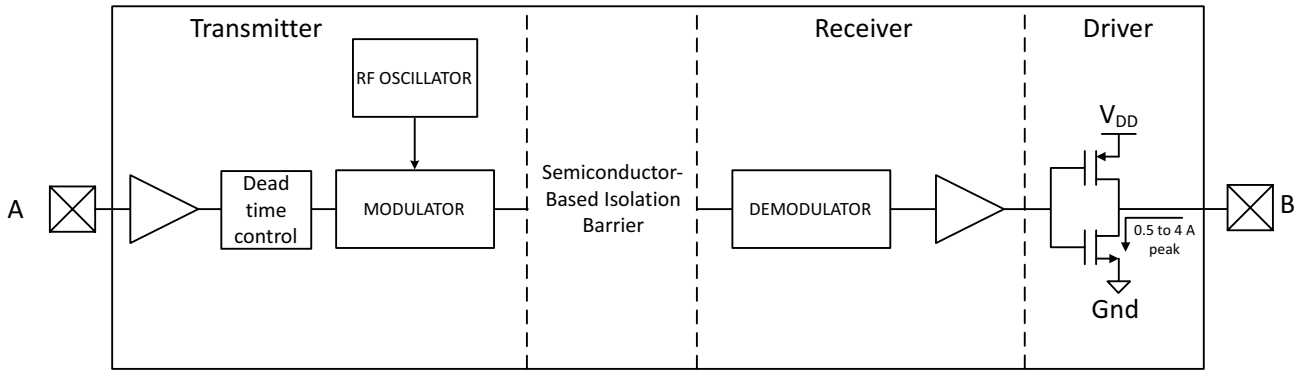


Figure 4. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the figure below for more details.

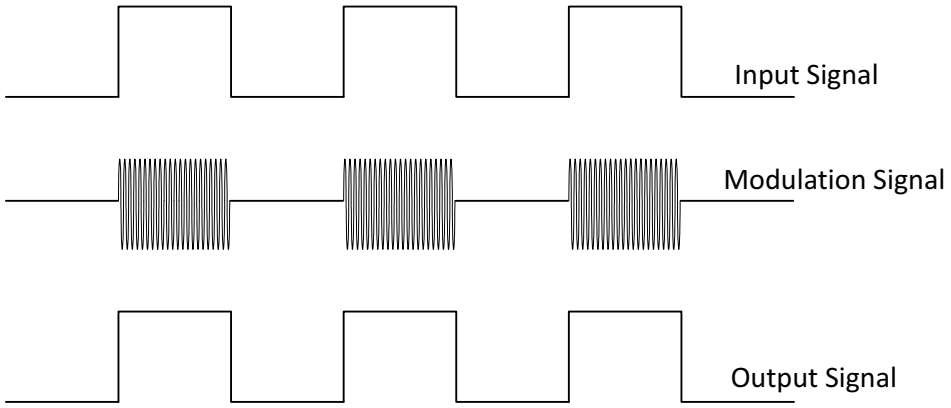


Figure 5. Modulation Scheme

2.3. Typical Operating Characteristics (0.5 Amp)

The typical performance characteristics depicted in Figure 6 through Figure 15 are for information purposes only. Refer to Table 6. "Electrical Characteristics" for actual specification limits.

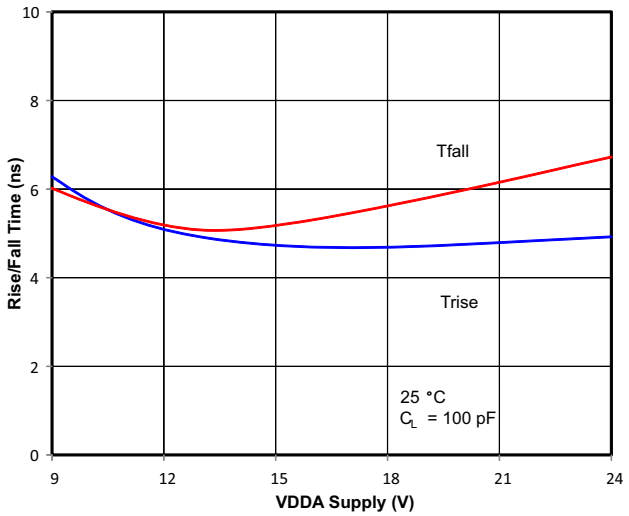


Figure 6. Rise/Fall Time vs. Supply Voltage

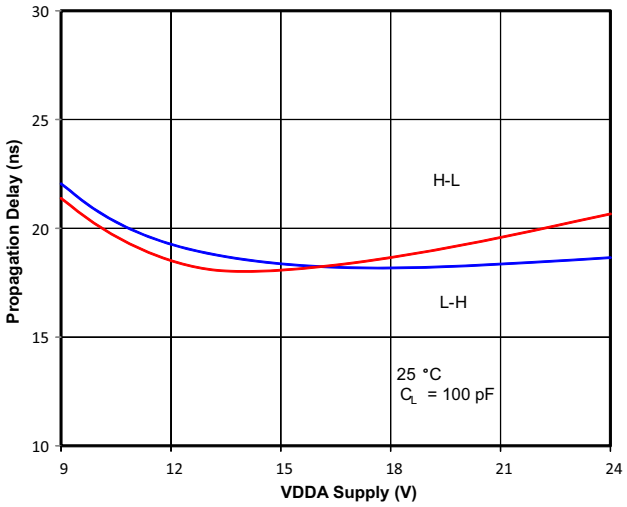


Figure 7. Propagation Delay vs. Supply Voltage

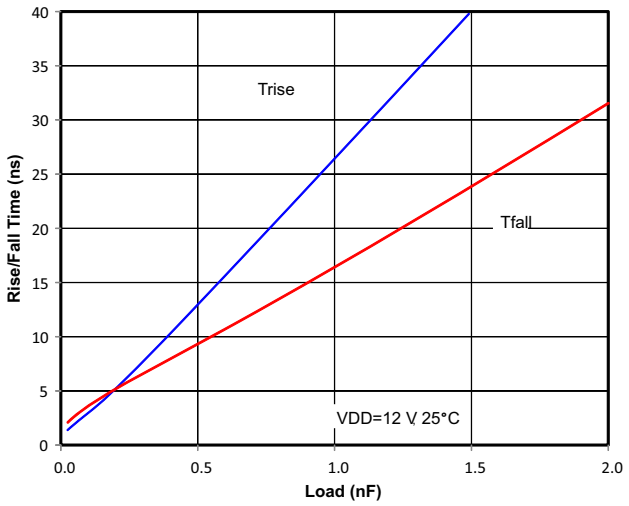


Figure 8. Rise/Fall Time vs. Load

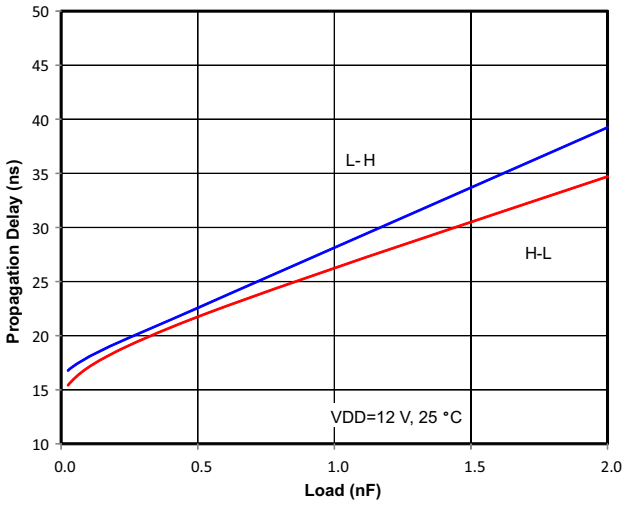


Figure 9. Propagation Delay vs. Load

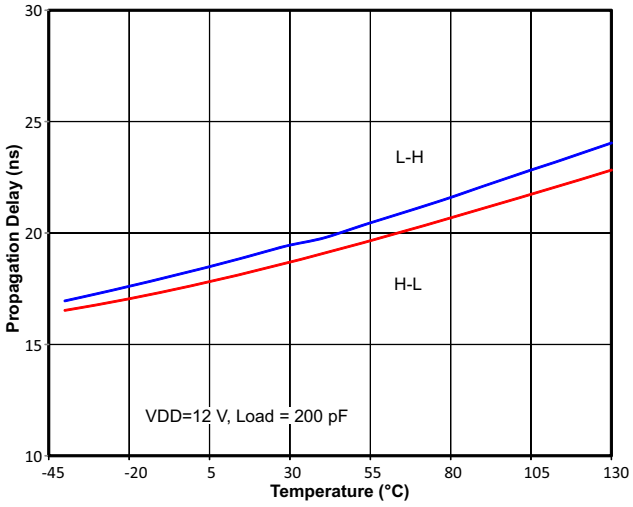


Figure 10. Propagation Delay vs. Temperature

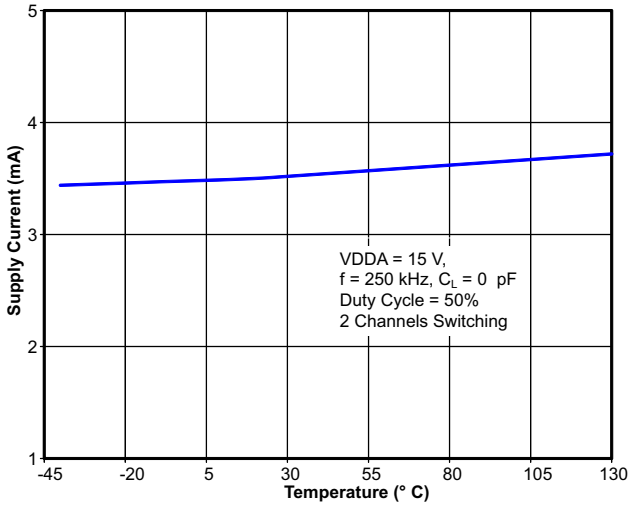


Figure 11. Supply Current vs. Temperature

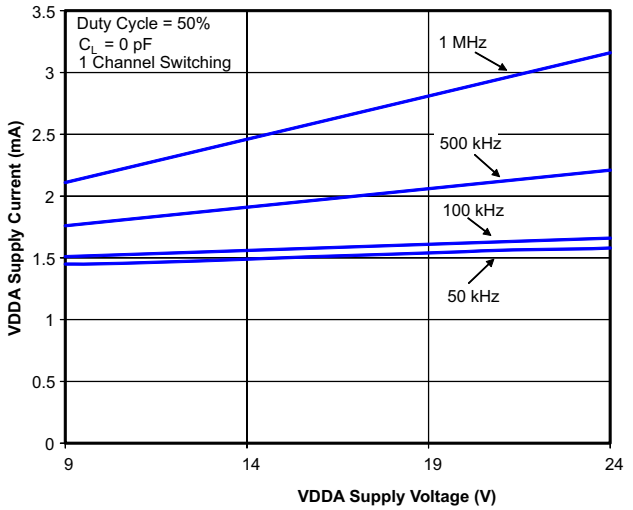


Figure 12. Supply Current vs. Supply Voltage

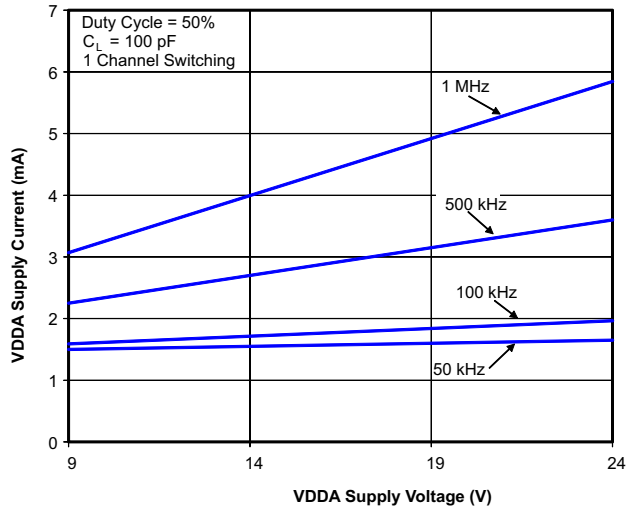


Figure 13. Supply Current vs. Supply Voltage

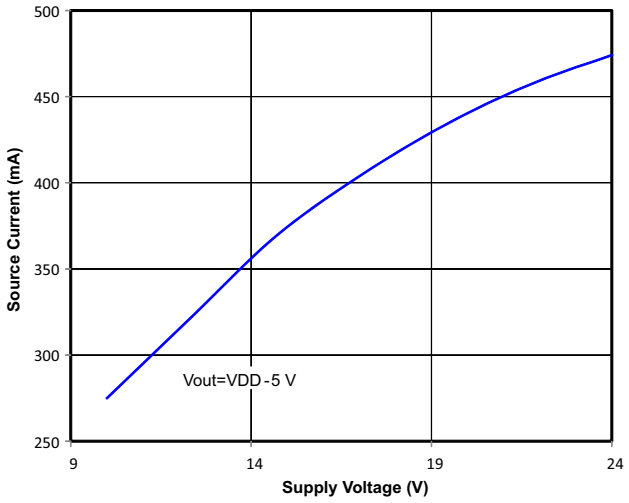


Figure 14. Output Source Current vs. Supply Voltage

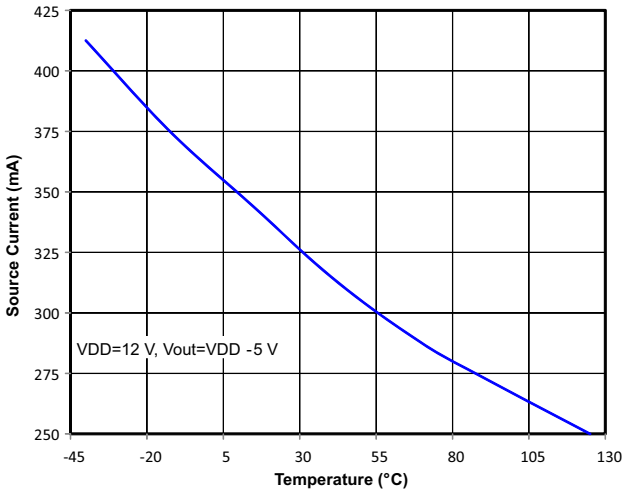


Figure 15. Output Source Current vs. Temperature

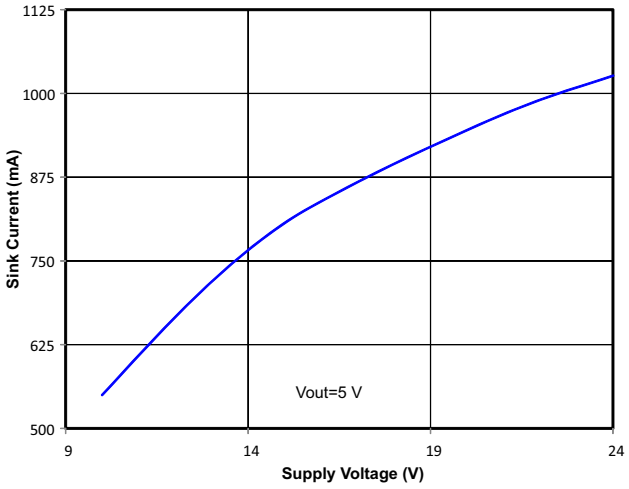


Figure 16. Output Sink Current vs. Supply Voltage

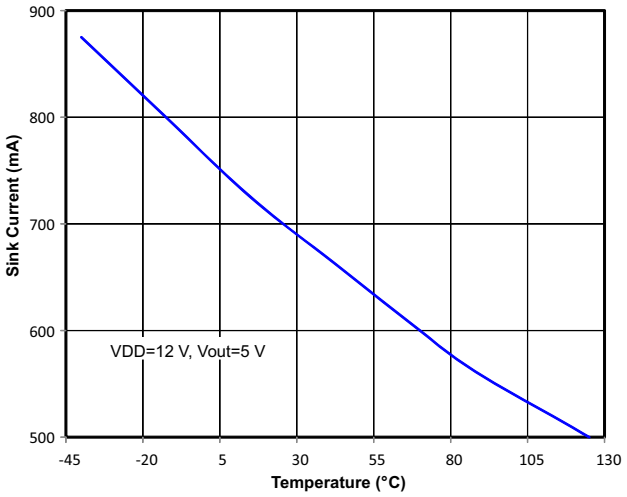


Figure 17. Output Sink Current vs. Temperature

2.4. Typical Operating Characteristics (4.0 Amp)

The typical performance characteristics depicted in Figure 18. "Rise/Fall Time vs. Supply Voltage" through Figure 27. "Output Source Current vs. Temperature" are for information purposes only. Refer to Table 6. "Electrical Characteristics" for actual specification limits.

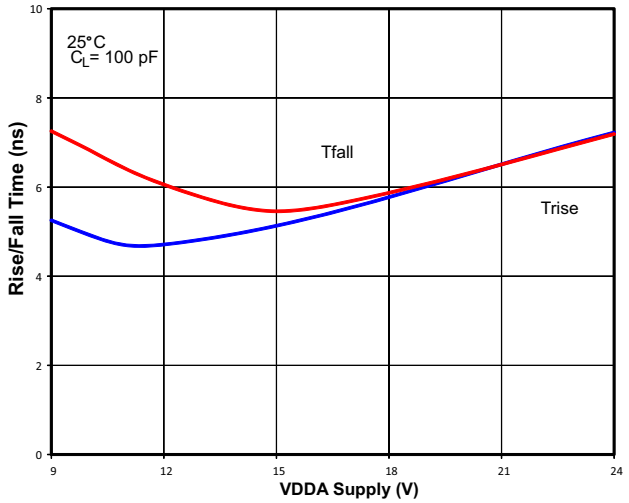


Figure 18. Rise/Fall Time vs. Supply Voltage

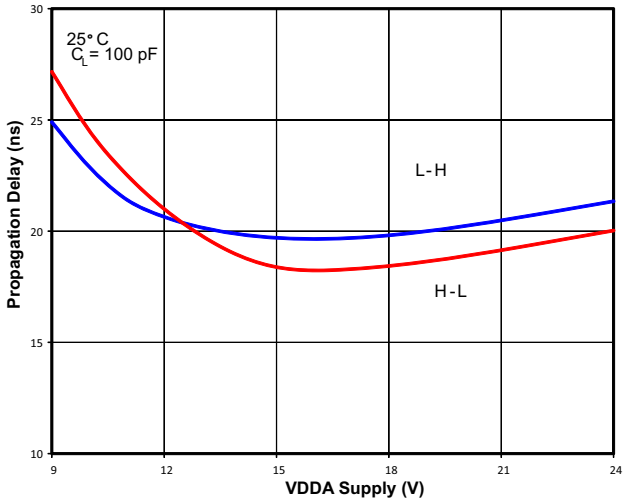


Figure 19. Propagation Delay vs. Supply Voltage

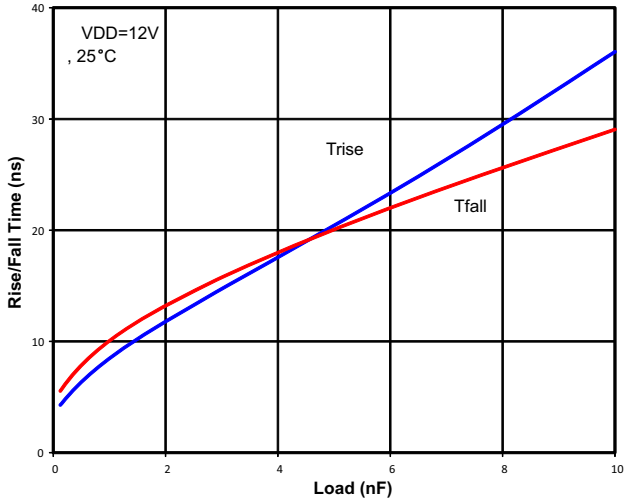


Figure 20. Rise/Fall Time vs. Load

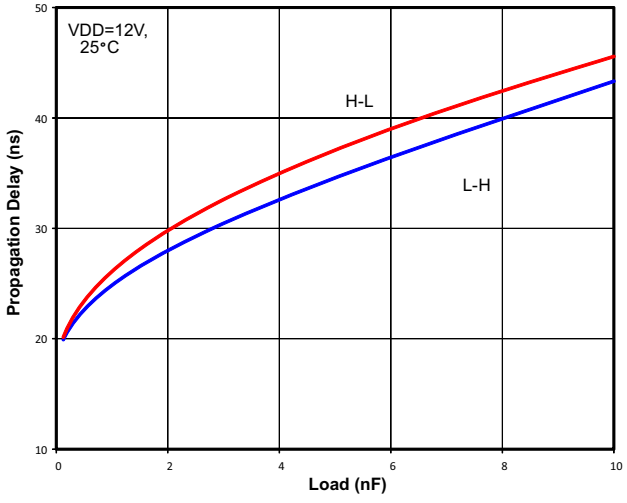


Figure 21. Propagation Delay vs. Load

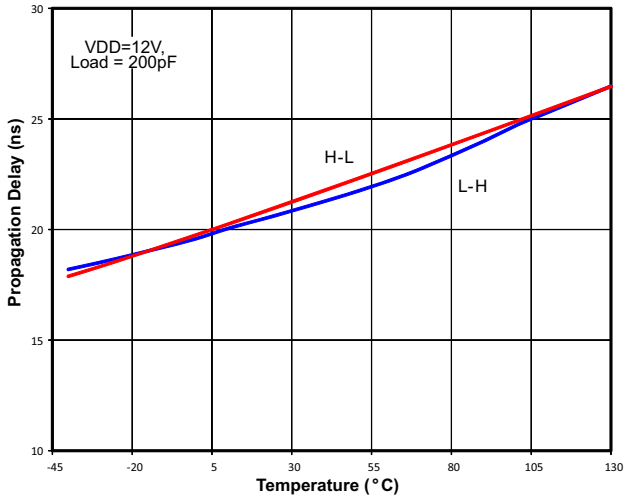


Figure 22. Propagation Delay vs. Temperature

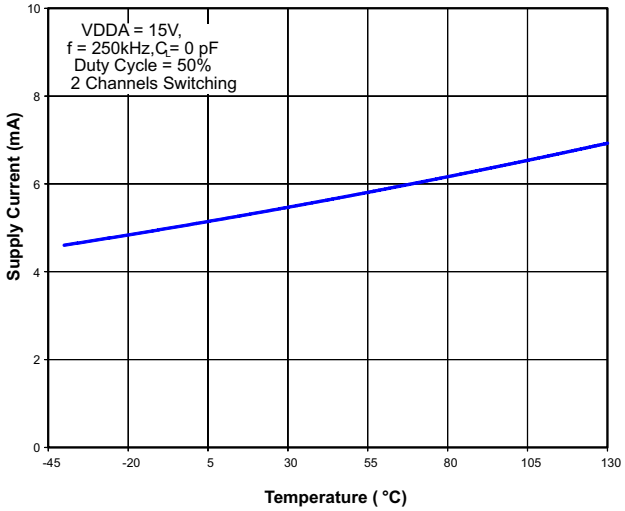


Figure 23. Supply Current vs. Temperature

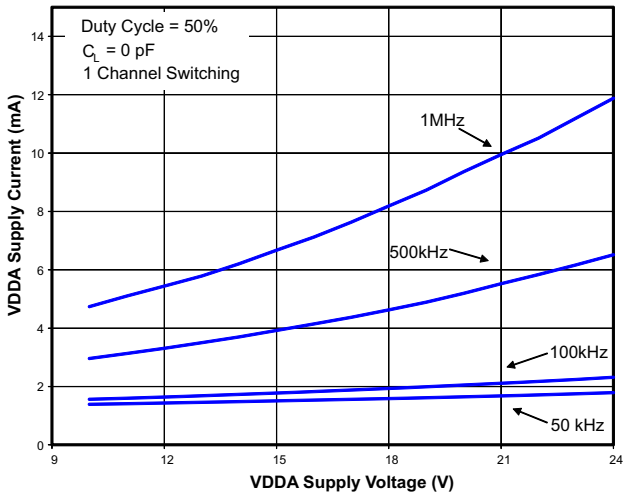


Figure 24. Supply Current vs. Supply Voltage

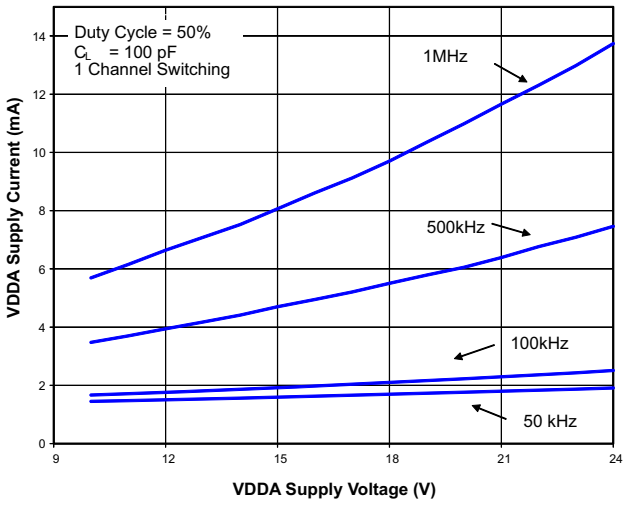


Figure 25. Supply Current vs. Supply Voltage

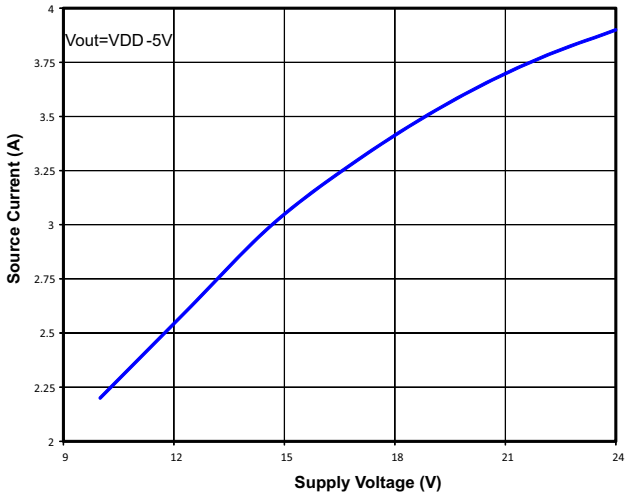


Figure 26. Output Source Current vs. Supply Voltage

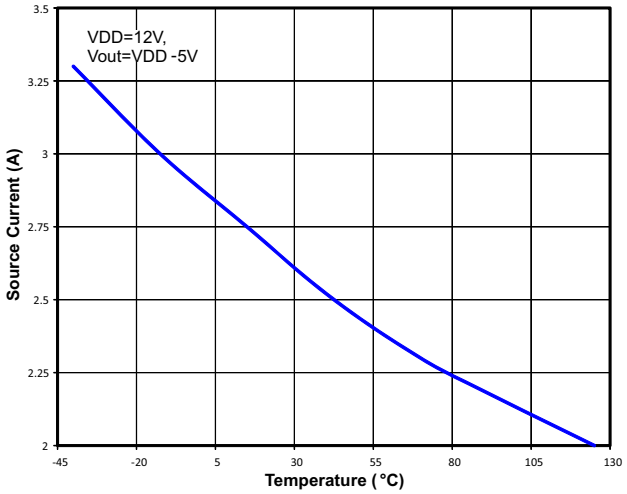


Figure 27. Output Source Current vs. Temperature

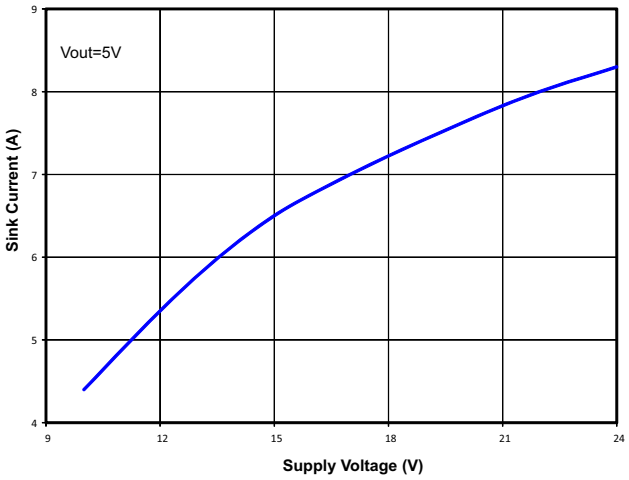


Figure 28. Output Sink Current vs. Supply Voltage

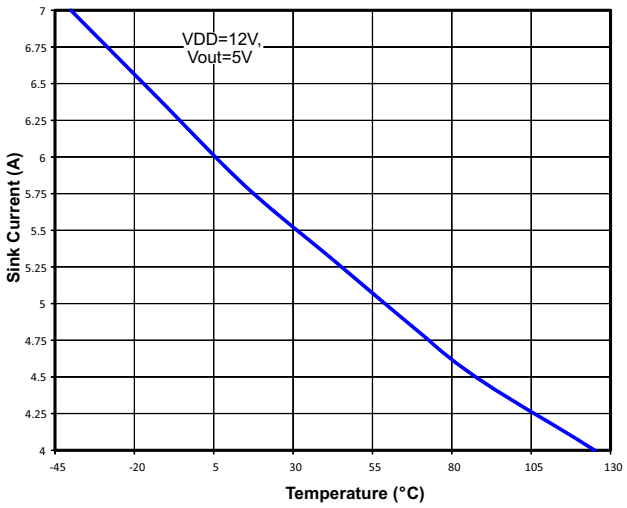


Figure 29. Output Sink Current vs. Temperature

2.5. Family Overview and Logic Operation During Startup

The Si823x family of isolated drivers consists of high-side, low-side, and dual driver configurations.

2.5.1. Products

The table below shows the configuration and functional overview for each product in this family.

Table 2. Si823x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8230	High-Side/Low-Side	✓	✓	VIA, VIB	0.5
Si8231	High-Side/Low-Side	✓	✓	PWM	0.5
Si8232/7	Dual Driver	—	—	VIA, VIB	0.5
Si8233	High-Side/Low-Side	✓	✓	VIA, VIB	4.0
Si8234	High-Side/Low-Side	✓	✓	PWM	4.0
Si8235/8	Dual Driver	—	—	VIA, VIB	4.0

2.5.2. Device Behavior

The following are truth tables for the Si8230/3, Si8231/4, and Si8232/5/7/8 families.

Table 3. Si8230/3 (High-Side/Low-Side) Truth Table[1]

Inputs		VDDI State	Disable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	L	L	L	Output transition occurs after internal dead time expires.
L	H	Powered	L	L	H	Output transition occurs after internal dead time expires.
H	L	Powered	L	H	L	Output transition occurs after internal dead time expires.
H	H	Powered	L	L	L	Invalid state. Output transition occurs after internal dead time expires.
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.

1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see 2.6. "Undervoltage Lockout Operation" for more information.
2. Note that an input can power the input die through an internal diode if its source has adequate current.

Table 4. Si8231/4 (PWM Input High-Side/Low-Side) Truth Table[1]

PWM Input	VDDI State	Disable	Output		Notes
			VOA	VOB	
H	Powered	L	H	L	Output transition occurs after internal dead time expires.
L	Powered	L	L	H	Output transition occurs after internal dead time expires.
X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	Powered	H	L	L	Device is disabled.

1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see 2.6. "Undervoltage Lockout Operation" for more information.
2. Note that an input can power the input die through an internal diode if its source has adequate current.

Table 5. Si8232/5/7/8 (Dual Driver) Truth Table[1]

Inputs		VDDI State	Disable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	L	L	L	Output transition occurs immediately (no internal dead time).
L	H	Powered	L	L	H	Output transition occurs immediately (no internal dead time).
H	L	Powered	L	H	L	Output transition occurs immediately (no internal dead time).
H	H	Powered	L	H	H	Output transition occurs immediately (no internal dead time).
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.

1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see 2.6. "Undervoltage Lockout Operation" for more information.
2. Note that an input can power the input die through an internal diode if its source has adequate current.

2.6. Undervoltage Lockout Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 30, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Note that outputs VOA and VOB default low when input side power supply (VDDI) is not present.

2.6.1. Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period t_{START}. Following this, the outputs follow the states of inputs VIA and VIB.

2.6.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own undervoltage lockout monitors.

The Si823x input side enters UVLO when VDDI $\leq$ $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The driver outputs, VOA and VOB, remain low when the input side of the Si823x is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

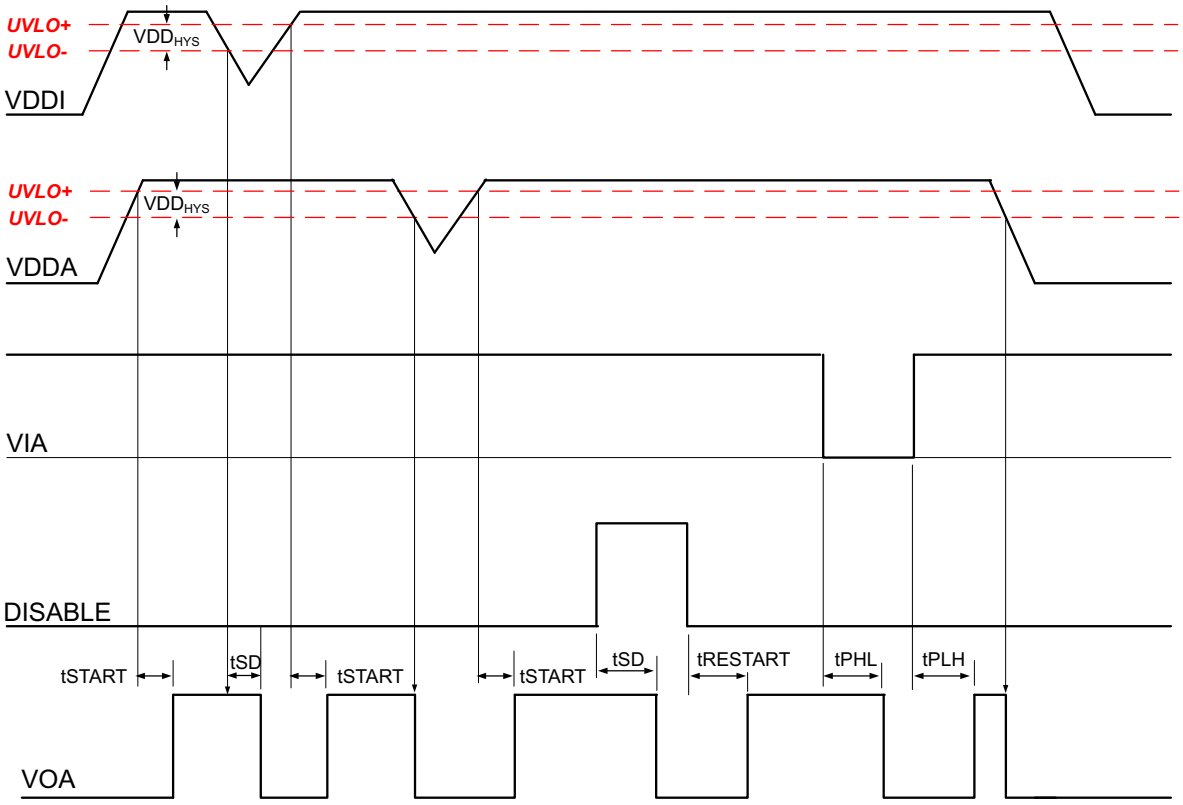


Figure 30. Device Behavior during Normal Operation and Shutdown

2.6.3. Control Inputs

VIA, VIB, and PWM inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high. For PWM input versions (Si8231/4), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

2.6.4. Disable Input

When brought high, the DISABLE input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within t_{SD} after DISABLE = V_{IH} and resumes within $t_{RESTART}$ after DISABLE = V_{IL}. The DISABLE input has no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low).

2.7. Programmable Dead Time and Overlap Protection

All high-side/low-side drivers (Si8230/1/3/4) include programmable overlap protection to prevent outputs VOA and VOB from being high at the same time. These devices also include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB. Programmable dead time control sets the amount of time between one output going low and the other output going high. When enabled, dead time is present on all transitions, even after overlap recovery. The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per Equation 1. Note that the dead time pin can be tied to VDDI or left floating to provide a nominal dead time at approximately 400 ps. To aid in noise immunity, place a 0.1 µF ceramic capacitor in parallel with RDT. The capacitor should be placed as close to the DT pin as possible.

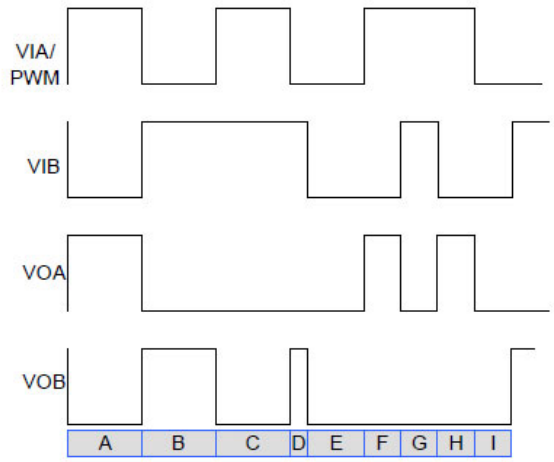
$$DT \approx 10 \times R_{DT}$$ where:

DT = dead time (ns) and

R_{DT} = dead time programming resistor (kΩ)

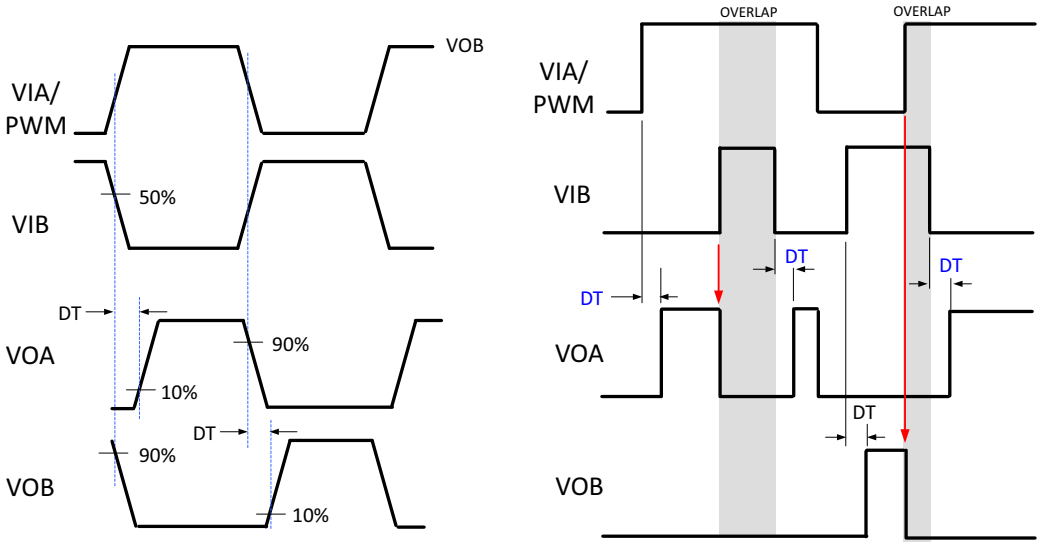
Equation 1.

The device driving VIA and VIB should provide a minimum dead time of TDD to avoid activating overlap protection. Input/output timing waveforms for the two-input drivers are shown in Figure 31. "Input/Output Waveforms for High-Side/Low-Side Two-Input Drivers", and dead time waveforms are shown in Figure 32. "Dead Time Waveforms for High-Side/Low-Side Two-Input Drivers".



Ref	Description
A	Normal operation: VIA high, VIB low.
B	Normal operation: VIB high, VIA low.
C	Contention: VIA = VIB = high.
D	Recovery from contention: VIA transitions low.
E	Normal operation: VIA = VIB = low.
F	Normal operation: VIA high, VIB low.
G	Contention: VIA = VIB = high.
H	Recovery from contention: VIB transitions low.
I	Normal operation: VIB transitions high.

Figure 31. Input/Output Waveforms for High-Side/Low-Side Two-Input Drivers



A. Typical Dead Time Operation B. Dead Time Operation During Overlap

Figure 32. Dead Time Waveforms for High-Side/Low-Side Two-Input Drivers

3. Application Information

The device is designed to be both flexible and robust to meet a wide range of application requirements, safely survive overloads, and rapidly recover normal operation. To achieve these objectives, the appropriate configuration must be selected and its circuit carefully designed.

3.1. Recommended Application Circuits

The following examples illustrate typical circuit configurations using the Si823x.

3.1.1. High-Side/Low-Side Driver

The Figure A in the drawing below shows the Si8230/3 controlled using the VIA and VIB input signals, and Figure B shows the Si8231/4 controlled by a single PWM signal.

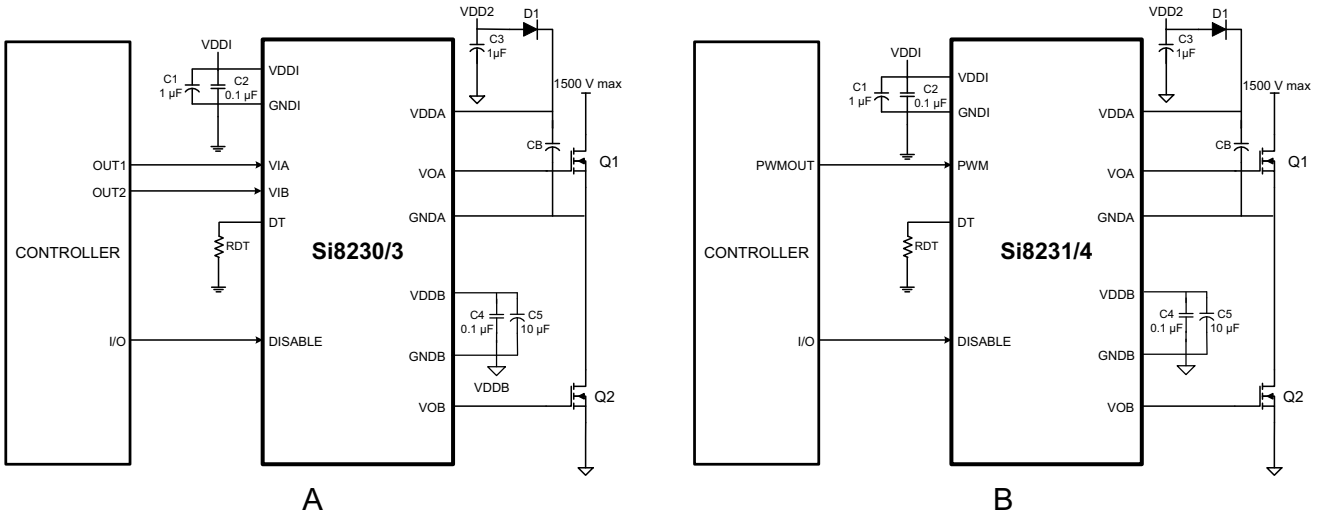


Figure 33. Si823x in Half-Bridge Application

For both cases, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. The boot-strap start up time will depend on the CB cap chosen. See "AN486: High-Side Bootstrap Design Using Si823x ISODrivers in Power Delivery Systems". VOB is connected as a conventional low-side driver, and, in most cases, VDD2 is the same as VDDB.
Note that the input side of the Si823x requires VDD in the range of 4.5 to 5.5 V (2.7 to 5.5 V for Si8237/8), while the VDDA and VDDB output side supplies must be between 6.5 and 24 V with respect to their respective grounds. It is recommended that bypass capacitors of 0.1 and 1 µF value be used on the Si823x input side and that they be located as close to the chip as possible. Moreover, it is recommended that 0.1 and 10 µF bypass capacitors, located as close to the chip as possible, be used on the Si823x output side to reduce high-frequency noise and maximize performance.

3.1.2. Dual Driver

Figure 34 shows the Si823x configured as a dual driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 1500 V dc between them.

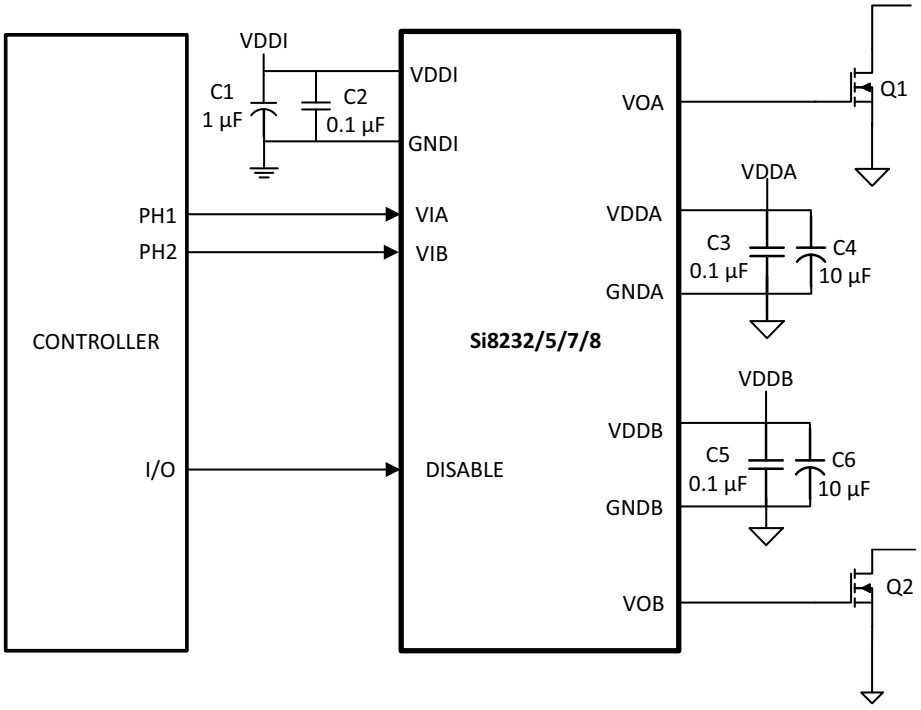


Figure 34. Si8232/5/7/8 in a Dual Driver Application

Because each output driver resides on its own die, the relative voltage polarities of VOA and VOB can reverse without damaging the driver. That is, the voltage at VOA can be higher or lower than that of VOB by VDD without damaging the driver. Therefore, a dual driver in a low-side high side/low side drive application can use either VOA or VOB as the high side driver. Similarly, a dual driver can operate as a dual low-side or dual high-side driver and is unaffected by static or dynamic voltage polarity changes.

3.2. Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDB. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the Si823x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it.
Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

3.3. Layout Considerations

The layout considerations are divided into general considerations for the entire device, the logic input side of the device, and the gate driver side. Please refer to "3.1. Recommended Application Circuits" on page 19 for specific parts referenced.

3.3.1. General Considerations

- The bypass capacitors (usually 0.1 µF || 10 µF) should be placed close to the device's power supply pins and connected to the device with thick and short traces.
- The isolation barrier should have the required distance for the traces, power planes, ground planes, and copper areas on the device's logic input and gate drive sides.
- Safety isolation between gate drivers A and B on the gate driver side is usually not required. If the system needs safety isolation between gate drivers A and B, the trace, power plane, ground plane, and the copper area between the two gate drivers should have the required distance. Even though safety isolation between gate drivers A and B is usually not required, to avoid arcing through the air, the traces operating at high voltage should have some distance (approximately 1 mm per 1 kV) from the low voltage signals.
- The Si823x device is often used in high-power systems with significant switching current and transient voltage. Attention should be paid to the proximity and orientation of the Si823x device and any high-current switching circuits. This should also apply to the traces and components surrounding the Si823x device to avoid unwanted noise coupling.

3.3.2. Logic Input Considerations

- Place resistor R_{DT} close to the device's dead time (DT) pin.
- If the application requires extremely high common mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no connect (NC) pins. This will help improve the CMTI performance.
- Using ≥6 mil trace width on all logic input pins is recommended. The interconnection between the controller and the device should be kept from any noisy signals in the system.

3.3.3. Gate Driver Considerations

- It is recommended to use ≥20 mil trace width for the VOA/B gate driver traces and their return path.
- For a multiple-layer PCB design, ground and power planes are recommended to create a power supply current path with the least inductance. If there is no dedicated power or ground plane on the gate driver side, please use ≥20 mil trace width for the power supply connections.
- If the design utilizes Y2 capacitors between the logic input and gate drivers, the Y2 capacitors across the isolation barrier should be placed as close as possible to the sides of the device without pins.

3.4. Power Dissipation Considerations

The device's average power dissipation is often required in order to estimate the silicon junction temperature and can be estimated using the equation provided in "AN1339: Driver Power Dissipation Considerations". To solve the equation, the intended supply voltages, the load characteristics, the gate resistor values, and the switching frequency need to be collected. Skyworks provides a Microsoft Excel® based calculator as part of "AN1339: Si82xx ISOdriver Power Dissipation Considerations" to easily estimate the device's power dissipation and silicon junction temperature.

4. Electrical Specifications

Table 6. Electrical Characteristics[1]

2.7 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V, T_A = –40 to +125 °C, Typical specs at 25 °C, T_J = –40 to +150 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Specifications						
Input-side power supply voltage	VDDI	Si8230/1/2/3/4/5 Si8237/8	4.5 2.7	— —	5.5 5.5	V
Driver supply voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB (see 1. "Ordering Guide")	6.5	—	24	V
Input supply quiescent current	IDDI(Q)	Si8230/2/3/5/7/8	—	2	3	mA
		Si8231/4	—	3.5	5	mA
Output supply quiescent current	IDDA(Q), IDDB(Q)	Current per channel	—	—	3.0	mA
Input supply active current	IDDI	Input freq = 500 kHz, no load	—	3.5	—	mA
Output supply active current	IDDA IDDB	Current per channel with Input freq = 500 kHz, no load	—	6	—	mA
Input pin leakage current	IVIA, IVIB, IPWM		–10	—	+10	µA dc
Input pin leakage current (Si8230/1/2/3/4/5)	IDISABLE		–10	—	+10	µA dc
Input pin leakage current (Si8237/8)			–1000	—	+1000	
Logic high input threshold	VIH		2.0	—	—	V
Logic low input threshold	VIL		—	—	0.8	V
Input hysteresis	VI_{HYST}	Si8230/1/2/3/4/5/7/8	400	450	—	mV
Logic high output voltage	VOAH, VOBH	IOA, IOB = –1 mA	(VDDA/VDDB) – 0.04	—	—	V
Logic low output voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output short-circuit pulsed sink current	IOA(SCL), IOB(SCL)	Si8230/1/2/7 (see Figure 35)	—	0.5	—	A
		Si8233/4/5/8 (see Figure 35)	—	4.0	—	A
Output short-circuit pulsed source current	IOA(SCH), IOB(SCH)	Si8230/1/2/7 (see Figure 36)	—	0.25	—	A
		Si8233/4/5/8 (see Figure 36)	—	2.0	—	A
Output sink resistance	$R_{ON(SINK)}$	Si8230/1/2/7	—	5.0	—	Ω
		Si8233/4/5/8	—	1.0	—	Ω
Output source resistance	$R_{ON(SOURCE)}$	Si8230/1/2/7	—	15	—	Ω
		Si8233/4/5/8	—	2.7	—	Ω
VDDI undervoltage threshold	$VDDI_{UV+}$	VDDI rising (Si8230/1/2/3/4/5)	3.60	4.0	4.45	V
VDDI undervoltage threshold	$VDDI_{UV–}$	VDDI falling (Si8230/1/2/3/4/5)	3.30	3.70	4.15	V
VDDI lockout hysteresis	$VDDI_{HYS}$	(Si8230/1/2/3/4/5)	—	250	—	mV
VDDI undervoltage threshold	$VDDI_{UV+}$	VDDI rising (Si8237/8)	2.15	2.3	2.5	V
VDDI undervoltage threshold	$VDDI_{UV–}$	VDDI falling (Si8237/8)	2.10	2.22	2.40	V
VDDI lockout hysteresis	$VDDI_{HYS}$	(Si8237/8)	—	75	—	mV

Table 6. Electrical Characteristics[1] (Continued)

2.7 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V, T_A = –40 to +125 °C, Typical specs at 25 °C, T_J = –40 to +150 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDDA, VDDB undervoltage threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA, VDDB rising				
5 V threshold			5.20	5.80	6.30	V
8 V threshold			7.50	8.60	9.40	V
10 V threshold			9.60	11.1	12.2	V
12.5 V threshold			12.4	13.8	14.8	V
VDDA, VDDB undervoltage threshold	$VDDA_{UV–}$, $VDDB_{UV–}$	VDDA, VDDB falling				
5 V threshold			4.90	5.52	6.0	V
8 V threshold			7.20	8.10	8.70	V
10 V threshold			9.40	10.1	10.9	V
12.5 V threshold			11.6	12.8	13.8	V
VDDA, VDDB lockout hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 5 V	—	280	—	mV
VDDA, VDDB lockout hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 8 V	—	600	—	mV
VDDA, VDDB lockout hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 10 V or 12.5 V	—	1000	—	mV
AC Specifications						
Minimum pulse width			—	10	—	ns
Propagation delay	t_{PHL}, t_{PLH}	CL = 200 pF	—	30	45	ns
Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD		—	—	5.60	ns
Minimum overlap time[2]	TDD	DT = VDDI, No-Connect	—	0.4	—	ns
Programmed dead time[3]	DT	RDT = 100 k (see Figure 32)	730	900	1170	ns
		RDT = 6 k (see Figure 32)	55	70	75	ns
Output rise and fall time	t_R,t_F	C_L = 200 pF (Si8230/1/2/7)	—	—	20	ns
		C_L = 200 pF (Si8233/4/5/8)	—	—	12	ns
Shutdown time from disable true	t_{SD}		—	—	60	ns
Restart time from disable false	$t_{RESTART}$		—	—	60	ns
Device start-up time	t_{START}	Time from VDD_ = VDD_UV+ to VOA, VOB = VIA, VIB	—	—	40	µs
Common mode transient immunity	CMTI	VIA, VIB, PWM = VDDI or 0 V, V_{CM} = 1500 V (see Figure 37)	20	45	—	kV/µs

1. VDDA = VDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 kΩ.

4.1. Test Circuits

Figure 35, Figure 36, and Figure 37 depict sink current, source current, and common-mode transient immunity test circuits, respectively.

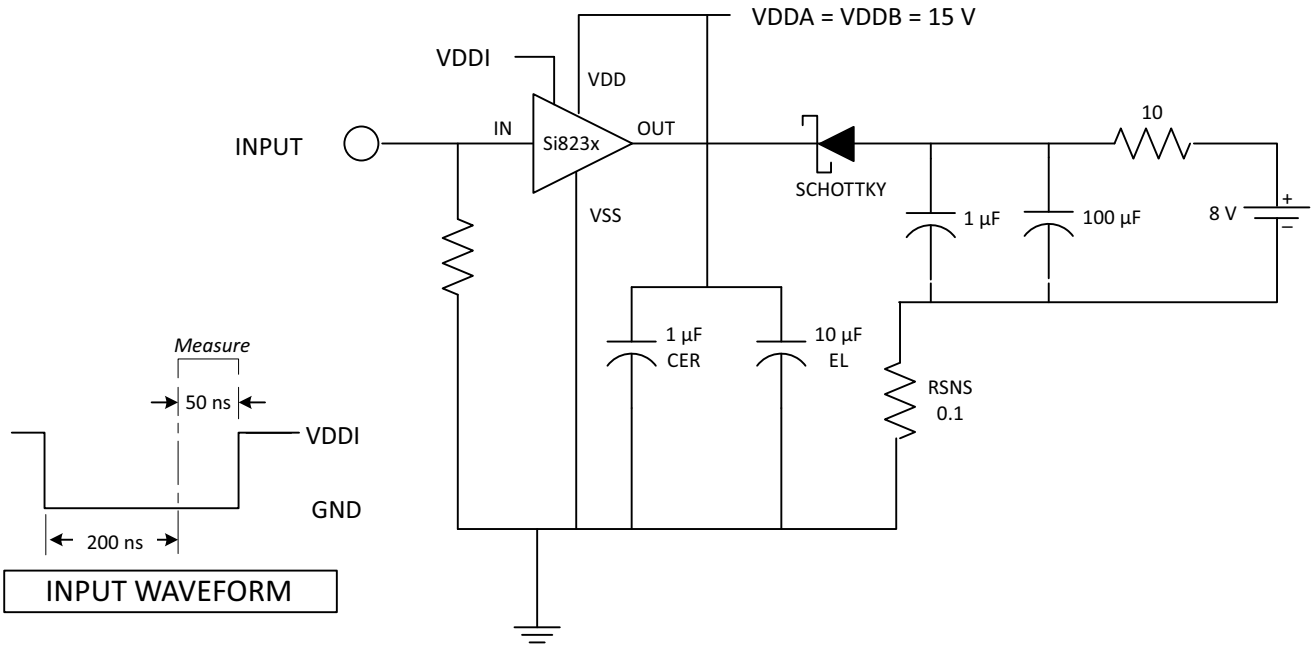


Figure 35. IOL Sink Current Test Circuit

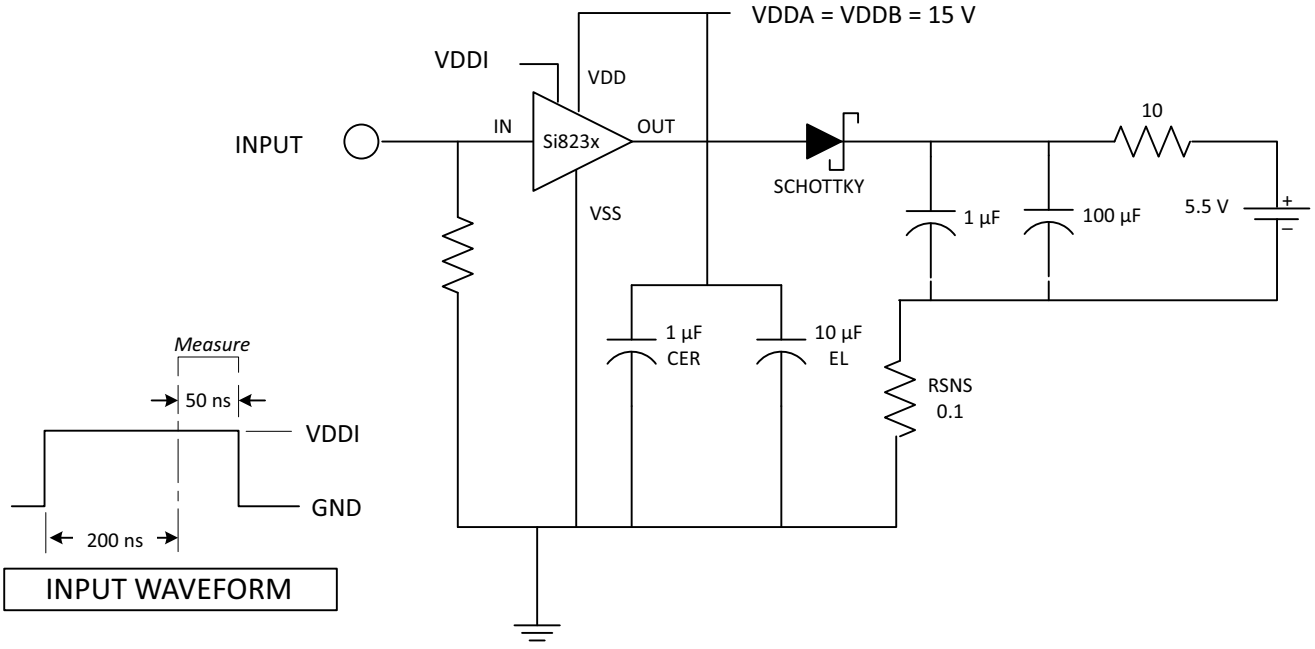


Figure 36. IOH Source Current Test Circuit

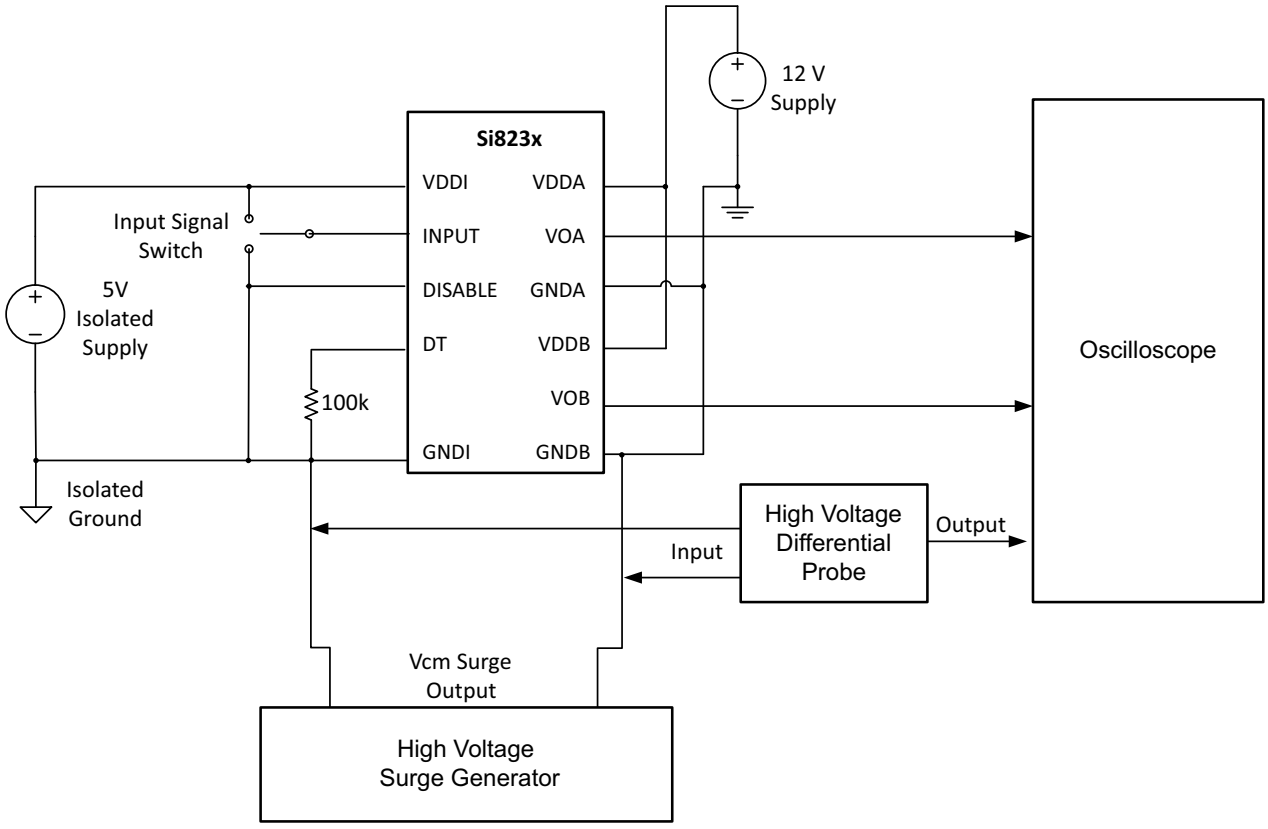


Figure 37. Common Mode Transient Immunity Test Circuit

4.2. Safety Certifications and Specifications

Table 7. Regulatory Information[1]

CSA
The Si823x is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Rated up to 600 V_{RMS} reinforced insulation working voltage; rated up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Rated up to 250 V_{RMS} working voltage and two means of patient protection (MOPP).
VDE
The Si823x is certified under VDE. For more details, see File 5028467.
60747-17: Rated up to 891 V_{PEAK} for basic insulation working voltage.
UL
The Si823x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5.0 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si823x is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see 1. "Ordering Guide".

Table 8. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			WBSOIC-14/16	NBSOIC-16	LGA-14	
Nominal external air gap (clearance)	CLR		8.0/7.6	3.9	3.5	mm
Nominal external tracking (creepage)	CRP		8.0/7.6	3.9	3.5	mm
Minimum internal gap (internal clearance)	DTI		0.014	0.014	0.014	mm
Tracking resistance	CTI or PTI	IEC60112	600	600	600	V_{RMS}
Erosion depth	ED		0.019/0.122	0.122	0.021	mm
Resistance (input-output)[1]	R_{IO}	Test voltage = 500 V, 25 °C	10^{12}	10^{12}	10^{12}	Ω
Capacitance (input-output)[1]	C_{IO}	f = 1 MHz	1.4	1.4	1.4	pF
Input capacitance[2]	C_I	f = 100 kHz	4.0	4.0	4.0	pF

1. To determine resistance and capacitance, the device is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal, and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input to ground.

Table 9. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification		
		WB SOIC-14/16	NB SOIC-16	LGA-14
Material Group		I	I	I
Overvoltage category	Rated mains voltages ≤ 100 V_{RMS}	I-IV	I-IV	I-IV
	Rated mains voltages ≤ 150 V_{RMS}	I-III	I-III	I-III
	Rated mains voltages ≤ 300 V_{RMS}	I-II	I-II	I-II
	Rated mains voltages ≤ 600 V_{RMS}	I	I	I

Table 10. IEC60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-14/16	NB SOIC-16/ LGA-14	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	630	396	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	891	560	V_{PEAK}
Apparent charge	Q_{PD}	Method b: At routine test (100% production) and preconditioning (type test); V_{INI} = 1.2 x V_{IOTM}, t_{INI} = 1 s; $V_{PD(M)}$ = 1.5 x V_{IORM}, t_M = 1 s (method b1) or $V_{PD(M)}$ = V_{INI}, t_M = t_{INI} (method b2)	≤ 5	≤ 5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	6000	4000/3535	V_{PEAK}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile (qualification)	4000	4000	V_{PEAK}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile (qualification)	3077	3077	V_{PEAK}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “basic electrical insulation” only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 11. IEC60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max			Unit
			WB SOIC-14/16	NB SOIC-16	LGA-14	
Safety Temperature	T_S		150	150	150	°C
Safety Input, Output, or Supply Current	I_S	Refer to θ_{JA} in Table 13 on page 28. V_{DDI} = 5.5 V, V_{DDA} = V_{DDB} = 24 V, T_J = 150 °C, T_A = 25 °C.	50	50	50	mA
Safety Input, Output, or Total Power	P_S		1.2	1.2	1.2	W

1. Maximum value allowed in the event of a failure. Refer to Figure 38 for the thermal derating curve.

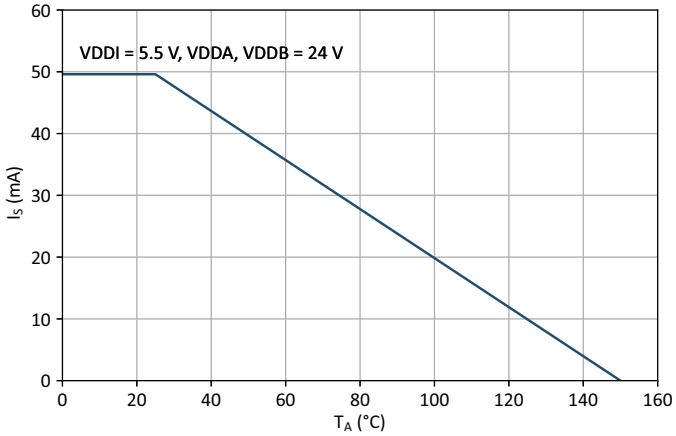


Figure 38. WB SOIC, NB SOIC, LGA-14 Safety Current vs. Ambient Temperature Derating Curve

Table 12. UL1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic			Unit
			WB SOIC-14/16	NB SOIC-16	LGA-14	
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	5000	3750	2500	V_{RMS}

Table 13. Thermal Characteristics

Parameter	Symbol	WB SOIC-14/16	NB SOIC-16	LGA-14	Unit
IC Junction-to-air thermal resistance	θ_{JA}	100	105	105	°C/W

Table 14. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage temperature[2]	T_{STG}	–65	+150	°C
Operating temperature	T_A	–40	+125	°C
Junction temperature	T_J	—	+150	°C
Logic input supply voltage	VDDI	–0.6	6.0	V
Gate driver supply voltage	VDDA, VDDB	–0.6	30	V
Voltage on any pin with respect to ground	V_{IO}	–0.5	V_{DD} + 0.5	V
Output voltage to GND, repeat spike of –2 V for 200 ns, 200 kHz	VOA to GNDA, VOB to GNDB	–2	$V_{DDA/B}$ + 0.5	V
Lead solder temperature (10 s)		—	260	°C

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VDE certifies storage temperature from –40 to 150 °C.

5. Pin Descriptions

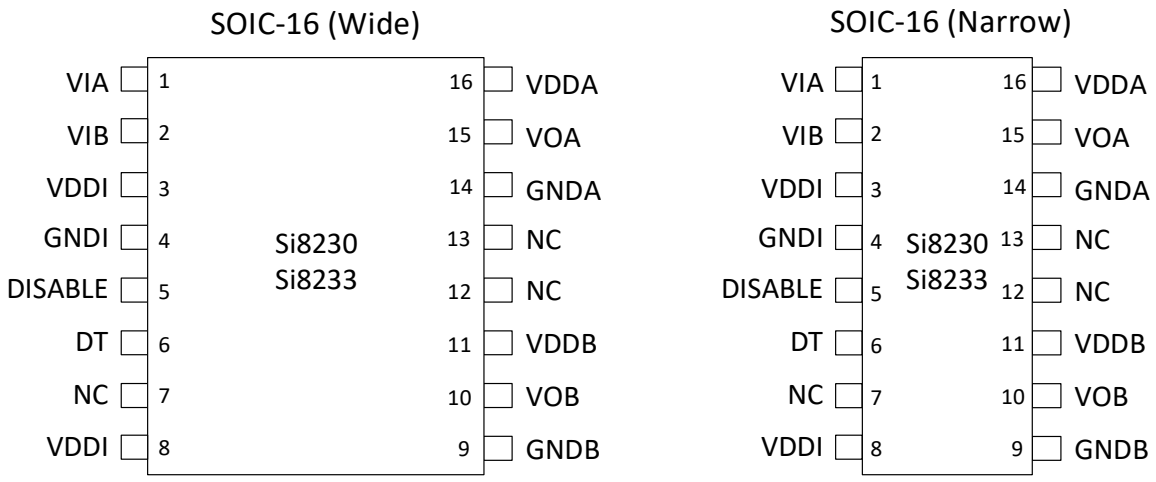


Figure 39. Si8230/3 SOIC-16 Wide and Narrow Pinouts

Table 15. Si8230/3 Two-Input HS/LS Isolated Driver (SOIC-16).
WB SOIC-14 with IS3 Package Designation (has Pins 12 and 13 missing).

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 2.7. "Programmable Dead Time and Overlap Protection"). If improved noise immunity is desired, a 10 nF capacitor may be added in parallel to the dead time programming resistor (RDT).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

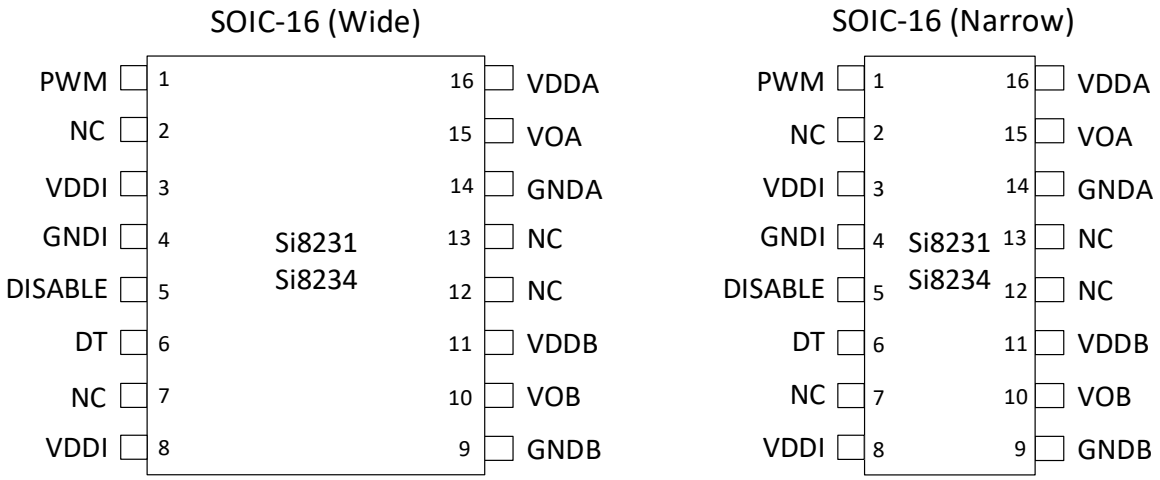


Figure 40. Si8231/4 SOIC-16 Wide and Narrow Pinouts

Table 16. Si8231/4 PWM Input HS/LS Isolated Driver (SOIC-16).
WB SOIC-14 with IS3 Package Designation (has Pins 12 and 13 missing).

Pin	Name	Description
1	PWM	PWM input.
2	NC	No connection.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 2.7. "Programmable Dead Time and Overlap Protection"). If improved noise immunity is desired, a 10 nF capacitor may be added in parallel to the dead time programming resistor (RDT).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

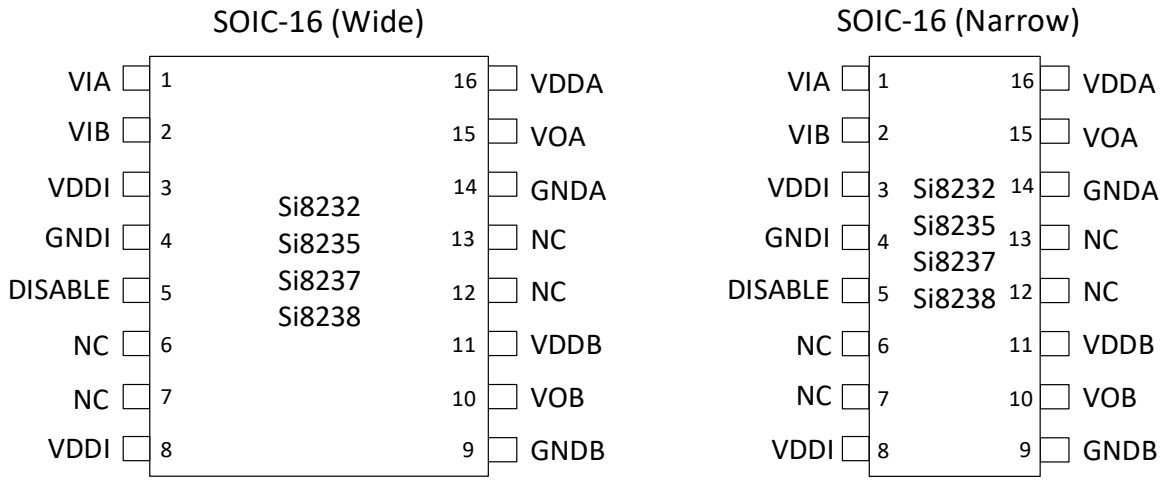


Figure 41. Si8232/5/7/8 SOIC-16 Wide and Narrow Pinouts

Table 17. Si8232/5/7/8 Dual Isolated Driver (SOIC-16).
WB SOIC-14 with IS3 Package Designation (has Pins 12 and 13 missing).

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V, (2.7 to 5.5 V for Si8237/8).
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	NC	No connection.
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V, (2.7 to 5.5 V for Si8237/8).
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output.
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output.
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

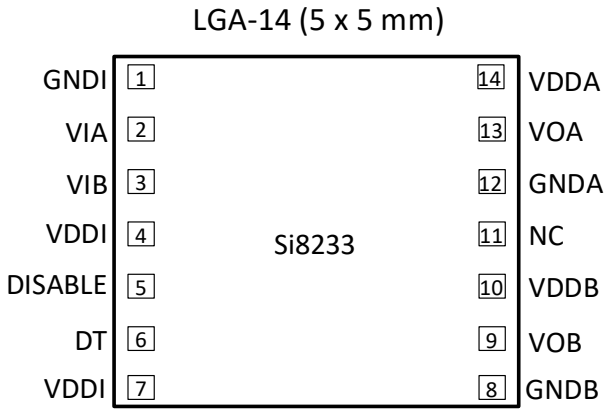


Figure 42. Si8233 LGA-14 (5x5 mm) Pinout

Table 18. Si8233 Two-Input HS/LS Isolated Driver (LGA-14)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
VIA	2	Non-inverting logic input terminal for Driver A.
VIB	3	Non-inverting logic input terminal for Driver B.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	6	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 2.7. "Programmable Dead Time and Overlap Protection"). If improved noise immunity is desired, a 10 nF capacitor may be added in parallel to the dead time programming resistor (RDT).
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

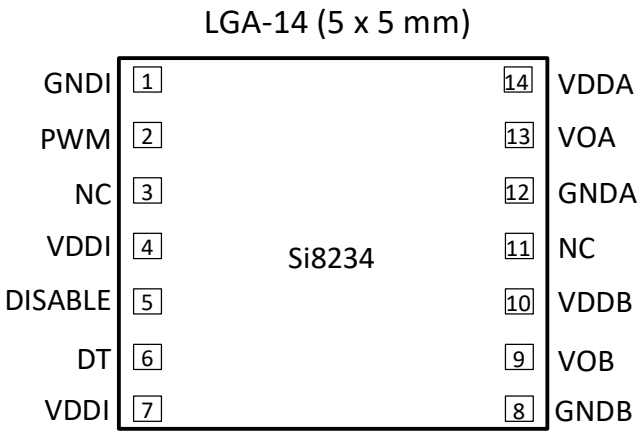


Figure 43. Si8234 LGA-14 (5x5 mm) Pinout

Table 19. Si8234 PWM Input HS/LS Isolated Driver (LGA-14)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
PWM	2	PWM input.
NC	3	No connection.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	6	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 2.7. "Programmable Dead Time and Overlap Protection"). If improved noise immunity is desired, a 10 nF capacitor may be added in parallel to the dead time programming resistor (RDT).
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

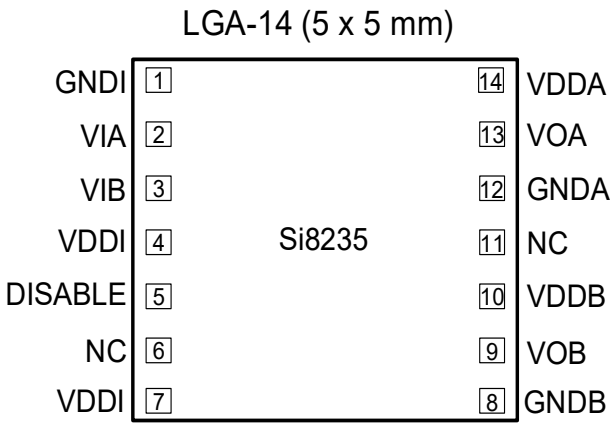


Figure 44. Si8235 LGA-14 (5x5 mm) Pinout

Table 20. Si8235 Dual Isolated Driver (LGA-14)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
VIA	2	Non-inverting logic input terminal for Driver A.
VIB	3	Non-inverting logic input terminal for Driver B.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
NC	6	No connection.
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

6. Package Outlines

6.1. Package Outline: 16-Pin Wide Body SOIC

Figure 45 illustrates the package details for the Si823x in a 16-Pin Wide Body SOIC. Table 21 lists the values for the dimensions shown in the illustration.

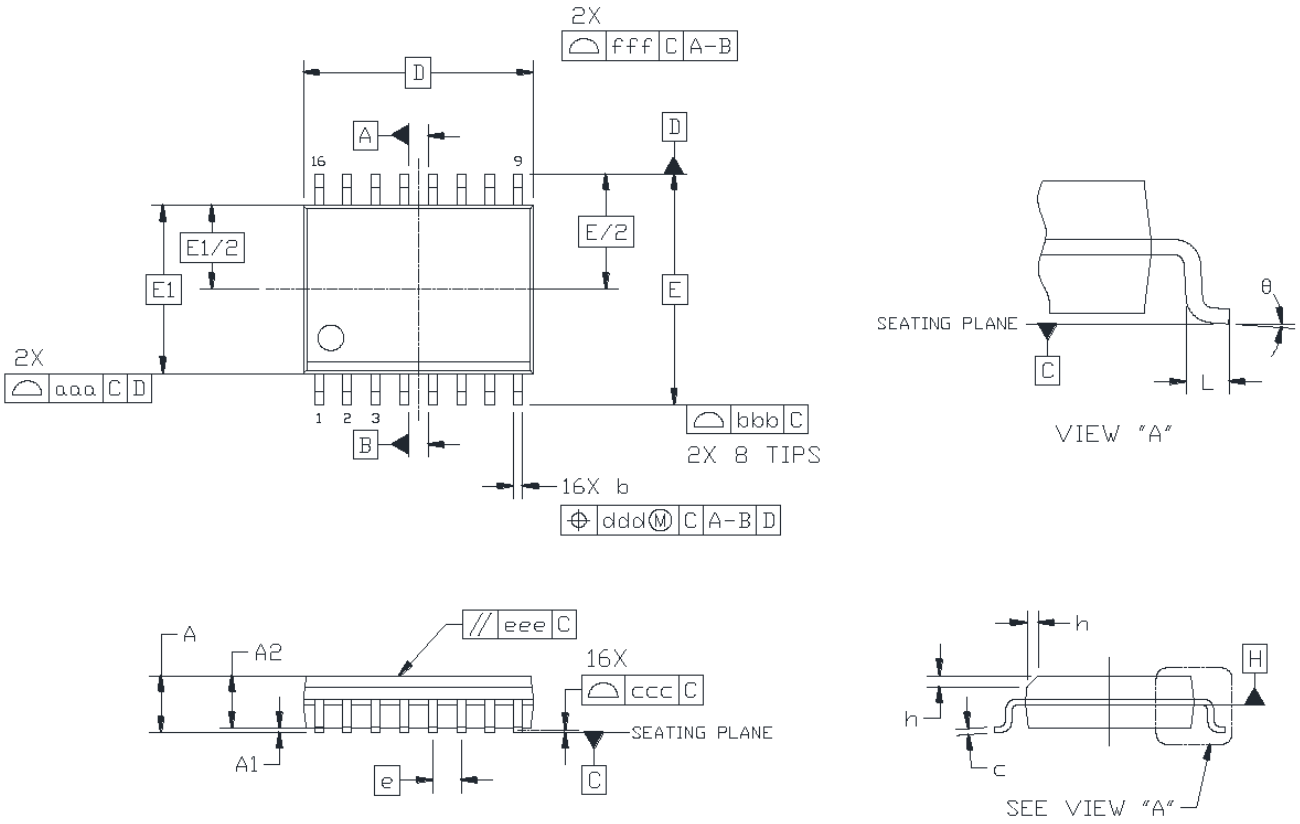


Figure 45. 16-Pin Wide Body SOIC

Table 21. Package Diagram Dimensions[1,2,3,4]

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
ααα	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

6.2. Package Outline: 14-Pin Wide Body SOIC

Figure 46 illustrates the package details for the Si823x in a 14-Pin Wide Body SOIC. Table 22 lists the values for the dimensions shown in the illustration.

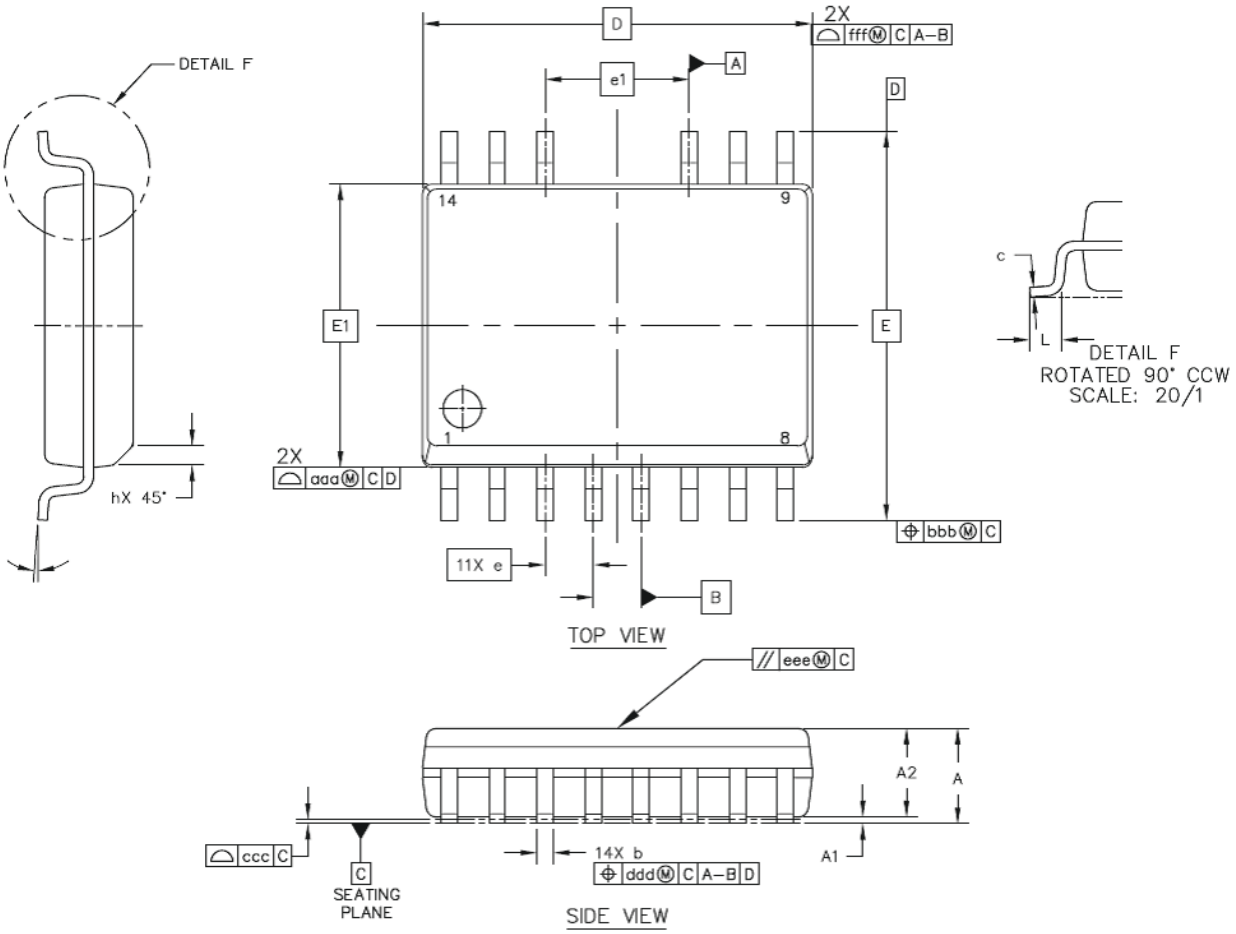


Figure 46. Si823x 14-Pin WB SOIC Outline

Table 22. Si823x 14-pin WB SOIC Outline Package Diagram Dimensions[1,2,3,4]

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
Θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

6.3. Package Outline: 16-Pin Narrow Body SOIC

Figure 47 illustrates the package details for the Si823x in a 16-pin narrow-body SOIC. Table 23 lists the values for the dimensions shown in the illustration.

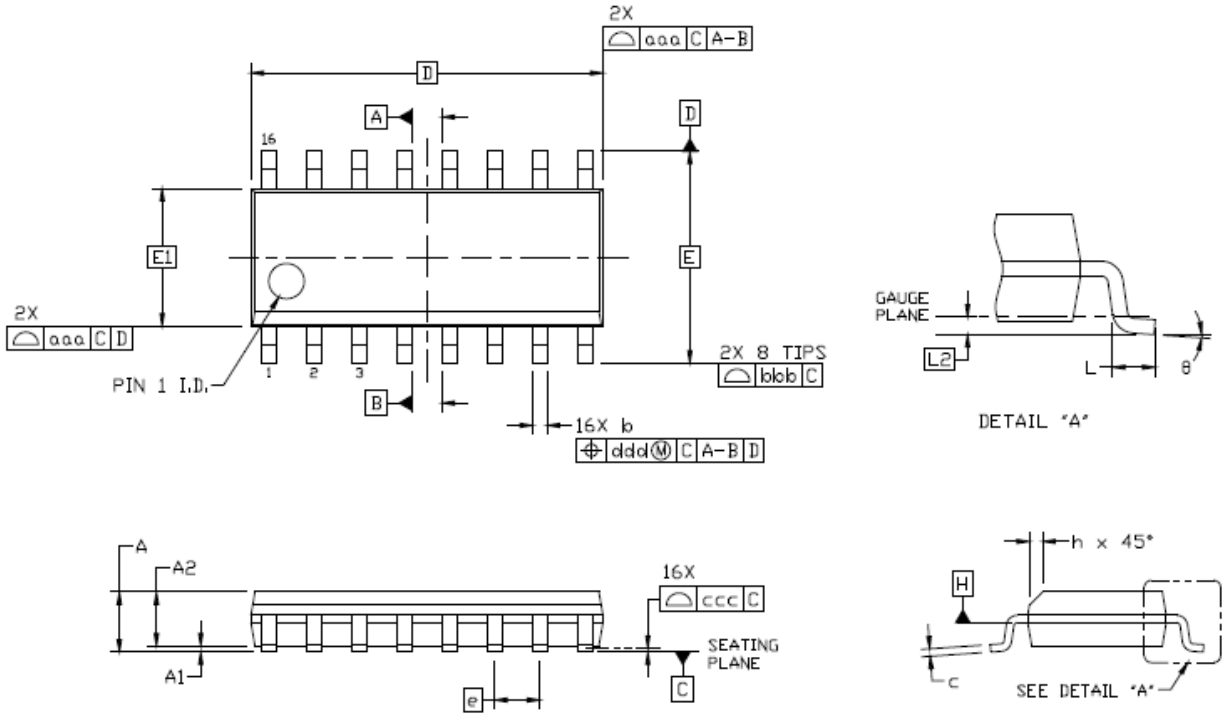


Figure 47. 16-Pin Small Outline Integrated Circuit (SOIC) Package

Table 23. 16-Pin Small Outline Integrated Circuit (SOIC) Package Diagram Dimensions[1,2,3,4]

Dimension	Min	Max		Dimension	Min	Max
A	—	1.75		L	0.40	1.27
A1	0.10	0.25		L2	0.25 BSC	
A2	1.25	—		h	0.25	0.50
b	0.31	0.51		θ	0°	8°
c	0.17	0.25		aaa	0.10	
D	9.90 BSC			bbb	0.20	
E	6.00 BSC			ccc	0.10	
E1	3.90 BSC			ddd	0.25	
e	1.27 BSC					

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.4. Package Outline: LGA-14 (5 x 5 mm)

Figure 48 illustrates the package details for the Si823x in an LGA outline. Table 24 lists the values for the dimensions shown in the illustration.

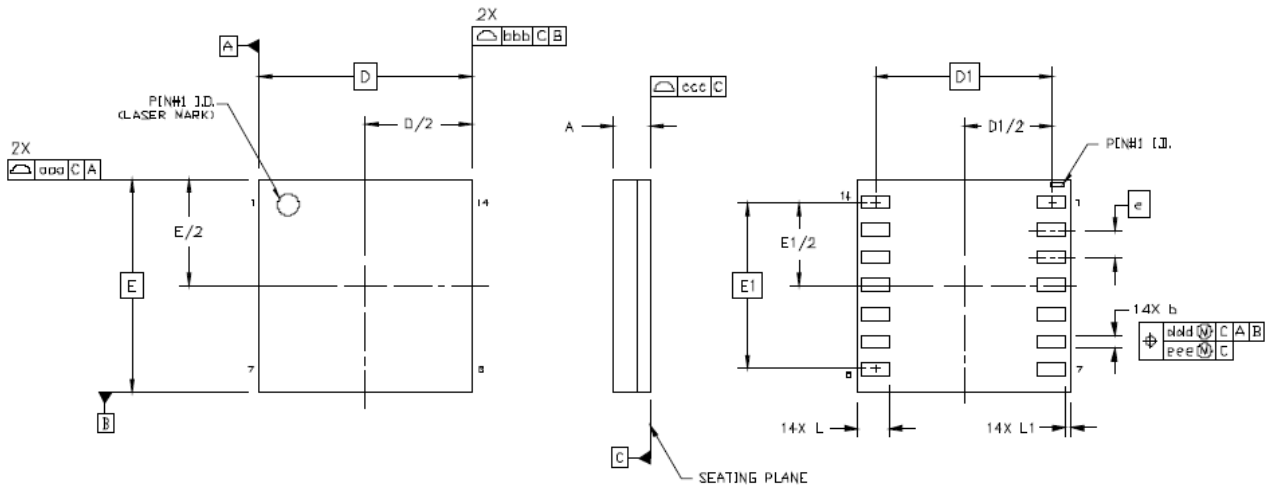


Figure 48. Si823x LGA Outline

Table 24. Package Diagram Dimensions[1,2]

Dimension	Min	Nom	Max
A	0.74	0.84	0.94
b	0.25	0.30	0.35
D		5.00 BSC	
D1		4.15 BSC	
e		0.65 BSC	
E		5.00 BSC	
E1		3.90 BSC	
L	0.70	0.75	0.80
L1	0.05	0.10	0.15
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.15
eee	—	—	0.08

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7. Land Patterns

7.1. Land Pattern: 16-Pin Wide Body SOIC

Figure 49 illustrates the recommended land pattern details for the Si823x in a 16-pin wide-body SOIC. Table 25 lists the values for the dimensions shown in the illustration.

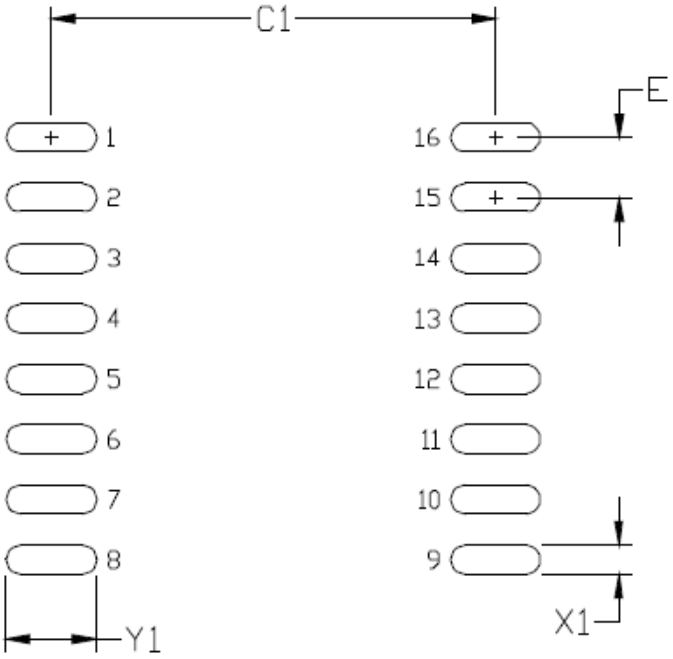


Figure 49. 16-Pin SOIC Land Pattern

Table 25. 16-Pin Wide Body SOIC Land Pattern Dimensions[1,2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.2. Land Pattern: 14-Pin Wide Body SOIC

Figure 50 illustrates the recommended land pattern details for the Si823x in a 14-pin Wide Body SOIC. Table 26 lists the values for the dimensions shown in the illustration.

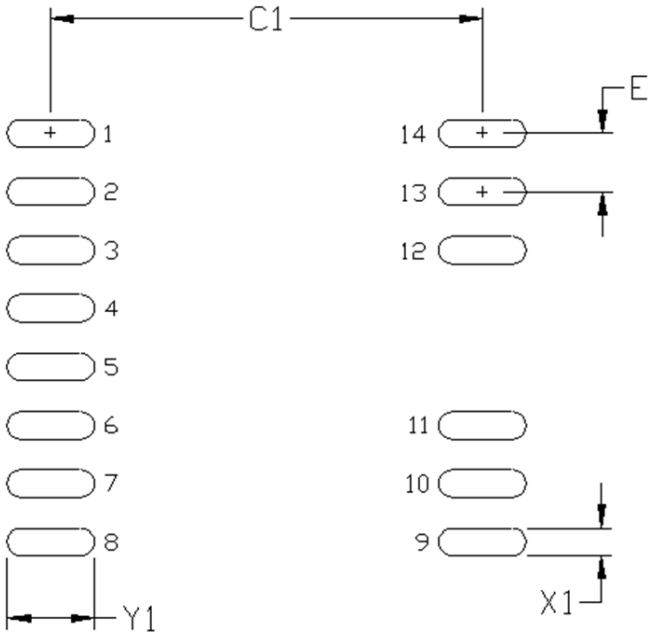


Figure 50. 14-Pin WB SOIC Land Pattern

Table 26. 14-Pin WB SOIC Land Pattern Dimensions[1,2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.70
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.3. Land Pattern: 16-Pin Narrow Body SOIC

Figure 51 illustrates the recommended land pattern details for the Si823x in a 16-pin narrow-body SOIC. Table 27 lists the values for the dimensions shown in the illustration.

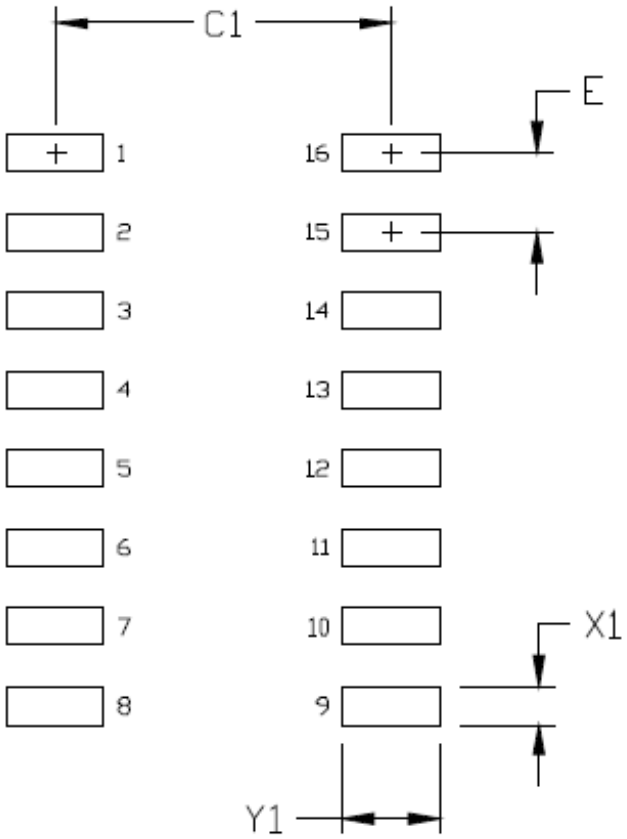


Figure 51. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 27. 16-Pin Narrow Body SOIC Land Pattern Dimensions[1,2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.4. Land Pattern: LGA-14

Figure 52 illustrates the recommended land pattern details for the Si823x in a 14-pin LGA. Table 28 lists the values for the dimensions shown in the illustration.

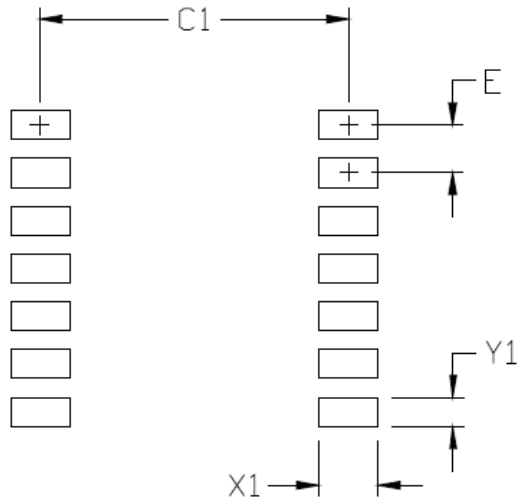


Figure 52. 14-Pin LGA Land Pattern

Table 28. 14-Pin LGA Land Pattern Dimensions

Dimension	(mm)
C1	4.20
E	0.65
X1	0.80
Y1	0.40

General:

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Markings

8.1. Si823x Top Marking (14/16-Pin Wide Body SOIC)

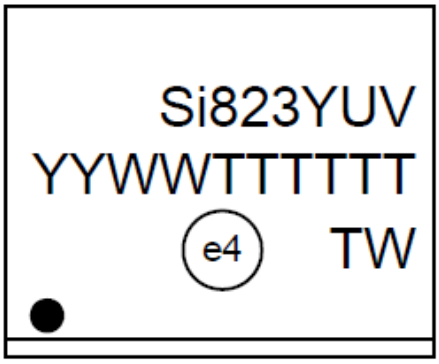


Figure 53. Si823x Top Marking (14/16-Pin Wide Body SOIC)

Table 29. Si823x Top Marking Explanation (14/16-Pin Wide Body SOIC)

Line 1 Marking:	Base part number ordering options. (See 1. "Ordering Guide" for more information)	Si823 = ISOdriver product series Y = Peak output current 0, 1, 2, 7 = 0.5 A 3, 4, 5, 8 = 4.0 A U = UVLO level A = 5 V; B = 8 V; C = 10 V; D = 12.5 V V = Isolation rating B = 2.5 kV; C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.5 mm diameter (Center Justified)	“e4” Pb-free symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan (as shown), TH = Thailand

8.2. Si823x Top Marking (16-Pin Narrow Body SOIC)

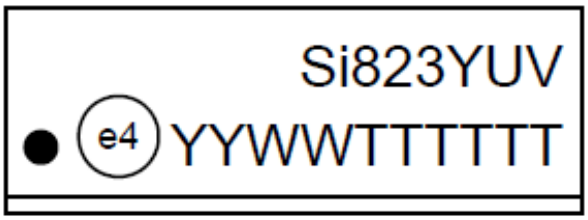


Figure 54. Si823x Top Marking (16-Pin Narrow Body SOIC)

Table 30. Si823x Top Marking Explanation (14/16-Pin Wide Body SOIC)

Line 1 Marking:	Base part number ordering options. (See 1. "Ordering Guide" for more information)	Si823 = ISOdriver product series Y = Peak output current 0, 1, 2, 7 = 0.5 A 3, 4, 5, 8 = 4.0 A U = UVLO level A = 5 V; B = 8 V; C = 10 V; D = 12.5 V V = Isolation rating A = 1.0 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.

8.3. Si823x Top Marking (LGA-14)

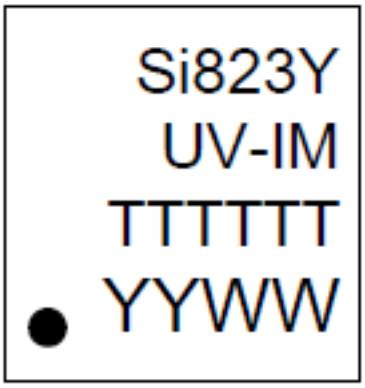


Figure 55. Si823x Top Marking (LGA-14)

Table 31. Si823x Top Marking Explanation (14/16-Pin Wide Body SOIC)

Line 1 Marking:	Base part number ordering options. (See 1. "Ordering Guide" for more information)	Si823 = ISOdriver product series Y = Peak output current 0, 1, 2 = 0.5 A 3, 4, 5 = 4.0 A
Line 2 Marking:	Ordering options	U = UVLO level A = 5 V; B = 8 V; C = 10 V; D = 12.5 V V = Isolation rating A = 1.0 kV; B = 2.5 kV; C = 3.75 kV I = –40 to +125 °C ambient temperature range M = LGA package type
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code from Assembly.
Line 4 Marking:	Circle = 1.5 mm diameter	Pin 1 identifier
	YYWW	Manufacturing date code

9. Revision History

Revision	Date	Description
B	December, 2024	• Updated Key Features on front page. - Removed QFN. • Updated Table 1. Si823x Ordering Guide" on page 2. - Removed QFN package options. • Updated "Table 8. Insulation and Safety-Related Specifications" on page 26. - Removed QFN. • Updated "Table 9. IEC 60664-1 Ratings" on page 27. - Removed QFN. • Updated "Table 10. IEC60747-17 Insulation Characteristics" on page 27. - Removed QFN. • Updated "Table 12. UL1577 Insulation Characteristics" on page 28. - Removed QFN. • Updated "Table 11. IEC60747-17 Safety Limiting Values" on page 28. - Removed QFN. • Updated "Table 13. Thermal Characteristics" on page 28. - Removed QFN. • Updated "Table 14. Absolute Maximum Ratings" on page 29. - Removed QFN. • Updated "Table 17. Si8232/5/7/8 Dual Isolated Driver (SOIC-16). WB SOIC-14 with IS3 Package Designation (has Pins 12 and 13 missing)." on page 32. - Removed QFN. • Updated "Table 18. Si8233 Two-Input HS/LS Isolated Driver (LGA-14)" on page 33. - Removed QFN. • Updated "Table 19. Si8234 PWM Input HS/LS Isolated Driver (LGA-14)" on page 34. - Removed QFN. • Updated "Table 20. Si8235 Dual Isolated Driver (LGA-14)" on page 35. - Removed QFN. • Removed 6.5. Package Outline: 14 LD QFN. • Updated "7.2. Land Pattern: 14-Pin Wide Body SOIC" on page 43. - Removed QFN. • Updated "8.3. Si823x Top Marking (LGA-14)" on page 48. - Removed FN.
A	May 2024	Specifications revised, changed format to comply with new standards.
2.15	September, 2019	• Updated 1. Ordering Guide.
2.14	June, 2019	• Added automotive grade OPN, Si8230BD-AS, to Ordering Guide for Automotive Grade OPNs.
2.13	September, 2018	• Added automotive grade OPNs in Ordering Guide for Automotive Grade OPNs. • Modified power equations in 2.7 Power Dissipation Considerations. • Corrected typo for IDISABLE in Table 3.1 Electrical Characteristics on page 24. • Reformatted Table 3.5 VDE 0884-10 Insulation Characteristics on page 30. • Added Absolute Max rating of –2V/200 ns on output pins in Table 3.8 Absolute Maximum Ratings on page 32. • Updated 7.2 Land Pattern: 14-Pin Wide Body SOIC.
2.12	May, 2018	• Updated the Ordering Guide for Automotive-Grade OPN options.
2.1.1	January, 2018	• Added new table to Ordering Guide for Automotive-Grade OPN options.
2.1	October, 2017	• Added IS3 and IM1 packaging options. • Added IEC 62368-1 references throughout. • Changed max propagation delay spec from 60 ns to 45 ns based on new test limits. • Removed references to IEC 61010. • Removed references to IEC 60747, replaced with references to VDE 0884-10.
1.9	July, 2017	• Updated Ordering Guide to designate tape and reel packaging option.
1.8	May, 2016	• Converted document from Framemaker to DITA.

Revision	Date	Description
1.7	April, 2015	• Updated Table 2 on page 11. - Added CQC certificate numbers. • Updated Table 3 on page 12. - Updated Erosion Depth. • Updated Table 5 on page 13. - Updated V_{PR} for WBSOIC-16. • Updated Table 8 on page 14. - Removed Io and added Peak Output Current specifications. • Updated Equation 1 example on page 23. • Updated Figure 43 on page 30. • Updated Figure 44 on page 31. • Updated Ordering Guide Table 18 on page 39. - Removed Note 2.
1.6	April, 2014	• Updated Table 18, Ordering Part Numbers. - Added Revision D Ordering Part Numbers. - Removed all Ordering Part Numbers of previous revisions.
1.5	March, 2014	• Updated Table 1, input and output supply current. • Added references to AEC-Q100 qualified throughout. • Changed all 60747-5-2 references to 60747-5-5. • Added references to CQC throughout. • Updated pin descriptions throughout. - Corrected dead time default to 400 ps from 1 ns. • Updated Table 18, Ordering Part Numbers. - Removed moisture sensitivity level table notes.
1.4	May, 2013	• Updated “6. Ordering Guide” on page 39. - Updated “3 V VDDI Ordering Options”.
1.3	May, 2013	• Added Si8237/8 throughout. • Updated Table 1. Electrical Characteristics on page 6. • Updated Figure 4. IOL Sink Current Test Circuit on page 9. • Updated Figure 5. IOH Source Current Test Circuit on page 9. • Added Figure 6. Common Mode Transient Immunity Test Circuit on page 10. • Updated Table 10. Si823x Family Truth Table to include Notes 1 and 2. • Updated 3.8. Programmable Dead Time and Overlap Protection on page 28. - Removed references to Figures 26A and 26B. • Updated Table 18. Ordering Part Numbers. - Added Si8235-BA-C-IS1 ordering part number. - Added table note.
1.2	June, 2012	• Updated “6. Ordering Guide” on page 38. - Updated moisture sensitivity level (MSL) for all package types. • Updated Table 8 on page 13. - Added junction temperature spec. • Updated Table 2 on page 10 with new notes. • Updated Figures 18, 19, 20, and 21 to reflect correct y-axis scaling. • Updated Figure 43 on page 30. • Updated 4.3. Dual Driver with Thermally Enhanced Package (Si8236). • Updated 7. Package Outline: 16-Pin Wide Body SOIC on page 41. • Updated Table 19. Package Diagram Dimensions on page 42. • Change references to 1.5 kV_{RMS} rated devices to 1.0 kV_{RMS} throughout. • Updated 3.5. Power Dissipation Considerations on page 22.
1.1	February, 2011	• Updated Features on page 1. - Updated CMTI specification. • Updated Table 1 on page 6. - Updated CMTI specification. • Updated Table 6, IEC 60747-5-2 Insulation Characteristics. • Updated “4.2 Dual Driver”. • Updated 6. Ordering Guide. • Replaced pin descriptions on page 1 with chip graphics.
1.0	August, 2010	• Updated Tables 3, 4, 5, and 6. • Updated 8. Ordering Guide. - Added 5 V UVLO ordering options • Added Device Marking sections.

Revision	Date	Description
0.3	April, 2010	• Moved Sections 2, 3, and 4 to after Section 5. • Updated Tables 15, 16, and 17. - Removed Si8230, Si8231, and Si8232 from pinout and from title. • Updated and added Ordering Guide footnotes. • Updated UVLO specifications in Table 1 on page 6. • Added PWD and Output Supply Active Current specifications in Table 1. • Updated and added typical operating condition graphs in 3. Typical Operating Characteristics (0.5 Amp) and 4. Typical Operating Characteristics (4.0 Amp).
0.2	December, 2009	• Updated all specs to reflect latest silicon revision. • Updated Table 1 on page 12 to include new UVLO options. • Updated Table 2 on page 15 to reflect new maximum package isolation ratings • Added Figures 14, 15, 16, and 17. • Updated Ordering Guide to reflect new package offerings. • Added “6.6.3 Under Voltage Lockout (UVLO)" on page 26 to describe UVLO operation.
0.11	May, 2008	Initial release.