Data Sheet

ACPL-M71T and ACPL-M72T

High-Speed, Low-Power Digital Optocouplers with R²Coupler™ Isolation and AEC-Q100 Grade 1 Qualification

Description

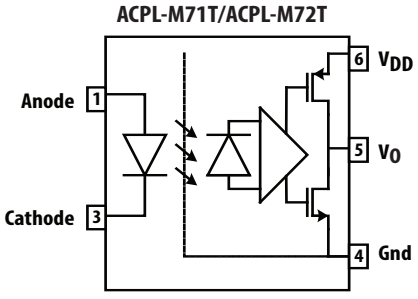
The Broadcom® ACPL-M71T and ACPL-M72T are high-temperature, digital CMOS optocouplers in SO-5 packages. Suitable for hybrid and electric vehicle applications, the optocouplers use the latest CMOS IC technology to achieve outstanding performance and very low-power consumption. All devices are AEC-Q100 compliant and operate over a –40°C to 125°C temperature range.

The ACPL-M71T uses a high-speed LED, and the ACPL-M72T uses a low-current LED for lower power dissipation. The high-speed ACPL-M71T features a 35-ns maximum propagation delay (I_F =10 mA). The ACPL-M72T optocoupler features very low power. With a low 4-mA LED drive current, ACPL-M72T typical propagation delay is 60 ns.

Each digital optocoupler has a CMOS detector IC, an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

Broadcom R²Coupler™ isolation products provide the reinforced insulation and reliability needed for automotive and high-temperature industrial applications.

Functional Block Diagram



Truth Table

LED	Output (V_O)
OFF	H
ON	L

NOTE: A 0.1-µF bypass capacitor must be connected between pins 4 and 6.

Features

- 5V CMOS compatible
- Common-mode rejection 40kV/µs @ V_{CM} = 1000V
- Wide automotive temperature range: –40°C to 125°C
- Low propagation delay:
  - High-speed ACPL-M71T: 26 ns @ I_F = 10 mA (typical)
  - Low-power ACPL-M72T: 60 ns @ I_F = 4 mA (typical)
- Worldwide safety approval:
  - UL 1577 recognized, 4000 V_{RMS} / 1 minute
  - CSA approved
  - IEC/EN/DIN EN 60747-5-5
- Qualified to AEC-Q100 Grade 1 test guidelines

Applications

- Automotive CAN bus communications interface
- Automotive isolated high-speed gate drivers for IGBTs and power MOSFETs
- High-temperature digital signal isolation
- Microcontroller interface
- Digital isolation for A/D and D/A conversion

CAUTION! Take normal static precautions in handling and assembling this component to prevent damage and/or degradation that might be induced by electrostatic discharge (ESD). The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Ordering Information

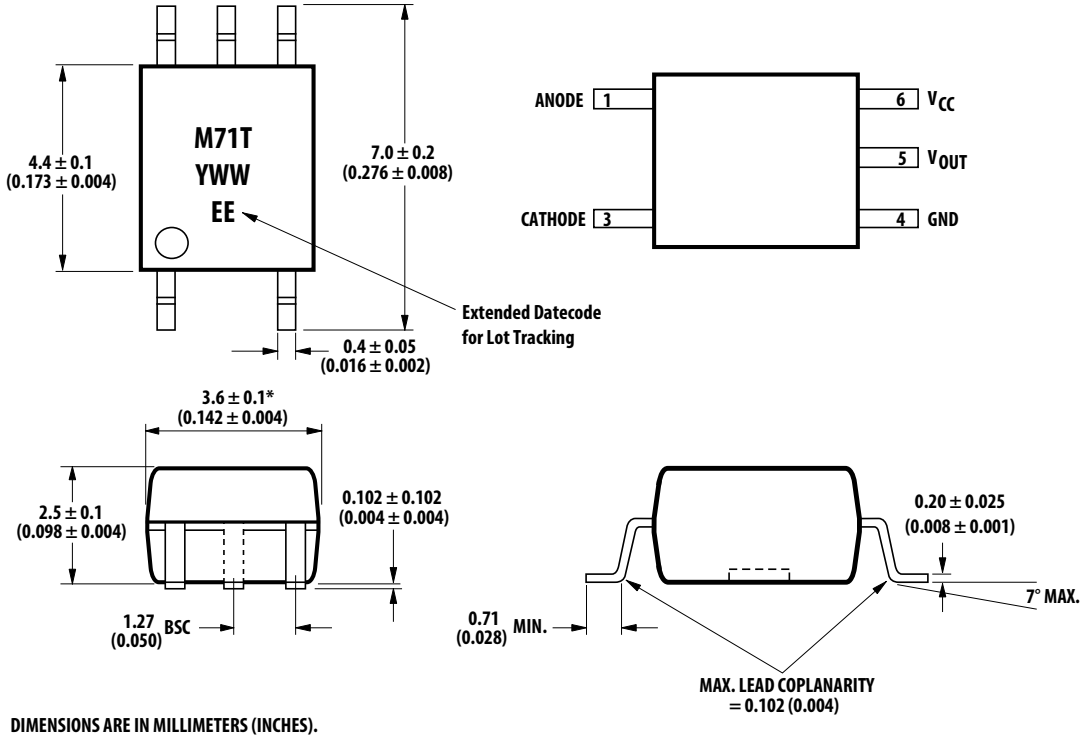
Part Number	Option (RoHS) Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-M71T	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel
ACPL-M72T	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

To form an order entry, choose a part number from the part number column and combine it with the desired option from the option column. For example, the part number ACPL-M71T-500E describes a device with a surface-mount SO-5 package; delivered in tape and reel with 1500 parts per reel; and full RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Dimensions

ACPL-M71T/ACPL-M72T (JEDEC MO-155 Package)

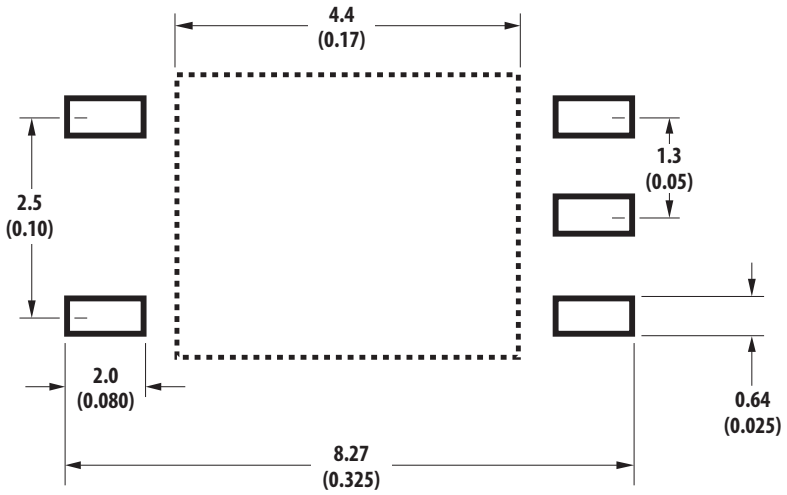


DIMENSIONS ARE IN MILLIMETERS (INCHES).

*** MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 MM (0.006 INCHES).**

NOTE: FLOATING LEAD PROTRUSION IS 0.15 MM (6 MILS) MAX.

Land Pattern Recommendation



DIMENSION IN MILLIMETERS (INCHES)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Non-halide flux should be used.

Regulatory Information

The ACPL-M71T and ACPL-M72T are approved by the following organizations:

UL	Approved under UL 1577, component recognition program up to V_{ISO} = 4000 V_{RMS}.
CSA	Approved under CSA Component Acceptance Notice #5.
IEC/EN/DIN EN 60747-5-5	IEC 60747-5-5: EN 60747-5-5: DIN EN 60747-5-5:

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	>5	mm	Measured from input terminals to output terminals, shortest distance through the air.
Minimum External Tracking (Creepage)	L(I02)	>5	mm	Measured from input terminals to output terminals, shortest distance path along the body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08	mm	Insulation thickness between the emitter and the detector; also known as the distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group	—	IIIa	—	Material Group (DIN VDE 0109).

IEC/EN/DIN EN 60747-5-5 Insulation-Related Characteristics

Description	Symbol	ACPL-M71T/ ACPL-M72T	Units
Maximum Working Insulation Voltage	V_{IORM}	567	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	1063	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	907	V_{PEAK}
Highest Allowable Overvoltage[a] (Transient Overvoltage, t_{ini} = 60 seconds)	V_{IOTM}	6000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure; also see the Thermal Derating curve, Figure 11.)			
Case Temperature	T_s	150	°C
Input Current	$I_{s,INPUT}$	150	mA
Output Power	$P_{s,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_{IO}	≥10^9	Ω

a. Refer to the optocoupler section of the *Isolation and Control Components Designer's Catalog*, under the Product Safety Regulations section (IEC/EN/DIN EN 60747-5-5), for a detailed description of Method a and Method b partial discharge test profiles.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Conditions
Storage Temperature	T_S	–55	+130	°C	—
Ambient Operating Temperature	T_A	–40	+125	°C	—
Supply Voltage	V_{DD}	0	6.5	V	—
Output Voltage	V_O	–0.5	V_{DD} + 0.5	V	—
Average Forward Input Current	I_F	—	20.0	mA	—
Peak Transient Input Current (I_F at 1-µs pulse width, <10% duty cycle)	$I_{F(TRAN)}$	—	1 80	A mA	<1-µs pulse width, 300 pps <1-µs pulse width, <10% duty cycle
Reverse Input Voltage	V_R	—	5	V	—
Input Power Dissipation	P_I	—	40	mW	—
Output Power Dissipation	P_O	—	30	mW	—
Lead Solder Temperature	—	260°C for 10 seconds, 1.6 mm below seating plane			
Solder Reflow Temperature Profile	—	See the Reflow Temperature Profile.			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+125	°C
Supply Voltage	V_{DD}	3.0	5.5	V
Forward Input Current	$I_{F(ON)}$	4.0	15	mA
Forward Off State Voltage	$V_{F(OFF)}$	—	0.8	V
Input Threshold Current	I_{TH}	—	3.5	mA

Electrical Specifications

Over recommended temperature (T_A = –40°C to +125°C), 3.0V ≤ V_{DD} ≤ 5.5V. All typical specifications are at T_A = +25°C, V_{DD} = +5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure
Input Capacitance	C_{in}	—	90	—	pF	—	—
Input Reverse Breakdown Voltage	BV_R	5.0	—	—	V	I_R = 10 µA	—
Logic High Output Voltage	V_{OH}	V_{DD} – 0.6	—	—	V	I_{OH} = –4 mA	4
Logic Low Output Voltage	V_{OL}	—	—	0.6	V	I_{OL} = 4 mA	3
Logic Low Output Supply Current	I_{DDL}	—	0.9	1.5	mA	—	—
Logic High Output Supply Current	I_{DDH}	—	0.9	1.5	mA	—	—
LED Forward Voltage	V_F	1.45	1.5	1.75	V	I_F = 10 mA, Ta = 25°C	—
		1.25	1.5	1.85	V	I_F = 10 mA, Ta = –40°C–125°C	—
V_F Temperature Coefficient	—	—	–1.5	—	mV/°C	—	—

ACPL-M71T High-Speed Mode Switching Specifications

Over recommended temperature (T_A = –40°C to +125°C), 4.5V ≤ V_{DD} ≤ 5.5V. All typical specifications are at T_A = +25°C, V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output[a]	t_{PHL}	—	26	35	ns	V_{in} = 4.5V–5.5V, R_{in} = 390Ω ±5%, C_{in} = 100 pF, C_L= 15 pF	5, 6, 11	a, b, c
Propagation Delay Time to Logic High Output[a]	t_{PLH}	—	26	35	ns			
Pulse Width Distortion[b]	PWD	—	0	12	ns			
Propagation Delay Skew[c]	t_{PSK}	—	—	15	ns			
Output Rise Time (10% – 90%)	t_R	—	10	—	ns			
Output Fall Time (90% – 10%)	t_F	—	10	—	ns			
Common Mode Transient Immunity at Logic High Output[d]	$\lvert CM_H \rvert$	15	25	—	kV/µs	V_{in} = 0V, R_{in} = 390Ω ±5%, C_{in} = 100 pF, V_{cm} = 1000V, T_A = 25°C	12	d
Common Mode Transient Immunity at Logic Low Output[e]	$\lvert CM_L \rvert$	15	25	—	kV/µs	V_{in} = 4.5V–5.5V, R_{in} = 390Ω ±5%, C_{in} = 100 pF, V_{cm} = 1000V, T_A = 25°C	13	e

a. The t_{PHL} propagation delay is measured from the 50% level (V_{in} or I_F) on the rising edge of the input pulse to 0.8V on the falling edge of the V_O signal. The t_{PLH} propagation delay is measured from the 50% level (V_{in} or I_F) on the falling edge of the input pulse to the 80% level on the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to ensure that the output will remain in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to ensure that the output will remain in a low logic state.

ACPL-M72T Low-Power Mode Switching Specifications

Over recommended temperature (–40°C to +125°C), 3.0V ≤ V_{DD} ≤ 5.5V. All typical specifications at +25°C and V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output[a]	t_{PHL}	—	60	100	ns	I_F = 4 mA, C_L = 15 pF	7, 8, 9, 10, 14	a, b, c
Propagation Delay Time to Logic High Output[a]	t_{PLH}	—	35	100	ns			
Pulse Width Distortion[b]	PWD	—	25	50	ns			
Propagation Delay Skew[c]	t_{PSK}	—		60	ns			
Output Rise Time (10% – 90%)	t_R	—	10	—	ns			
Output Fall Time (90% – 10%)	t_F	—	10	—	ns			
Common Mode Transient Immunity at Logic High Output[d]	$\lvert CM_H \rvert$	25	40	—	kV/µs	Using Broadcom LED Driving Circuit, V_{in} = 0V, R_1 = 350Ω ±5%, R_2 = 350Ω ±5%, V_{CM} = 1000V, T_A = 25°C	15	d
Common Mode Transient Immunity at Logic Low Output[e]	$\lvert CM_L \rvert$	25	40	—	kV/µs	Using Broadcom LED Driving Circuit, V_{in} = 4.5V–5.5V, R_1 = 350Ω ±5%, R_2 = 350Ω, V_{CM} = 1000V, T_A = 25°C	16	e

a. The t_{PHL} propagation delay is measured from the 50% level (V_{in} or I_F) on the rising edge of the input pulse to 0.8V on the falling edge of the V_O signal. The t_{PLH} propagation delay is measured from the 50% level (V_{in} or I_F) on the falling edge of the input pulse to the 80% level on the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to ensure that the output will remain in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to ensure that the output will remain in a low logic state.

Package Characteristics

All typical at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage	V_{ISO}	4000	—	—	V_{RMS}	RH ≤ 50%, t = 1 minute, T_A = 25°C
Input-Output Resistance	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 V dc
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz, T_A = 25°C

Performance Plots

Figure 1: Typical Diode Input Forward Current Characteristic

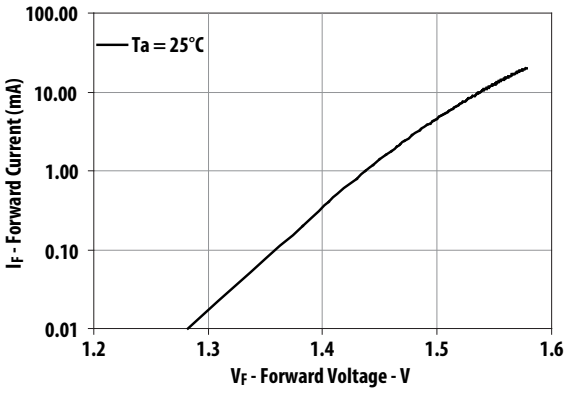


Figure 2: Typical Output Voltage vs Input Forward Current

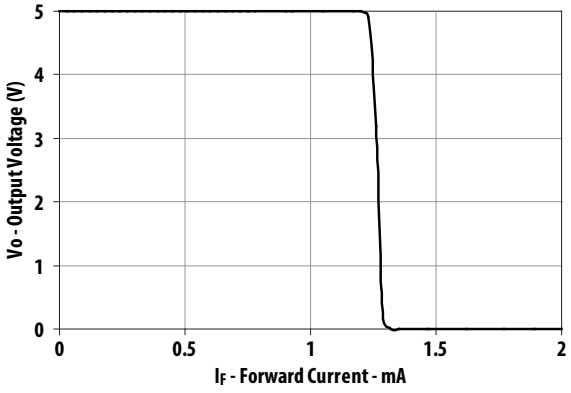


Figure 3: Typical Logic Low Output Voltage vs Logic Low Output Current

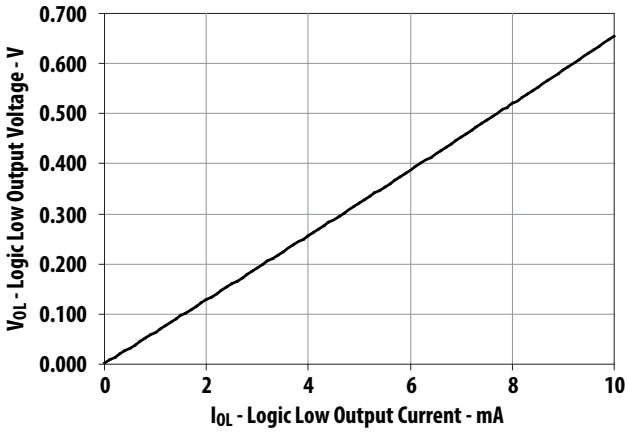


Figure 4: Typical Logic High Output Voltage vs Logic High Output Current

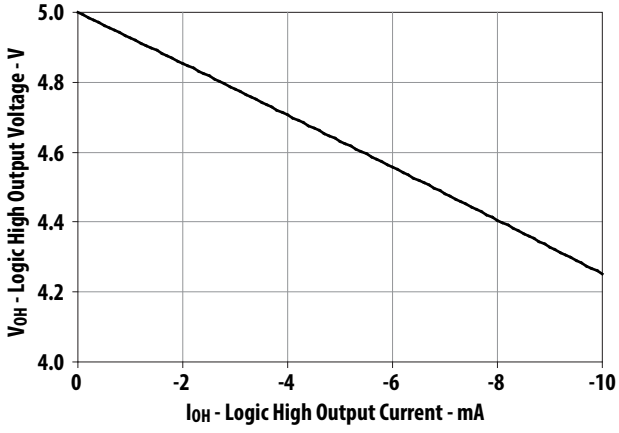


Figure 5: ACPL-M71T (High-Speed) Typical Propagation Delay vs Temperature

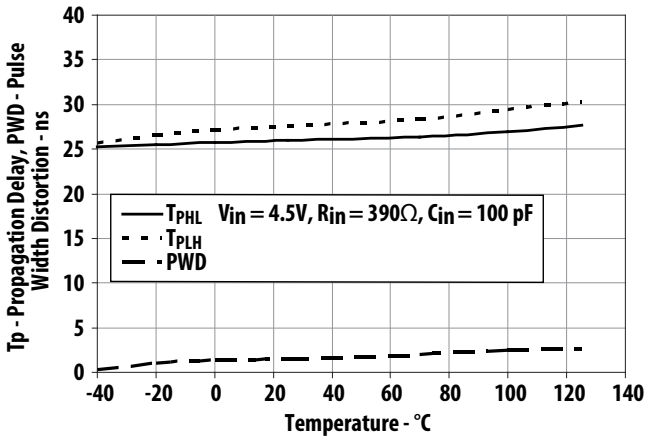


Figure 6: ACPL-M71T (High-Speed) Typical Propagation Delay vs Forward Current

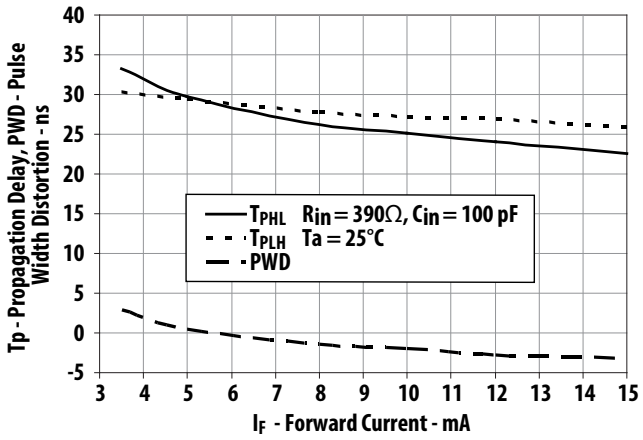


Figure 7: ACPL-M72T (5V) Typical Propagation Delay vs Temperature

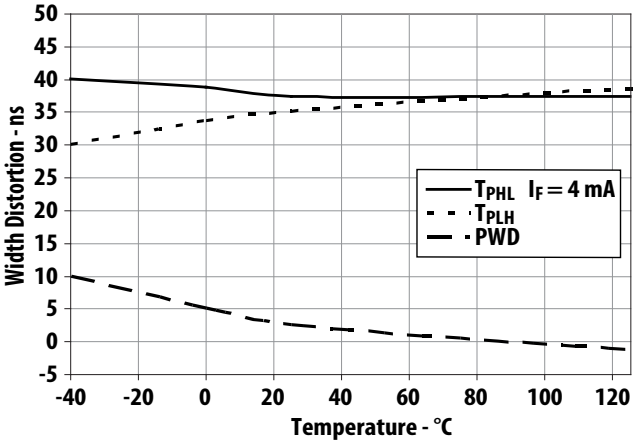


Figure 8: ACPL-M72T (5V) Typical Propagation Delay vs Forward Current

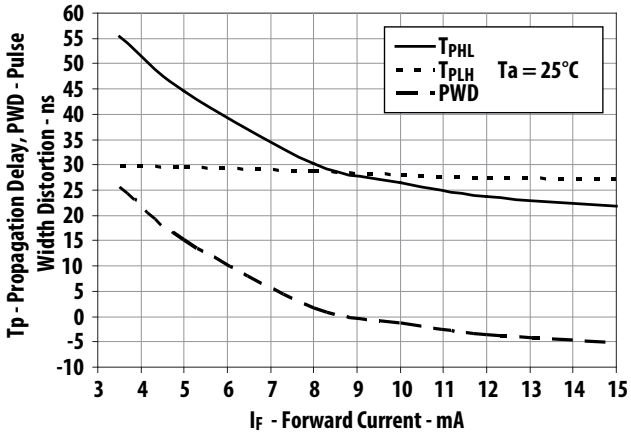


Figure 9: ACPL-M72T (3V) Typical Propagation Delay vs Temperature

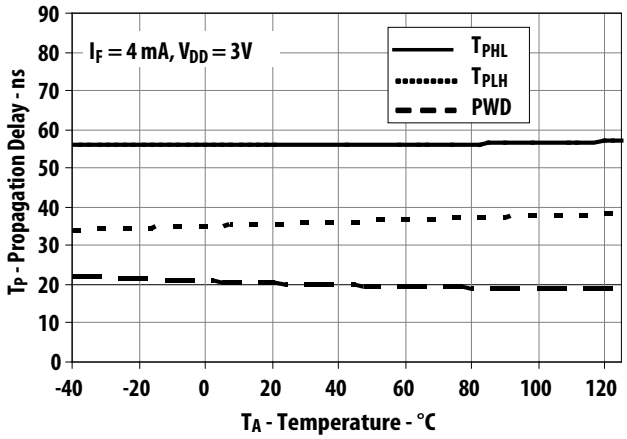
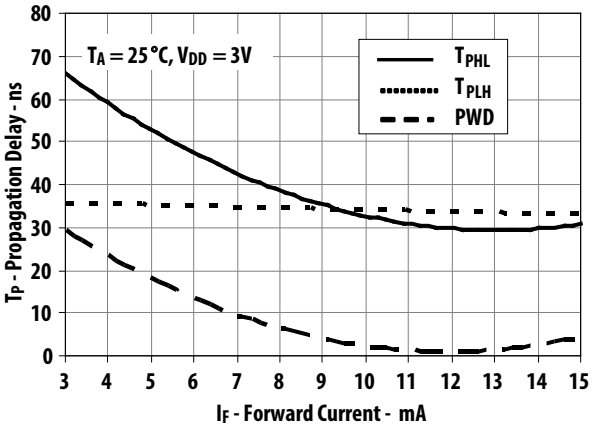


Figure 10: ACPL-M72T (3V) Typical Propagation Delay vs Forward Current



Test Circuit Diagrams

ACPL-M71T High-Speed Mode

Figure 11: High-Speed Mode Test Circuit and Typical Waveform

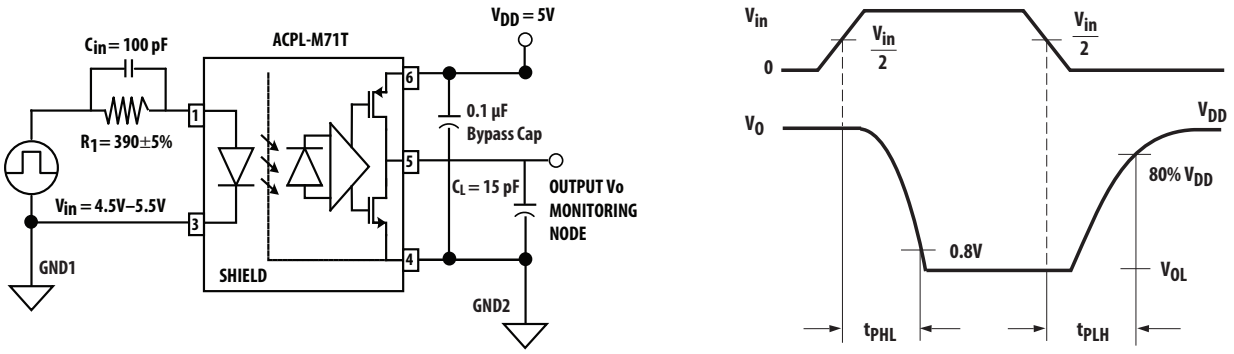


Figure 12: High-Speed Mode CMH Test Circuit and Typical Waveform

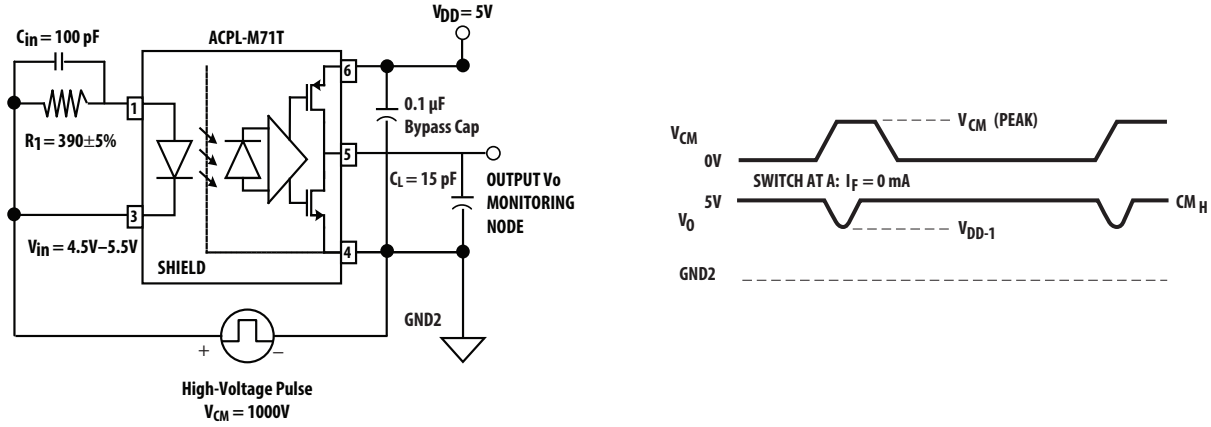
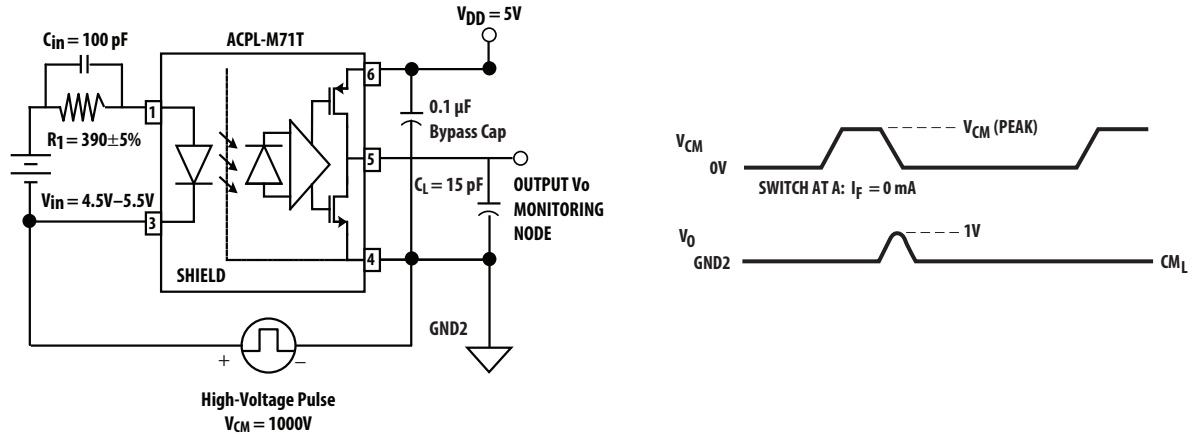


Figure 13: High-Speed Mode CML Test Circuit and Typical Waveform



ACPL-M72T Low-Power Mode

Figure 14: Low-Power Mode Switching Test Circuit and Typical Waveform

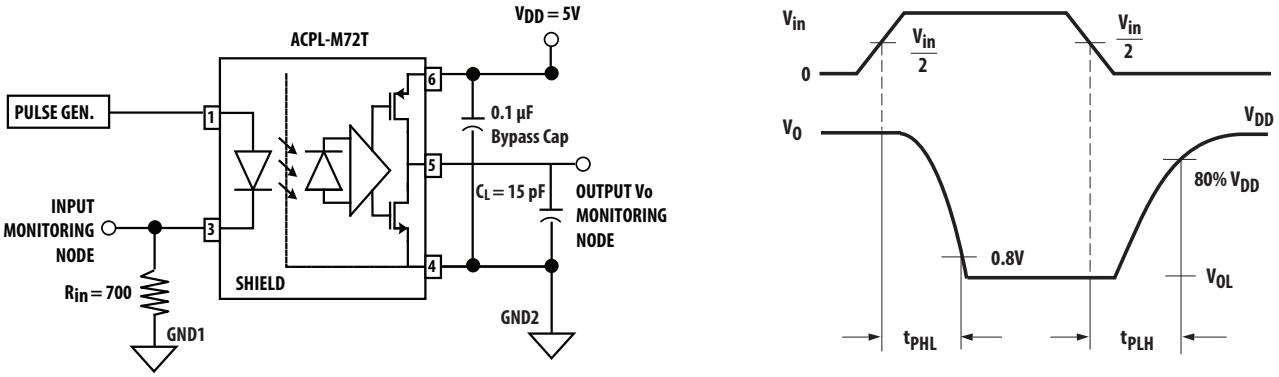


Figure 15: Low-Power Mode High CMR, CMH Test Circuit

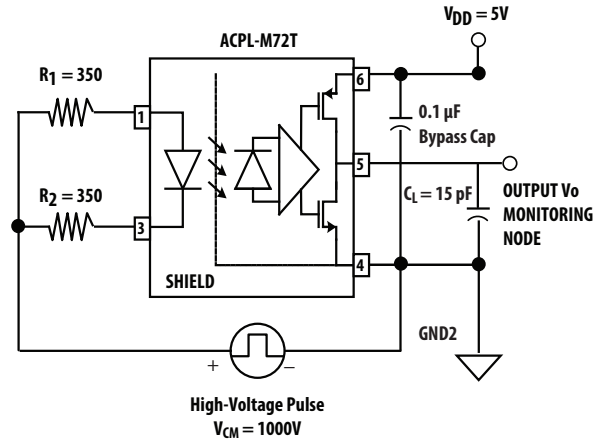
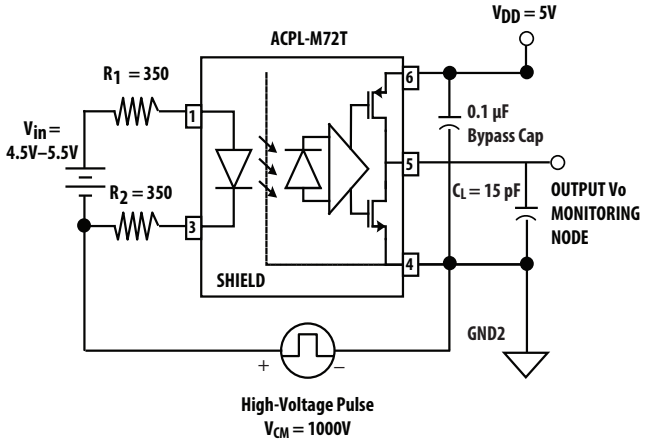
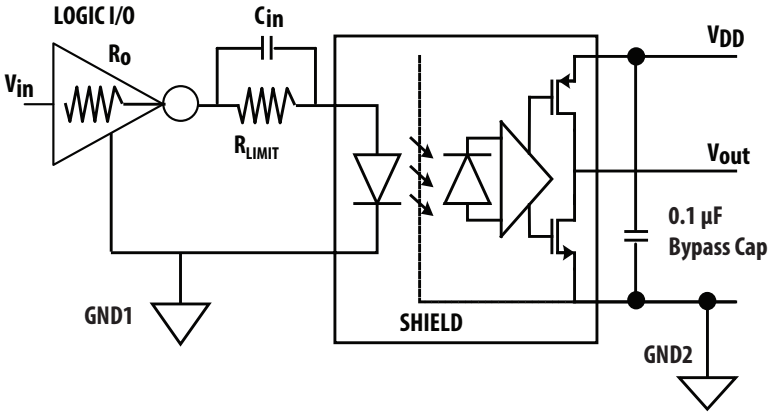


Figure 16: Low-Power Mode High CMR, CML Test Circuit



Application Circuits

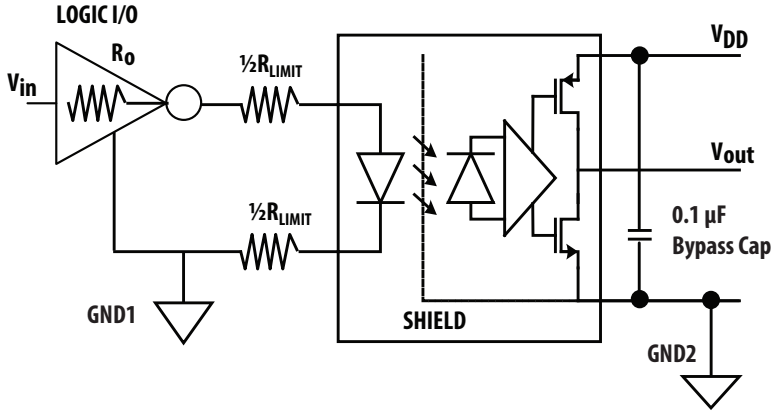
Figure 17: Recommended Application Circuit for ACPL-M71T High-Speed Performance



Truth Table

V_{in}	LED	V_{out}
L	ON	L
H	OFF	H

Figure 18: Recommended Application Circuit for ACPL-M72T Low-Power Performance



Truth Table

V_{in}	LED	V_{out}
L	ON	L
H	OFF	H