AMC3306M05 High-Precision, ±50-mV Input, Reinforced Isolated Delta-Sigma Modulator With Integrated DC/DC Converter

1 Features

- 3.3-V or 5-V single supply with integrated DC/DC converter
- ±50-mV input voltage range optimized for current measurement using shunt resistors
- Low DC errors:
  - Offset error: ±50 µV (max)
  - Offset drift: ±0.4 µV/°C (max)
  - Gain error: ±0.2% (max)
  - Gain drift: ±35 ppm/°C (max)
- High CMTI: 75 kV/µs (min)
- System-level diagnostic features
- Low EMI: meets CISPR-11 and CISPR-25 standards
- Safety-related certifications:
  - 6000-V_{PEAK} reinforced isolation per DIN VDE V 0884-11
  - 4250-V_{RMS} isolation for 1 minute per UL1577
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- Compact, isolated shunt-based current sensing in:
  - Protection relays
  - Motor drives
  - Power supplies
  - Photovoltaic inverters

3 Description

The AMC3306M05 is a precision, isolated delta-sigma (ΔΣ) modulator, optimized for shunt-based current measurements. The fully integrated, isolated DC/DC converter allows single-supply operation from the low-side of the device which makes the device a unique solution for space-constrained applications. The reinforced capacitive isolation barrier is certified according to VDE V 0884-11 and UL1577 and supports a working voltage of up to 1.2 kV_{RMS}.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage.

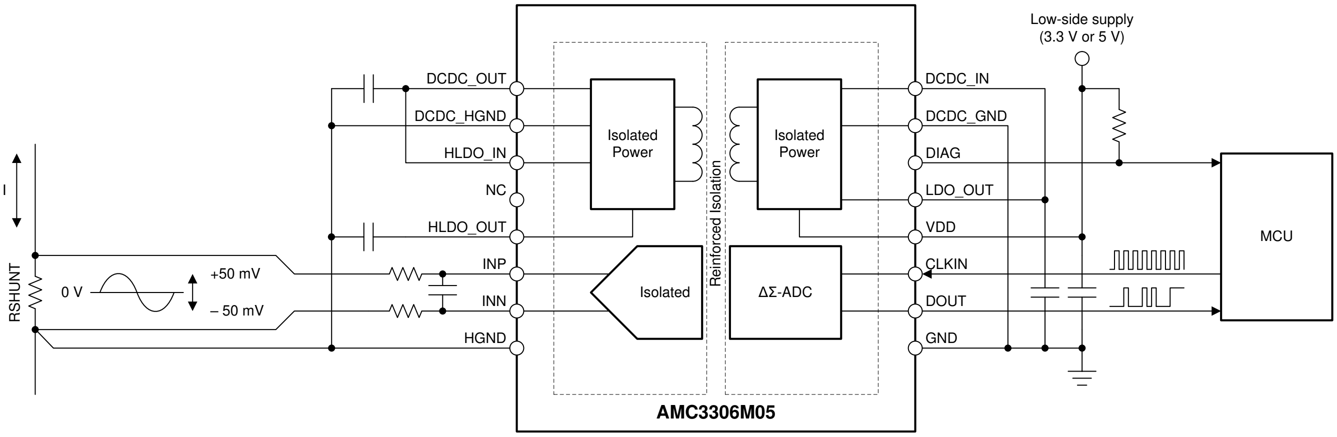
The input of the AMC3306M05 is optimized for direct connection to a low-impedance shunt resistor or other, low-impedance voltage source with low signal levels. The excellent DC accuracy and low temperature drift supports accurate current measurments over the extended industrial temperature range from –40°C to +125°C.

By using a digital filter (such as a sinc^3 filter) to decimate the bitstream, the device can achieve 16 bits of resolution with a dynamic range of 85 dB at a data rate of 78 kSPS.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC3306M05	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Typical Application

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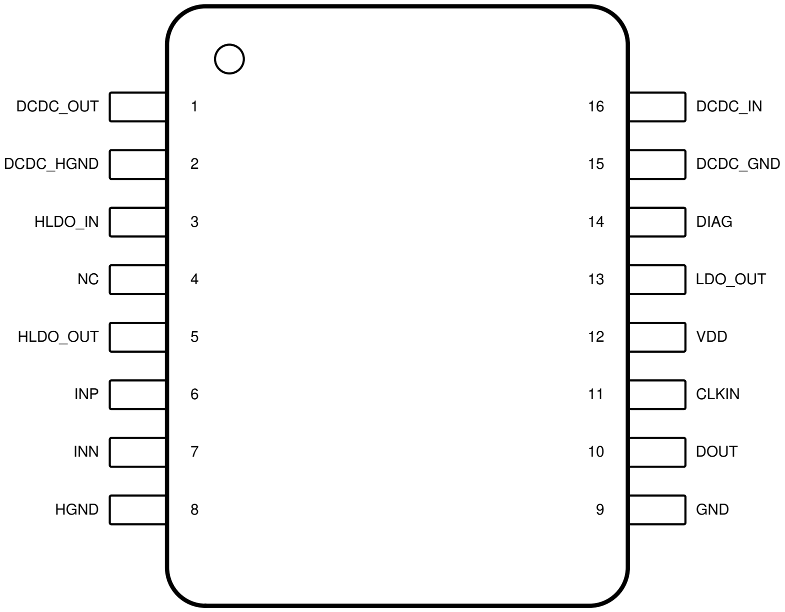
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (January 2021)	Page
• Changed *Typical Application* figure	1
• Added discussion to pin 13 description regarding the output of the LDO	3
• Changed A*bsolute Maximum Ratings*: *changed max* for *DIAG* pin from 5.5 V to 6.5 V	4
• Changed Operating common-mode input voltage (min) from -0.16 V to -0.032 V	4
• Changed overvoltage category for rated mains voltage ≤ 600 V from I-IV to I-III and for rated mains voltage ≤1000 V from I-III to I-II	6
• Changed *Typical Characteristics* section: deleted histograms	12
• Changed the *Isolated DC/DC Converter* section: clarified that the low-side LDO is not intended for driving external loads	23
• Changed *Differential Input Filter* figure	27
• Changed *What To Do and What Not To Do* section	28

5 Pin Configuration and Functions



Not to scale

Figure 5-1. DWE Package, 16-Pin SOIC, Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DCDC_OUT	Power	High-side output of the DC/DC converter; connect this pin to the HLDO_IN pin.(1)
2	DCDC_HGND	High-side power ground	High-side ground reference for the DC/DC converter; connect this pin to the HGND pin.
3	HLDO_IN	Power	Input of the high-side LDO; connect this pin to the DCDC_OUT pin.(1)
4	NC	—	No internal connection. Connect this pin to the high-side ground or leave unconnected (floating).
5	HLDO_OUT	Power	Output of the high-side LDO.(1)
6	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage.(2)
7	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage.(2)
8	HGND	High-side signal ground	High-side analog signal ground; connect this pin to the DCDC_HGND pin.
9	GND	Low-side signal ground	Low-side analog signal ground; connect this pin to the DCDC_GND pin.
10	DOUT	Digital output	Modulator data output.
11	CLKIN	Digital input	Modulator clock input with internal pulldown resistor (typical value: 1.5 MΩ).
12	VDD	Low-side power	Low-side power supply.(1)
13	LDO_OUT	Power	Output of the low-side LDO; connect this pin to the DCDC_IN pin. The output of the LDO must not be loaded by external circuitry.(1)
14	DIAG	Digital output	Active-low, open-drain status indicator output; connect this pin to the pullup supply (for example, VDD) using a resistor or leave this pin floating if not used.
15	DCDC_GND	Low-side power ground	Low-side ground reference for the DC/DC converter; connect this pin to the GND pin.
16	DCDC_IN	Power	Low-side input of the DC/DC converter; connect this pin to the LDO_OUT pin.(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2) See the *Layout* section for details.

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	6.5	V
Analog input voltage	INP, INN	HGND – 6	V_{HLDO_OUT} + 0.5	V
Digital input voltage	CLKIN	GND – 0.5	VDD + 0.5	V
Digital output voltage	DOUT	GND – 0.5	VDD + 0.5	V
	DIAG	GND – 0.5	6.5	
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Low-side power supply	VDD to GND	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±64		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} – V_{INN}$	–50		50	mV
	Absolute common-mode input voltage (1)	$(V_{INP} + V_{INN}) / 2$ to HGND	–2		V_{HLDO_OUT}	V
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to HGND	–0.032		0.9	V
DIGITAL I/O						
V_{IO}	Digital input / output voltage		0		VDD	V
f_{CLKIN}	Input clock frequency		5	20	21	MHz
	Input clock duty cycle	5 MHz ≤ f_{CLKIN} ≤ 21 MHz	40%	50%	60%	
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.

6.4 Thermal Information

THERMAL METRIC[1]		AMC3306M05 DWE (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation	VDD = 5.5 V	231	mW
		VDD = 3.6 V	151	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance - capacitive signal isolation)	≥ 21	µm
		Minimum internal gap (internal clearance - transformer power isolation)	≥ 120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage (bipolar)	1700	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1200	V_{RMS}
		At DC voltage	1700	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	6000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	7200	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification)	6250	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.5\ V_{PP}$ at 1 MHz	~3.5	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 4250 V_{RMS} or 6000 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	4250	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings must be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 73.5°C/W, VDD = 5.5 V, T_J = 150°C, T_A = 25°C			309	mA
		$R_{\theta JA}$ = 73.5°C/W, VDD = 3.6 V, T_J = 150°C, T_A = 25°C			472	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 73.5°C/W, T_J = 150°C, T_A = 25°C			1700	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum low-side voltage.

6.9 Electrical Characteristics

all minimum and maximum specifications are at T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –50 mV to +50 mV, INN = 0 V, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical values are at T_A = 25°C, CLKIN = 20 MHz, VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Single-ended input resistance	INN = HGND		4.75		kΩ
R_{IND}	Differential input resistance			4.9		kΩ
I_{IB}	Input bias current	INP = INN = HGND; $I_{IB} = (I_{IBP} + I_{IBN}) / 2$	–48	–36	–28	µA
I_{IO}	Input offset current(1)	$I_{IO} = I_{IBP} – I_{IBN}$; INP = INN = HGND		±10		nA
C_{IN}	Single-ended input capacitance	INN = HGND, f_{IN} = 310 kHz		4		pF
C_{IND}	Differential input capacitance	f_{IN} = 310 kHz		2		pF
ACCURACY						
E_O	Offset error(1)	INN = INP = HGND, T_A = 25°C	–50	±10	50	µV
TCE_O	Offset error thermal drift(4)	INN = INP = HGND	–0.4		0.4	µV/°C
E_G	Gain error	T_A = 25°C	–0.2%	±0.005%	0.2%	
TCE_G	Gain error drift(5)		–35		35	ppm/°C
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity	Resolution: 16 bits	–4	±1	4	LSB
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	77	81		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	77	81		dB
THD	Total harmonic distortion(3)	5 MHz ≤ f_{CLKIN} ≤ 21 MHz, f_{IN} = 1 kHz		–93	–86	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	87	94		dB
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–100		dB
		f_{IN} = 10 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$, $V_{INP} = V_{INN}$ = 100 mV_{PP}		–100		
PSRR	Power-supply rejection ratio	VDD from 3.0 V to 5.5 V, at DC		–120		dB
		INP = INN = HGND, VDD from 3.0 V to 5.5 V, 10 kHz, 100 mV ripple		–120		
DIGITAL I/O						
I_{IN}	Input leakage current	GND ≤ V_{IN} ≤ VDD	0		7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 × VDD		VDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × VDD	V
C_{LOAD}	Output load capacitance			15	30	pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	VDD – 0.1			V
		I_{OH} = –4 mA	VDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
CMTI	Common-mode transient immunity		75	135		kV/µs

6.9 Electrical Characteristics (continued)

all minimum and maximum specifications are at T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –50 mV to +50 mV, INN = 0 V, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical values are at T_A = 25°C, CLKIN = 20 MHz, VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
IDD	Low-side supply current	no external load on HLDO		26	40	mA
		1 mA external load on HLDO		28	42	
V_{DCDC_OUT}	DC/DC output voltage	DCDC_OUT to HGND	3.1	3.5	4.65	V
V_{DCDCUV}	DC/DC output undervoltage detection threshold voltage	V_{DCDC_OUT} falling	2.1	2.25		V
V_{HLDO_OUT}	High-side LDO output voltage	HLDO_OUT to HGND, up to 1 mA external load(2)	3	3.2	3.4	V
V_{HLDOUV}	High-side LDO output undervoltage detection threshold voltage	V_{HLDO_OUT} falling	2.4	2.6		V
I_H	High-side supply current for auxiliary circuitry	Load connected from HLDO_OUT to HGND; non-switching; -40℃ ≤ T_A ≤ 85℃(2)			1	mA
t_{START}	Device startup time	VDD step to 3.0 V to bitstream valid		0.9	1.4	ms

(1) The typical value includes one sigma statistical variation at nominal operating conditions.
(2) High-side LDO supports external loads only up to T_A = 85℃. See the *Isolated DC/DC Converter* section for more details.
(3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCE_O = (Value_{MAX} - Value_{MIN}) / TempRange$
(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25℃)} \times TempRange) \times 10^6$

6.10 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_H	DOUT hold time after rising edge of CLKIN	C_{LOAD} = 15 pF	3.5			ns
t_D	Rising edge of CLKIN to DOUT valid delay	C_{LOAD} = 15 pF; CLKIN 50% to DOUT 10% / 90%			15	ns
t_r	DOUT rise time	10% to 90%, 3.0 V ≤ VDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	6	ns
		10% to 90%, 4.5 V ≤ VDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.2	6	
t_f	DOUT fall time	10% to 90%, 3.0 V ≤ VDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.2	6	ns
		10% to 90%, 4.5 V ≤ VDD ≤ 5.5 V,C_{LOAD} = 15 pF		2.9	6	

6.11 Timing Diagrams

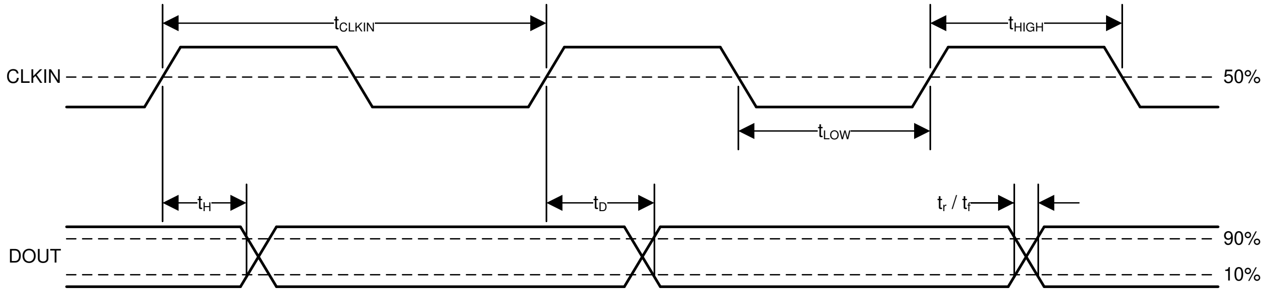


Figure 6-1. Digital Interface Timing

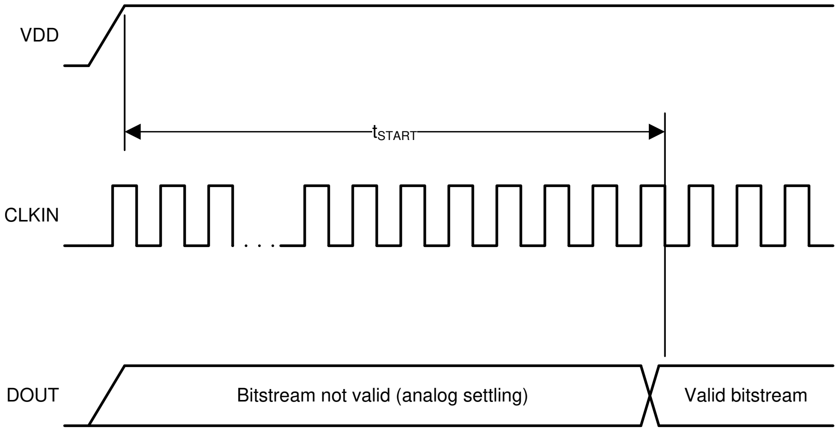


Figure 6-2. Device Startup Timing

6.12 Insulation Characteristics Curves

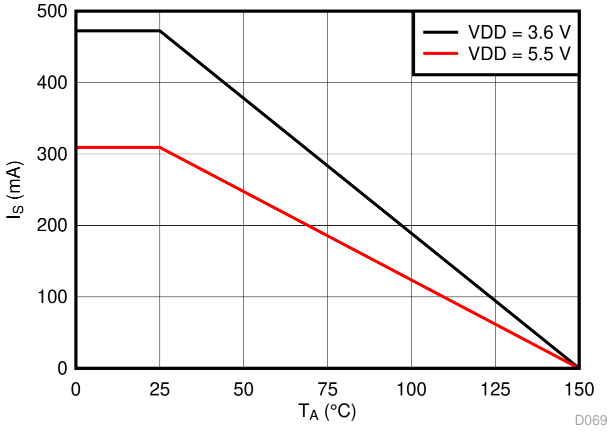


Figure 6-3. Thermal Derating Curve for Safety-Limiting Current Per VDE

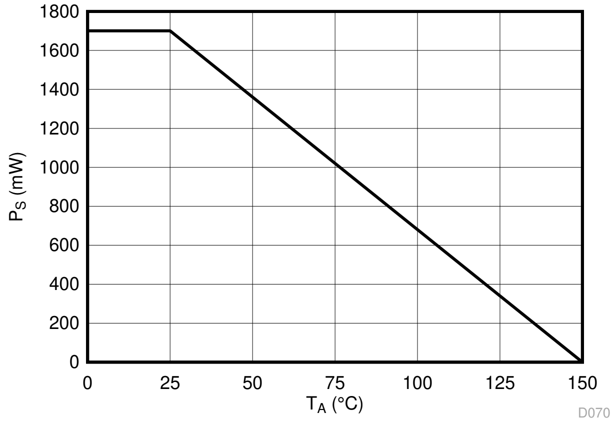
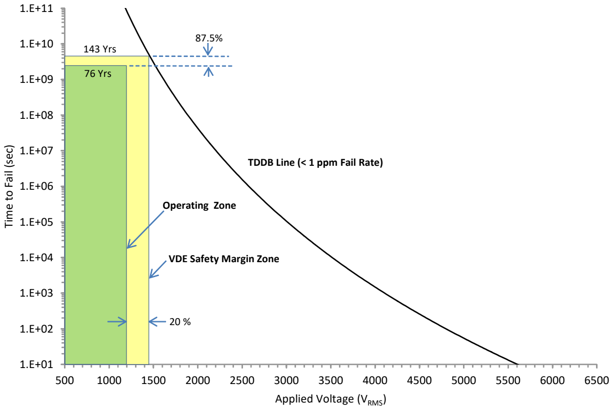


Figure 6-4. Thermal Derating Curve for Safety-Limiting Power Per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1200 V_{RMS}, operating lifetime = 76 years

Figure 6-5. Reinforced Isolation Capacitor Lifetime Projection

6.13 Typical Characteristics

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, 16-bit resolution (unless otherwise noted)

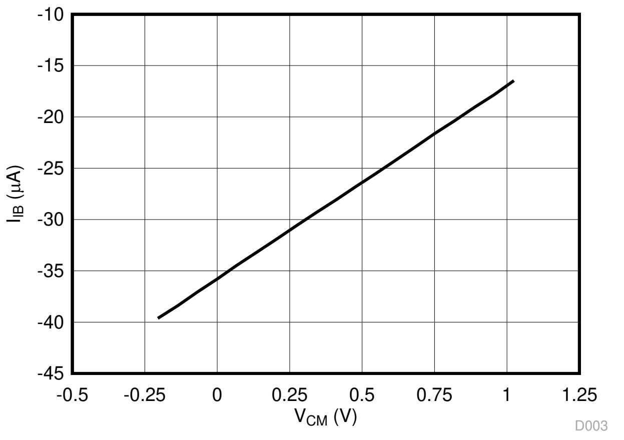


Figure 6-6. Input Bias Current vs Common-Mode Input Voltage

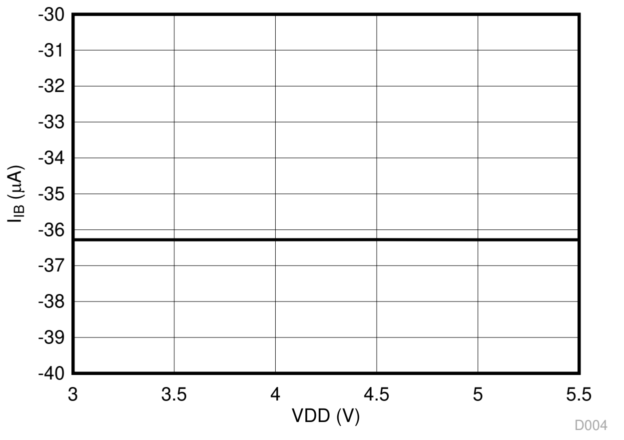


Figure 6-7. Input Bias Current vs Supply Voltage

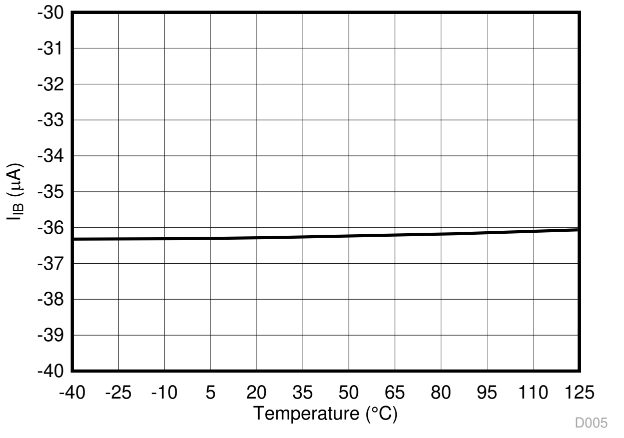


Figure 6-8. Input Bias Current vs Temperature

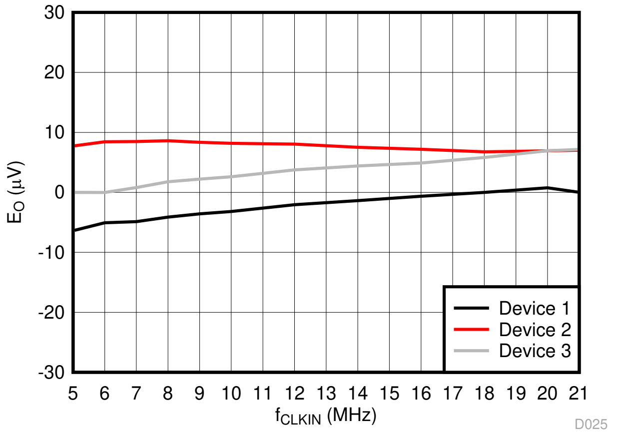


Figure 6-9. Offset Error vs Input Clock Frequency

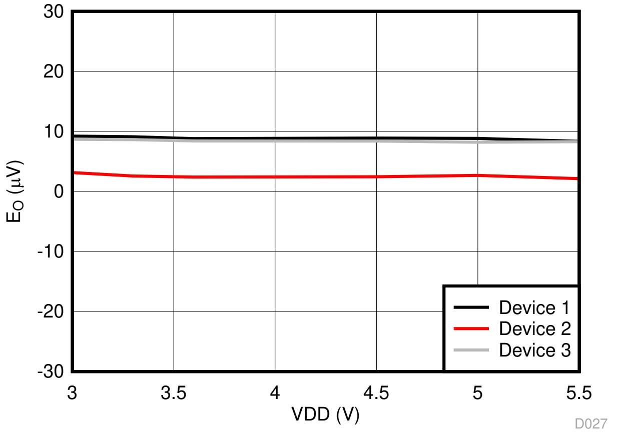


Figure 6-10. Offset Error vs Supply Voltage

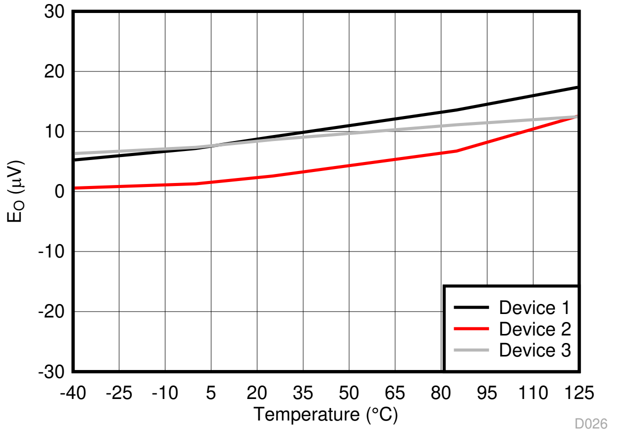


Figure 6-11. Offset Error vs Temperature

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256, 16-bit resolution (unless otherwise noted)

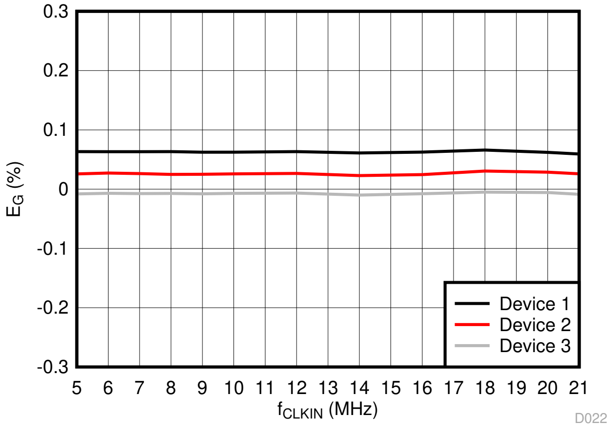


Figure 6-12. Gain Error vs Input Clock Frequency

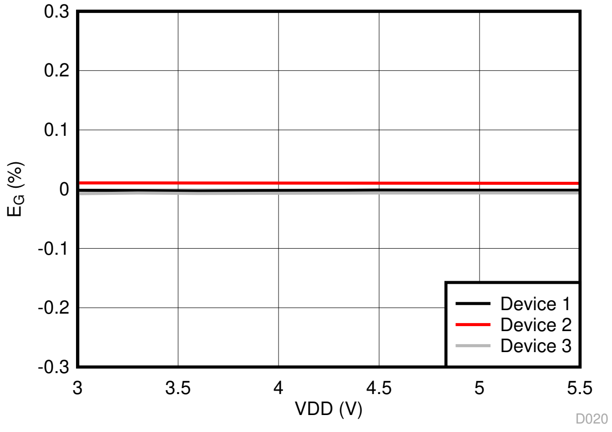


Figure 6-13. Gain Error vs Supply Voltage

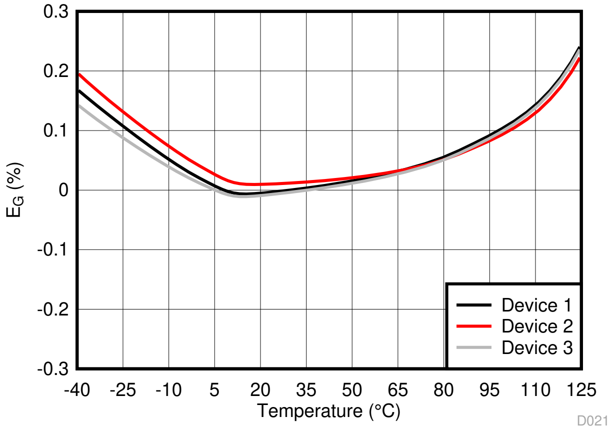


Figure 6-14. Gain Error vs Temperature

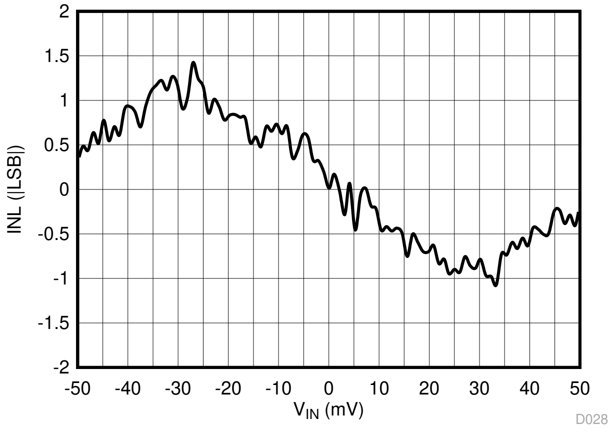


Figure 6-15. Integral Nonlinearity vs Input Voltage

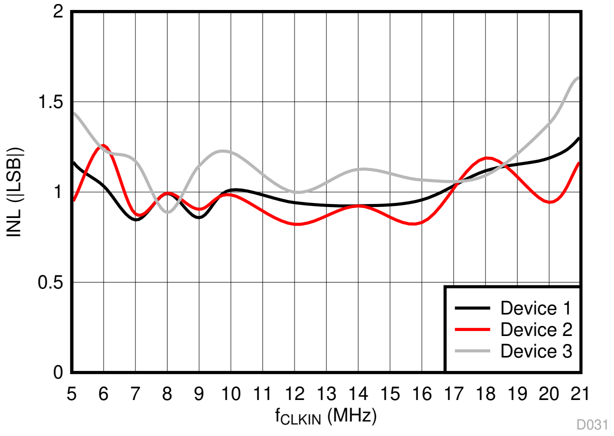


Figure 6-16. Integral Nonlinearity vs Input Clock Frequency

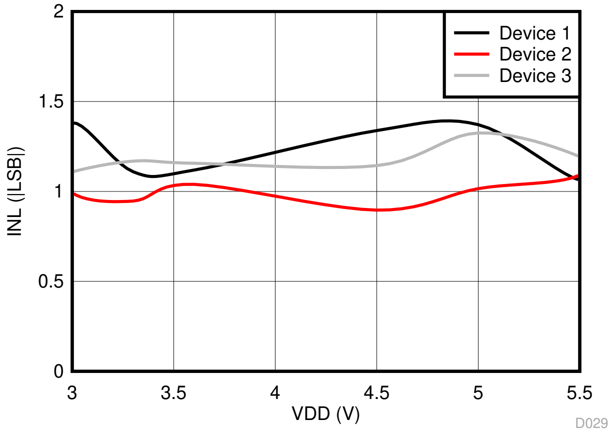


Figure 6-17. Integral Nonlinearity vs Supply Voltage

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, 16-bit resolution (unless otherwise noted)

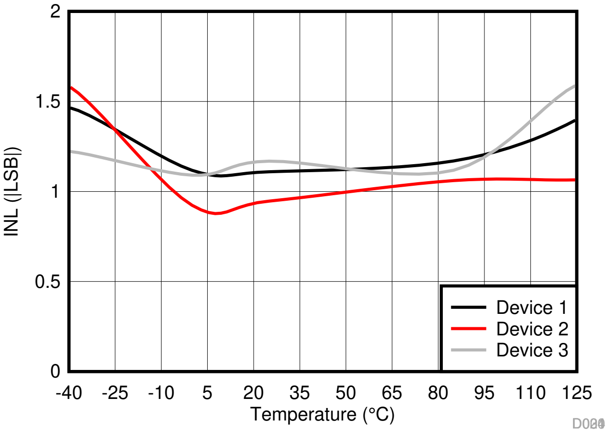


Figure 6-18. Integral Nonlinearity vs Temperature

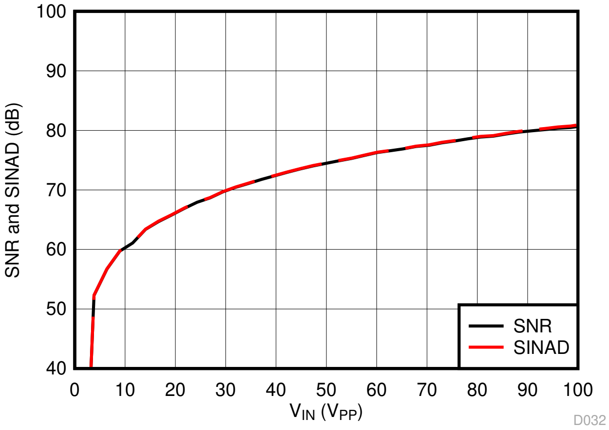


Figure 6-19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

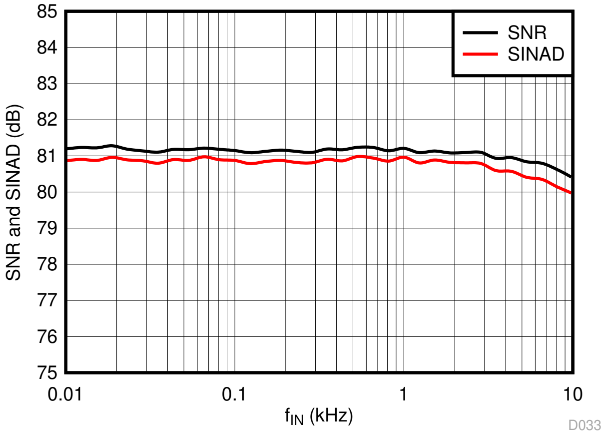


Figure 6-20. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

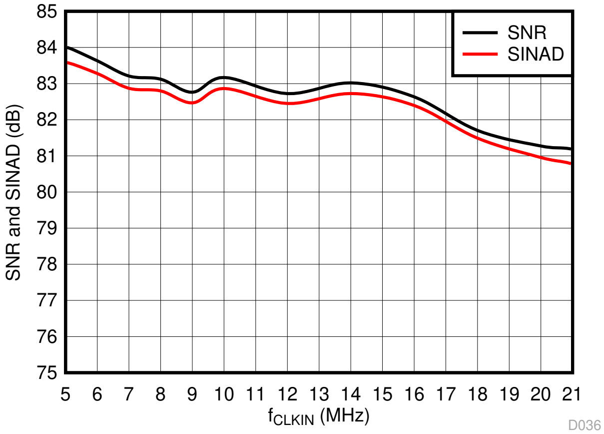


Figure 6-21. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Clock Frequency

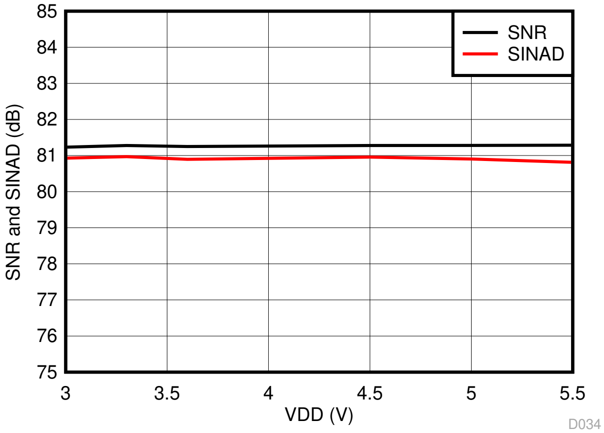


Figure 6-22. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Supply Voltage

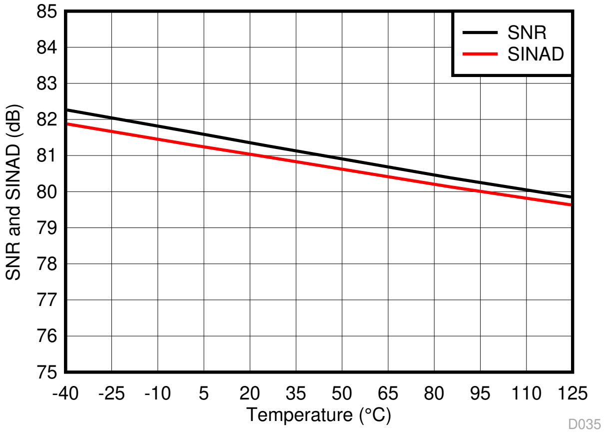


Figure 6-23. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256, 16-bit resolution (unless otherwise noted)

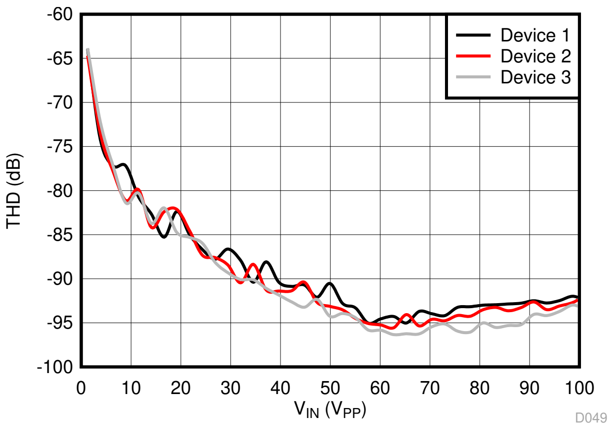


Figure 6-24. Total Harmonic Distortion vs Input Signal Amplitude

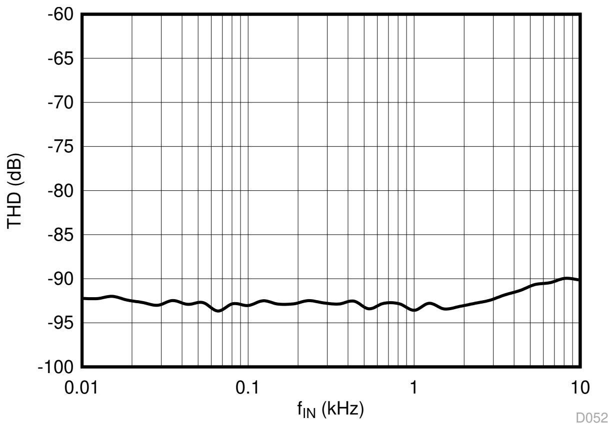


Figure 6-25. Total Harmonic Distortion vs Input Signal Frequency

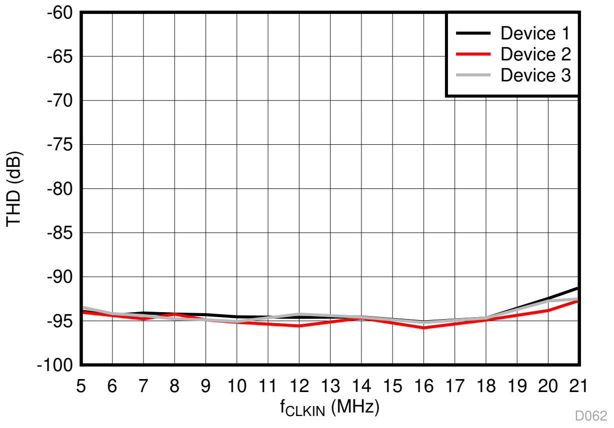


Figure 6-26. Total Harmonic Distortion vs Input Clock Frequency

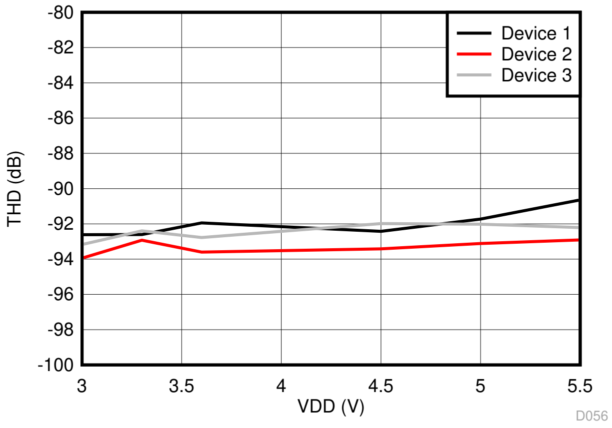


Figure 6-27. Total Harmonic Distortion vs Supply Voltage

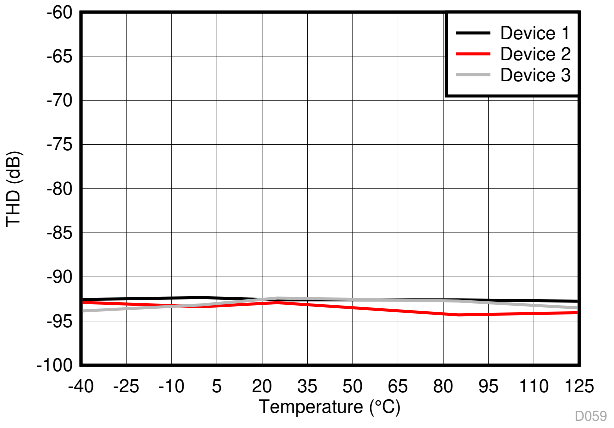


Figure 6-28. Total Harmonic Distortion vs Temperature

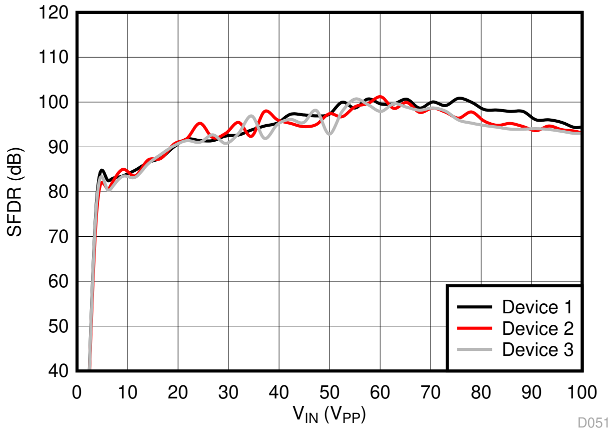


Figure 6-29. Spurious-Free Dynamic Range vs Input Signal Amplitude

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, 16-bit resolution (unless otherwise noted)

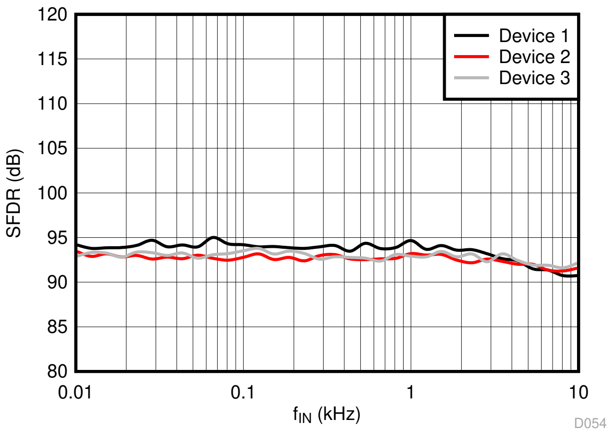


Figure 6-30. Spurious-Free Dynamic Range vs Input Signal Frequency

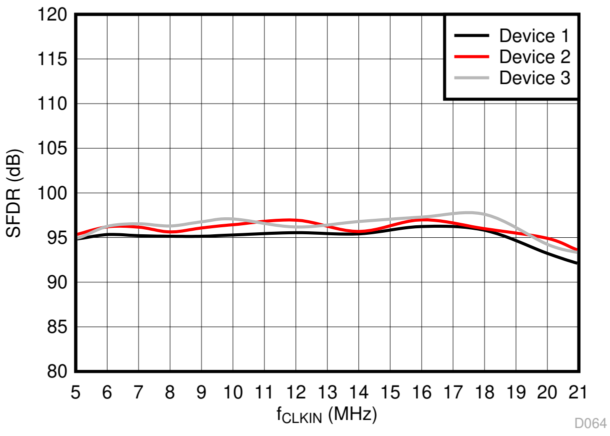


Figure 6-31. Spurious-Free Dynamic Range vs Input Clock Frequency

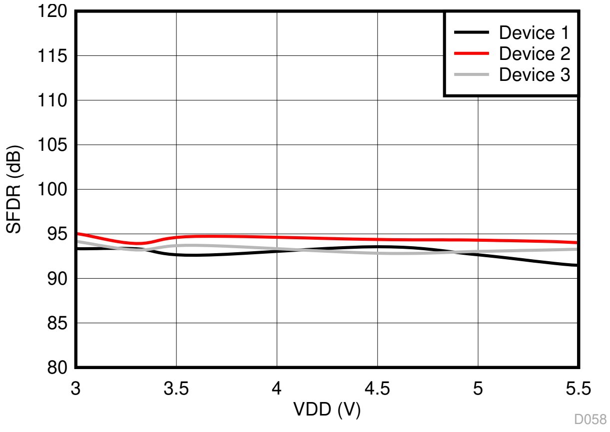


Figure 6-32. Spurious-Free Dynamic Range vs Supply Voltage

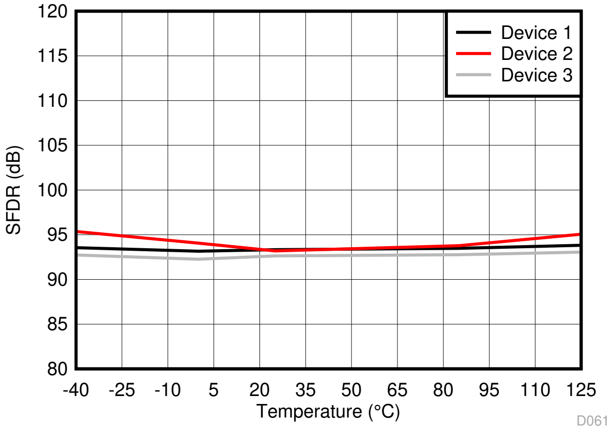


Figure 6-33. Spurious-Free Dynamic Range vs Temperature

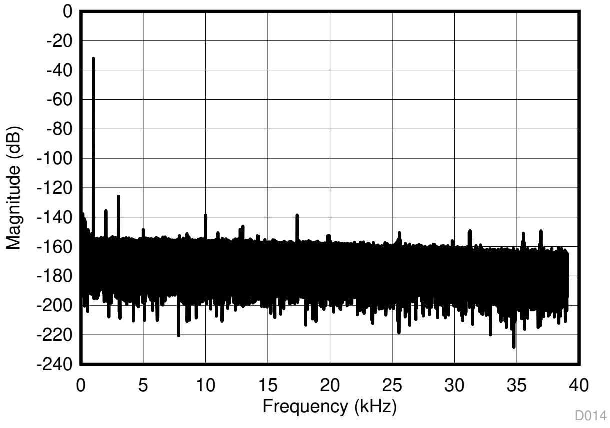


Figure 6-34. Output Frequency Spectrum With a 1-kHz Input Signal

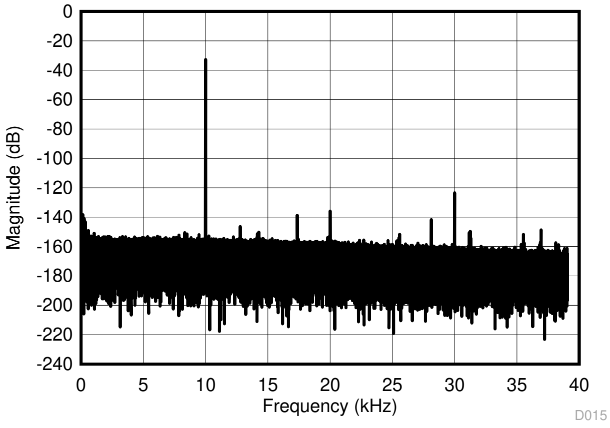


Figure 6-35. Output Frequency Spectrum With a 10-kHz Input Signal

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, 16-bit resolution (unless otherwise noted)

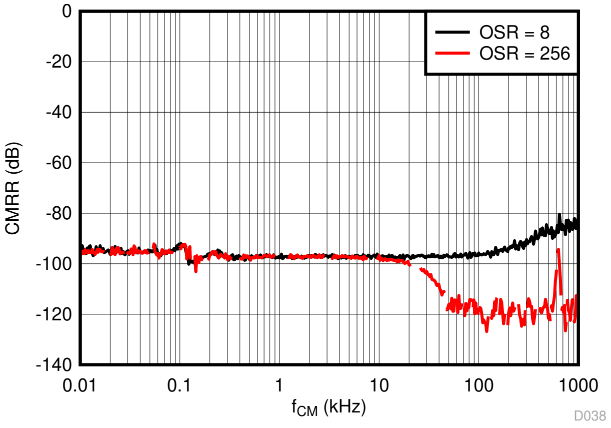


Figure 6-36. Common-Mode Rejection Ratio vs Input Signal Frequency

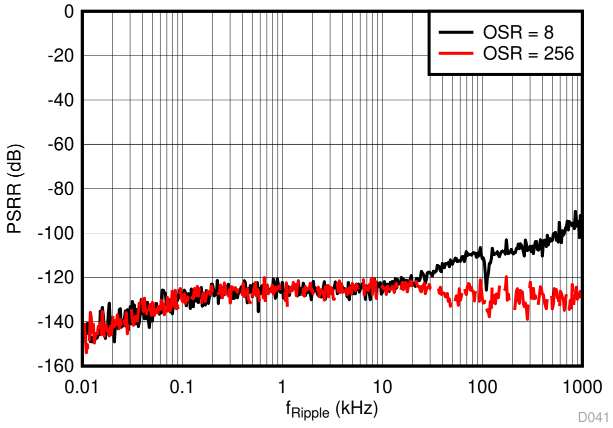


Figure 6-37. Power-Supply Rejection Ratio vs Ripple Frequency

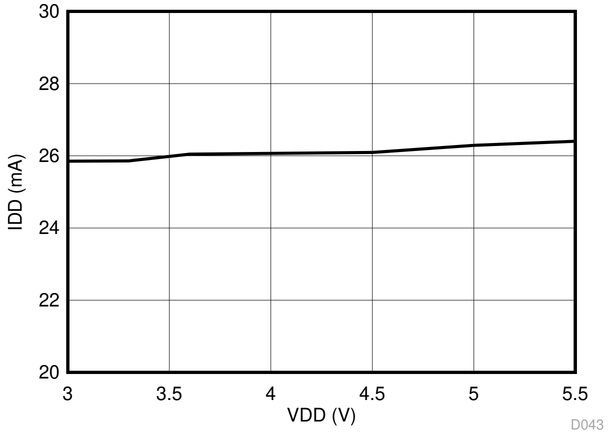


Figure 6-38. Supply Current vs Supply Voltage

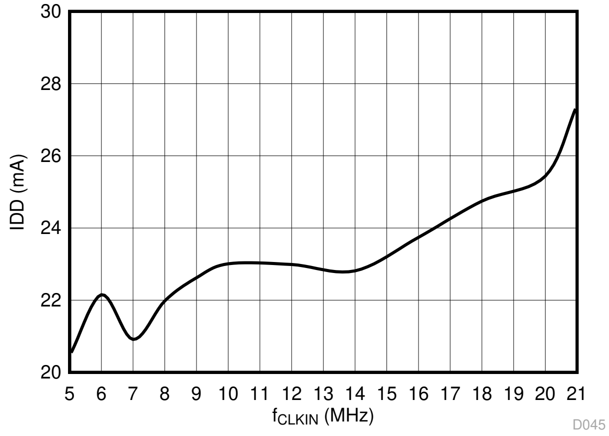


Figure 6-39. Supply Current vs Input Clock Frequency

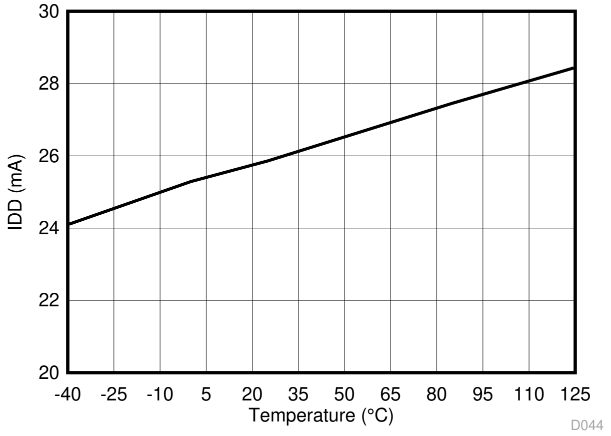


Figure 6-40. Supply Current vs Temperature

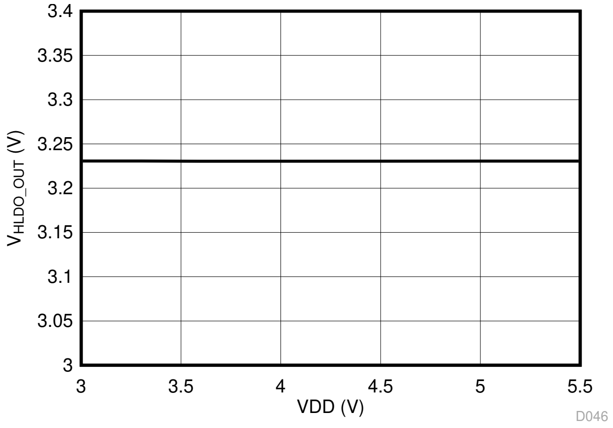


Figure 6-41. High-Side LDO Output Voltage vs Supply Voltage

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –50 mV to +50 mV, INN = HGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256, 16-bit resolution (unless otherwise noted)

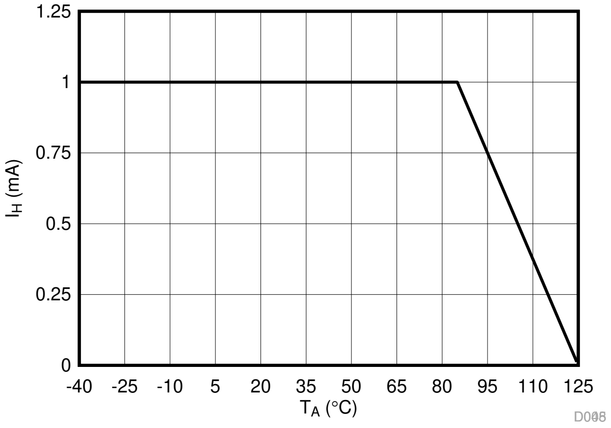


Figure 6-42. I_H Derating vs Ambient Temperature

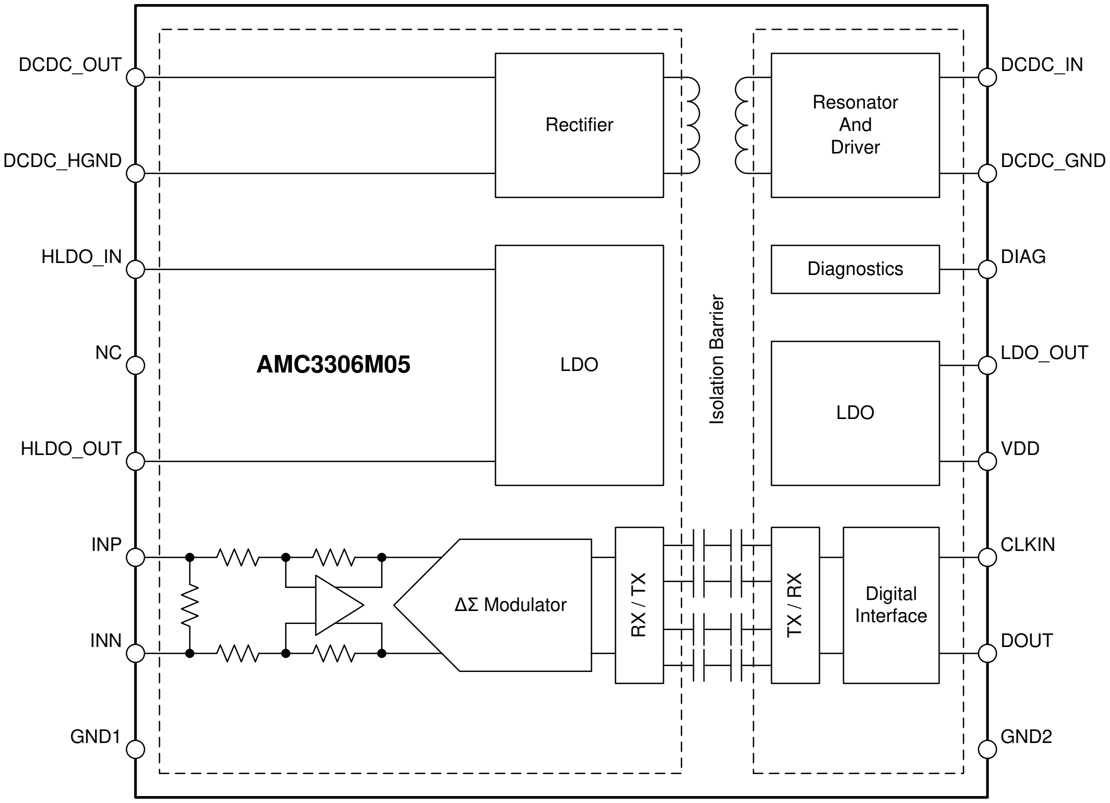
7 Detailed Description

7.1 Overview

The AMC3306M05 is a fully differential, precision, isolated modulator with an integrated DC/DC converter that can supply the high-side of the device from a single 3.3-V or 5-V voltage supply on the low side. The analog input pins INP and INN are connected to a fully differential amplifier that feeds the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier and separates the high-side from the low-side. The isolated data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally-provided clock source at the CLKIN pin. The time average of this serial bitstream output is proportional to the analog input voltage. The external clock input simplifies the synchronization of multiple current-sensing channels on the system level.

The signal path is isolated by a double capacitive silicon dioxide (SiO_2) insuation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

7.2 Functional Block Diagram

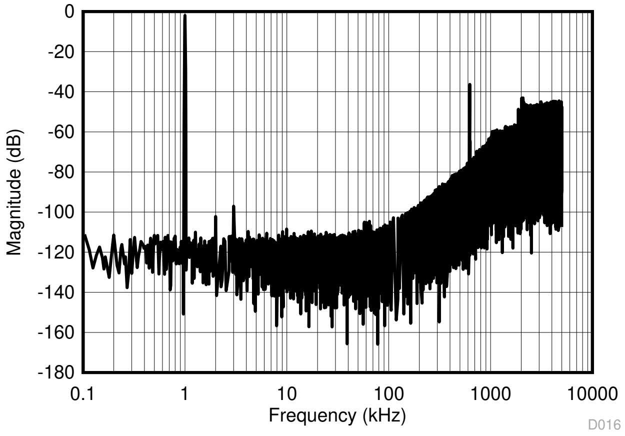


7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC3306M05 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND}. The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

For reduced offset and offset drift, the differential amplifier is chopper-stabilized with the switching frequency set at f_{CLKIN} / 32. As shown in Figure 7-1, the switching frequency generates a spur at 625 kHz.



sinc^3 filter, OSR = 2, f_{CLKIN} = 20 MHz, f_{IN} = 1 kHz

Figure 7-1. Quantization Noise Shaping

There are two restrictions on the analog input signals INP and INN. First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the *Absolute Maximum Ratings* table, the input currents must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}) as specified in the *Recommended Operating Conditions* table.

7.3.2 Modulator

The second-order, switched-capacitor, feed-forward ΔΣ modulator conceptualized in Figure 7-2 is implemented in the AMC3306M05 . The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is differentiated with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

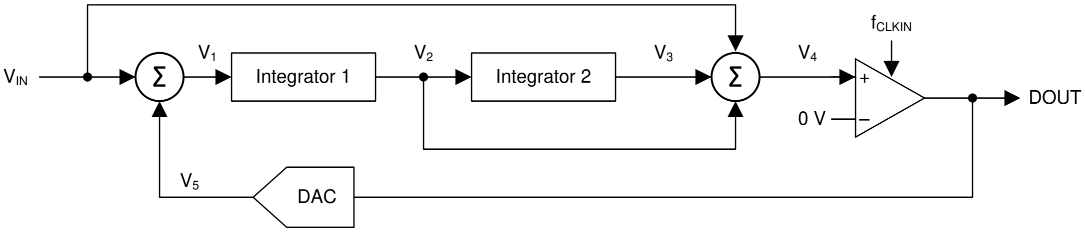


Figure 7-2. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies, as shown in Figure 7-1. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's C2000™ and Sitara™ microcontroller families offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC3306M05. Alternatively, a field-programmable gate array (FPGA) or complex programmable logic device (CPLD) can be used to implement the filter.

7.3.3 Isolation Channel Signal Transmission

The AMC3306M05 uses an on-off keying (OOK) modulation scheme, as shown in Figure 7-3, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC3306M05 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and produces the output. The AMC3306M05 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

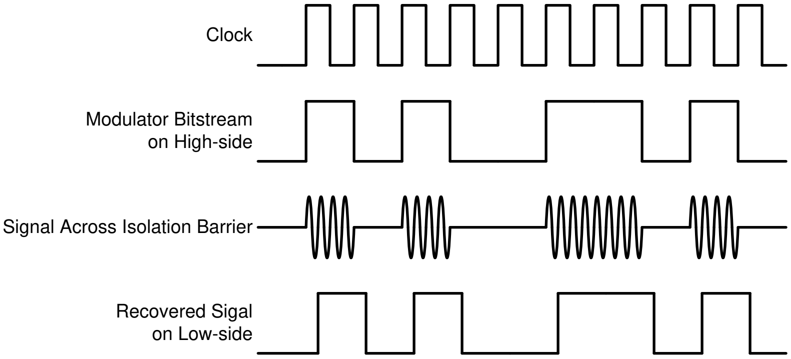


Figure 7-3. OOK-Based Modulation Scheme

7.3.4 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 50 mV produces a stream of ones and zeros that are high 89.06% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58368. A differential input of –50 mV produces a stream of ones and zeros that are high 10.94% of the time and ideally results in code 7168 with 16-bit resolution. These input voltages are also the specified linear range of the AMC3306M05. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior as the quantization noise increases. The output of the modulator clips with a constant stream of zeros with an input less than or equal to –64 mV or with a constant stream of ones with an input greater than or equal to 64 mV. In this case, however, the AMC3306M05 generates a single 1 (if the input is at negative full-scale) or 0 (if the input is at positive full-scale) every 128 clock cycles to indicate proper device function (see the *Output Behavior in Case of a Full-Scale Input* section for more details). Figure 7-4 shows the input voltage versus the output modulator signal.

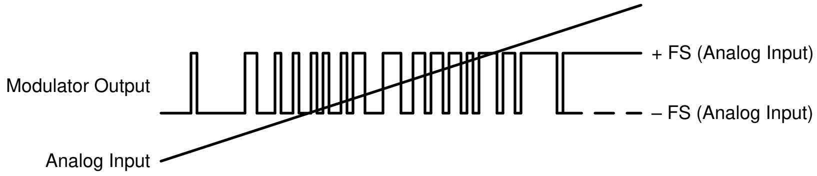


Figure 7-4. AMC3306M05 Modulator Output vs Analog Input

The density of ones in the output bitstream can be calculated using Equation 1 for any input voltage value with the exception of a full-scale input signal, as described in *Output Behavior in Case of a Full-Scale Input*:

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \tag{1}$$

7.3.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC3306M05 (that is, $|V_{IN}| \geq V_{Clipping}$), the device generates a single one or zero every 128 bits at DOUT, as shown in Figure 7-5, depending on the actual polarity of the signal being sensed. In this way, differentiating between a missing high-side supply and a full-scale input signal is possible on the system level.

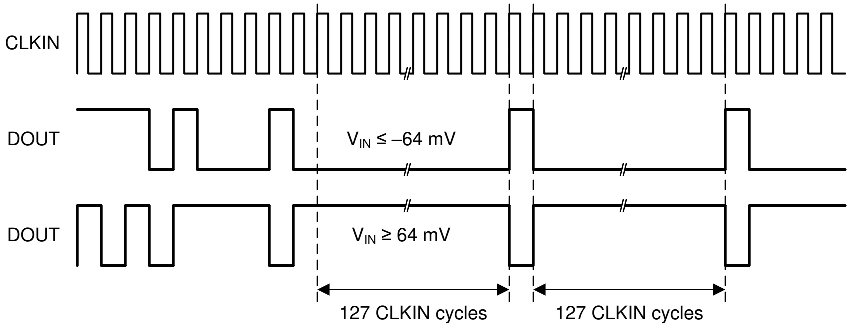


Figure 7-5. Full-Scale Output of the AMC3306M05

7.3.4.2 Output Behavior in Case of a High-Side Supply Failure

The AMC3306M05 provides a failsafe output that ensures that the output DOUT of the device is a constant bitstream of logic 0's in case the integrated DC/DC converter output voltage is below the undervoltage detection threshold. See the *Diagnostic Output* section for more information.

7.3.5 Isolated DC/DC Converter

The AMC3306M05 offers a fully integrated isolated DC/DC converter that includes the following components illustrated in the *Functional Block Diagram* section:

- Low-dropout regulator (LDO) on the low-side to stabilize the supply voltage VDD that drives the low-side of the converter. This circuit does not output a constant voltage and is not intended for driving any external load.
- Low-side full-bridge inverter and drivers
- Laminate-based, air-core transformer for high immunity to magnetic fields
- High-side full-bridge rectifier
- High-side LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path. The high-side LDO outputs a constant voltage and can provide a limited amount of current to power external circuitry.

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronized to the operation of the ΔΣ modulator to minimize interference with data transmission and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3306M05 and can source up to I_H of additional DC current for an optional auxiliary circuit such as an active filter, preamplifier, or comparator. As shown in Figure 7-6, I_H is specified up to an ambient temperature of 85°C and derates linearly at higher temperatures.

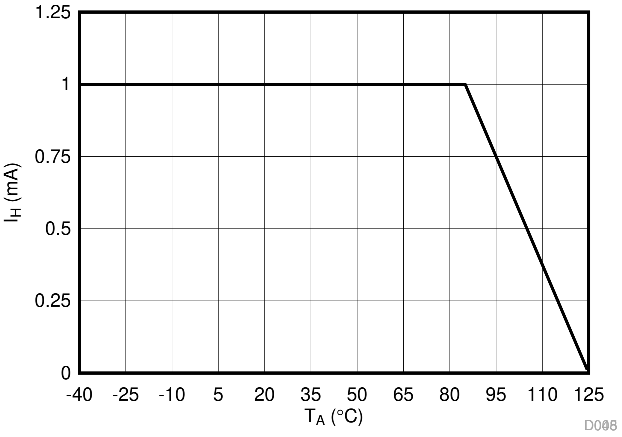


Figure 7-6. Derating of I_H at Ambient Temperatures >85°C

7.3.6 Diagnostic Output

As shown in Figure 7-7, the open-drain DIAG pin can be monitored to confirm the device is operational, and the output data are valid. During power-up, the DIAG pin is actively held low until the high-side supply is in regulation and the modulator starts outputting data. The DIAG pin is actively pulled low if:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high-side). The modulator itself outputs a constant bitstream of logic 0's in this case, that is, the DOUT pin is permanently low.
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out). In this case, the low-side may still receive data from the high-side but the data may not be valid. However, the modulator itself outputs a constant bitstream of logic 0's in this case, meaning that the DOUT pin is permanently low.

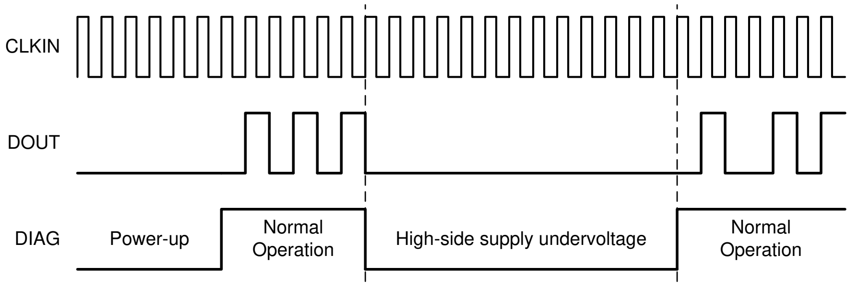


Figure 7-7. DIAG and Output Under Different Operating Conditions

7.4 Device Functional Modes

The AMC3306M05 is operational when VDD is applied, as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the AMC3306M05 a high performance solution for industrial applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

8.1.1 Digital Filter Usage

The modulator generates a bitstream that must be processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, as shown in Equation 2, built with minimal effort and hardware, is a sinc^3-type filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All characterization in this document is done with a sinc^3 filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits, unless specified otherwise. The measured effective number of bits (ENOB) as a function of the OSR is illustrated in Figure 8-3 of the *Typical Application* section.

A *delta sigma modulator filter calculator* is available for download at www.ti.com that aids in the filter design and selecting the right OSR and filter-order to achieve the desired output resolution and filter response time.

An example code for implementing a sinc^3 filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

8.2 Typical Application

8.2.1 Solar Inverter Application

The AMC3306M05 is ideally suited for shunt-based current sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC3306M05 integrates an isolated power supply for the high-voltage side and therefore makes the device particularly easy to use in applications that do not have a high-side supply readily available or where a high-side supply is referenced to a different ground potential than the signal to be measured.

Figure 8-1 shows a simplified schematic of the AMC3306M05 in a solar inverter where the phase current is measured on the grid-side of an LCL filter. Although the system offers a supply for the high-side gate driver, there is a large common-mode voltage between the gate driver supply ground reference and the shunt resistor on the other side of the LCL filter. Therefore, the gate driver supply is not suitable for powering the high-side of an isolated modulator that measures the voltage across the shunt. The integrated isolated power supply of the AMC3306M05 solves that problem and enables current sensing at locations that is optimal for the system.

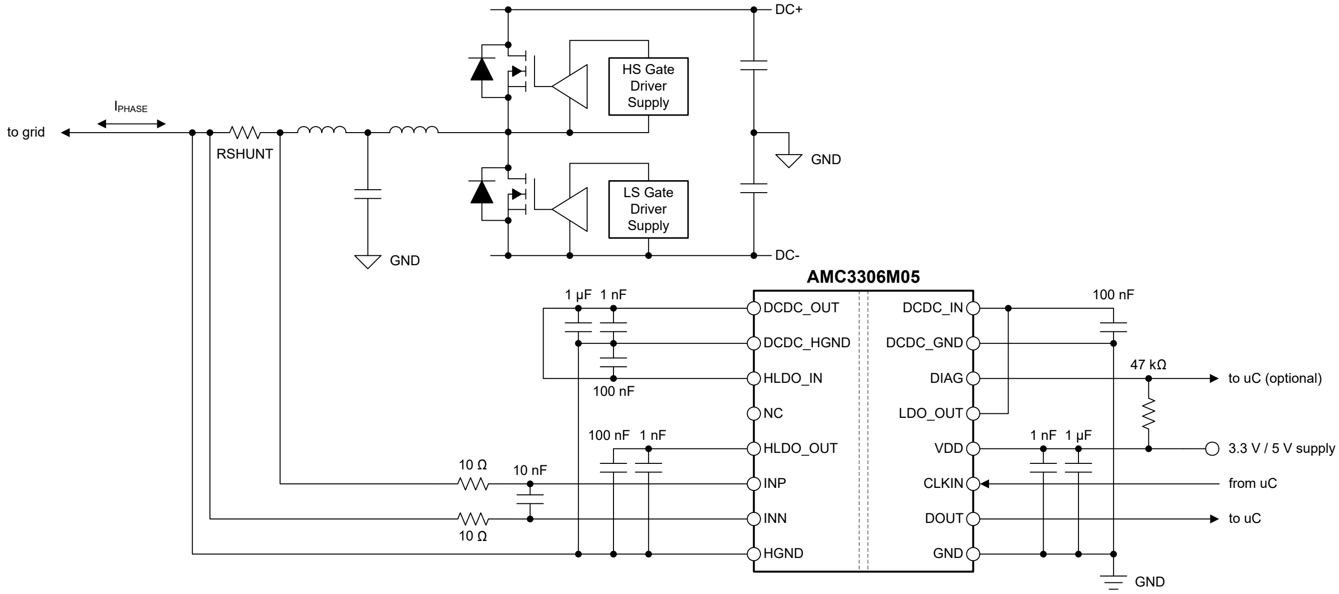


Figure 8-1. The AMC3306M05 in a Solar Inverter Application

8.2.1.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
Low-side supply voltage	3.3 V or 5 V
Voltage drop across RSHUNT for a linear response	±50 mV (maximum)

8.2.1.2 Detailed Design Procedure

The AMC3306M05 requires a single 3.3-V or 5-V supply on its low-side. The high-side supply is internally generated by an integrated DC/DC converter as explained in the *Isolated DC/DC Converter* section.

The ground reference (HGND) is derived from the terminal of the shunt resistor that is connected to the negative input (INN) of the AMC3306M05. If a four-pin shunt is used, the inputs of the device are connected to the inner leads and HGND is connected to one of the outer leads. To minimize offset and improve accuracy, set the ground connection to a separate trace that connects directly to the shunt resistor rather than shorting HGND to INN directly at the input to the device. See the *Layout* section for more details.

8.2.1.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: V_{SHUNT} = I × RSHUNT.

Consider the following two restrictions to choose the proper value of the shunt resistor, RSHUNT:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range for linear response: $|V_{SHUNT}| \leq V_{FSR}$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

8.2.1.2.2 Input Filter Design

TI recommends placing a RC filter in front of a ΔΣ modulator to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency of the ΔΣ modulator (f_{CLKIN})
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications the structure shown in Figure 8-2 achieves excellent performance.

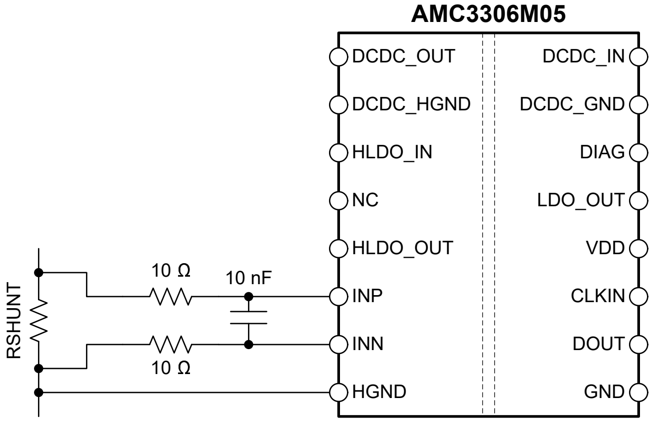


Figure 8-2. Differential Input Filter

8.2.1.2.3 Bitstream Filtering

For modulator output bitstream filtering, a device from TI's C2000™ or Sitara™ microcontroller families is recommended. These families support up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high-accuracy results for the control loop and one fast-response path for overcurrent detection.

A *delta sigma modulator filter calculator* is available for download at www.ti.com that aids in the filter design and selecting the right OSR and filter-order to achieve the desired output resolution and filter response time.

8.2.1.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 8-3 shows the ENOB of the AMC3306M05 with different oversampling ratios. By using Equation 3, this number can also be calculated from the SINAD:

$$\text{SINAD} = 1.76\ \text{dB} + 6.02\ \text{dB} \times \text{ENOB} \tag{3}$$

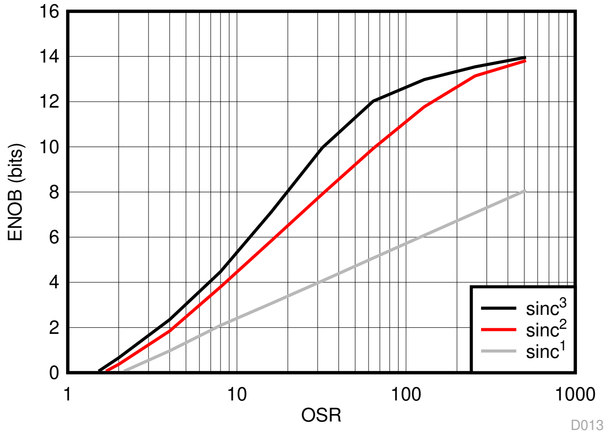


Figure 8-3. Measured Effective Number of Bits vs Oversampling Ratio

8.2.2 What To Do and What Not To Do

Do not leave the inputs of the AMC3306M05 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the output of the device is undetermined.

Connect the negative input (INN) to the high-side ground (HGND), either by a hard short or through a resistive path. A DC current path between INN and HGND is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting AGND to INN directly at the input to the device. See the *Layout* section for more details.

The high-side LDO can source a limited amount of current (I_H) to power external circuitry. Take care not to overload the high-side LDO and be aware of derating I_H at high temperatures as explained in the *Isolated DC/DC Converter* section.

The low-side LDO does not output a constant voltage and is not intended for powering any external circuitry. Do not connect any external load to the HLDO_OUT pin.

9 Power Supply Recommendations

The AMC3306M05 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V or 5 V. TI recommends a low-ESR decoupling capacitor of 1 nF (C8 in Figure 9-1) placed as close as possible to the VDD pin, followed by a 1-µF capacitor (C9) to filter this power-supply path.

The low-side of the DC/DC converter is decoupled with a low-ESR, 100-nF capacitor (C4) positioned close to the device between the DCDC_IN and DCDC_GND pins. Use a 1-µF capacitor (C2) to decouple the high-side in addition to a low-ESR, 1-nF capacitor (C3) placed as close as possible to the device and connected to the DCDC_OUT and DCDC_HGND pins.

For the high-side LDO, use low-ESR capacitors of 1-nF (C6), placed as close as possible to the AMC3306M05, followed by a 100-nF decoupling capacitor (C5).

The ground reference for the high-side (HGND) is derived from the terminal of the shunt resistor that is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection instead of shorting HGND to INN directly at the device input. The high-side DC/DC ground terminal (DCDC_HGND) is shorted to HGND directly at the device pins.

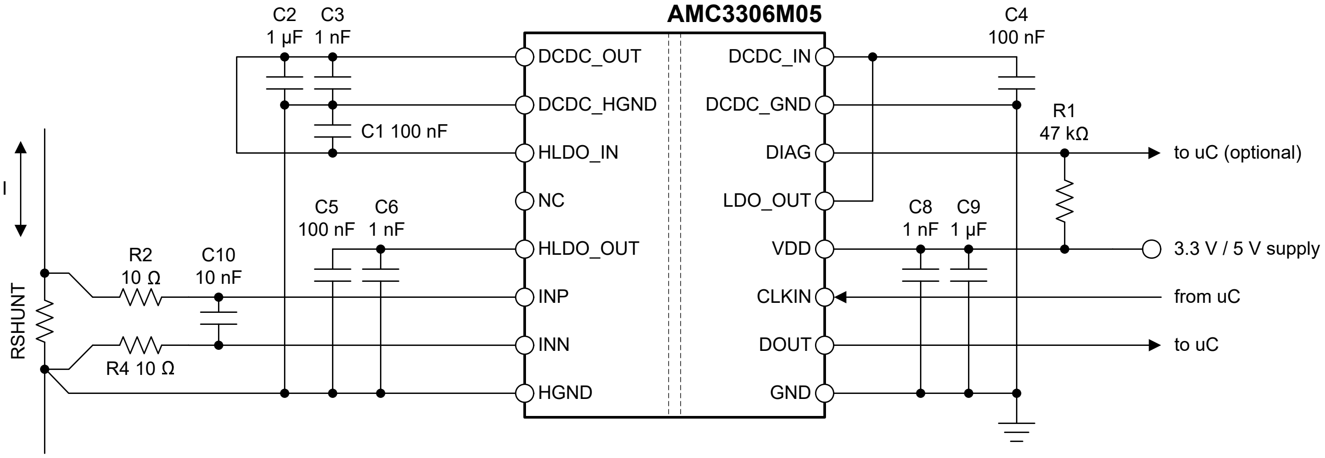


Figure 9-1. Decoupling the AMC3306M05

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. MLCC capacitors typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

Table 9-1 lists components suitable for use with the AMC3306M05. This list is not exhaustive. Other components may exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC3306M05.

Table 9-1. Recommended External Components

DESCRIPTION		PART NUMBER	MANUFACTURER	SIZE (EIA, L x W)
VDD				
C8	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm
C9	1 µF ± 10%, X7R, 25 V	12063C105KAT2A	AVX	1206, 3.2 mm x 1.6 mm
DC/DC CONVERTER				
C4	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C3	1 nF ± 10%, X7R, 50 V	C0603C102K5RACTU	Kemet	0603, 1.6 mm x 0.8 mm
C2	1 µF ± 10%, X7R, 25 V	CGA3E1X7R1E105K080AC	TDK	0603, 1.6 mm x 0.8 mm
HLDO				
C1	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C5	100 nF ± 5%, NP0, 50 V	C3216NP01H104J160AA	TDK	1206, 3.2 mm x 1.6 mm
C6	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm

10 Layout

10.1 Layout Guidelines

Figure 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC3306M05 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC3306M05 and keep the layout of both connections symmetrical.

This layout is used on the AMC3306M05 EVM and supports CISPR-11 compliant electromagnetic radiation levels.

10.2 Layout Example

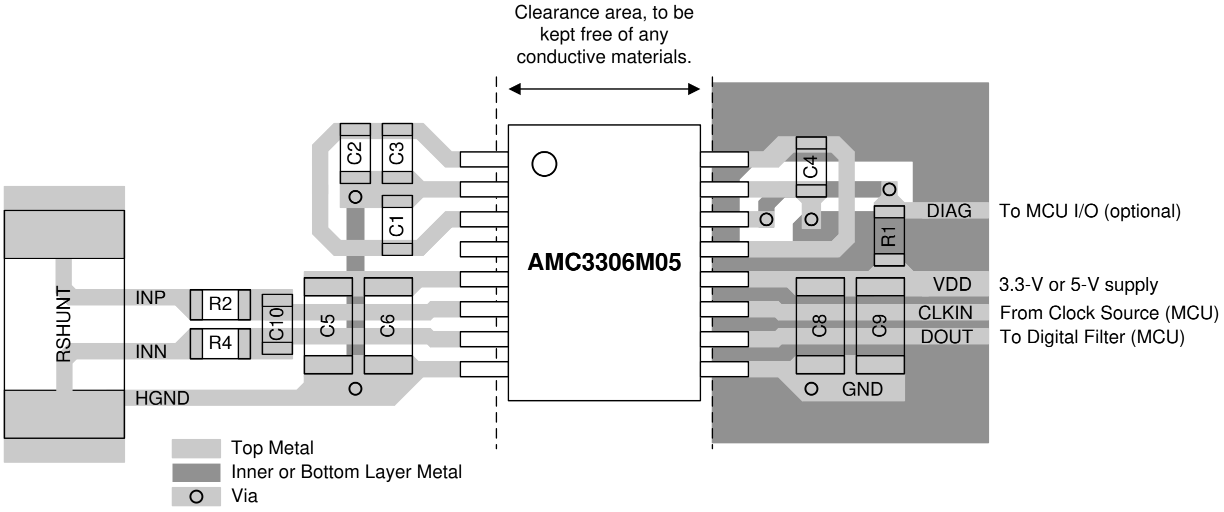


Figure 10-1. Recommended Layout of the AMC3306M05

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

11.1.1.1 Isolation Glossary

See the *Isolation Glossary*

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *Delta Sigma Modulator Filter Calculator* design tool

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC3306M05DWE	Active	Production	SOIC (DWE) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3306M05
AMC3306M05DWE.A	Active	Production	SOIC (DWE) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3306M05
AMC3306M05DWE.B	Active	Production	SOIC (DWE) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3306M05
AMC3306M05DWER	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3306M05
AMC3306M05DWER.A	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3306M05
AMC3306M05DWER.B	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3306M05
AMC3306M05DWERG4.A	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3306M05
AMC3306M05DWERG4.B	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3306M05

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF AMC3306M05 :

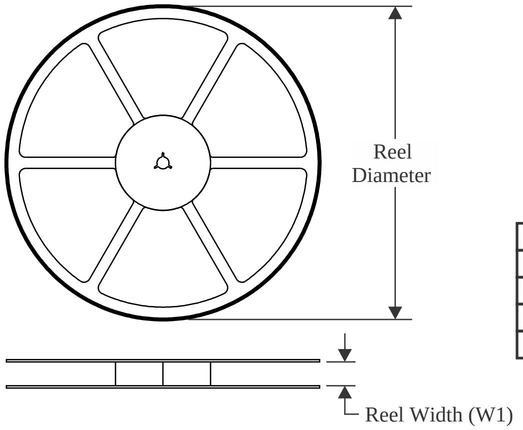
- Automotive : AMC3306M05-Q1

NOTE: Qualified Version Definitions:

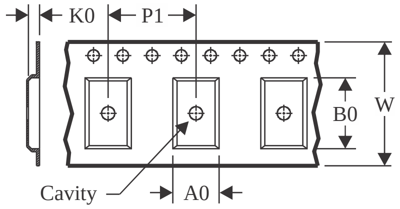
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

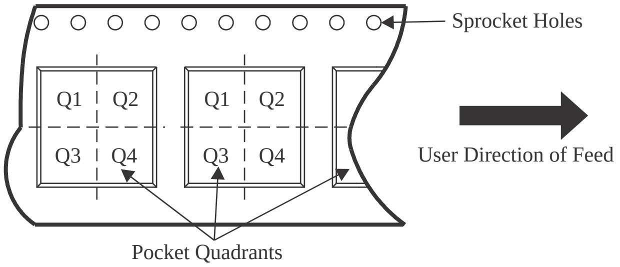


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

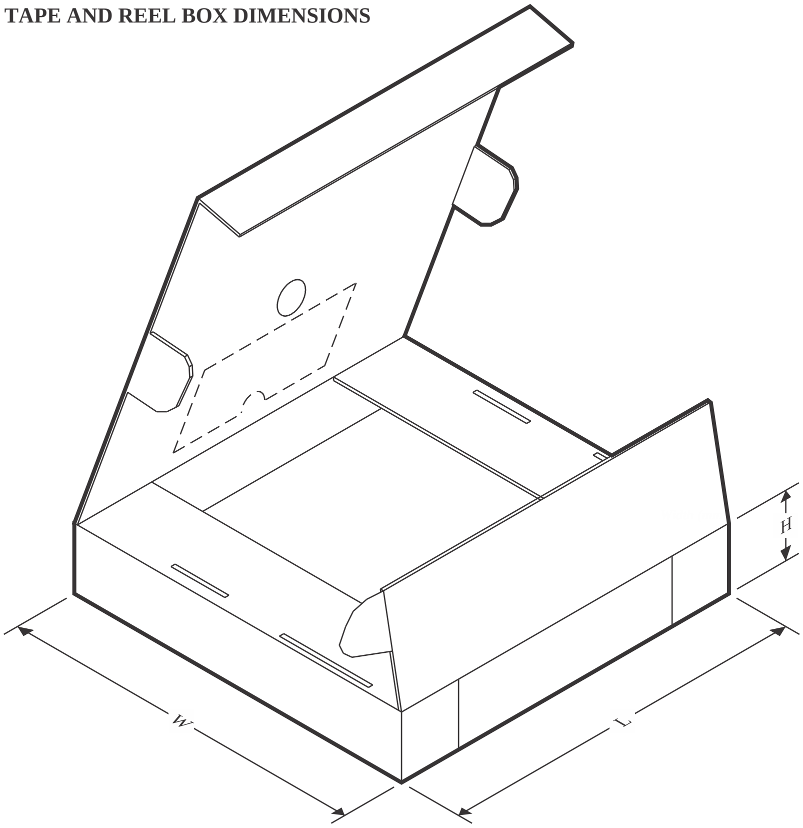
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC3306M05DWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

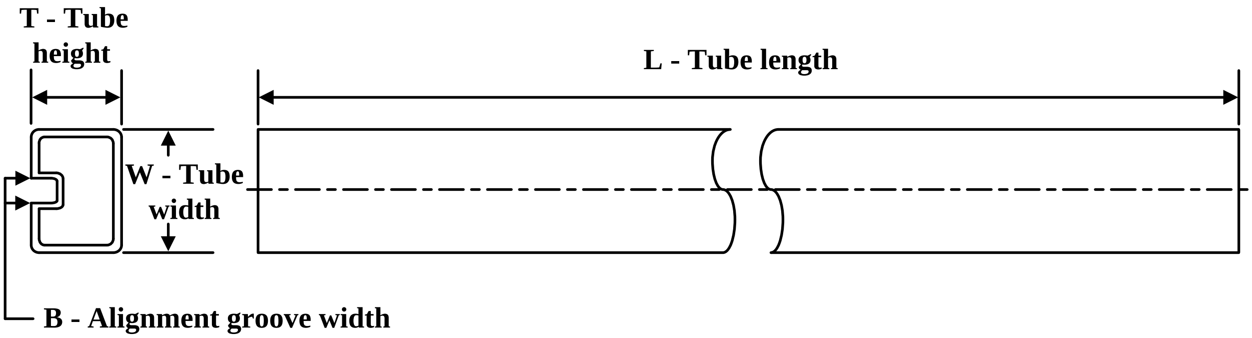
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

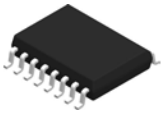
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC3306M05DWER	SOIC	DWE	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC3306M05DWE	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6
AMC3306M05DWE.A	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6
AMC3306M05DWE.B	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6

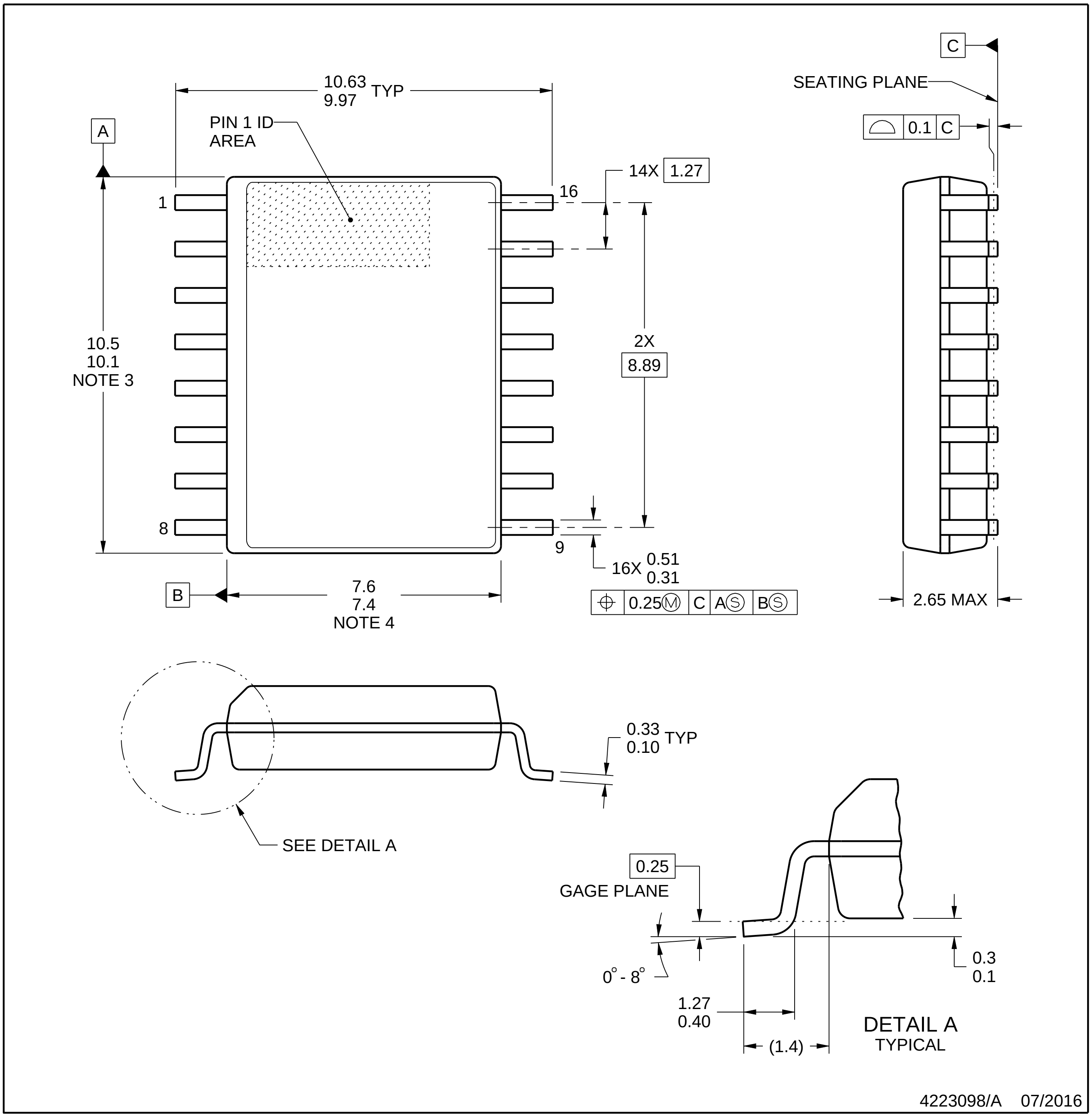


PACKAGE OUTLINE

DWE0016A

SOIC - 2.65 mm max height

SOIC



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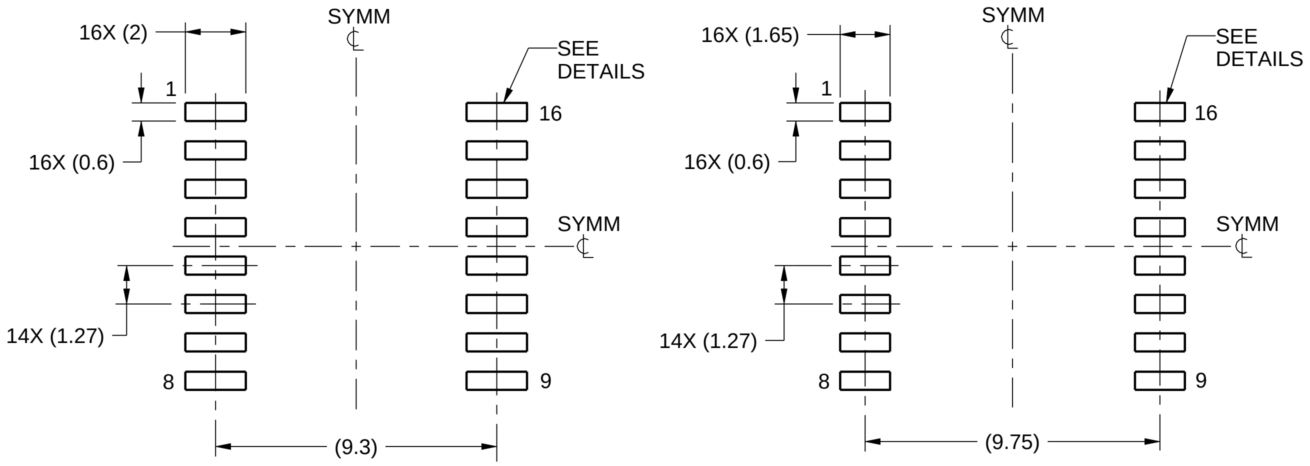
NOTES:

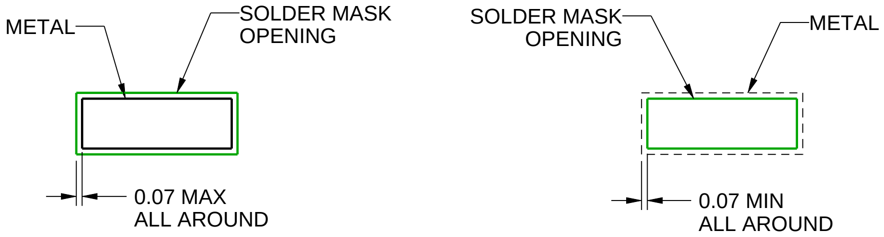
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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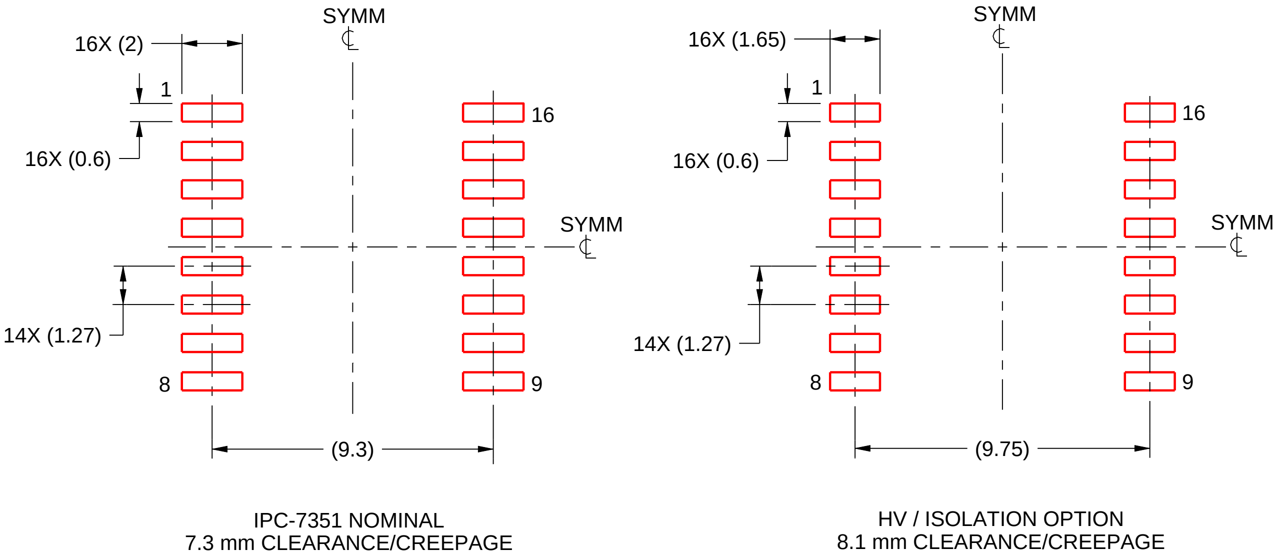
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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