SCANSTA112 7-Port Multidrop IEEE 1149.1 (JTAG) Multiplexer

Check for Samples: SCANSTA112

FEATURES

- **True IEEE 1149.1 Hierarchical and Multidrop Addressable Capability**
- **The 8 Address Inputs Support up to 249 Unique Slot Addresses, an Interrogation Address, Broadcast Address, and 4 Multi-Cast Group Addresses (Address 000000 is Reserved)**
- **7 IEEE 1149.1-Compatible Configurable Local Scan Ports**
- **Bi-directional Backplane and LSP_0 Ports are Interchangeable Slave Ports**
- **Capable of Ignoring $\overline{TRST}$ of the Backplane Port when it Becomes the Slave.**
- **Stitcher Mode Bypasses Level 1 and 2 Protocols**
- **Mode $Register_0$ Allows Local TAPs to be Bypassed, Selected for Insertion into the Scan Chain Individually, or Serially in Groups of Two or Three**
- **Transparent Mode can be Enabled with a Single Instruction to Conveniently Buffer the Backplane IEEE 1149.1 Pins to Those on a Single Local Scan Port**
- **General Purpose Local Port Pass Through Bits are Useful for Delivering Write Pulses for Flash Programming or Monitoring Device Status.**
- **Known Power-Up State**
- **$\overline{TRST}$ on all Local Scan Ports**
- **32-bit TCK Counter**
- **16-bit LFSR Signature Compactor**
- **Local TAPs can Become TRI-STATE via the $\overline{OE}$ Input to Allow an Alternate Test Master to Take Control of the Local TAPs (LSP_{0-3} have a TRI-STATE Notification Output)**
- **3.0-3.6V V_{CC} Supply Operation**
- **Supports Live Insertion/Withdrawal**

DESCRIPTION

The SCANSTA112 extends the IEEE Std. 1149.1 test bus into a multidrop test bus environment. The advantage of a multidrop approach over a single serial scan chain is improved test throughput and the ability to remove a board from the system and retain test access to the remaining modules. Each SCANSTA112 supports up to 7 local IEEE1149.1 scan chains which can be accessed individually or combined serially.

Addressing is accomplished by loading the instruction register with a value matching that of the Slot inputs. Backplane and inter-board testing can easily be accomplished by parking the local TAP Controllers in one of the stable TAP Controller states via a Park instruction. The 32-bit TCK counter enables built in self test operations to be performed on one port while other scan chains are simultaneously tested.

The STA112 has a unique feature in that the backplane port and the LSP0 port are bidirectional. They can be configured to alternatively act as the master or slave port so an alternate test master can take control of the entire scan chain network from the LSP0 port while the backplane port becomes a slave.

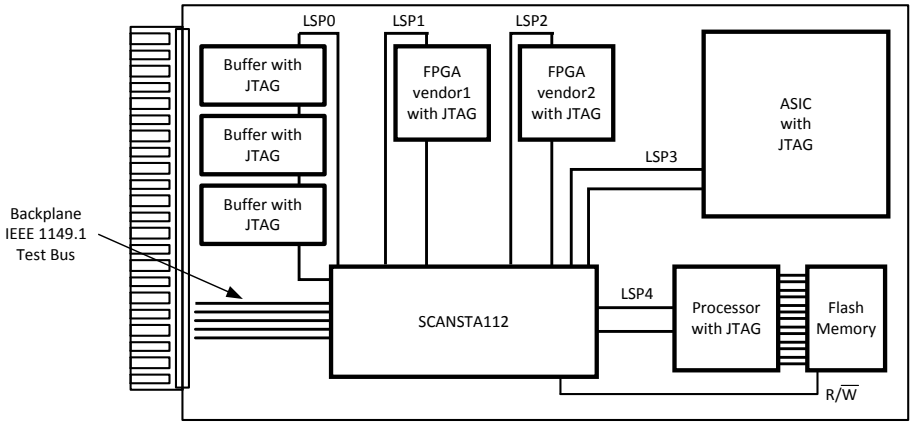


Figure 1. Typical use of SCANSTA112 for board-level management of multiple scan chains.

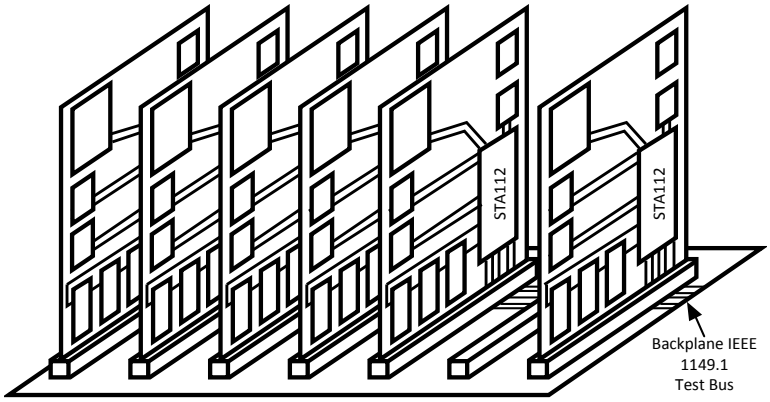


Figure 2. Example of SCANSTA112 in a multidrop addressable backplane.

Introduction

The SCANSTA112 is the third device in a series that enable multi-drop address and multiplexing of IEEE-1149.1 scan chains. The SCANSTA112 is a superset of its predecessors - the SCANPSC110 and the SCANSTA111. The STA112 has all features and functionality of these two previous devices.

The STA112 is essentially a support device for the IEEE 1149.1 standard. It is primarily used to partition scan chains into managable sizes, or to isolate specific devices onto a seperate chain (Figure 1). The benefits of multiple scan chains are improved fault isolation, faster test times, faster programiing times, and smaller vector sets.

In addition to scan chain partitioning, the device is also addressable for use in a multidrop backplane environment (Figure 2). In this configuration, multiple IEEE-1149.1 accessible cards with an STA112 on board can utilize the same backplane test bus for system-level IEEE-1149.1 access. This approach facilitates a system-wide commitment to structural test and programming throughout the entire system life sycle.

Architecture

Figure 3 shows the basic architecture of the 'STA112. The device's major functional blocks are illustrated here.

The TAP Controller, a 16-state state machine, is the central control for the device. The instruction register and various test data registers can be scanned to exercise the various functions of the 'STA112 (these registers behave as defined in IEEE Std. 1149.1).

The 'STA112 selection controller provides the functionality that allows the 1149.1 protocol to be used in a multi-drop environment. It primarily compares the address input to the slot identification and enables the 'STA112 for subsequent scan operations.

The Local Scan Port Network (LSPN) contains multiplexing logic used to select different port configurations. The LSPN control block contains the Local Scan Port Controllers (LSPC) for each Local Scan Port (LSP_0, LSP_1 ... LSP_n). This control block receives input from the 'STA112 instruction register, mode registers, and the TAP controller. Each local port contains all four boundary scan signals needed to interface with the local TAPs plus the optional Test Reset signal ($\overline{TRST}$).

The TDI/TDO Crossover Master/Slave logic is used to define the bidirectional B0 and B1 ports in a Master/Slave configuration.

Block Diagram

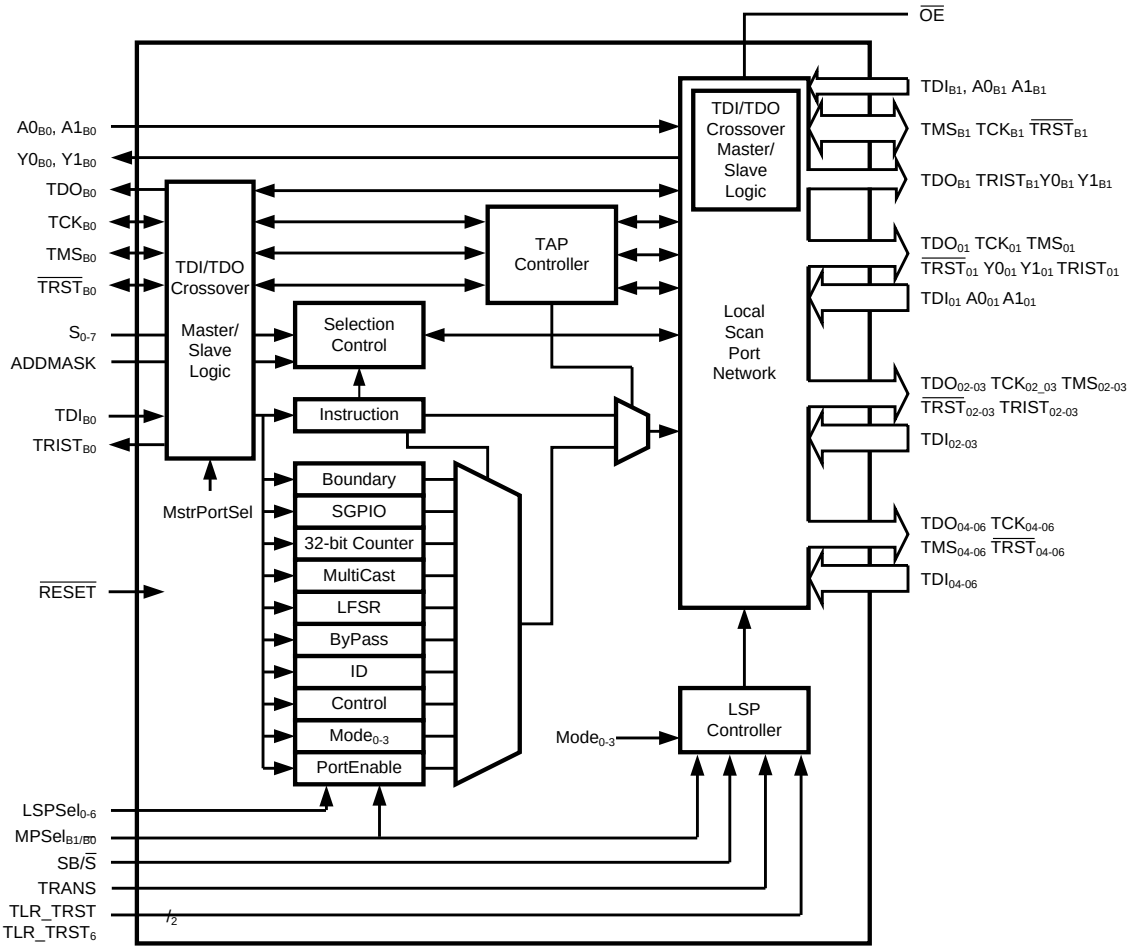


Figure 3. SCANSTA112 Block Diagram

Connection Diagrams

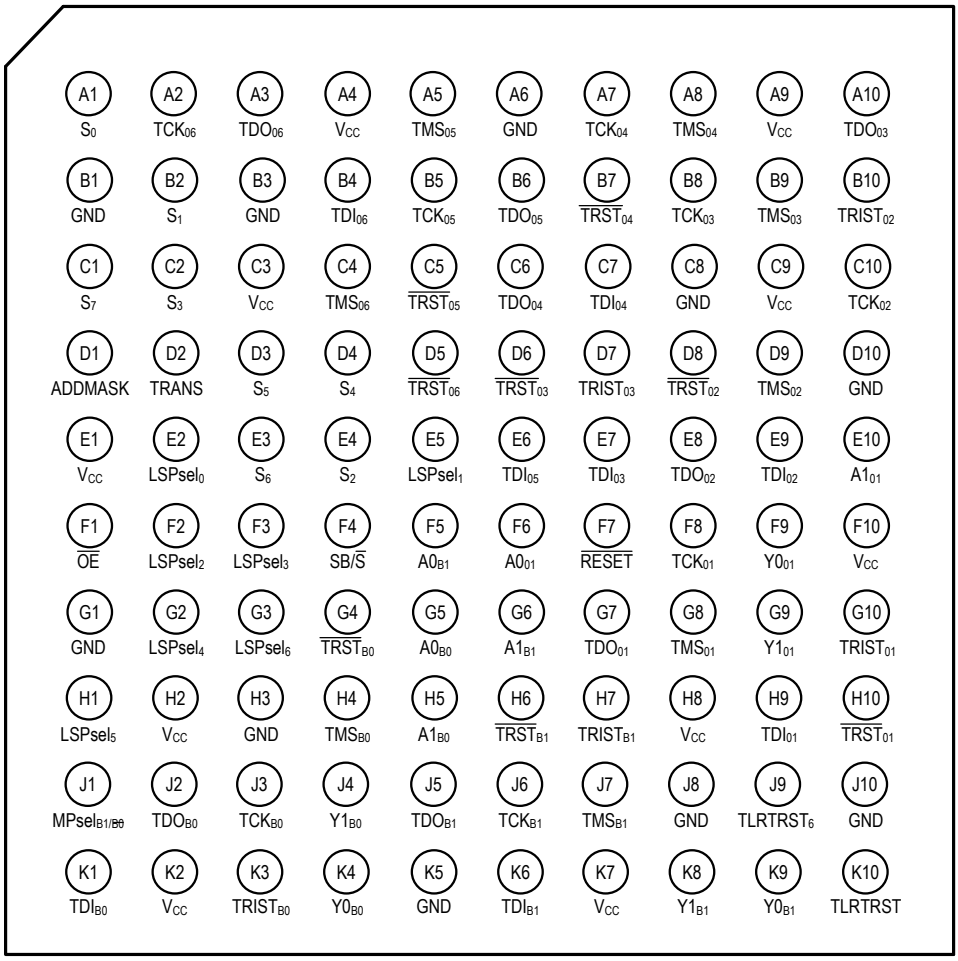


Figure 4. (NFBGA Top view)

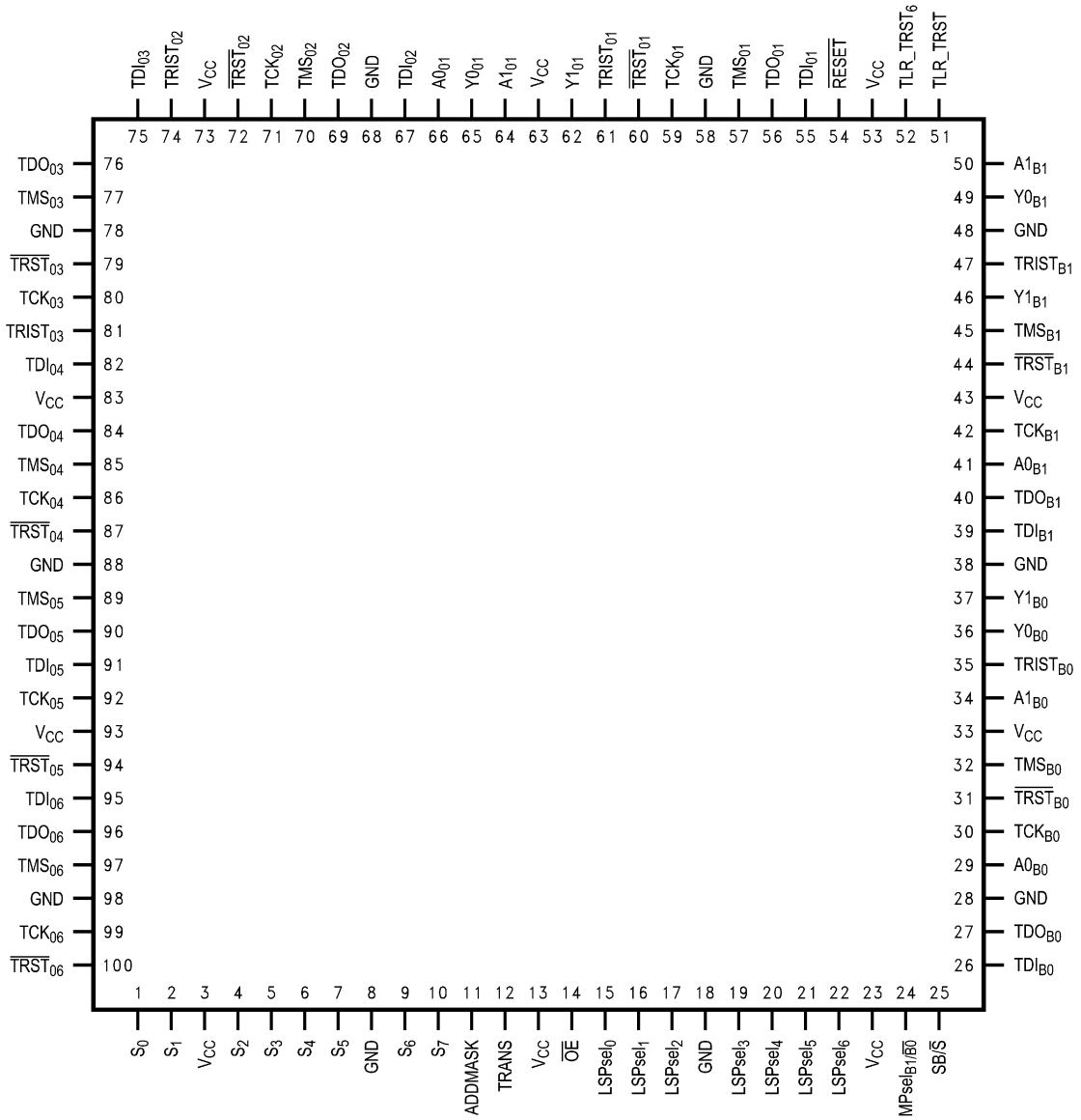


Figure 5. TQFP pinout

PIN DESCRIPTIONS

Pin Name	No. Pins	I/O	Description
VCC	10	N/A	Power
GND	10	N/A	Ground
$\overline{\text{RESET}}$	1	I	RESET Input: will force a reset of the device regardless of the current state.
ADDMASK	1	I	ADDRESS MASK input: Allows masking of lower slot input pins.
$\text{MPsel}_{B1/\overline{B0}}$	1	I	MASTER PORT SELECTION: Controls selection of LSP_{B0} or LSP_{B1} as the backplane port. The unselected port becomes LSP_{00}. A value of "0" will select LSP_{B0} as the master port.
SB/$\overline{\text{S}}$	1	I	Selects ScanBridge or Stitcher Mode.
$\text{LSPsel}_{(0-6)}$	7	I	In Stitcher Mode these inputs define which LSP's are to be included in the scan chain
TRANS	1	I	Transparent Mode enable input: The value of this pin is loaded into the TRANSENABLE bit of the control register at power-up. This value is used to control the presence of registers and pad-bits in the scan chain while in the stitcher mode.
TLR_TRST	1	I	Sets the driven value of $\overline{\text{TRST}}_{0-5}$ when LSP TAPs are in TLR and the device is not being reset. During $\overline{\text{RESET}}$ = "0" or $\overline{\text{TRST}}_B$ = "0" (IgnoreReset = "0") $\overline{\text{TRST}}_n$ = "0". This pin is to be tied low to match the function of the SCANSTA111
TLR_TRST_6	1	I	This pin affects $\overline{\text{TRST}}$ of LSP_6 only. This pin is to be tied low to match the function of the SCANSTA111
TDI_{B0}, TDI_{B1}	2	I	BACKPLANE TEST DATA INPUT: All backplane scan data is supplied to the 'STA112 through this input pin. $\text{MPsel}_{B1/\overline{B0}}$ determines which port is the master backplane port and which is LSP_{00}. This input has a 25KΩ internal pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (V_{DD} floating), this input appears to be a capacitive load to ground (1). When V_{DD} = 0V (i.e.; not floating but tied to V_{SS}) this input appears to be a capacitive load with the pull-up to ground.
TMS_{B0}, TMS_{B1}	2	I/O	BACKPLANE TEST MODE SELECT: Controls sequencing through the TAP Controller of the 'STA112. Also controls sequencing of the TAPs which are on the local scan chains. $\text{MPsel}_{B1/\overline{B0}}$ determines which port is the master backplane port and which is LSP_{00}. This bidirectional TRI-STATE pin has 24mA of drive current, with a 25KΩ internal pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (V_{DD} floating), this input appears to be a capacitive load to ground (1). When V_{DD} = 0V (i.e.; not floating but tied to V_{SS}) this input appears to be a capacitive load with the pull-up to ground.
TDO_{B0}, TDO_{B1}	2	I/O	BACKPLANE TEST DATA OUTPUT: This output drives test data from the 'STA112 and the local TAPs, back toward the scan master controller. This bidirectional TRI-STATE pin has 12mA of drive current. $\text{MPsel}_{B1/\overline{B0}}$ determines which port is the master backplane port and which is LSP_{00}. Output is sampled during interrogation addressing. When the device is power-off (V_{DD} = 0V or floating), this output appears to be a capacitive load (1).
TCK_{B0}, TCK_{B1}	2	I/O	TEST CLOCK INPUT FROM THE BACKPLANE: This is the master clock signal that controls all scan operations of the 'STA112 and of the local scan ports. $\text{MPsel}_{B1/\overline{B0}}$ determines which port is the master backplane port and which is LSP_{00}. These bidirectional TRI-STATE pins have 24mA of drive current with hysterisis. This input has no pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (V_{DD} floating), this input appears to be a capacitive load to ground (1). When V_{DD} = 0V (i.e.; not floating but tied to V_{SS}) this input appears to be a capacitive load to ground.
$\overline{\text{TRST}}_{B0}$, $\overline{\text{TRST}}_{B1}$	2	I/O	TEST RESET: An asynchronous reset signal (active low) which initializes the 'STA112 logic. $\text{MPsel}_{B1/\overline{B0}}$ determines which port is the master backplane port and which is LSP_{00}. This bidirectional TRI-STATE pin has 24mA of drive current, with a 25KΩ internal pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (V_{DD} floating), this pin appears to be a capacitive load to ground (1). When V_{DD} = 0V (i.e.; not floating but tied to V_{SS}) this input appears to be a capacitive load with the pull-up to ground.
TRIST_{B0}, TRIST_{B1}, $\text{TRIST}_{(01-03)}$	5	O	TRI-STATE NOTIFICATION OUTPUT: This signal is asserted high when the associated TDO is TRI-STATEd. Associated means TRIST_{B0} is for TDO_{B0}, TRIST_{01} is for TDO_{01}, etc. This output has 12mA of drive current.
A0_{B0}, A1_{B0}, A0_{B1}, A1_{B1}	4	I	BACKPLANE PASS-THROUGH INPUT: A general purpose input which is driven to the Y_n of a single selected LSP. (Not available when multiple LSPs are selected). This input has a 25KΩ internal pull-up resistor. $\text{MPsel}_{B1/\overline{B0}}$ determines which port is the master backplane port and which is LSP_{00}.
Y0_{B0}, Y1_{B0}, Y0_{B1}, Y1_{B1}	4	O	BACKPLANE PASS-THROUGH OUTPUT: A general purpose output which is driven from the A_n of a single selected LSP. (Not available when multiple LSPs are selected). This TRI-STATE output has 12mA of drive current. $\text{MPsel}_{B1/\overline{B0}}$ determines which port is the master backplane port and which is LSP_{00}.

(1) Refer to the IBIS model on our website for I/O characteristics.

PIN DESCRIPTIONS (continued)

Pin Name	No. Pins	I/O	Description
$S_{(0-7)}$	8	I	SLOT IDENTIFICATION: The configuration of these pins is used to identify (assign a unique address to) each 'STA112 on the system backplane
$\overline{OE}$	1	I	OUTPUT ENABLE for the Local Scan Ports, active low. When high, this active-low control signal TRI-STATEs all local scan ports on the 'STA112, to enable an alternate resource to access one or more of the local scan chains.
$TDO_{(01-06)}$	6	O	TEST DATA OUTPUTS: Individual output for each of the local scan ports . These TRI-STATE outputs have 12mA of drive current.
$TDI_{(01-06)}$	6	I	TEST DATA INPUTS: Individual scan data input for each of the local scan ports. This input has a 25KΩ internal pull-up resistor.
$TMS_{(01-06)}$	6	O	TEST MODE SELECT OUTPUTS: Individual output for each of the local scan ports. TMS_n does not provide a pull-up resistor (which is assumed to be present on a connected TMS input, per the IEEE 1149.1 requirement) . These TRI-STATE outputs have 24mA of drive current.
$TCK_{(01-06)}$	6	O	LOCAL TEST CLOCK OUTPUTS: Individual output for each of the local scan ports. These are buffered versions of TCK_B . These TRI-STATE outputs have 24mA of drive current.
$\overline{TRST}_{(01-06)}$	6	O	LOCAL TEST RESETS: A gated version of $\overline{TRST}_B$. These TRI-STATE outputs have 24mA of drive current.
$A0_{01}$, $A1_{01}$	2	I	LOCAL PASS-THROUGH INPUTS: General purpose inputs which can be driven to the backplane pin Y_B. (Only on LSP_0 and LSP_1. Only available when a single LSP is selected) . These inputs have a 25KΩ internal pull-up resistor.
$Y0_{01}$, $Y1_{01}$	2	O	LOCAL PASS-THROUGH OUTPUT: General purpose outputs which can be driven from the backplane pin A_B. (Only on LSP_0 and LSP_1. Only available when a single LSP is selected) . These TRI-STATE outputs have 12mA of drive current.

APPLICATION OVERVIEW

ADDRESSING SCHEME

The SCANSTA112 architecture extends the functionality of the IEEE 1149.1 Standard by supplementing that protocol with an addressing scheme which allows a test controller to communicate with specific 'STA112s within a network of 'STA112s. That network can include both multi-drop and hierarchical connectivity. In effect, the 'STA112 architecture allows a test controller to dynamically select specific portions of such a network for participation in scan operations. This allows a complex system to be partitioned into smaller blocks for testing purposes. The 'STA112 provides two levels of test-network partitioning capability. First, a test controller can select individual 'STA112s, specific sets of 'STA112s (multi-cast groups), or all 'STA112s (broadcast). This 'STA112-selection process is supported by a Level-1 communication protocol. Second, within each selected 'STA112, a test controller can select one or more of the chip's seven local scan-ports. That is, individual local ports can be selected for inclusion in the (single) scan-chain which a 'STA112 presents to the test controller. This mechanism allows a controller to select specific scan-chains within the overall scan network. The port-selection process is supported by a Level-2 protocol.

HIERARCHICAL SUPPORT

Multiple SCANSTA112's can be used to assemble a hierarchical boundary-scan tree. In such a configuration, the system tester can configure the local ports of a set of 'STA112s so as to connect a specific set of local scan-chains to the active scan chain. Using this capability, the tester can selectively communicate with specific portions of a target system. The tester's scan port is connected to the backplane scan port of a root layer of 'STA112s, each of which can be selected using multi-drop addressing. A second tier of 'STA112s can be connected to this root layer, by connecting a local port (LSP) of a root-layer 'STA112 to the backplane port of a second-tier 'STA112. This process can be continued to construct a multi-level scan hierarchy. 'STA112 local ports which are not cascaded into higher-level 'STA112s can be thought of as the terminal leaves of a scan tree. The test master can select one or more target leaves by selecting and configuring the local ports of an appropriate set of 'STA112s in the test tree.

STANDARD SCANBRIDGE MODE

ScanBridge mode refers to functionality and protocol that has been used since the introduction of the PSC110 in 1993. This functionality consists of a multidrop addressable IEEE1149.1 switch. This enables one (or more) device to be selected from many that are connected to a parallel IEEE1149.1 bus or backplane. The second function that ScanBridge mode accomplishes is to act as a mux for multiple IEEE1149.1 local scan chains. The Local Scan Ports (LSP) of the device creates a connection between one or more of the local scan chains to the backplane bus.

To accomplish this functionality the ScanBridge has two levels of protocol and an operational mode. Level 1 protocol refers to the required actions to address/select the desired ScanBridge. Level 2 protocol is required to configuring the mux'ing function and enable the connection (UNPARK) between the local scan chain and the backplane bus via an LSP. Upon completion of level 1 and 2 protocols the ScanBridge is prepared for its operational mode. This is where scan vectors are moved from the backplane bus to the desired local scan chain(s).

STITCHER MODE

Stitcher Mode is a method of skipping level 1 and 2 protocol of the ScanBridge mode of operation. This is accomplished via external pins. When in stitcher mode the SCANSTA112 will go directly to the operational mode.

TRANSPARENT MODE

Transparent mode refers to a condition of operation in which there are no pad-bits or SCANSTA112 registers in the scan chain. The Transparent mode of operation is available in both ScanBridge and Stitcher modes. Only the activation method differs. Once transparent mode has been activated there is no difference in operation. Transparent mode allows for the use of vectors that have been generated for a chain where these bits were not included.

Check with your ATPG tool vendor to ensure support of these features.

For details regarding the internal operation of the SCANSTA112 device, refer to applications note AN-1259(SNLA055) SCANSTA112 Designers Reference.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage (V_{CC})		−0.3V to +4.0V
DC Input Diode Current (I_{IK}) V_I = −0.5V		−20 mA
DC Input Voltage (V_I)		−0.5V to +3.9V
DC Output Diode Current (I_{OK}) V_O = −0.5V		−20 mA
DC Output Voltage (V_O)		−0.3V to +3.9V
DC Output Source/Sink Current (I_O)		±50 mA
DC V_{CC} or Ground Current per Output Pin		±50 mA
DC Latchup Source or Sink Current		±300 mA
Junction Temperature (Plastic)		+150°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Solder, 4sec)	100L NFBGA	220°C
	100L TQFP	220°C
Max Package Power Capacity @ 25°C	100L NFBGA	3.57W
	100L TQFP	2.11W
Thermal Resistance (θ_{JA})	100L NFBGA	35°C/W
	100L TQFP	59.1°C/W
Package Derating above +25°C	100L NFBGA	28.57mW/°C
	100L TQFP	16.92mW/°C
ESD Last Passing Voltage (HBM Min)		2500V

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. TI does not recommend operation of SCAN STA products outside of recommended operation conditions.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC}) 'STA112	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A) Industrial	−40°C to +85°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating supply voltage and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Minimum High Input Voltage	V_{OUT} = 0.1V or V_{CC} −0.1V	2.1		V
V_{IL}	Maximum Low Input Voltage	V_{OUT} = 0.1V or V_{CC} −0.1V		0.8	V
V_{OH}	Minimum High Output Voltage All Outputs and I/O Pins	I_{OUT} = −100 µA V_{IN} = V_{IH} or V_{IL}	V_{CC} - 0.2v		V
V_{OH}	Minimum High Output Voltage TDO_{B0}, TDO_{B1}, $TRIST_{B0}$, $TRIST_{B1}$, $Y0_{B0}$, $Y1_{B0}$, $Y0_{B1}$, $Y1_{B1}$, $TDO_{(01-06)}$, $Y0_{01}$, $Y1_{01}$, $TRIST_{(01-03)}$	I_{OUT} = −12 mA All Outputs Loaded	2.4		V
V_{OH}	Minimum High Output Voltage TMS_{B0}, TMS_{B1}, TCK_{B0}, TCK_{B1}, $\overline{TRST}_{B0}$, $\overline{TRST}_{B1}$, $TMS_{(01-06)}$, $TCK_{(01-06)}$, $\overline{TRST}_{(01-06)}$	I_{OUT} = −24mA	2.2		V
V_{OL}	Maximum Low Output Voltage All Outputs and I/O Pins	I_{OUT} = +100 µA V_{IN} = V_{IH} or V_{IL}		0.2	V

DC ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Maximum Low Output Voltage TDO_{B0}, TDO_{B1}, $TRIST_{B0}$, $TRIST_{B1}$, $Y0_{B0}$, $Y1_{B0}$, $Y0_{B1}$, $Y1_{B1}$, $TDO_{(01-06)}$, $Y0_{01}$, $Y1_{01}$, $TRIST_{(01-03)}$	I_{OUT} = +12 mA		0.4	V
V_{OL}	Maximum Low Output Voltage TMS_{B0}, TMS_{B1}, TCK_{B0}, TCK_{B1}, $\overline{TRST}_{B0}$, $\overline{TRST}_{B1}$, $TMS_{(01-06)}$, $TCK_{(01-06)}$, $\overline{TRST}_{(01-06)}$	I_{OUT} = +24mA		0.55	V
VIKL	Maximum Input Clamp Diode Voltage	IIK = -18mA		-1.2	V
I_{IN}	Maximum Input Leakage Current (non-resistor input pins)	V_{IN} = V_{CC} or GND		±5.0	µA
I_{ILR}	Input Current Low (Input and I/O pins with pull-up resistors: TDI_{B0}, TDI_{B1}, TMS_{B0}, TMS_{B1}, $\overline{TRST}_{B0}$, $\overline{TRST}_{B1}$, $A0_{B0}$, $A1_{B0}$, $A0_{B1}$, $A1_{B1}$, $TDI_{(01-06)}$, $A0_{01}$, $A1_{01}$)	V_{IN} = GND	-45	-200	µA
I_{IH}	Input High Current (Input and I/O pins with pull-up resistors: TDI_{B0}, TDI_{B1}, TMS_{B0}, TMS_{B1}, $\overline{TRST}_{B0}$, $\overline{TRST}_{B1}$, $A0_{B0}$, $A1_{B0}$, $A0_{B1}$, $A1_{B1}$, $TDI_{(01-06)}$, $A0_{01}$, $A1_{01}$)	V_{IN} = V_{CC}		5.0	µA
I_{OFF}	Power-off Leakage Current Outputs and I/O pins without pull-up resistors	V_{CC} = 0V, V_{IN} = 3.6V(1)		±5.0	µA
	Outputs and I/O pins with pull-up resistors			±200	µA
I_{OZ}	Maximum TRI-STATE Leakage Current Outputs and I/O pins without pull-up resistors			±5.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND		3.8	mA
I_{CCD}	Maximum Dynamic Supply Current	V_{IN} = V_{CC} or GND, Input Freq = 25MHz		68	mA

(1) Specified by equivalent test method.

AC ELECTRICAL CHARACTERISTICS: SCAN BRIDGE MODE

Over recommended operating supply voltage and temperature ranges unless otherwise specified(1).

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B0} to TDO_{B0} or TDO_{B1}		8.5	13.5	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B1} to TDO_{B0} or TDO_{B1}		8.5	14.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B0} to $TDO_{(01-06)}$		7.5	12.5	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B1} to $TDO_{(01-06)}$		7.5	13.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TMS_{B0} to TMS_{B1}		8.0	12.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TMS_{B1} to TMS_{B0}		8.0	12.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TMS_{B0} to $TMS_{(01-06)}$		8.0	12.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TMS_{B1} to $TMS_{(01-06)}$		8.0	12.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B0} to TCK_{B1}		8.0	12.0	ns

(1) R_L = 500Ω to GND, C_L = 50pF to GND, t_R/t_F = 2.5ns, Frequency = 25MHz, V_M = 1.5V

AC ELECTRICAL CHARACTERISTICS: SCAN BRIDGE MODE (continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified(1).

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B1} to TCK_{B0}		8.0	12.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B0} to $TCK_{(01-06)}$		7.5	12.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B1} to $TCK_{(01-06)}$		7.5	12.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B0} to $\overline{TRST}_{B1}$		11.5	18.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B1} to $\overline{TRST}_{B0}$		11.5	18.0	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B0} to $\overline{TRST}_{(01-06)}$		12.0	18.5	ns
t_{PHL}, t_{PLH}	Propagation Delay TCK_{B1} to $\overline{TRST}_{(01-06)}$		12.0	18.5	ns
t_{PHL}	Propagation Delay TCK_{Bn} to $TRIST_{Bn}$		8.5	12.5	ns
t_{PHL}	Propagation Delay TCK_{Bn} to $TRIST_{(01-03)}$		8.0	12.0	ns
t_{PZL}, t_{PZH}	Propagation Delay TCK_{Bn} to TDO_{Bn} or $TDO_{(01-06)}$		9.0	14.5	ns
t_{PHL}, t_{PLH}	Propagation Delay An to Yn		6.0	9.0	ns

AC TIMING CHARACTERISTICS: SCAN BRIDGE MODE

Over recommended operating supply voltage and temperature ranges unless otherwise specified(1)(2).

Symbol	Parameter	Conditions	Min	Max	Units
t_S	Setup Time TMS_{Bn} to TCK_{Bn}		2.5		ns
t_H	Hold Time TMS_{Bn} to TCK_{Bn}		1.5		ns
t_S	Setup Time TDI_{Bn} to TCK_{Bn}		3.0		ns
t_H	Hold Time TDI_{Bn} to TCK_{Bn}		2.0		ns
t_S	Setup Time $TDI_{(01-06)}$ to TCK_{Bn}		1.0		ns
t_H	Hold Time $TDI_{(01-06)}$ to TCK_{Bn}		3.5		ns

(1) Specified by Design (GBD) by statistical analysis
(2) R_L = 500Ω to GND, C_L = 50pF to GND, t_R/t_F = 2.5ns, Frequency = 25MHz, V_M = 1.5V

AC TIMING CHARACTERISTICS: SCAN BRIDGE MODE (continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified(1)(2).

Symbol	Parameter	Conditions	Min	Max	Units
t_{REC}	Recovery Time TCK_{Bn} from $\overline{TRST}_{Bn}$		1.0		ns
t_W	Clock Pulse Width TCK_{Bn}(H or L)	t_R/t_F = 1.0ns	10.0		ns
t_WL	Reset Pulse Width $\overline{TRST}_{Bn}$(L)	t_R/t_F = 1.0ns	2.5		ns
F_{MAX}	Maximum Clock Frequency(3)	t_R/t_F = 1.0ns	25		MHz

(3) When sending vectors one-way to a target device on an LSP (such as in FPGA/PLD configuration/programming), the clock frequency may be increased above this specification. In Scan Mode (expecting to capture returning data at the LSP), the F_{MAX} must be limited to the above specification.

AC ELECTRICAL CHARACTERISTICS: STITCHER TRANSPARENT MODE

Over recommended operating supply voltage and temperature ranges unless otherwise specified (1).

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay TDI_{B0} to TDO_{B1}, TDI_{B1} to TDO_{B0}			12.5	ns
t_{PHL}, t_{PLH}	Propagation Delay TDI_{B0} to TDO_{01}, TDI_{B1} to TDO_{01}			12.5	ns
t_{PHL}, t_{PLH}	Propagation Delay TDI_{LSPn} to TDO_{LSPn+1}			12.5	ns
t_{PHL}, t_{PLH}	Propagation Delay TMS_{B0} to TMS_{B1}, TMS_{B1} to TMS_{B0}			12.5	ns
t_{PHL}, t_{PLH}	Propagation Delay TMS_{B0} to $TMS_{(01-06)}$, TMS_{B1} to $TMS_{(01-06)}$			12.5	ns
t_{PHL}, t_{PLH}	Propagation Delay $\overline{TRST}_{B0}$ to $\overline{TRST}_{B1}$, $\overline{TRST}_{B1}$ to $\overline{TRST}_{B0}$			12.5	ns
t_{PHL}, t_{PLH}	Propagation Delay $\overline{TRST}_{B0}$ to $\overline{TRST}_{(01-06)}$, $\overline{TRST}_{B1}$ to $\overline{TRST}_{(01-06)}$			12.5	ns

(1) R_L = 500Ω to GND, C_L = 50pF to GND, t_R/t_F = 2.5ns, Frequency = 25MHz, V_M = 1.5V

TEST CIRCUIT DIAGRAMS

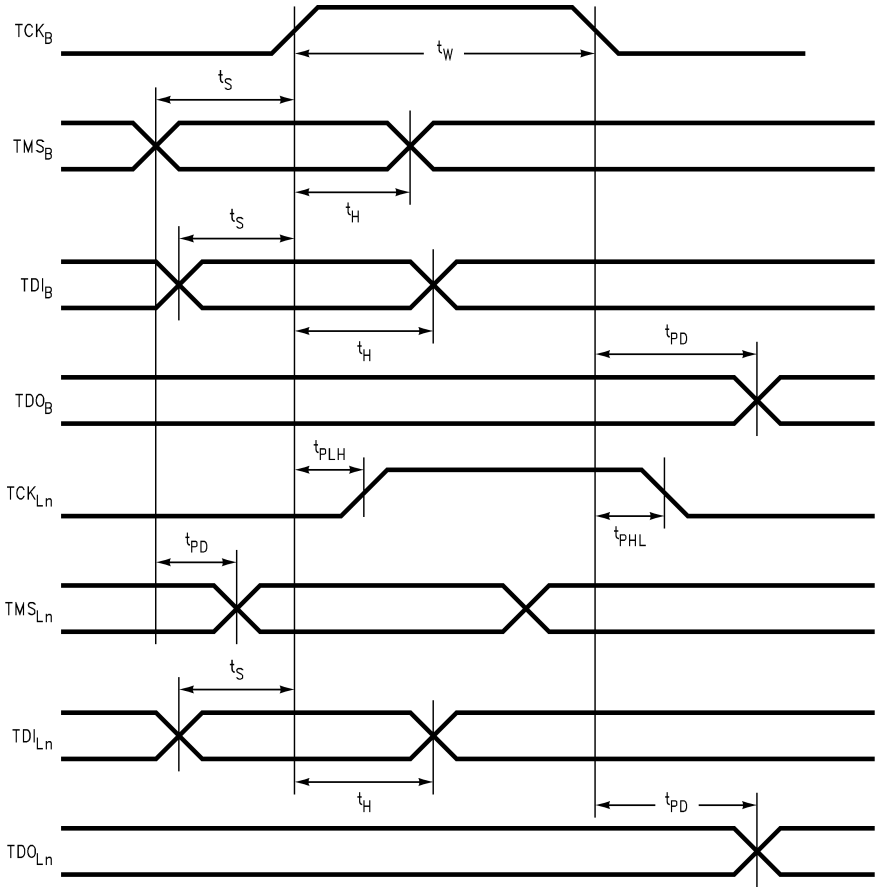


Figure 6. Waveforms for an Unparked STA112 in the Shift-DR (IR) TAP Controller State

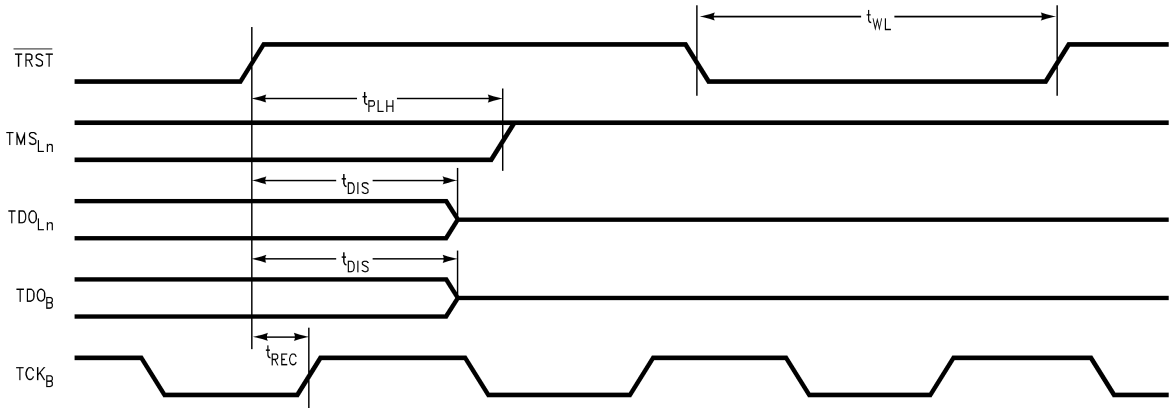


Figure 7. Reset Waveforms

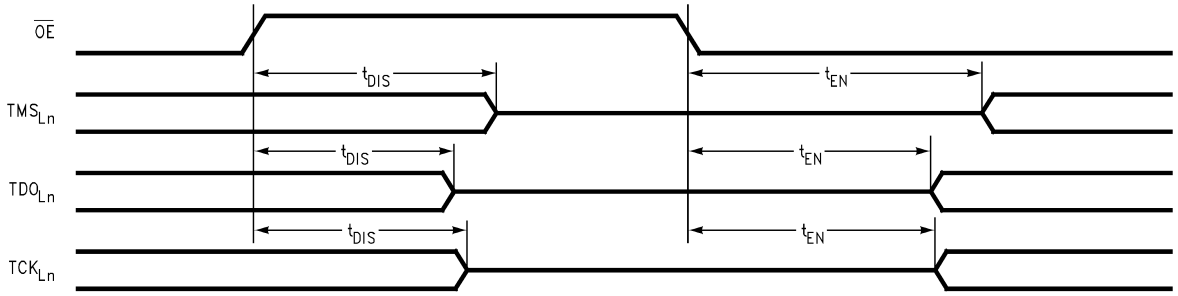


Figure 8. Output Enable Waveforms

Capacitance & I/O Characteristics

Refer to TI's website for IBIS models at www.ti.com.com/lsds/ti/analog/interface.page

REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SCANSTA112SM	Active	Production	NFBGA (NZD) | 100	240 | JEDEC TRAY (10+1)	No	Call TI	Call TI	-40 to 85	SCANSTA112 SM
SCANSTA112SM.A	Active	Production	NFBGA (NZD) | 100	240 | JEDEC TRAY (10+1)	No	Call TI	Level-3-235C-168 HR	-40 to 85	SCANSTA112 SM
SCANSTA112SM/NOPB	Active	Production	NFBGA (NZD) | 100	240 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	SCANSTA112 SM
SCANSTA112SM/NOPB.A	Active	Production	NFBGA (NZD) | 100	240 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	SCANSTA112 SM
SCANSTA112SMX	NRND	Production	NFBGA (NZD) | 100	1000 | LARGE T&R	No	Call TI	Level-3-235C-168 HR	-40 to 85	SCANSTA112 SM
SCANSTA112SMX.A	NRND	Production	NFBGA (NZD) | 100	1000 | LARGE T&R	No	Call TI	Level-3-235C-168 HR	-40 to 85	SCANSTA112 SM
SCANSTA112SMX/NOPB	Active	Production	NFBGA (NZD) | 100	1000 | LARGE T&R	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	SCANSTA112 SM
SCANSTA112SMX/NOPB.A	Active	Production	NFBGA (NZD) | 100	1000 | LARGE T&R	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	SCANSTA112 SM
SCANSTA112VS	Obsolete	Production	TQFP (NEZ) | 100	-	-	Call TI	Call TI	-40 to 85	SCANSTA112 VS
SCANSTA112VS/NOPB	Active	Production	TQFP (NEZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	SCANSTA112 VS
SCANSTA112VS/NOPB.A	Active	Production	TQFP (NEZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	SCANSTA112 VS
SCANSTA112VSNOPBG4.A	Active	Production	TQFP (NEZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	SCANSTA112 VS
SCANSTA112VSX/NOPB	Active	Production	TQFP (NEZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	SCANSTA112 VS
SCANSTA112VSX/NOPB.A	Active	Production	TQFP (NEZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	SCANSTA112 VS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

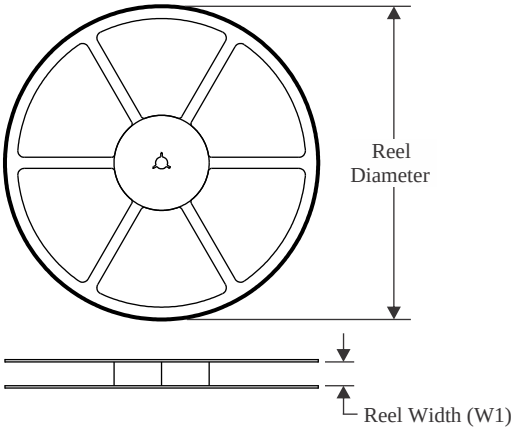
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

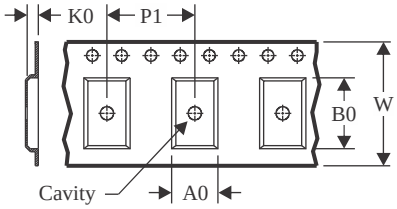
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

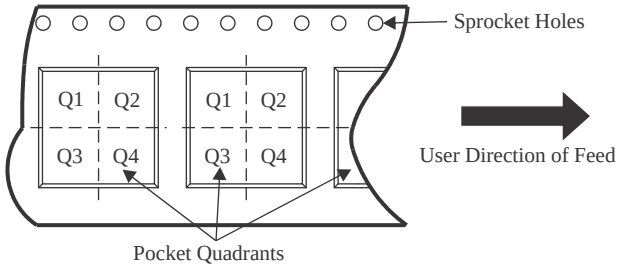


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

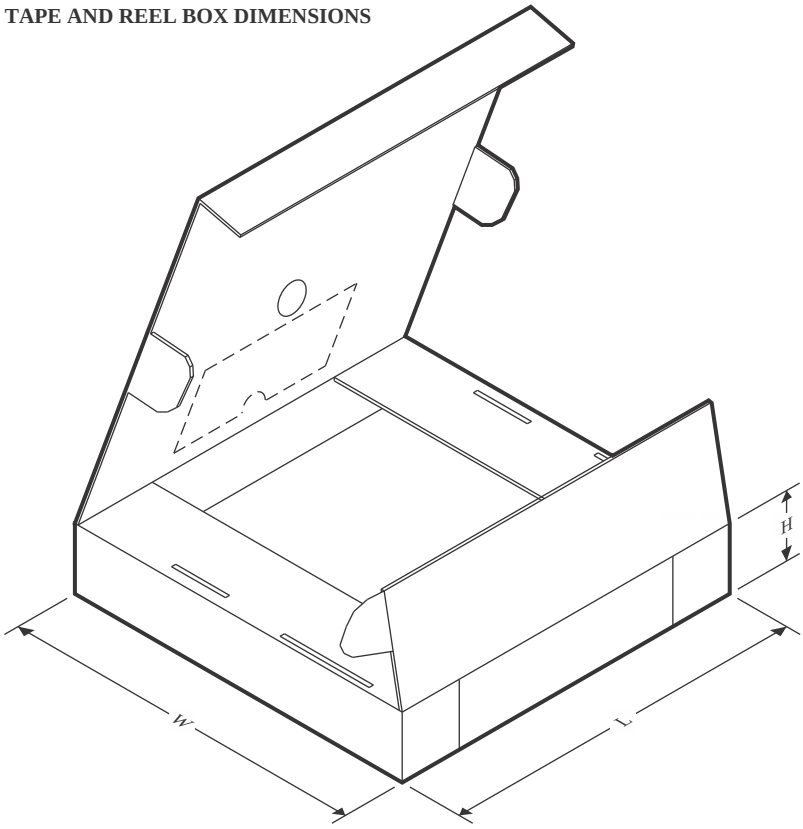
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SCANSTA112SMX	NFBGA	NZD	100	1000	330.0	24.4	10.3	10.3	2.0	16.0	24.0	Q1
SCANSTA112SMX/NOPB	NFBGA	NZD	100	1000	330.0	24.4	10.3	10.3	2.0	16.0	24.0	Q1
SCANSTA112VSX/NOPB	TQFP	NEZ	100	1000	330.0	32.4	18.0	18.0	1.6	24.0	32.0	Q2

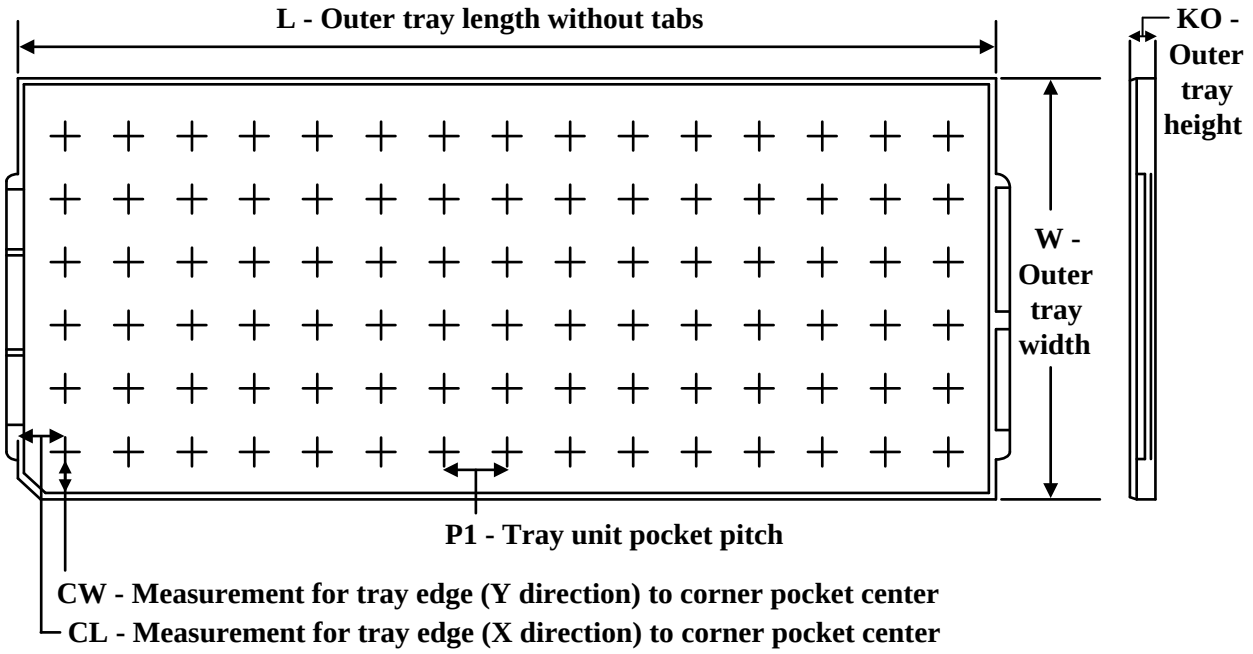
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SCANSTA112SMX	NFBGA	NZD	100	1000	356.0	356.0	45.0
SCANSTA112SMX/NOPB	NFBGA	NZD	100	1000	356.0	356.0	45.0
SCANSTA112VSX/NOPB	TQFP	NEZ	100	1000	367.0	367.0	55.0

TRAY

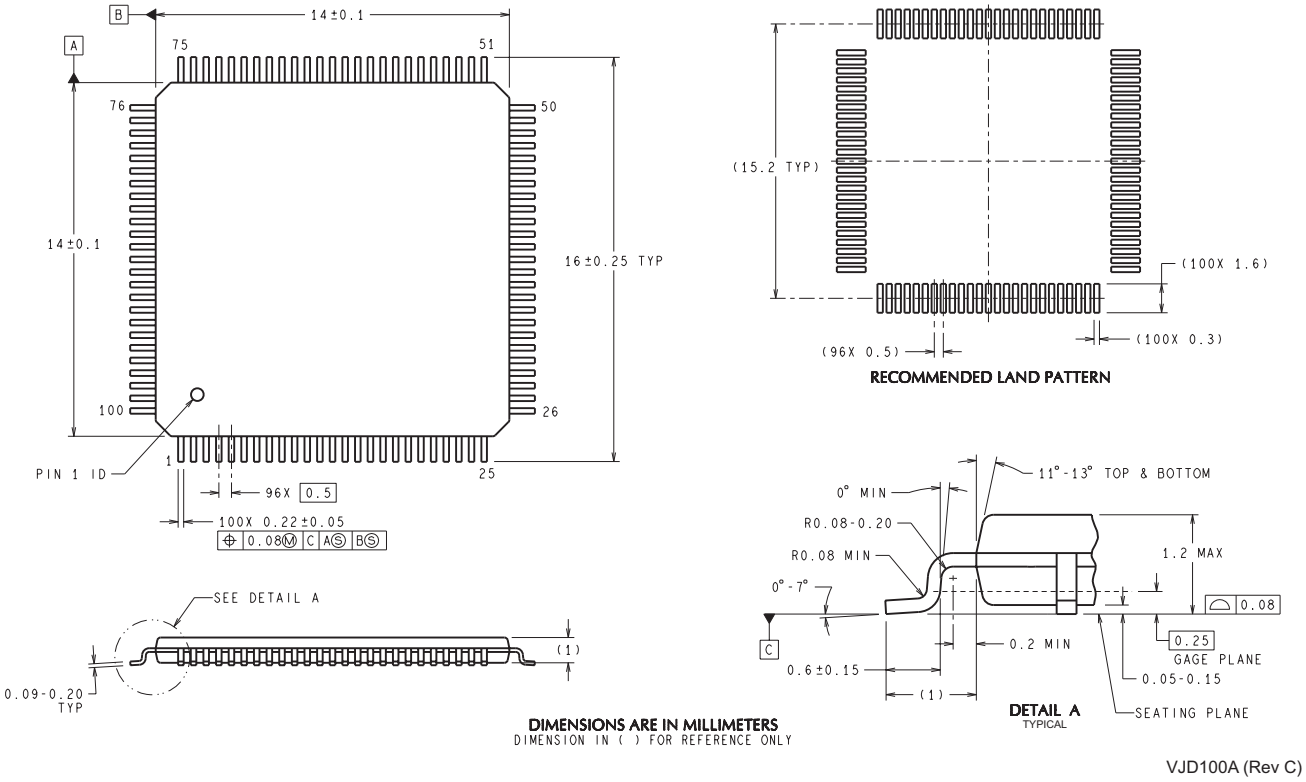


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SCANSTA112SM	NZD	NFBGA	100	240	10 X 24	150	322.6	135.9	7620	12.4	14.9	12.15
SCANSTA112SM.A	NZD	NFBGA	100	240	10 X 24	150	322.6	135.9	7620	12.4	14.9	12.15
SCANSTA112SM/NOPB	NZD	NFBGA	100	240	10 X 24	150	322.6	135.9	7620	12.4	14.9	12.15
SCANSTA112SM/ NOPB.A	NZD	NFBGA	100	240	10 X 24	150	322.6	135.9	7620	12.4	14.9	12.15
SCANSTA112VS/NOPB	NEZ	TQFP	100	90	6 x 15	150	322.6	135.9	7620	20.3	15.4	15.45
SCANSTA112VS/ NOPB.A	NEZ	TQFP	100	90	6 x 15	150	322.6	135.9	7620	20.3	15.4	15.45
SCANSTA112VSNOPBG4.A	NEZ	TQFP	100	90	6 x 15	150	322.6	135.9	7620	20.3	15.4	15.45

NEZ0100A



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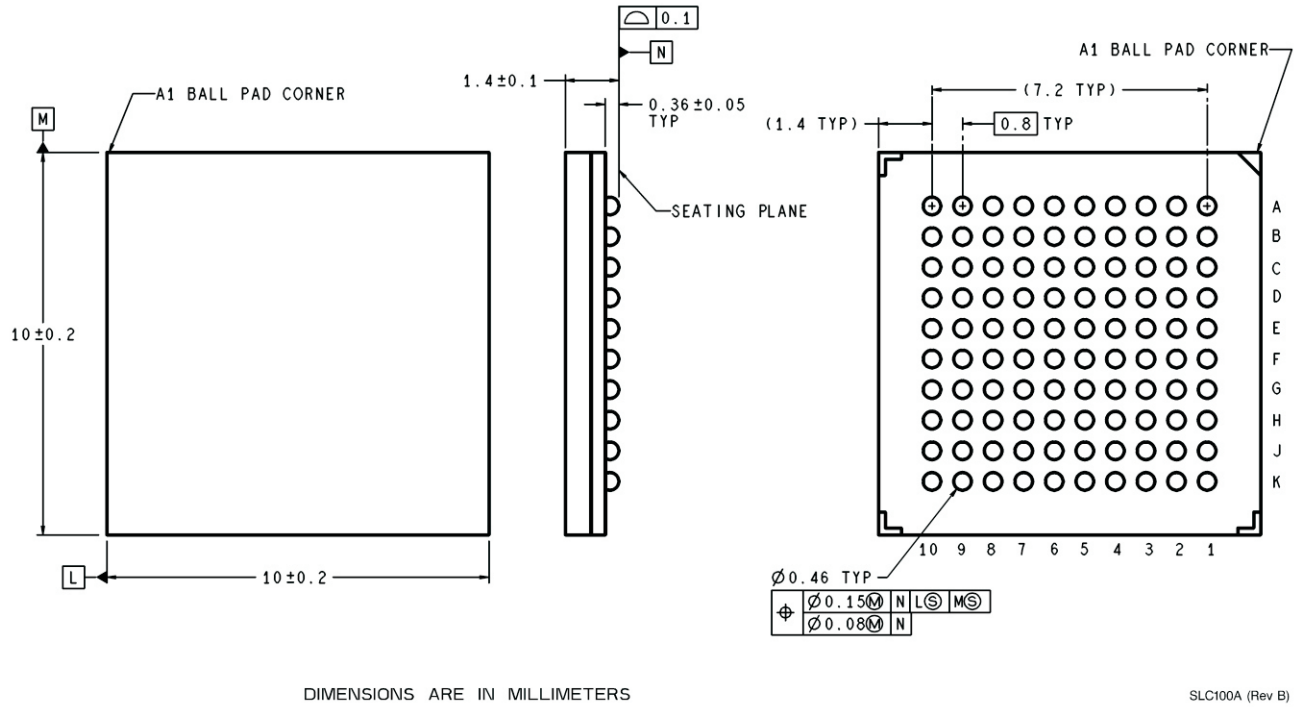
VJD100A (Rev C)

NZD0100A



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SLC100A (Rev B)

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