

# DS90C383

*DS90C383/DS90CF384 +3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-65 MHz, +3.3V LVDS Receiver 24-Bit Flat Panel Display (FPD) Link-65 MHz*



Literature Number: SNLS124A

# DS90C383/DS90CF384

## +3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link—65 MHz, +3.3V LVDS Receiver 24-Bit Flat Panel Display (FPD) Link—65 MHz

### General Description

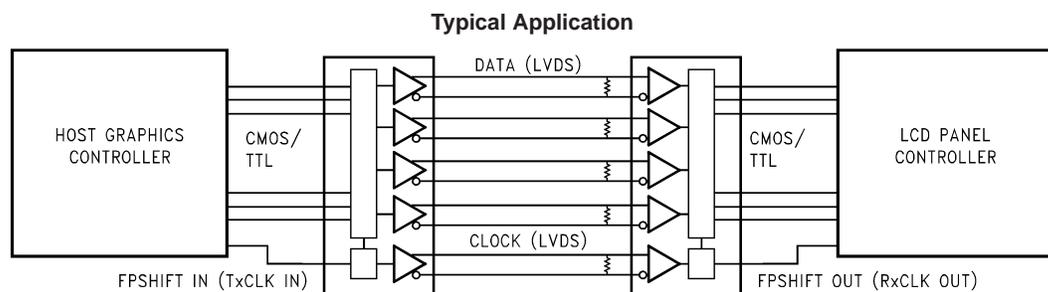
The DS90C383 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CF384 receiver converts the LVDS data streams back into 28 bits of LVCMOS/LVTTL data. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughputs is 227 Mbytes/sec. The transmitter is offered with programmable edge data strobes for convenient interface with a variety of graphics controllers. The transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge transmitter will inter-operate with a Falling edge receiver (DS90CF384) without any translation logic. Both devices are also offered in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package which provides a 44 % reduction in PCB footprint compared to the TSSOP package.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

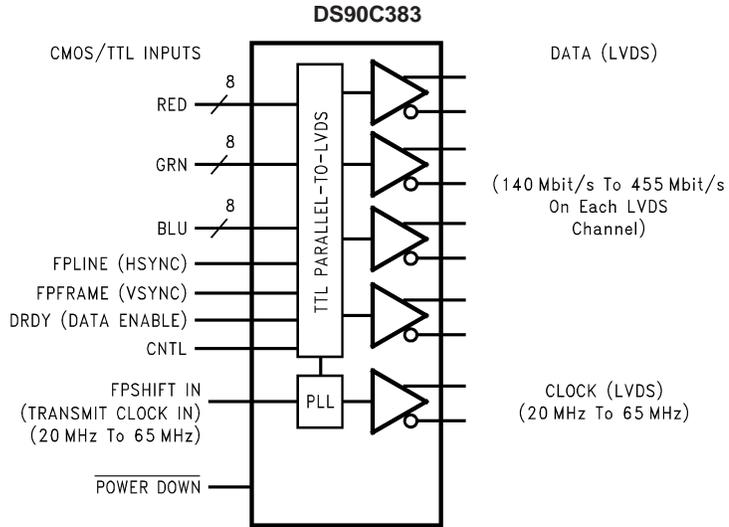
### Features

- 20 to 65 MHz shift clock support
- Programmable transmitter (DS90C383) strobe select (Rising or Falling edge strobe)
- Single 3.3V supply
- Chipset (Tx + Rx) power consumption < 250 mW (typ)
- Power-down mode (< 0.5 mW total)
- Single pixel per clock XGA (1024x768) ready
- Supports VGA, SVGA, XGA and higher addressability.
- Up to 227 Megabytes/sec bandwidth
- Up to 1.8 Gbps throughput
- Narrow bus reduces cable size and cost
- 290 mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 56-lead TSSOP package.
- Also available in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package
- Falling edge data strobe Receiver
- Compatible with TIA/EIA-644 LVDS standard
- ESD rating >7 kV
- Operating Temperature: -40°C to +85°C

### Block Diagrams

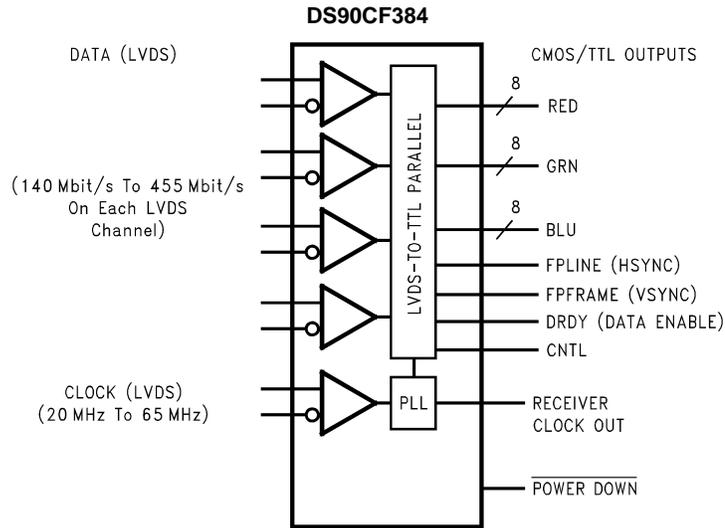


**Block Diagrams** (Continued)



DS012887-1

**Order Number DS90C383MTD or DS90C383SLC**  
**See NS Package Number MTD56 or SLC64A**



DS012887-24

**Order Number DS90CF384MTD or DS90CF384SLC**  
**See NS Package Number MTD56 or SLC64A**

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.3V to +4V
CMOS/TTL Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
CMOS/TTL Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Receiver Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Driver Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 4 sec for TSSOP)	+260°C
Solder Reflow Temperature (20 sec for FBGA)	+220°C
Maximum Package Power Dissipation Capacity 25°C	
MTD56 (TSSOP) Package:	
DS90C383MTD	1.63 W
DS90CF384MTD	1.61 W
Package Derating:	
DS90C383MTD	12.5 mW/°C above +25°C

DS90CF384MTD	12.4 mW/°C above +25°C
Maximum Package Power Dissipation Capacity 25°C	
SLC64A Package:	
DS90C383SLC	2.0 W
DS90CF384SLC	2.0 W
Package Derating:	
DS90C383SLC	10.2 mW/°C above +25°C
DS90CF384SLC	10.2 mW/°C above +25°C

ESD Rating (HBM, 1.5 k $\Omega$ , 100 pF)	> 7 kV
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**Recommended Operating Conditions**

	Min	Nom	Max	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.3	3.6	V
Operating Free Air Temperature ( $T_A$ )	-40	+25	+85	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage ( $V_{CC}$ )			100	mV <sub>PP</sub>

**Electrical Characteristics**

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>LVC MOS/LVTTL DC SPECIFICATIONS</b>							
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V	
$V_{IL}$	Low Level Input Voltage		GND		0.8	V	
$V_{OH}$	High Level Output Voltage	$I_{OH} = -0.4$ mA	2.7	3.3		V	
$V_{OL}$	Low Level Output Voltage	$I_{OL} = 2$ mA		0.06	0.3	V	
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA		-0.79	-1.5	V	
$I_{IN}$	Input Current	$V_{IN} = V_{CC}, GND, 2.5V$ or 0.4V		$\pm 5.1$	$\pm 10$	$\mu A$	
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V$		-60	-120	mA	
<b>LVDS DC SPECIFICATIONS</b>							
$V_{OD}$	Differential Output Voltage	$R_L = 100\Omega$	250	345	450	mV	
$\Delta V_{OD}$	Change in $V_{OD}$ between complimentary output states				35	mV	
$V_{OS}$	Offset Voltage (Note 4)		1.125	1.25	1.375	V	
$\Delta V_{OS}$	Change in $V_{OS}$ between complimentary output states				35	mV	
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V, R_L = 100\Omega$		-3.5	-5	mA	
$I_{OZ}$	Output TRI-STATE® Current	Power Down = 0V, $V_{OUT} = 0V$ or $V_{CC}$		$\pm 1$	$\pm 10$	$\mu A$	
$V_{TH}$	Differential Input High Threshold	$V_{CM} = +1.2V$			+100	mV	
$V_{TL}$	Differential Input Low Threshold		-100			mV	
$I_{IN}$	Input Current	$V_{IN} = +2.4V, V_{CC} = 3.6V$			$\pm 10$	$\mu A$	
		$V_{IN} = 0V, V_{CC} = 3.6V$			$\pm 10$	$\mu A$	
<b>TRANSMITTER SUPPLY CURRENT</b>							
ICCTW	Transmitter Supply Current	$R_L = 100\Omega,$ $C_L = 5$ pF,	f = 32.5 MHz		31	45	mA
	Worst Case	Worst Case Pattern	f = 37.5 MHz		32	50	mA

## Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>TRANSMITTER SUPPLY CURRENT</b>							
		(Figures 1, 3), $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	$f = 65\text{ MHz}$		42	55	mA
ICCTG	Transmitter Supply Current  16 Grayscale	$R_L = 100\Omega$ , $C_L = 5\text{ pF}$ , 16 Grayscale Pattern (Figures 2, 3), $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	$f = 32.5\text{ MHz}$		23	35	mA
			$f = 37.5\text{ MHz}$		28	40	mA
			$f = 65\text{ MHz}$		31	45	mA
ICCTZ	Transmitter Supply Current Power Down	Power Down = Low Driver Outputs in TRI-STATE® under Power Down Mode		10	55	$\mu\text{A}$	
<b>RECEIVER SUPPLY CURRENT</b>							
ICCRW	Receiver Supply Current Worst Case	$C_L = 8\text{ pF}$ , Worst Case Pattern (Figures 1, 4), $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	$f = 32.5\text{ MHz}$		49	65	mA
			$f = 37.5\text{ MHz}$		53	70	mA
			$f = 65\text{ MHz}$		78	105	mA
ICCRG	Receiver Supply Current, 16 Grayscale	$C_L = 8\text{ pF}$ , 16 Grayscale Pattern (Figures 2, 4), $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	$f = 32.5\text{ MHz}$		28	45	mA
			$f = 37.5\text{ MHz}$		30	47	mA
			$f = 65\text{ MHz}$		43	60	mA
ICCRZ	Receiver Supply Current Power Down	Power Down = Low Receiver Outputs Stay Low during Power Down Mode		10	55	$\mu\text{A}$	

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

**Note 2:** Typical values are given for  $V_{CC} = 3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ .

**Note 3:** Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except  $V_{OD}$  and  $\Delta V_{OD}$ ).

**Note 4:**  $V_{OS}$  previously referred as  $V_{CM}$ .

## Transmitter Switching Characteristics

Over recommended operating supply and  $-40^\circ\text{C to } +85^\circ\text{C}$  ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
LLHT	LVDS Low-to-High Transition Time (Figure 3)		0.75	1.5	ns	
LHLT	LVDS High-to-Low Transition Time (Figure 3)		0.75	1.5	ns	
TCIT	TxCLK IN Transition Time (Figure 5)			5	ns	
TCCS	TxOUT Channel-to-Channel Skew (Figure 6)		250		ps	
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 17)	$f = 65\text{ MHz}$	-0.4	0	0.3	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		1.8	2.2	2.5	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.0	4.4	4.7	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.2	6.6	6.9	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.4	8.8	9.1	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.6	11	11.3	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.8	13.2	13.5	ns
TCIP	TxCLK IN Period (Figure 7)	15	T	50	ns	
TCIH	TxCLK IN High Time (Figure 7)	0.35T	0.5T	0.65T	ns	
TCIL	TxCLK IN Low Time (Figure 7)	0.35T	0.5T	0.65T	ns	
TSTC	TxIN Setup to TxCLK IN (Figure 7)	$f = 65\text{ MHz}$	2.5			ns
THTC	TxIN Hold to TxCLK IN (Figure 7)		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay $25^\circ\text{C}$ , $V_{CC} = 3.3\text{V}$ (Figure 9)	3.0	3.7	5.5	ns	

## Transmitter Switching Characteristics (Continued)

Over recommended operating supply and  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
TPLLS	Transmitter Phase Lock Loop Set (Figure 11)			10	ms
TPDD	Transmitter Power Down Delay (Figure 15)			100	ns

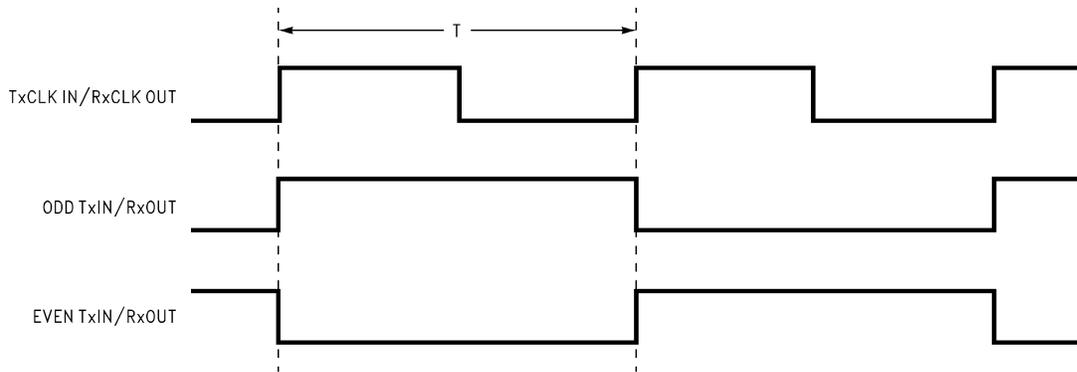
## Receiver Switching Characteristics

Over recommended operating supply and  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units		
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 4)		2.2	5.0	ns		
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 4)		2.2	5.0	ns		
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 18)	f = 65 MHz		0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1			2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2			5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3			7.3	7.7	8.0	ns
RSPos4	Receiver Input Strobe Position for Bit 4			9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5			11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6			13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin (Note 5) (Figure 19)	f = 65 MHz		400		ps	
RCOP	RxCLK OUT Period (Figure 8)	15	T	50	ns		
RCOH	RxCLK OUT High Time (Figure 8)	f = 65 MHz		7.3	8.6		ns
RCOL	RxCLK OUT Low Time (Figure 8)			3.45	4.9		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 8)			2.5	6.9		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 8)			2.5	5.7		ns
RCCD	RxCLK IN to RxCLK OUT Delay $25^{\circ}\text{C}$ , $V_{\text{CC}} = 3.3\text{V}$ (Figure 10)	5.0	7.1	9.0	ns		
RPLLS	Receiver Phase Lock Loop Set (Figure 12)			10	ms		
RPDD	Receiver Power Down Delay (Figure 16)			1	$\mu\text{s}$		

**Note 5:** Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window-RSPOS). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).

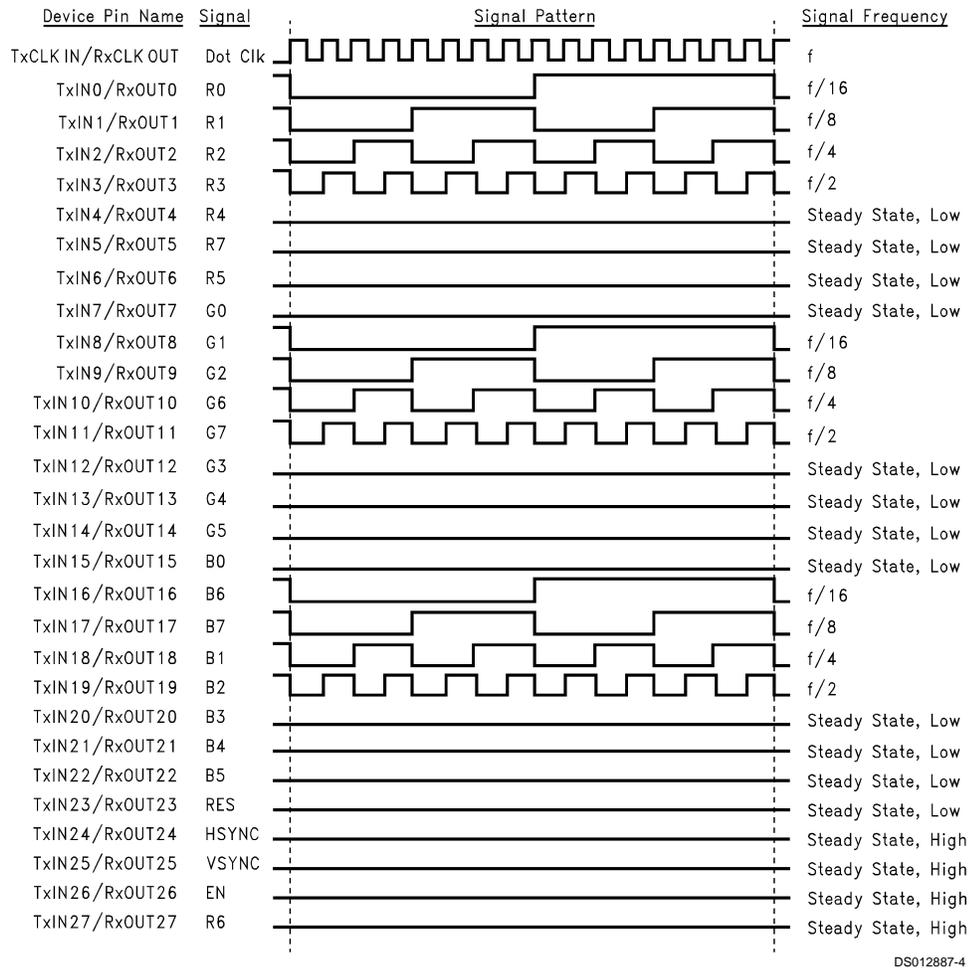
## AC Timing Diagrams



DS012887-3

FIGURE 1. "Worst Case" Test Pattern

## AC Timing Diagrams (Continued)



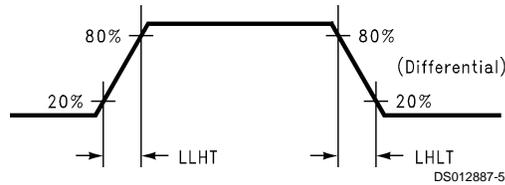
**FIGURE 2. "16 Grayscale" Test Pattern (Notes 6, 7, 8, 9)**

**Note 6:** The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

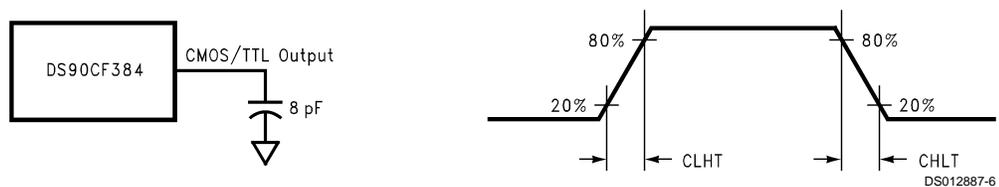
**Note 7:** The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

**Note 8:** Figures 1, 2 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

**Note 9:** Recommended pin to signal mapping. Customer may choose to define differently.



**FIGURE 3. DS90C383 (Transmitter) LVDS Output Load and Transition Times**



**FIGURE 4. DS90CF384 (Receiver) CMOS/TTL Output Load and Transition Times**

AC Timing Diagrams (Continued)

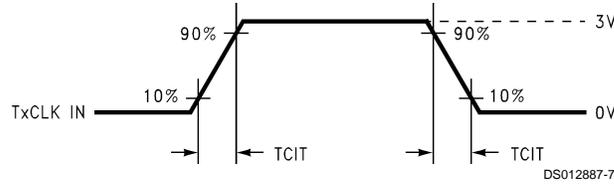
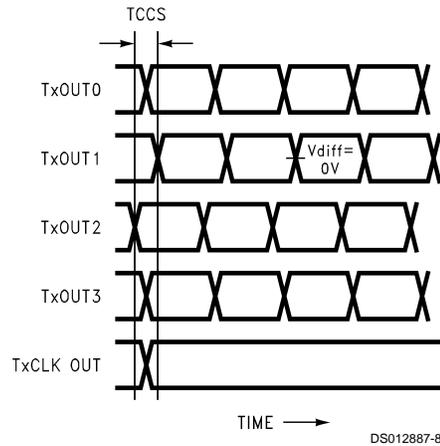


FIGURE 5. DS90C383 (Transmitter) Input Clock Transition Time



Measurements at  $V_{diff} = 0V$   
 TCCS measured between earliest and latest LVDS edges.  
 TxCLK Differential Low → High Edge

FIGURE 6. DS90C383 (Transmitter) Channel-to-Channel Skew

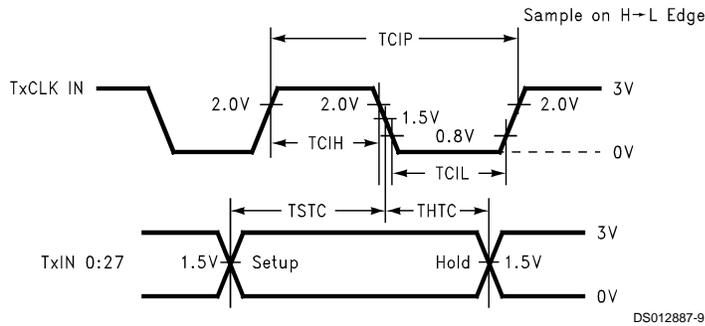


FIGURE 7. DS90C383 (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

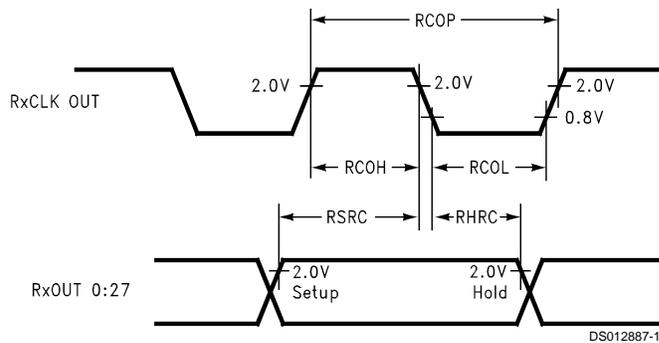


FIGURE 8. DS90CF384 (Receiver) Setup/Hold and High/Low Times

AC Timing Diagrams (Continued)

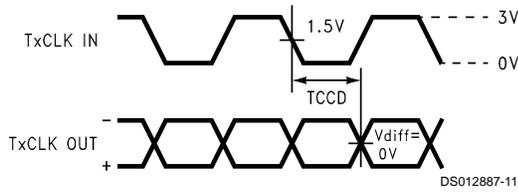


FIGURE 9. DS90C383 (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)

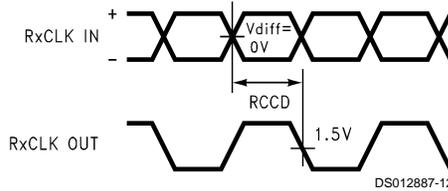


FIGURE 10. DS90CF384 (Receiver) Clock In to Clock Out Delay

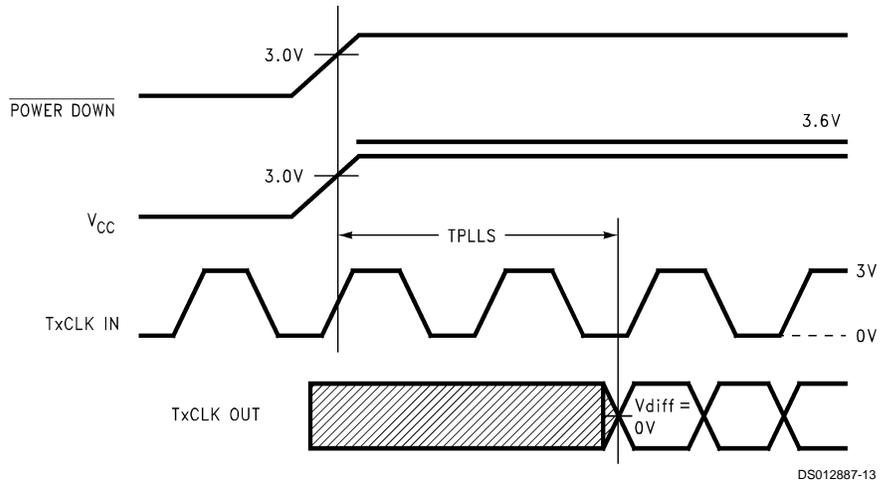


FIGURE 11. DS90C383 (Transmitter) Phase Lock Loop Set Time

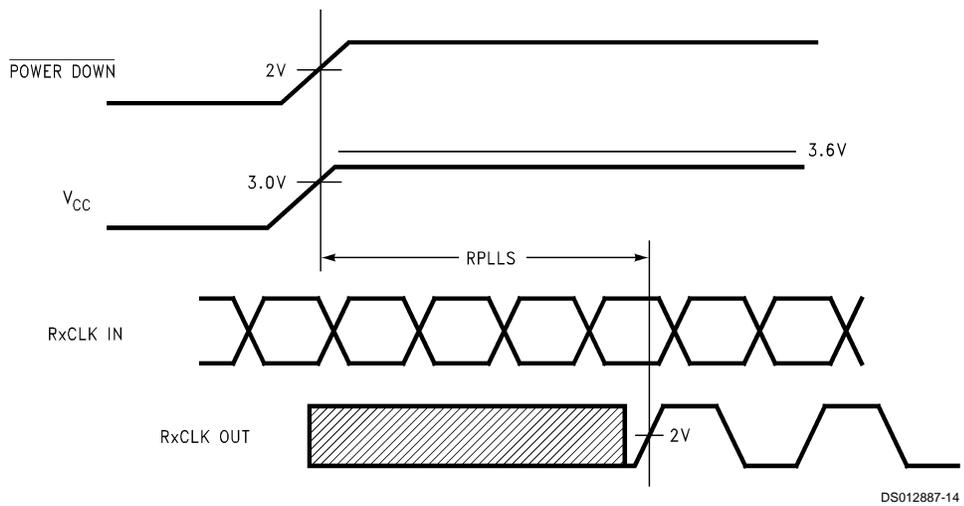


FIGURE 12. DS90CF384 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

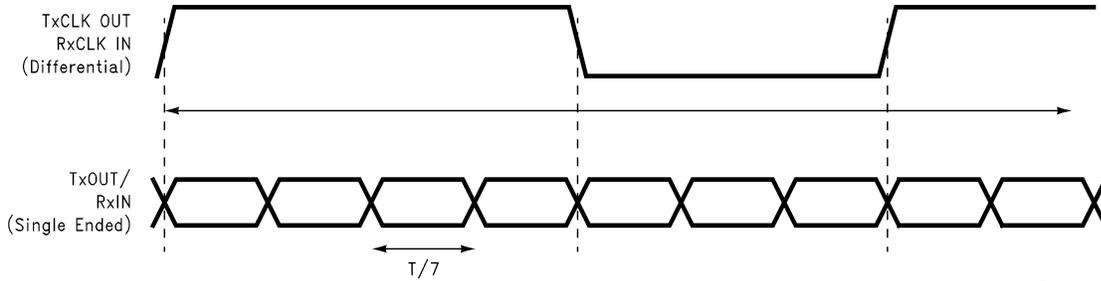


FIGURE 13. Seven Bits of LVDS in Once Clock Cycle

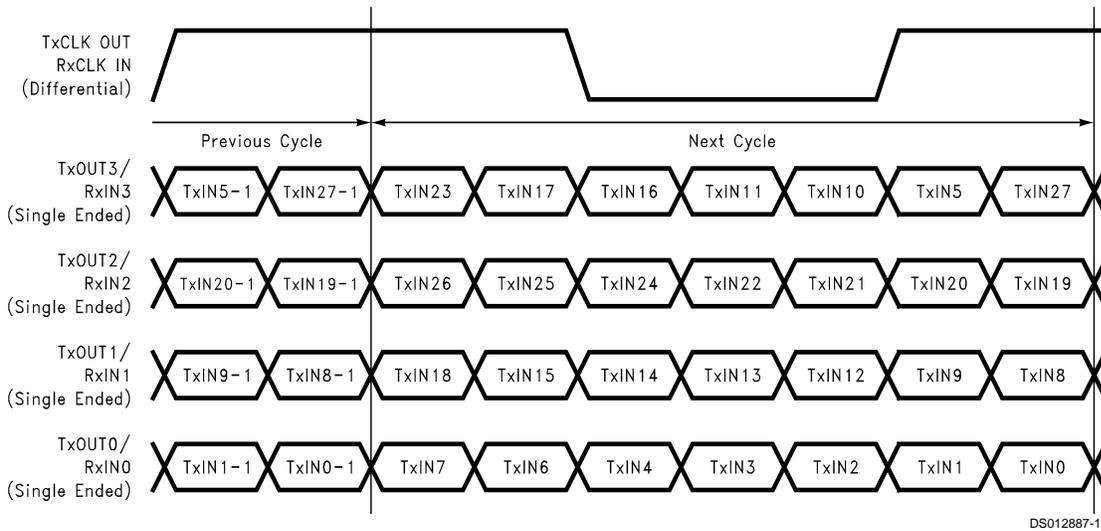


FIGURE 14. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs

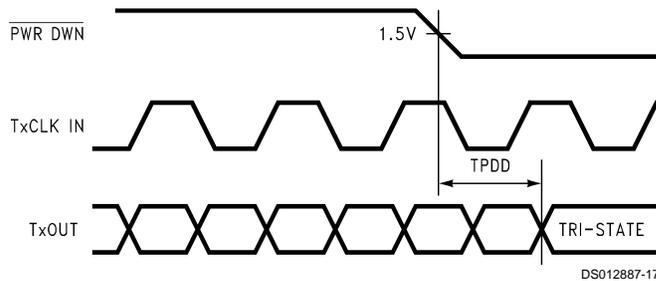
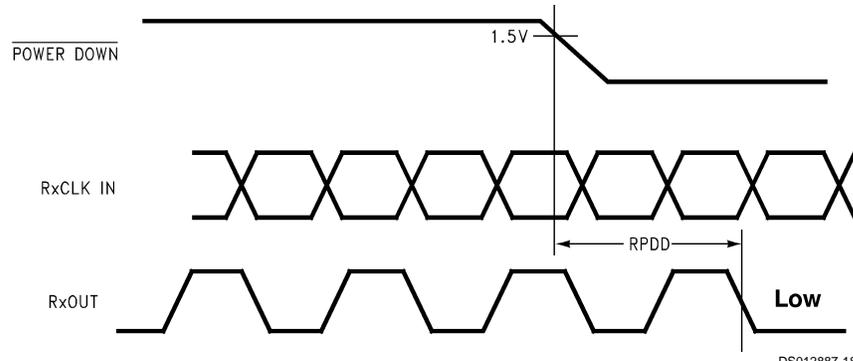


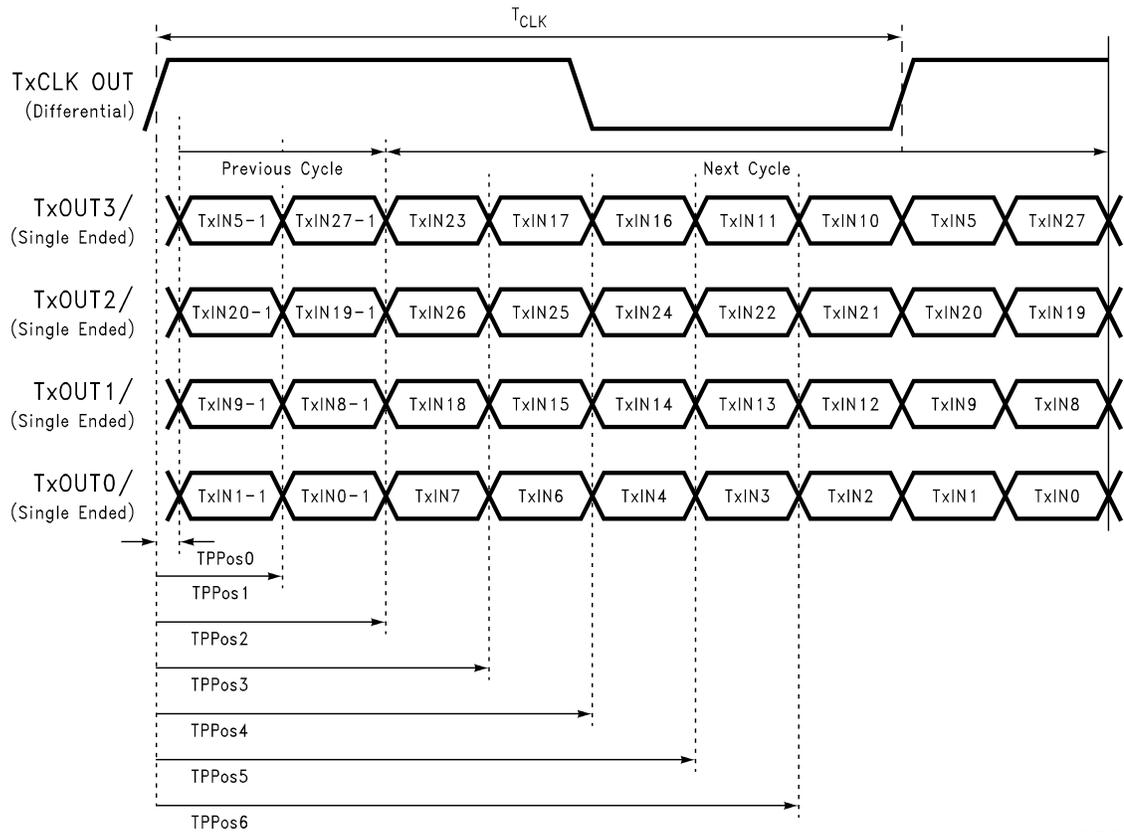
FIGURE 15. Transmitter Power Down Delay

AC Timing Diagrams (Continued)



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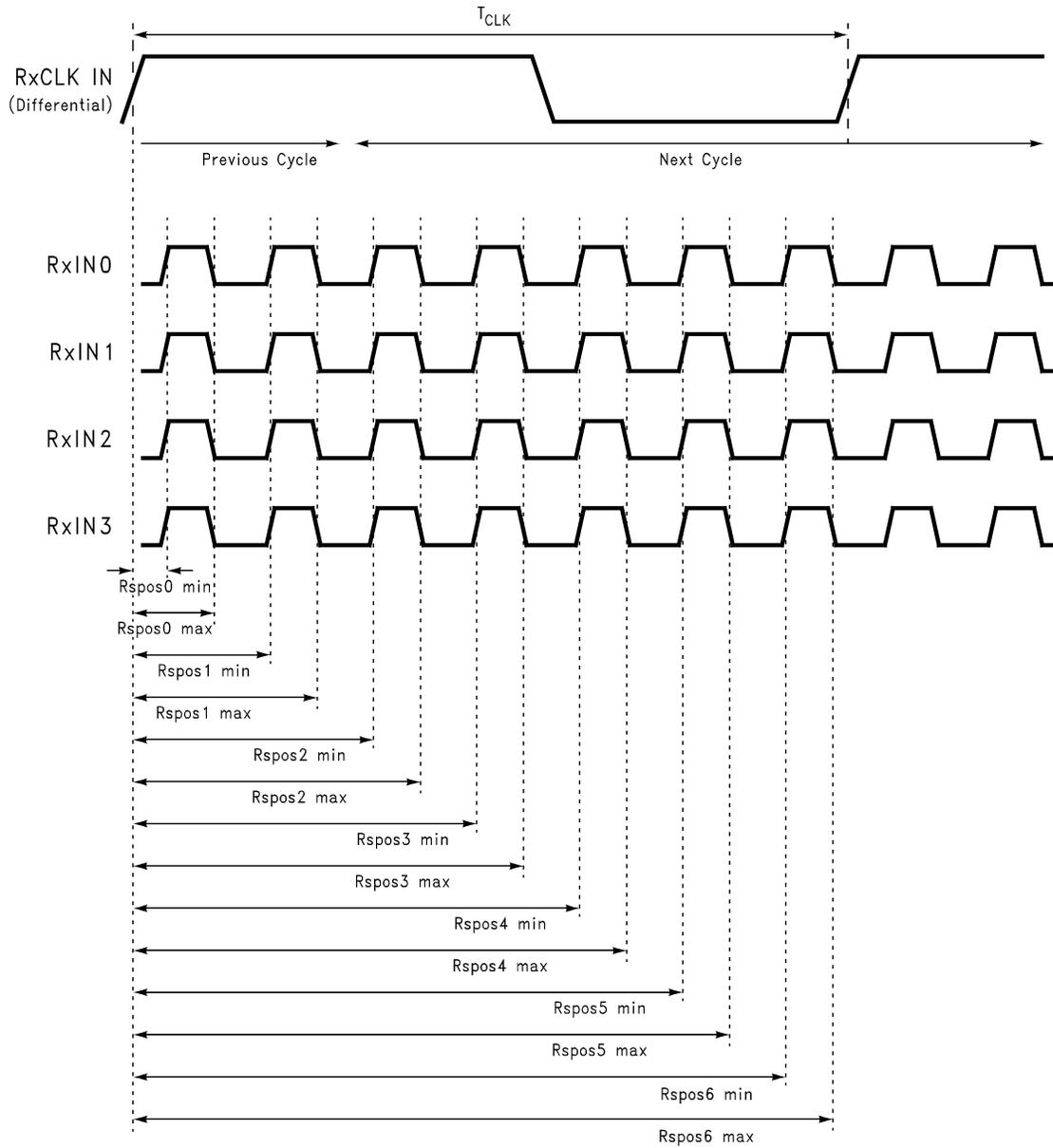
FIGURE 16. Receiver Power Down Delay



DS012887-26

FIGURE 17. Transmitter LVDS Output Pulse Position Measurement

AC Timing Diagrams (Continued)



DS012887-25

FIGURE 18. Receiver LVDS Input Strobe Position



## DS90C383 TSSOP Package Pin Description — FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT-	O	4	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
R_FB	I	1	Programmable strobe select.
RTxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT-	O	1	Negative LVDS differential clock output.
PWR DOWN	I	1	TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down.
V <sub>CC</sub>	I	3	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V <sub>CC</sub>	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

## DS90C383SLC SLC64A (FBGA) Package Pin Summary — FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input.
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT-	O	4	Negative LVDS differential data output.
TxCLKIN	I	1	TTL level clock input. The rising edge acts as data strobe. Pin name TxCLK IN.
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT-	O	1	Negative LVDS differential clock output.
PWR DWN	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
R_FB	I	1	Programmable strobe select. HIGH = rising edge, LOW = falling edge.
V <sub>CC</sub>	I	3	Power supply pins for TTL inputs.
GND	I	5	Ground pins for TTL inputs.
PLL V <sub>CC</sub>	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V <sub>CC</sub>	I	2	Power supply pin for LVDS outputs.
LVDS GND	I	4	Ground pins for LVDS outputs.
NC		6	Pins not connected.

## DS90C383SLC SLC64A (FBGA) Package Pin Description — FPD Link Transmitter

By Pin			By Pin Type		
Pin	Pin Name	Type	Pin	Pin Name	Type
A1	TxIN27	I	D3	GND	G
A2	TxOUT0-	O	E4	GND	G
A3	TxOUT0+	O	E8	GND	G
A4	LVDS VCC	P	G1	GND	G
A5	LVDS VCC	P	G6	GND	G
A6	TxCLKOUT-	O	B3	LVDS GND	G

## DS90C383SLC SLC64A (FBGA) Package Pin Description — FPD Link Transmitter (Continued)

By Pin			By Pin Type		
A7	TxCLKOUT+	O	B4	LVDS GND	G
A8	TxOUT3+	O	B7	LVDS GND	G
B1	TxIN1	I	D5	LVDS GND	G
B2	TxIN0	I	C6	PLL GND	G
B3	LVDS GND	G	D6	PLL GND	G
B4	LVDS GND	G	D7	PWR DWN	I
B5	TxOUT2-	O	G5	R_FB	I
B6	TxOUT3-	O	C8	TxCLKIN	I
B7	LVDS GND	G	B2	TxIN0	I
B8	NC		B1	TxIN1	I
C1	TxIN3	I	D2	TxIN2	I
C2	NC		C1	TxIN3	I
C3	NC		D1	TxIN4	I
C4	TxOUT1-	O	F1	TxIN5	I
C5	TxOUT2+	O	E2	TxIN6	I
C6	PLL GND	G	E3	TxIN7	I
C7	PLL VCC	P	G2	TxIN8	I
C8	TxCLKIN	I	H1	TxIN9	I
D1	TxIN4	I	G3	TxIN10	I
D2	TxIN2	I	H3	TxIN11	I
D3	GND	G	F4	TxIN12	I
D4	TxOUT1+	O	G4	TxIN13	I
D5	LVDS GND	G	H4	TxIN14	I
D6	PLL GND	G	H5	TxIN15	I
D7	PWR DWN	I	E5	TxIN16	I
D8	TxIN26	I	F5	TxIN17	I
E1	VCC	P	H6	TxIN18	I
E2	TxIN6	I	H7	TxIN19	I
E3	TxIN7	I	H8	TxIN20	I
E4	GND	G	G7	TxIN21	I
E5	TxIN16	I	F7	TxIN22	I
E6	VCC	P	G8	TxIN23	I
E7	TxIN24	I	E7	TxIN24	I
E8	GND	G	F8	TxIN25	I
F1	TxIN5	I	D8	TxIN26	I
F2	NC		A1	TxIN27	I
F3	NC		A6	TxCLKOUT-	O
F4	TxIN12	I	A7	TxCLKOUT+	O
F5	TxIN17	I	A2	TxOUT0-	O
F6	NC		A3	TxOUT0+	O
F7	TxIN22	I	C4	TxOUT1-	O
F8	TxIN25	I	D4	TxOUT1+	O
G1	GND	G	B5	TxOUT2-	O
G2	TxIN8	I	C5	TxOUT2+	O
G3	TxIN10	I	B6	TxOUT3-	O
G4	TxIN13	I	A8	TxOUT3+	O
G5	R_FB	I	A4	LVDS VCC	P
G6	GND	G	A5	LVDS VCC	P

## DS90C383SLC SLC64A (FBGA) Package Pin Description — FPD Link Transmitter (Continued)

By Pin			By Pin Type		
G7	TxIN21	I	C7	PLL VCC	P
G8	TxIN23	I	E1	VCC	P
H1	TxIN9	I	E6	VCC	P
H2	VCC	P	H2	VCC	P
H3	TxIN11	I	B8	NC	
H4	TxIN14	I	C2	NC	
H5	TxIN15	I	C3	NC	
H6	TxIN18	I	F2	NC	
H7	TxIN19	I	F3	NC	
H8	TxIN20	I	F6	NC	

G : Ground  
 I : Input  
 O : Output  
 P : Power  
 NC : No Connect

## DS90CF384 MTD56 TSSOP Package Pin Description — FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN-	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN-	I	1	Negative LVDS differential clock input.
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe. Pin name RxCLK OUT.
PWR DOWN	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V <sub>CC</sub>	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V <sub>CC</sub>	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

## DS90CF384 64 ball FBGA Package Pin Description — FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN-	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN-	I	1	Negative LVDS differential clock input.
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe. Pin name RxCLK OUT.
PWR DOWN	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V <sub>CC</sub>	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V <sub>CC</sub>	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V <sub>CC</sub>	I	2	Power supply pin for LVDS inputs.

**DS90CF384 64 ball FBGA Package Pin Description — FPD Link Receiver**

(Continued)

Pin Name	I/O	No.	Description
LVDS GND	I	4	Ground pins for LVDS inputs.
NC		6	Pins not connected.

**DS90CF384 64 ball, FBGA Package Pin Definition — FPD Link Receiver**

By Pin			By Pin Type		
Pin	Pin Name	Type	Pin	Pin Name	Type
A1	RxOUT17	O	A4	GND	G
A2	VCC	P	B1	GND	G
A3	RxOUT15	O	B6	GND	G
A4	GND	G	D8	GND	G
A5	RxOUT12	O	E3	GND	G
A6	RxOUT8	O	E5	LVDS GND	G
A7	RxOUT7	O	G3	LVDS GND	G
A8	RxOUT6	O	G7	LVDS GND	G
B1	GND	G	H5	LVDS GND	G
B2	NC		F6	PLL GND	G
B3	RxOUT16	O	G8	PLL GND	G
B4	RxOUT11	O	E6	PWR DWN	I
B5	VCC	P	H6	RxCLKIN-	I
B6	GND	G	H7	RxCLKIN+	I
B7	RxOUT5	O	H2	RxIN0-	I
B8	RxOUT3	O	H3	RxIN0+	I
C1	RxOUT21	O	F4	RxIN1-	I
C2	NC		G4	RxIN1+	I
C3	RxOUT18	O	G5	RxIN2-	I
C4	RxOUT14	O	F5	RxIN2+	I
C5	RxOUT9	O	G6	RxIN3-	I
C6	RxOUT4	O	H8	RxIN3+	I
C7	NC		E7	RxCLKOUT	O
C8	RxOUT1	O	E8	RxOUT0	O
D1	VCC	P	C8	RxOUT1	O
D2	RxOUT20	O	D7	RxOUT2	O
D3	RxOUT19	O	B8	RxOUT3	O
D4	RxOUT13	O	C6	RxOUT4	O
D5	RxOUT10	O	B7	RxOUT5	O
D6	VCC	P	A8	RxOUT6	O
D7	RxOUT2	O	A7	RxOUT7	O
D8	GND	G	A6	RxOUT8	O
E1	RxOUT22	O	C5	RxOUT9	O
E2	RxOUT24	O	D5	RxOUT10	O
E3	GND	G	B4	RxOUT11	O
E4	LVDS VCC	P	A5	RxOUT12	O
E5	LVDS GND	G	D4	RxOUT13	O
E6	PWR DWN	I	C4	RxOUT14	O
E7	RxCLKOUT	O	A3	RxOUT15	O
E8	RxOUT0	O	B3	RxOUT16	O
F1	RxOUT23	O	A1	RxOUT17	O

## DS90CF384 64 ball, FBGA Package Pin Definition — FPD Link Receiver

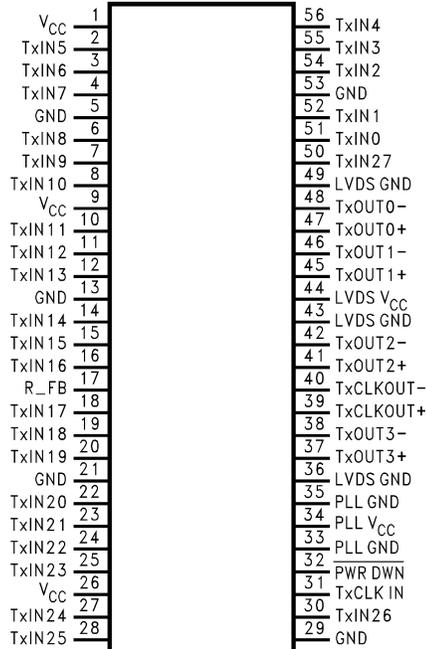
(Continued)

By Pin			By Pin Type		
F2	RxOUT26	O	C3	RxOUT18	O
F3	NC		D3	RxOUT19	O
F4	RxIN1-	I	D2	RxOUT20	O
F5	RxIN2+	I	C1	RxOUT21	O
F6	PLL GND	G	E1	RxOUT22	O
F7	PLL VCC	P	F1	RxOUT23	O
F8	NC		E2	RxOUT24	O
G1	RxOUT25	O	G1	RxOUT25	O
G2	NC		F2	RxOUT26	O
G3	LVDS GND	G	H1	RxOUT27	O
G4	RxIN1+	I	E4	LVDS VCC	P
G5	RxIN2-	I	H4	LVDS VCC	P
G6	RxIN3-	I	F7	PLL VCC	P
G7	LVDS GND	G	A2	VCC	P
G8	PLL GND	G	B5	VCC	P
H1	RxOUT27	O	D1	VCC	P
H2	RxIN0-	I	D6	VCC	P
H3	RxIN0+	I	B2	NC	
H4	LVDS VCC	P	C2	NC	
H5	LVDS GND	G	C7	NC	
H6	RxCLKIN-	I	F3	NC	
H7	RxCLKIN+	I	F8	NC	
H8	RxIN3+	I	G2	NC	

G : Ground  
 I : Input  
 O : Output  
 P : Power  
 NC : Not Connect

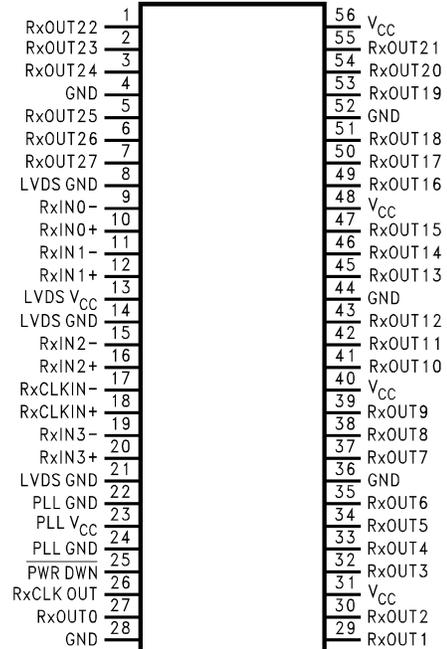
## Pin Diagrams for TSSOP Packages

**DS90C383MTD**



DS012887-22

**DS90CF384MTD**

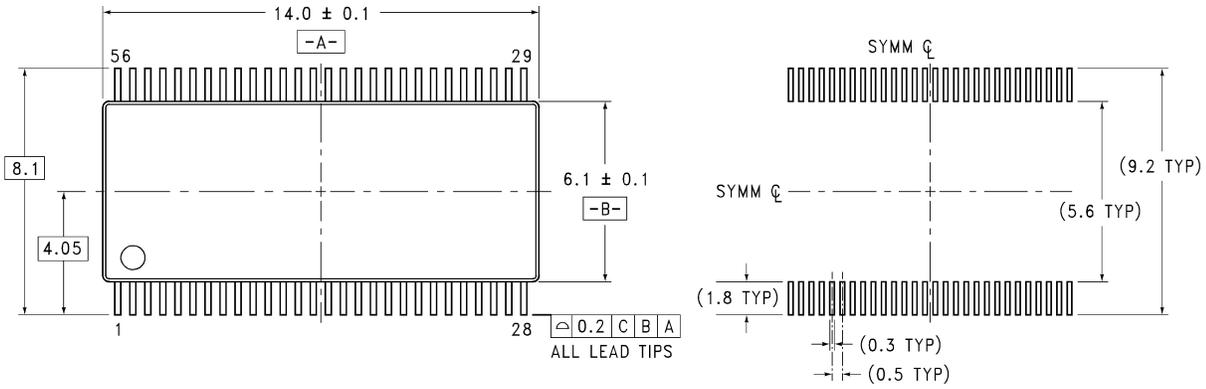


DS012887-23

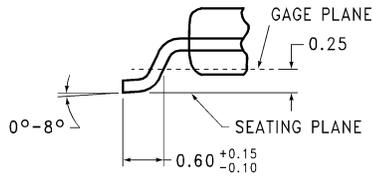
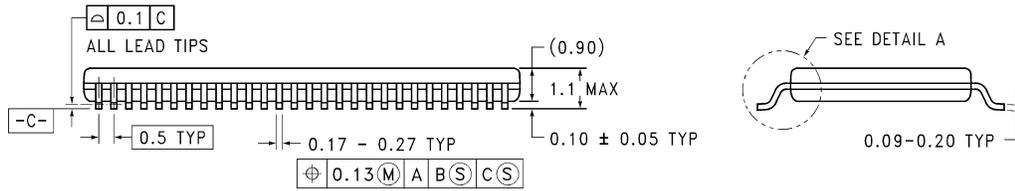
**TABLE 1. Programmable Transmitter**

Pin	Condition	Strobe Status
R_FB	R_FB = V <sub>CC</sub>	Rising edge strobe
R_FB	R_FB = GND	Falling edge strobe

**Physical Dimensions** inches (millimeters) unless otherwise noted



**LAND PATTERN RECOMMENDATION**

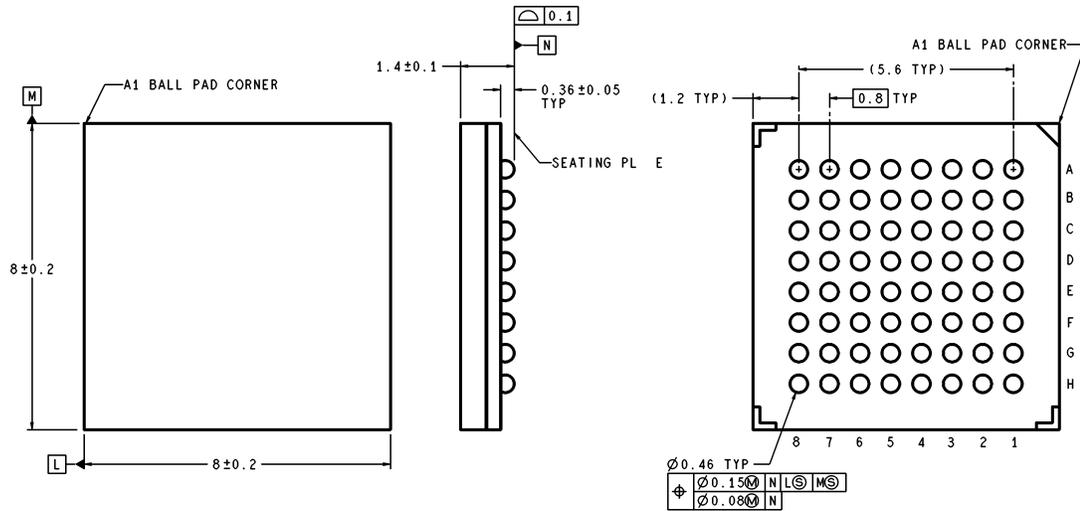


**DETAIL A**  
TYPICAL

MTD56 (REV B)

**56-Lead Molded Thin Shrink Small Outline Package, JEDEC**  
**Dimensions show in millimeters**  
**Order Number DS90C383MTD, DS90CF384MTD**  
**NS Package Number MTD56**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

SLC64A (Rev B)

**64 ball, 0.8mm fine pitch ball grid array (FBGA) Package**  
**Dimensions show in millimeters only**  
**Order Number DS90CF384SLC or DS90C383SLC**  
**NS Package Number SLC64A**

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**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90C383MTD/NOPB	NRND	Production	TSSOP (DGG)   56	34   TUBE	Yes	SN	Level-2-260C-1 YEAR	-	DS90C383MTD >B
DS90C383MTD/NOPB.B	NRND	Production	TSSOP (DGG)   56	34   TUBE	Yes	SN	Level-2-260C-1 YEAR	See DS90C383MTD/ NOPB	DS90C383MTD >B
DS90C383MTDX/NOPB	NRND	Production	TSSOP (DGG)   56	1000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-	DS90C383MTD >B
DS90C383MTDX/NOPB.B	NRND	Production	TSSOP (DGG)   56	1000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	See DS90C383MTDX/ NOPB	DS90C383MTD >B
<a href="#">DS90CF384MTD/NOPB</a>	Active	Production	TSSOP (DGG)   56	34   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CF384MTD >B
DS90CF384MTD/NOPB.B	Active	Production	TSSOP (DGG)   56	34   TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CF384MTD >B
<a href="#">DS90CF384MTDX/NOPB</a>	Active	Production	TSSOP (DGG)   56	1000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CF384MTD >B
DS90CF384MTDX/NOPB.B	Active	Production	TSSOP (DGG)   56	1000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CF384MTD >B

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

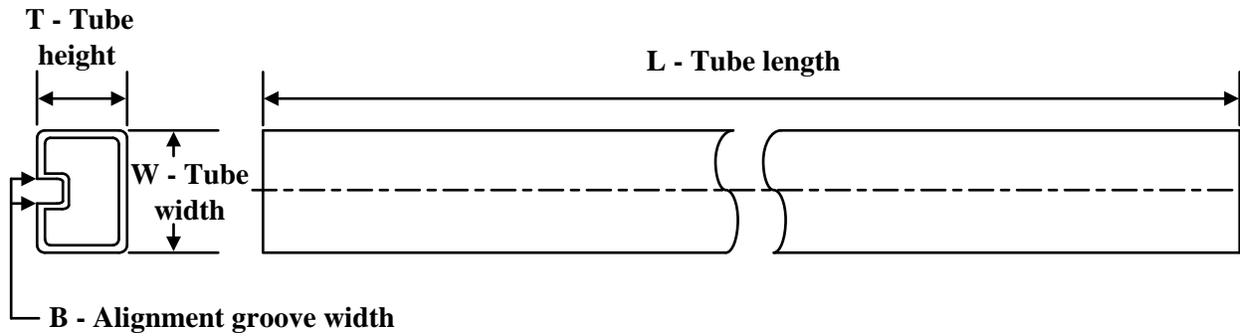

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C383MTDX/NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
DS90CF384MTDX/NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

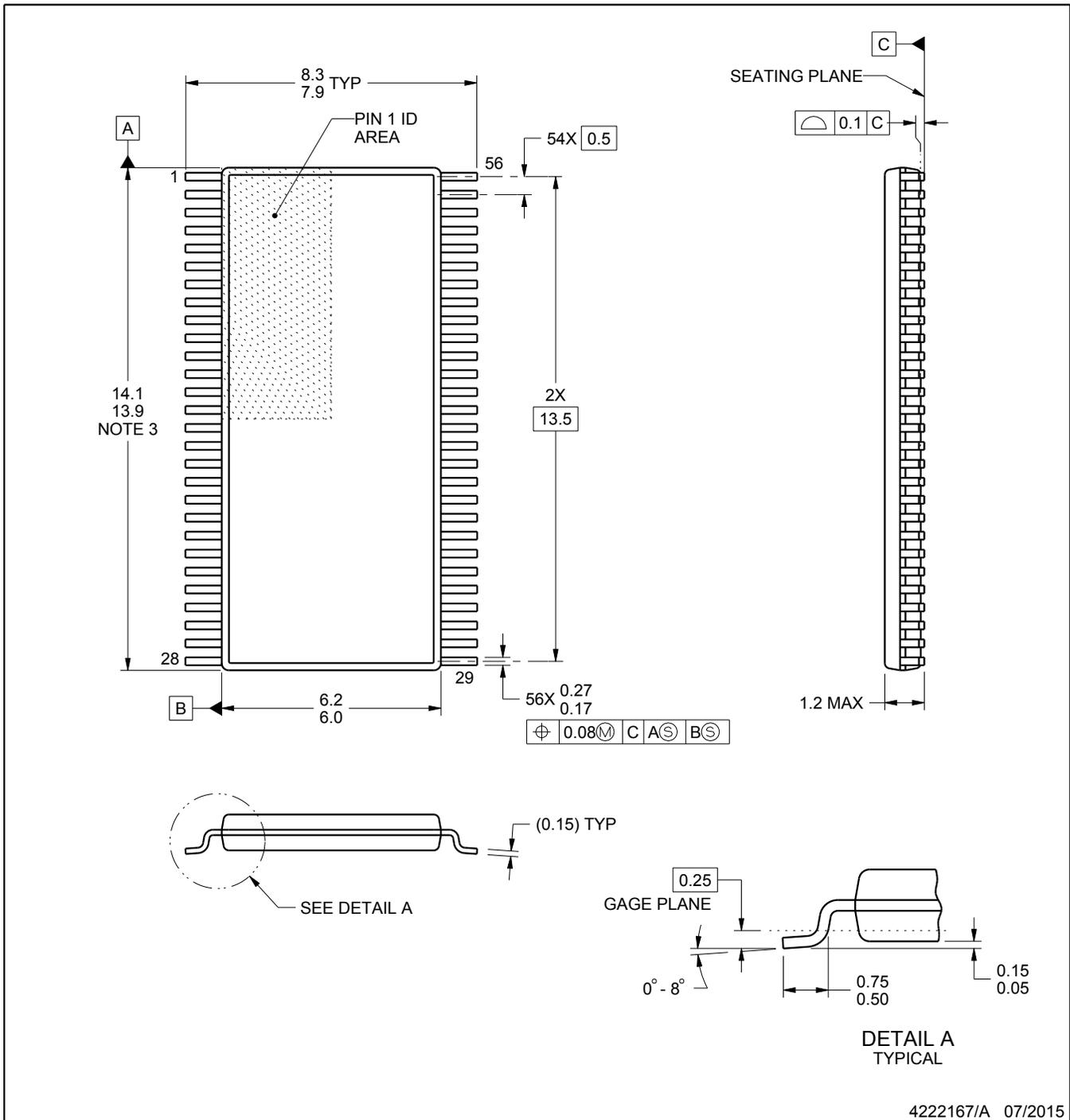

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C383MTDX/NOPB	TSSOP	DGG	56	1000	356.0	356.0	45.0
DS90CF384MTDX/NOPB	TSSOP	DGG	56	1000	356.0	356.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS90C383MTD/NOPB	DGG	TSSOP	56	34	495	10	2540	5.79
DS90C383MTD/NOPB.B	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CF384MTD/NOPB	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CF384MTD/NOPB.B	DGG	TSSOP	56	34	495	10	2540	5.79



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NOTES:

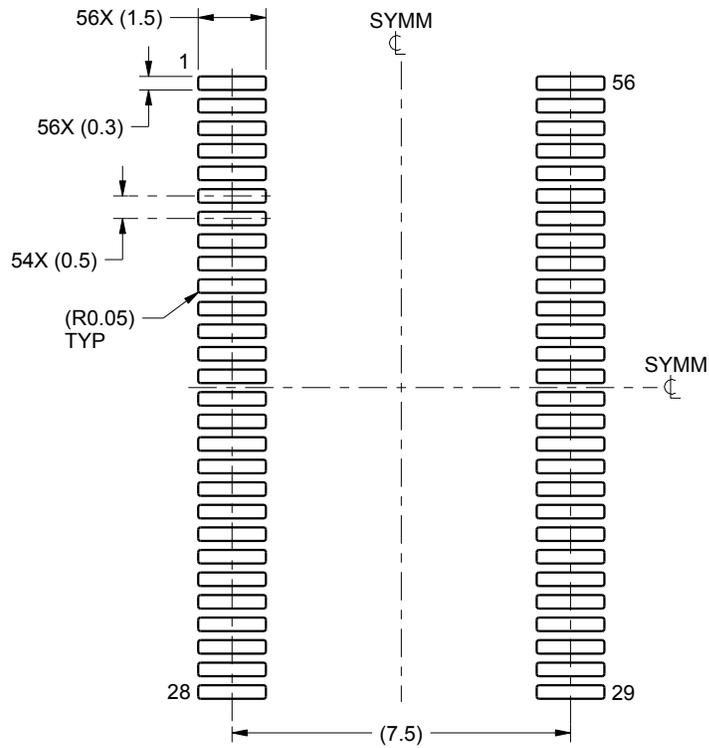
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

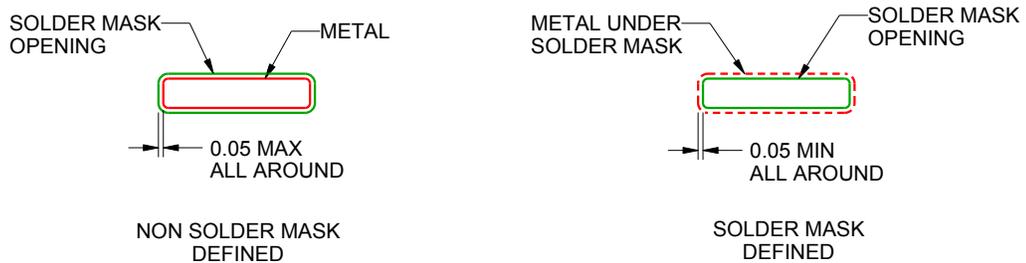
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

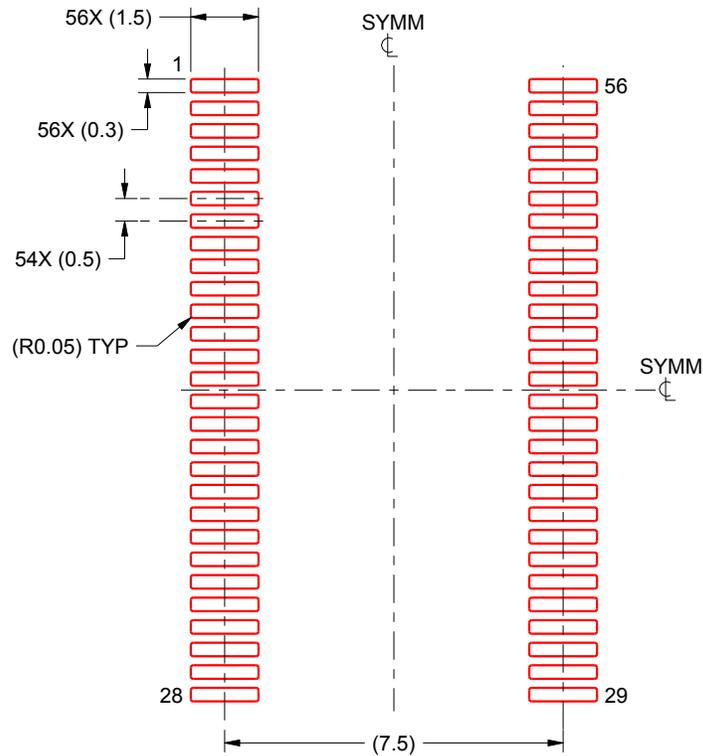
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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