

# TPSF12C3-Q1 Standalone, Active, EMI Filter for Common-mode Noise Mitigation in Three-Phase, AC, Automotive Power Systems

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ambient operating temperature
- **Functional Safety-Capable**
  - [Documentation available to aid functional safety system design](#)
- Voltage-sense, current-inject active EMI filter
  - Optimized for CISPR 25 Class 5 automotive EMI requirements
  - Low impedance for common-mode emissions
  - 50%+ reduction in choke size, weight and cost
  - Peak inject current of  $\pm 80$  mA (typical)
- Wide supply voltage range of 8 V to 16 V
- Junction temperature range of  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$
- Simple configuration for three-phase AC systems
  - Integrated sensing filter and summing network
  - Low leakage current at line frequency
  - Simplified compensation network
- Inherent protection features for robust design
  - Withstands [surge](#) of 6 kV (IEC 61000-4-5) with minimal external component count
  - Enable pin for remote ON and OFF control
  - VDD voltage UVLO protection with hysteresis
  - Thermal shutdown protection with hysteresis
- 4.2-mm × 2-mm SOT-23 14-pin (DYY) package

## 2 Applications

- [On-board charger](#) for BEVs and PHEVs
- [Automotive isolated DC/DC regulators](#)
- [HVAC motor control, aerospace and defense](#)

## 3 Description

The TPSF12C3-Q1 is an active filter IC designed to reduce common-mode (CM) electromagnetic interference (EMI) in three-phase AC power systems.

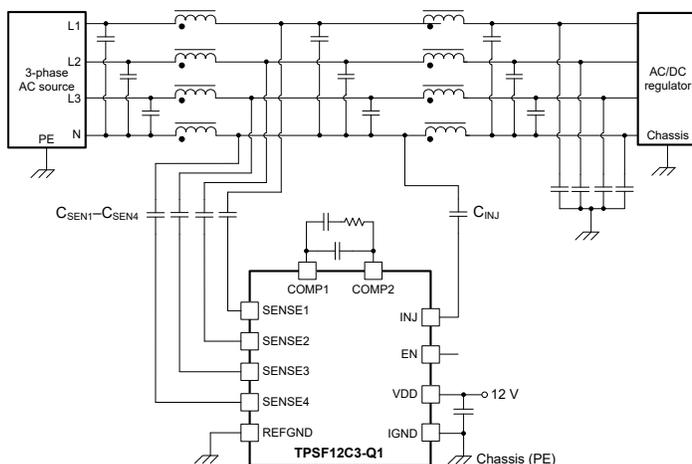
The active EMI filter (AEF) configured with voltage sense and current inject (VSCI) uses a capacitive multiplier circuit to emulate the Y-capacitors in a conventional passive filter design. The device senses the high-frequency noise on each power line using a set of sense capacitors and injects noise-canceling currents back into the power lines using an injection capacitor. The effective active capacitance is set by the circuit gain and the injection capacitance. The AEF sensing and injection impedances use relatively low capacitance values with small component footprints. The device includes integrated filtering, compensation and protection circuitry, and an enable input.

The TPSF12C3-Q1 provides a very low impedance path for CM noise in the frequency range of interest for EMI measurement. Enabling up to 30 dB of CM noise reduction at the lower end of specified frequency ranges (for example, 150 kHz to 3 MHz) significantly reduces the size, weight and cost of the CM filter implementation.

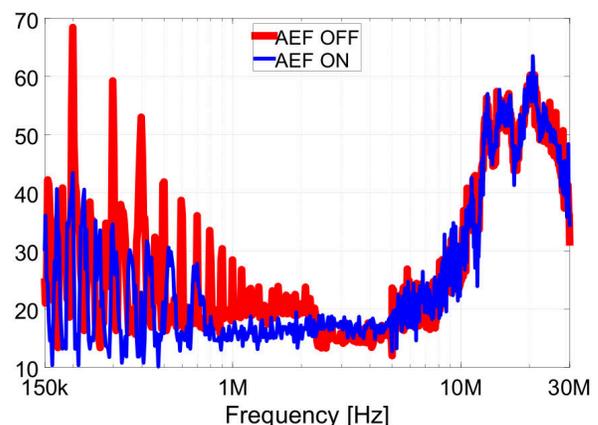
### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
TPSF12C3-Q1	DYY (SOT-23-THIN, 14)	4.20 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Schematic**



**EMI Mitigation Result**



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## 4 Revision History

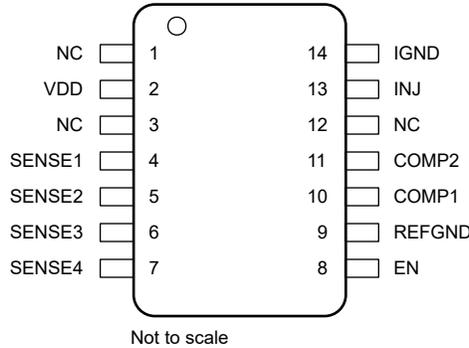
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (January 2023) to Revision A (April 2023)</b>	<b>Page</b>
• Changed status from Advance Information to Production Data.....	1

## 5 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	PHASES	GRADE	JUNCTION TEMPERATURE RANGE
<a href="#">TPSF12C3-Q1</a>	TPSF12C3QDYRQ1	3	Automotive	–40°C to 150°C
<a href="#">TPSF12C1-Q1</a>	TPSF12C1QDYRQ1	1	Automotive	–40°C to 150°C
<a href="#">TPSF12C3</a>	TPSF12C3DYR	3	Commercial	–40°C to 150°C
<a href="#">TPSF12C1</a>	TPSF12C1DYR	1	Commercial	–40°C to 150°C

## 6 Pin Configuration and Functions



**Figure 6-1. 14-Pin SOT-23-THIN DYY Package (Top View)**

**Table 6-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1, 3, 12	NC	–	No internal connection. Tie to the GND plane on the PCB.
2	VDD	P	Power supply for IC. Bypass to IGND with a 1-μF X7R ceramic capacitor.
4	SENSE1	I	Sense input (power line 1, 2, 3, or neutral)
5	SENSE2	I	Sense input (power line 1, 2, 3, or neutral)
6	SENSE3	I	Sense input (power line 1, 2, 3, or neutral)
7	SENSE4	I	Sense input (power line 1, 2, 3, or neutral)
8	EN	I	Enable signal to activate noise cancellation
9	REFGND	G	Reference ground (Kelvin connected to IGND)
10	COMP1	I	Connection 1 for external compensation circuit
11	COMP2	I	Connection 2 for external compensation circuit
13	INJ	O	Injection signal output
14	IGND	G	Injection ground

(1) P = Power, G = Ground, I = Input, O = Output

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Pin voltage	VDD to IGND and REFGND	-0.3	18	V
Pin voltage	SENSE1, SENSE2, SENSE3, SENSE4 to REFGND	-5.5	5.5	V
Pin voltage	COMP1 to IGND and REFGND	-0.3	5.5	V
Pin voltage	COMP2 to IGND and REFGND	-0.3	15	V
Pin voltage	INJ to IGND	-0.3	$V_{\text{VDD}}$	V
Pin voltage	EN to IGND and REFGND	-0.3	18	V
Pin voltage	IGND to REFGND	-0.3	0.3	V
Sink current	INJ		150	mA
Source current	INJ		150	mA
$T_{\text{J}}$	Operating junction temperature	-40	150	$^{\circ}\text{C}$
$T_{\text{stg}}$	Storage temperature	-55	150	$^{\circ}\text{C}$

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 7.2 ESD Ratings

			VALUE	UNIT	
$V_{\text{(ESD)}}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 2	$\pm 2000$	V	
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 7, 8, and 14)		$\pm 750$
			Other pins		$\pm 500$

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{\text{VDD}}$	VDD voltage range	8	12	16	V
$V_{\text{INJ}}$	Output voltage range	2.5		$V_{\text{VDD}} - 2$	V
$V_{\text{SENSE}}$	Sense voltage range	-5		5	V
$V_{\text{EN}}$	Pin voltage	0		16	V
$I_{\text{INJ}}$	Output current range			80	mA
			Source and sink magnitude		
$T_{\text{A}}$	Operating ambient temperature	-40		105	$^{\circ}\text{C}$

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DYY (SOT-23-THIN)	UNIT
		14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	94	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	43	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	30	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	28	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

Limits apply over the junction temperature (T<sub>J</sub>) range of –40°C to 150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T<sub>J</sub> = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V<sub>VDD</sub> = 12 V<sup>(1)</sup>.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY</b>						
I <sub>Q</sub>	VDD quiescent current	SENSE1, SENSE2, SENSE3, and SENSE4 grounded, V <sub>EN</sub> = 5 V, 8 V ≤ V <sub>VDD</sub> ≤ 16 V	6.25	13.2	25.5	mA
		SENSE1, SENSE2, SENSE3, and SENSE4 grounded, V <sub>EN</sub> = 5 V, V <sub>VDD</sub> = 12 V, T <sub>J</sub> = 25°C	11	13.2	15.5	
I <sub>SD</sub>	VDD shutdown supply current	V <sub>EN</sub> = 0 V	55		μA	
<b>SUPPLY VOLTAGE UVLO</b>						
V <sub>VDD-UV-R</sub>	UVLO rising threshold	V <sub>VDD</sub> rising	7.35	7.7	7.95	V
V <sub>VDD-UV-F</sub>	UVLO falling threshold	V <sub>VDD</sub> falling	6.4	6.7	7.0	V
V <sub>VDD-UV-HYS</sub>	UVLO hysteresis		0.97			V
<b>ENABLE</b>						
V <sub>EN-H</sub>	EN voltage high		2.2		V	
V <sub>EN-L</sub>	EN voltage low			0.8	V	
R <sub>EN</sub>	EN pin pull-up resistance to VDD	V <sub>EN</sub> = 0 V	850		kΩ	
I <sub>EN-LKG</sub>	EN input leakage current	V <sub>EN</sub> = 12 V	840		nA	
<b>INPUT FILTER NETWORK</b>						
A <sub>CM</sub>	Gain from shorted power lines through single sense cap, C <sub>SEN</sub> , to COMP1 vs. REFGND	C <sub>SEN</sub> = 2 μF <sup>(2)</sup> , 60 Hz		–44	dB	
		C <sub>SEN</sub> = 2 μF <sup>(2)</sup> , 50 kHz		–4		
		C <sub>SEN</sub> = 2 μF <sup>(2)</sup> , 500 kHz <sup>(3)</sup>		–2		
		C <sub>SEN</sub> = 2 μF <sup>(2)</sup> , 1 MHz <sup>(3)</sup>		–1		

## 7.5 Electrical Characteristics (continued)

Limits apply over the junction temperature ( $T_J$ ) range of  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}\text{C}$ , and are provided for reference purposes only. Unless otherwise stated, the following conditions apply:  $V_{\text{VDD}} = 12\text{ V}^{(1)}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{\text{DM}}$	Gain from differential signal applied to SENSE lines to COMP1 vs. REFGND	SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, $C_{\text{SEN1}} = C_{\text{SEN3}} = 1\ \mu\text{F}^{(2)}$ , 60 Hz		-71		dB
		SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, $C_{\text{SEN1}} = C_{\text{SEN3}} = 1\ \mu\text{F}^{(2)}$ , 1 kHz		-59		
		SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, $C_{\text{SEN1}} = C_{\text{SEN3}} = 1\ \mu\text{F}^{(2)}$ , 500 kHz <sup>(3)</sup>		-42		
		SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, $C_{\text{SEN1}} = C_{\text{SEN3}} = 1\ \mu\text{F}^{(2)}$ , 1 MHz <sup>(3)</sup>		-43		
		SENSE1 shorted to SENSE2, SENSE3 shorted to SENSE4, $C_{\text{SEN1}} = C_{\text{SEN3}} = 1\ \mu\text{F}^{(2)}$ , 10 MHz <sup>(3)</sup>		-35		
<b>AMPLIFIER</b>						
$A_{\text{DC}}$	DC gain		52	58	69	dB
$f_{\text{BW}}$	Unity gain bandwidth <sup>(3)</sup>			113		MHz
$f_{\text{BW}40}$	40 dB gain frequency			1		MHz
$V_{\text{OFST}}$	COMP1 offset voltage			2		V
$V_{\text{INJ-MAX}}$	Maximum output voltage for linear operation <sup>(3)</sup>	COMP2 to INJ gain > 36 dB	$V_{\text{VDD}} - 2$			V
$V_{\text{INJ-MIN}}$	Minimum output voltage for linear operation <sup>(3)</sup>	COMP2 to INJ gain > 36 dB			2.5	V
$I_{\text{INJ-MAX-OP}}$	INJ current at linearity limits <sup>(3)</sup>	$V_{\text{INJ}} = V_{\text{VDD}} - 2\text{ V}$	80			mA
		$V_{\text{INJ}} = V_{\text{IGND}} + 2.5\text{ V}$			-80	mA
<b>PSRR</b>						
$\text{PSRR}_{10}$		10 pF in parallel with the series combination of 10 nF and 2 k $\Omega$ between COMP1 and COMP2, 10 kHz		0		dB
$\text{PSRR}_{100}$		10 pF in parallel with the series combination of 10 nF and 2 k $\Omega$ between COMP1 and COMP2, 100 kHz		6		
<b>STARTUP</b>						
$t_{\text{W}}$	Startup delay <sup>(3)</sup>	Time from VDD = EN applied until output valid		43		ms
$t_{\text{SU}}$	EN high to valid output			42		ms
$t_{\text{SD}}$	EN low to stop output signal			0.32		$\mu\text{s}$
<b>THERMAL SHUTDOWN</b>						
$T_{\text{J-SHD}}$	Thermal shutdown threshold <sup>(3)</sup>	Temperature rising		175		$^{\circ}\text{C}$
$T_{\text{J-HYS}}$	Thermal shutdown hysteresis <sup>(3)</sup>			20		$^{\circ}\text{C}$

- (1) MIN and MAX limits are 100% production tested at  $25^{\circ}\text{C}$  unless otherwise specified. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
- (2) Capacitance chosen for effective test only. Do not use this capacitance in applications.
- (3) Parameter specified by design, statistical analysis and production testing of correlated parameters.

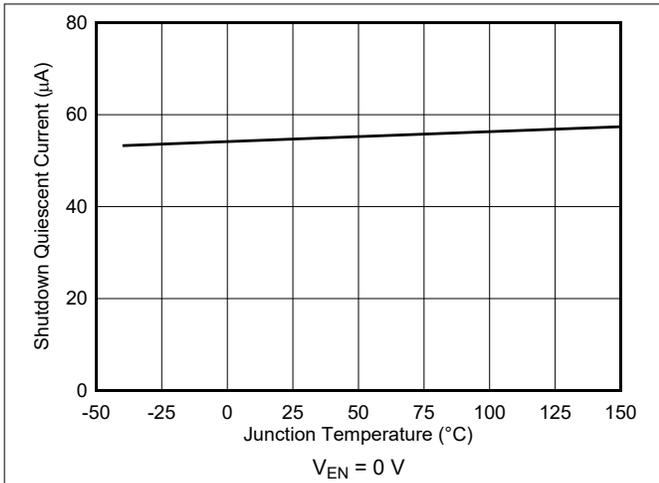
## 7.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 12\text{ V}$  only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ . These specifications are not ensured by production testing.

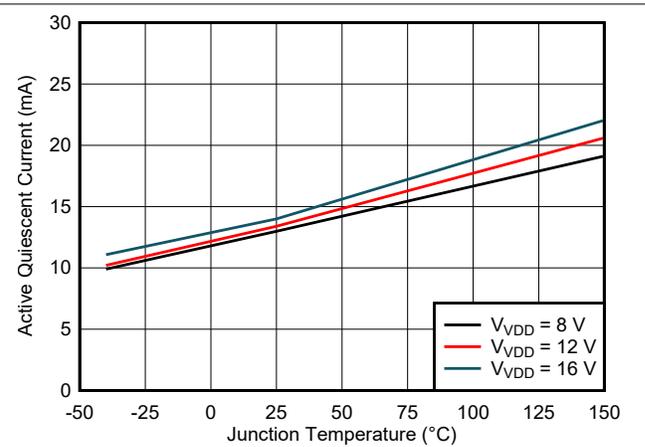
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$I_{\text{SUPPLY}}$	Input supply current with INJ loaded			15		mA

## 7.7 Typical Characteristics

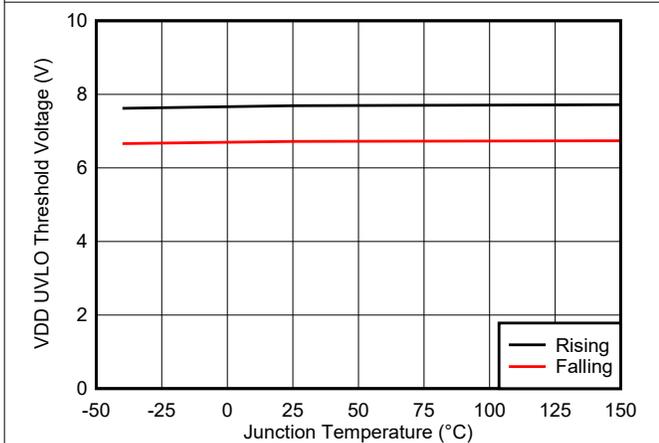
$V_{DD} = V_{EN} = 12\text{ V}$ , unless otherwise specified.



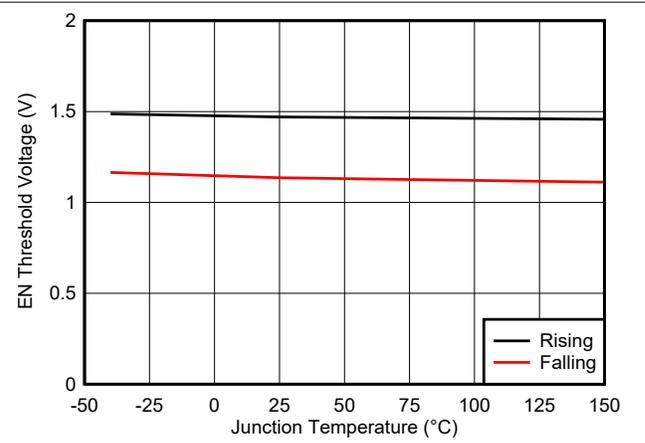
**Figure 7-1. Shutdown Supply Current vs. Temperature**



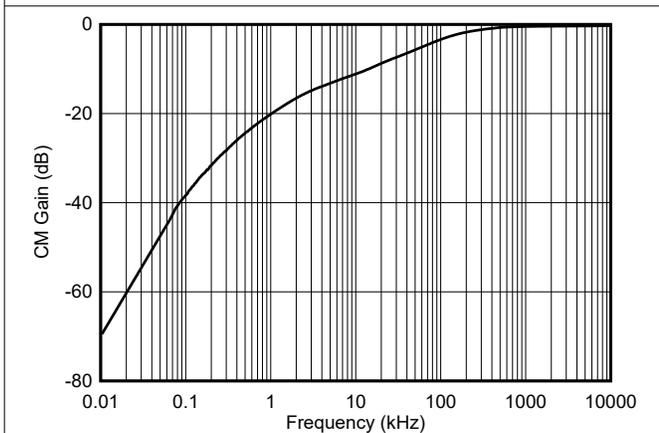
**Figure 7-2. Quiescent Supply Current vs. Temperature**



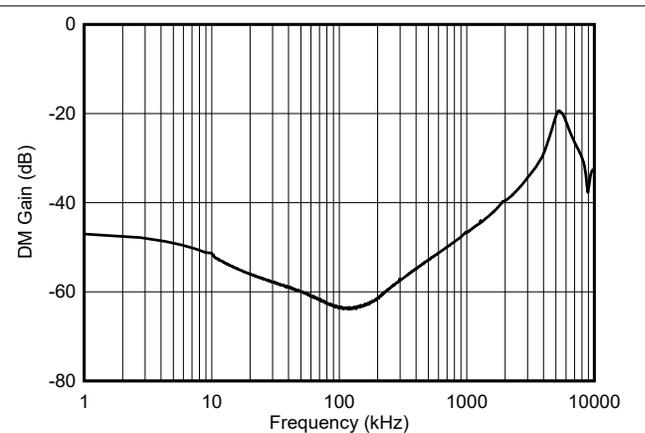
**Figure 7-3. VDD UVLO Thresholds vs. Temperature**



**Figure 7-4. EN Threshold vs. Temperature**



**Figure 7-5. Input Filter Response – Common Mode**



**Figure 7-6. Input Filter Response – Differential Mode**

## 8 Detailed Description

### 8.1 Overview

The TPSF12C3-Q1 is an active electromagnetic interference (EMI) filter that is designed to reduce common-mode (CM) conducted emissions in off-line power converter systems. Using a VSCI architecture, the device senses the high-frequency noise on each power line using a set of Y-rated capacitors,  $C_{SEN1-4}$ , then injects noise-canceling currents back into the power lines using a Y-rated capacitor,  $C_{INJ}$ , along with a damping circuit that ensures stability. The device includes integrated filtering, compensation and protection circuitry.

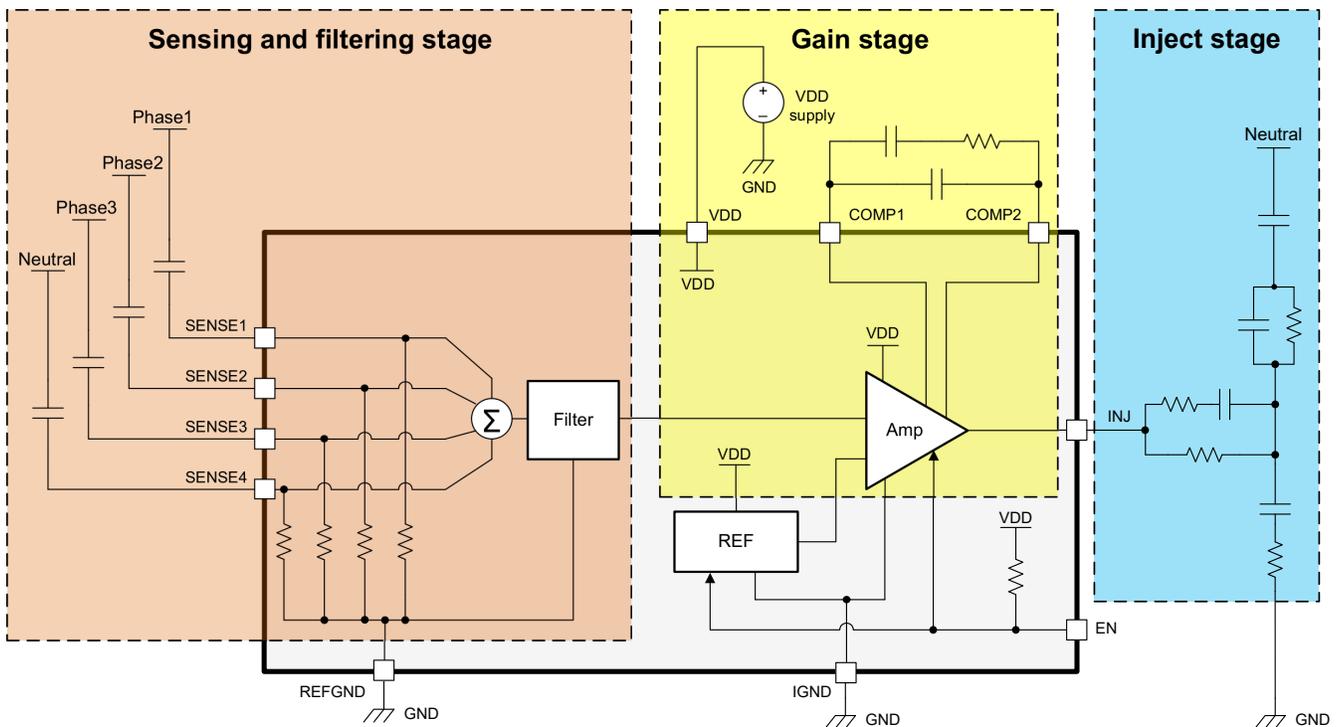
The TPSF12C3-Q1 provides a low-impedance shunt path for CM noise in the frequency range of interest for EMI measurement. This feature can achieve approximately 15 to 30 dB of CM attenuation over the applicable frequency range (for example, 100 kHz to 3 MHz) helping to reduce the size of CM chokes, typically the largest components in the filter.

The TPSF12C3-Q1 operates over a supply voltage range of 8 V to 16 V and can withstand 18 V. The device features include:

- Internal circuitry that simplifies compensation and design
- Built-in supply voltage UVLO to ensure proper operation
- Built-in thermal shutdown protection
- An EN input that allows power saving when the system is idling

The active EMI filter circuit significantly reduces EMI filter cost, size, and weight, while helping to meet CISPR 25 Class 5 limits for conducted emissions. Leveraging a pin arrangement designed for simple layout that requires relatively few external components, the TPSF12C3-Q1 is specified for maximum ambient and junction temperatures of 105°C and 150°C, respectively.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Active EMI Filtering

A compact and efficient design of the input EMI filter is one of the main challenges in high-density switching regulator design and is critical to achieving the full benefits of electrification in highly constrained

system environments such as automotive. For AC-input applications in general, CM chokes and Y-capacitors provide CM filtering, whereas the leakage inductance of the CM chokes and the X-capacitors provide DM filtering. However, CM filters for such applications may have limited Y-capacitance due to touch-current safety requirements and thus require large-sized CM chokes to achieve the requisite attenuation – ultimately resulting in filter designs with bulky, heavy and expensive passive components. Fortunately, the deployment of active filter circuits enable more compact filter solutions for next-generation power conversion systems.

### 8.3.1.1 Schematics

Figure 8-1 and Figure 8-2 show schematics for conventional two-stage passive EMI filters with and without neutral, respectively, in kilowatt-scale, grid-connected applications. L, N and PE refer to the respective live, neutral and protective earth connections. Multistage filters as shown provide high roll-off and are widely used in high-power AC line applications where CM noise is often more challenging to mitigate than DM noise. The low-order switching harmonics usually dictate the size of the reactive filter components based on the required corner frequency (or multiple corner frequencies in multistage designs).

Also included in Figure 8-1 and Figure 8-2 are the corresponding active filter designs. The active circuit replaces the bank of Y-capacitors positioned between the CM chokes with a three-phase AEF circuit using the TPSF12C3-Q1 to provide a lower impedance shunt path for CM currents. The sense pins of the TPSF12C3-Q1 interface with the power lines using a set of Y-rated sense capacitors, typically 680 pF, and feed into an internal high-pass filter and signal combiner. The IC rejects both line-frequency (50-Hz or 60-Hz) AC voltage as well as DM disturbances, while amplifying high-frequency CM disturbances and maintaining closed-loop stability using an external tunable damping circuit.

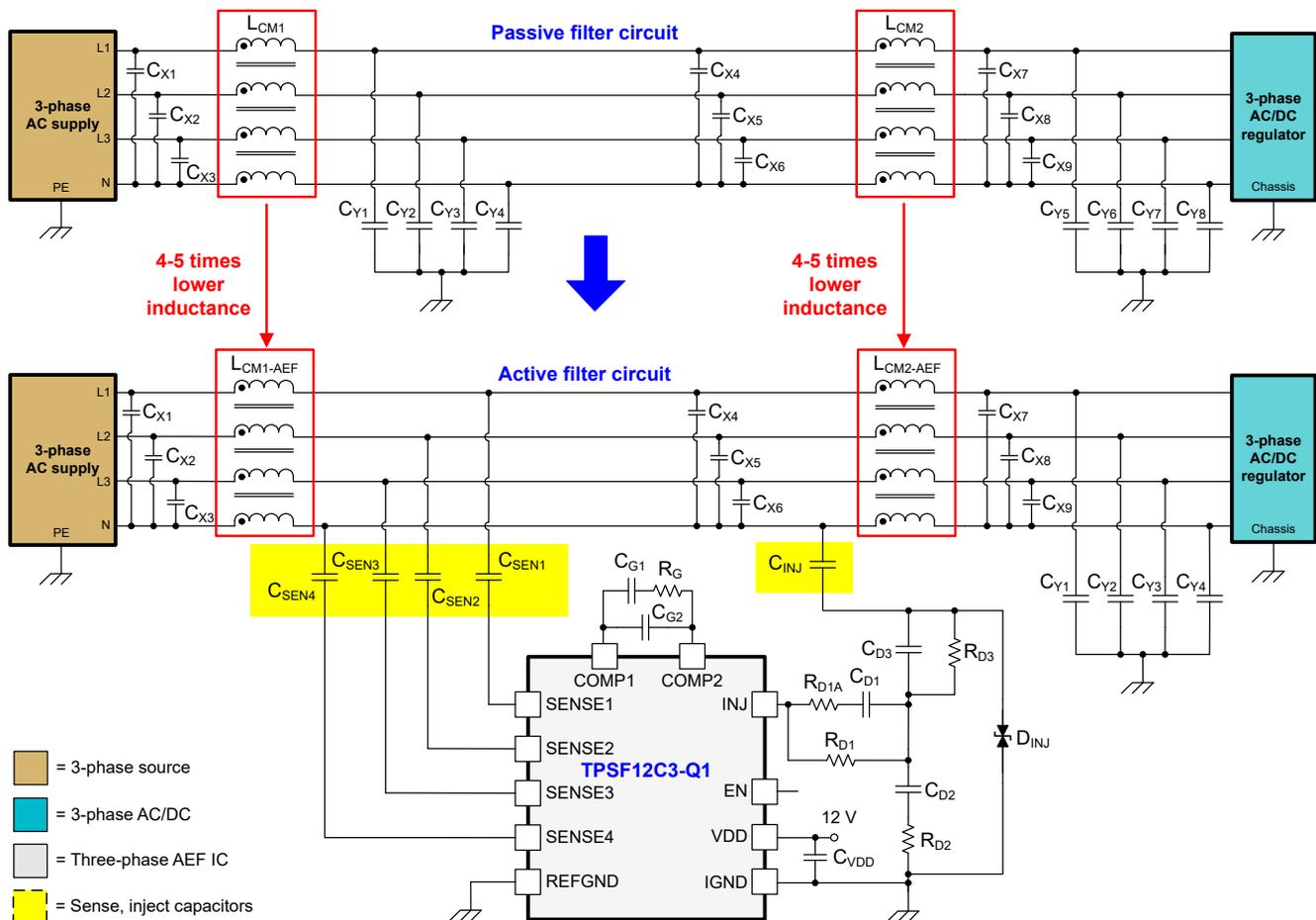
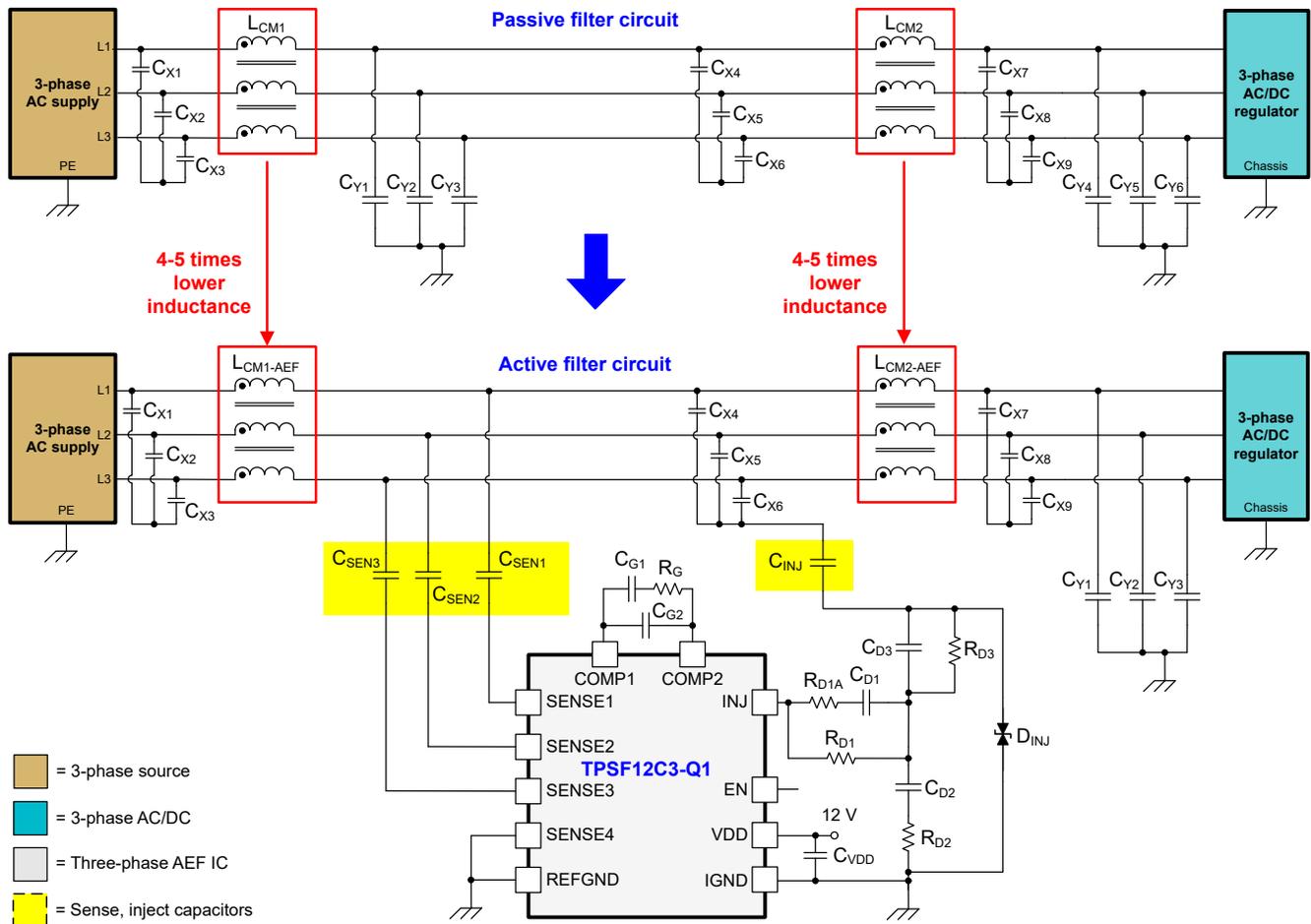


Figure 8-1. Circuit Schematic of a Three-Phase, Four-Wire Passive Filter and Corresponding Active Filter Solution for CM Attenuation



**Figure 8-2. Circuit Schematic of a Three-Phase, Three-Wire Passive Filter and Corresponding Active Filter Solution for CM Attenuation**

The X-capacitors placed between the two CM chokes effectively provide a low-impedance path between the power lines from a CM standpoint, typically up to low-MHz frequencies. This allows current injection onto one power line, typically neutral, using only one inject capacitor. If the three-phase filter is a three-wire system without neutral as shown in Figure 8-2, the SENSE4 pin of the TPSF12C3-Q1 ties to ground and the inject capacitor couples through a star-point connection of the X-capacitors.

### 8.3.2 Capacitive Amplification

An AEF circuit for CM noise mitigation fundamentally either amplifies the apparent inductance of a CM choke or the apparent capacitance of a Y-capacitor over the frequency range of interest. A VSCI AEF circuit configured for CM attenuation uses an amplifier stage as a capacitive multiplier of the inject capacitor,  $C_{INJ}$ . This higher value of the active capacitance supports lower values for the CM chokes to achieve a target attenuation. More specifically, the amplified Y-capacitance enables a reduction of each CM choke inductance by up to 80% (while keeping the filter corner frequencies effectively unchanged), resulting in lower size, weight, and cost of the CM chokes.

Capacitive multiplication of the inject capacitance occurs over a relevant frequency range for low- and mid-frequency emissions, while not impacting the value at low frequency applicable for touch current measurement. The total capacitance of the sense and inject capacitors (highlighted in yellow in Figure 8-1 and Figure 8-2) is kept less than or equal to that of the replaced Y-capacitors in the equivalent passive filter, which results in the total line-frequency leakage current remaining effectively unchanged or reduced.

### 8.3.3 Integrated Line Rejection Filter

The TPSF12C3-Q1 has a built-in input line filter. The high-pass filter stage attenuates the large line-frequency (50 Hz or 60 Hz) components of the power-line voltages, both line-to-line and line-to-earth, thus maximizing the useful voltage range of the low-voltage output at INJ.

The circuit also sums the signals in a CM combiner, rejecting the DM components of the voltages and extracting a signal that represents the CM noise signature without line-frequency components. Combined with the action of the high-pass filter, the net result is that the COMP1 pin voltage represents the sensed high-frequency CM noise that the device attempts to cancel. Because the entire filter is integrated in the device, matching is better than what can be achieved using discrete components.

### 8.3.4 Compensation

The TPSF12C3-Q1 contains partial internal compensation that, when combined with two capacitors and a resistor between COMP1 and COMP2, forms a lead-lag network. This internal network allows fewer external components to be used.

### 8.3.5 Remote Enable

The TPSF12C3-Q1 has an enable input, EN, that allows the device to be shut down, drastically reducing power consumption during intervals when EMI mitigation is not required. The typical quiescent current consumption is 13.2 mA and 55  $\mu$ A when the device is enabled and disabled, respectively. Because many designs may not use this feature, a 850-k $\Omega$  pullup resistor connects internally between VDD and EN, allowing the EN pin to be left open.

In addition, INJ is pulled low when the device is disabled to reduce the effective resistance in series with  $C_{INJ}$ .

### 8.3.6 Supply Voltage UVLO Protection

To ensure that the TPSF12C3-Q1 operates safely while VDD is powered on and off as well as during brownout conditions, this device has a built-in UVLO protection to provide predictable behavior while VDD is below its operating voltage. UVLO releases when the VDD voltage exceeds 7.7 V (typical), allowing normal operation. UVLO engages if the VDD voltage falls below approximately 6.7 V (typical). There is approximately 1 V of UVLO hysteresis.

### 8.3.7 Thermal Shutdown Protection

The TPSF12C3-Q1 provides built-in overtemperature protection that shuts down the device if the junction temperature exceeds approximately 175°C. After the junction temperature decreases by approximately 20°C, the device restarts. This process is repeated until the ambient temperature or power dissipation is reduced. The device has a relatively low thermal time constant and can cycle into and out of thermal shutdown at a high rate during a sustained overtemperature condition.

## 8.4 Device Functional Modes

### 8.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TPSF12C3-Q1. When the EN voltage is below approximately 0.8 V, the device is in shutdown mode. Most internal circuitry is shutdown. The quiescent current in shutdown mode drops to 55  $\mu$ A (typical). The TPSF12C3-Q1 also employs VDD internal undervoltage protection. If the VDD voltage is below its UVLO threshold, the device remains off. The INJ output pulls to ground while in shutdown mode.

### 8.4.2 Active Mode

The TPSF12C3-Q1 is in active mode when  $V_{VDD}$  is above its UVLO threshold, EN is high, and there is no overtemperature fault. The simplest way to enable operation is to connect EN to VDD, which allows startup when the applied supply voltage exceeds the UVLO threshold voltage. In this mode, the device amplifies signals on COMP2 and outputs the amplified signal on the INJ pin.

## 9 Applications and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The TPSF12C3-Q1 common-mode AEF IC helps to improve the CM EMI signature of three-phase AC power systems. The device provides a very low impedance path for CM noise in the frequency range of interest for EMI measurement and helps to meet prescribed limits for EMI standards, such as:

- CISPR 11, EN 55011 – Industrial, Scientific and Medical (ISM) applications
- CISPR 25, EN 55025 – Automotive applications
- CISPR 32, EN 55032 – Multimedia applications

To expedite and streamline the process of designing of a TPSF12C3-Q1-based solution, a comprehensive TPSF12C3-Q1 [quickstart calculator](#) is available by download to assist the system designer with component selection for a given application.

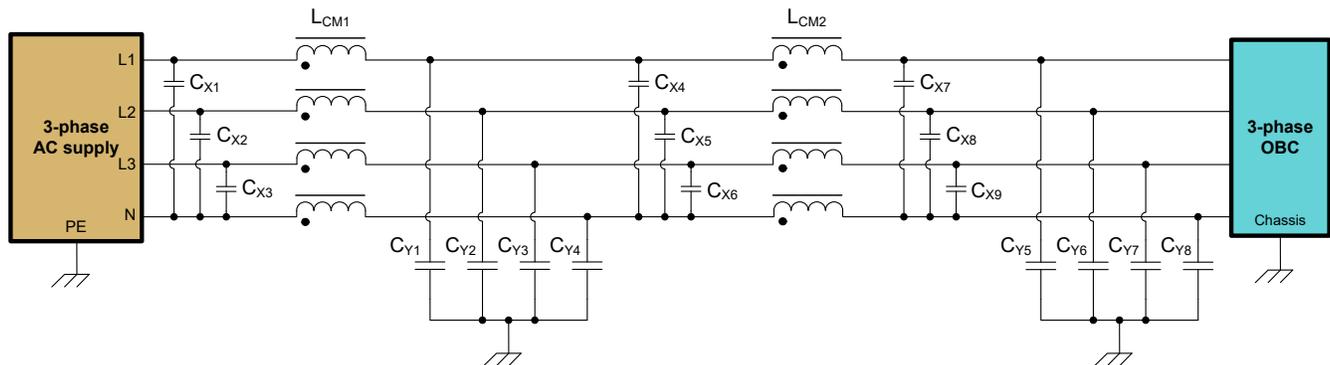
### 9.2 Typical Applications

For the circuit schematic, bill of materials, PCB layout files, and test results of a TPSF12C3-Q1-powered implementation, see the TPSF12C3-Q1 [EVM](#).

#### 9.2.1 Design 1 – AEF Circuit for High-Density On-Board Charger (OBC) in Electric Vehicles (EVs)

[Figure 9-1](#) shows a schematic diagram of a 22-kW high-density OBC with conventional two-stage passive EMI filter. The CM chokes and Y-capacitors provide CM filtering, whereas the leakage inductance of the CM chokes and the X-capacitors provide DM filtering. The circuit uses a three-phase power-factor correction (PFC) front-end followed by a full-bridge CLLLC topology with active synchronous rectification.

The PFC stage runs at a fixed switching frequency of 100 kHz. The CLLLC isolated DC/DC stage runs at a variable frequency from 200 kHz to 800 kHz (500-kHz nominal) and provides galvanic isolation in addition to battery voltage and current regulation. Even though the use of GaN or SiC power switches enables a high power density, the conventional passive EMI filter typically occupies over 20% of the total solution size.

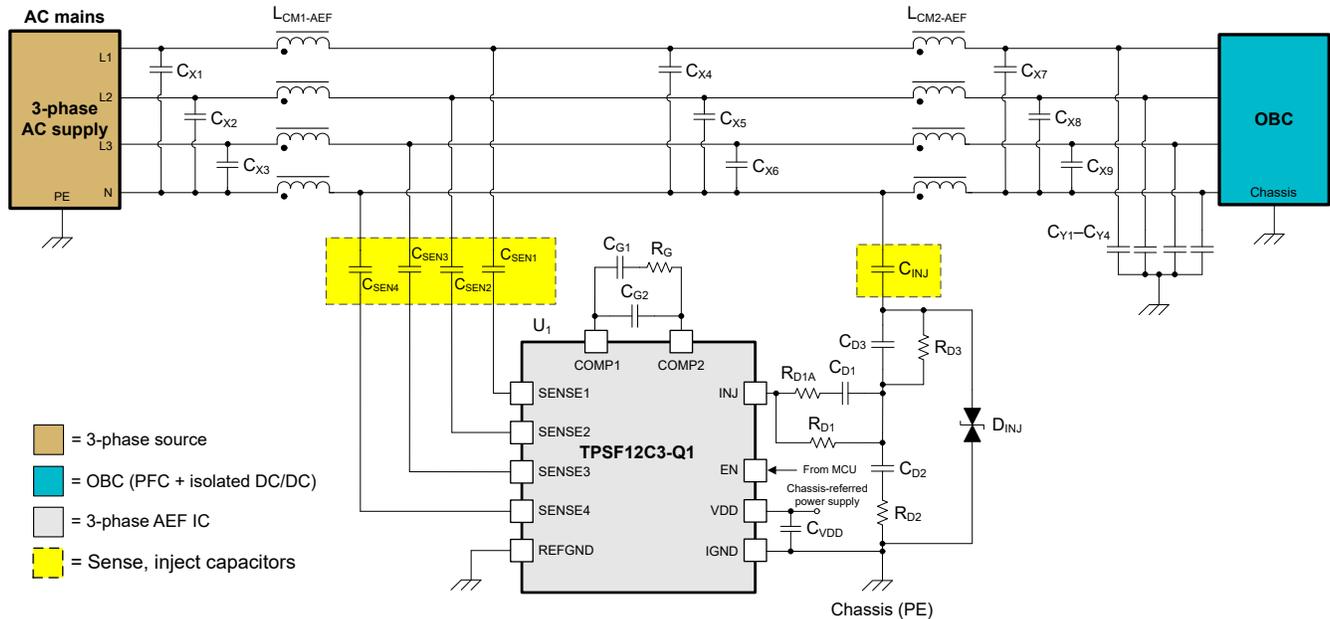


**Figure 9-1. Circuit Schematic of a Three-phase OBC With a Conventional Two-Stage Passive EMI Filter**

Note that the DC/DC stage in particular increases the CM EMI signature based on the high  $dv/dt$  of the GaN power switches, the transformer interwinding capacitance as well as the various switch-node parasitic capacitances to chassis ground.

This application example replaces the four Y-capacitors, designated as  $C_{Y1}$ ,  $C_{Y2}$ ,  $C_{Y3}$  and  $C_{Y4}$  in [Figure 9-1](#), with a three-phase AEF circuit using the TPSF12C3-Q1. See [Figure 9-2](#). The AEF circuit effectively provides

capacitive multiplication of the inject capacitor, which reduces the CM inductance values to maintain the target LC corner frequencies and thus the size, weight, and cost of the CM chokes, now designated as  $L_{CM1-AEF}$  and  $L_{CM2-AEF}$ . The total capacitance of the sense and inject capacitors is kept less than or equal to that of the replaced Y-capacitors, which results in the total line-frequency leakage current remaining effectively unchanged or reduced.



**Figure 9-2. Circuit Schematic of a Three-phase OBC With AEF Circuit Connected**

### 9.2.1.1 Design Requirements

Table 9-1 shows the intended operating parameters for this application example. Also included is the total Y-rated filter capacitance that is allowed in order to meet the applicable touch current fault specification.

**Table 9-1. Design Parameters**

DESIGN PARAMETER	VALUE
AC input voltage	230 V L-N or 400 V L-L (RMS)
AC input line frequency	47 Hz to 63 Hz
DC output voltage range	250 V to 450 V
Rated output power	22 kW
Output current (maximum)	60 A
AC/DC stage switching frequency (fixed)	100 kHz
DC/DC stage switching frequency (variable)	200 kHz to 800 kHz
Total Y-rated filter capacitance (maximum)	10 nF

### 9.2.1.2 Detailed Design Procedure

Table 9-2 gives the selected component values, which are the same as those used in the TPSF12C3-Q1 EVM. This design uses a TVS diode placed at the low-voltage side of the inject capacitor for clamping during input surge conditions.

**Table 9-2. AEF Circuit Components for Application Circuit 1**

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER <sup>(1)</sup>	PART NUMBER
C <sub>SEN1</sub> , C <sub>SEN2</sub> , C <sub>SEN3</sub> , C <sub>SEN4</sub> <sup>(2)</sup>	4	Capacitor, ceramic, 680 pF, 300 VAC, Y2	MuRata	DE2B3SA681KN3AX02F
C <sub>INJ</sub> <sup>(2)</sup>	1	Capacitor, ceramic, 4.7 nF, 300 VAC, Y2	MuRata	DE2E3SA472MA3BX02F
C <sub>D1</sub> <sup>(2)</sup>	1	Capacitor, ceramic, 4.7 nF, 50 V, 0603	Various	–
C <sub>D2</sub> <sup>(2)</sup>	1	Capacitor, ceramic, 22 nF, 50 V, 0603	Various	–
C <sub>D3</sub>	1	Capacitor, ceramic, 4.7 nF, 50 V, 0603	Various	–
C <sub>G1</sub>	1	Capacitor, ceramic, 10 nF, 50 V, 0603	Various	–
C <sub>G2</sub>	1	Capacitor, ceramic, 10 pF, 50 V, 0603	Various	–
C <sub>VDD</sub>	1	Capacitor, ceramic, 1 μF, 25 V, X7R, 0603	Various	–
D <sub>INJ</sub>	1	TVS diode, bidirectional, 24 V, SOD-323	Eaton	STS321240B301
R <sub>D1</sub>	1	Resistor, 1 kΩ, 0.1 W, 0603	Various	–
R <sub>D1A</sub>	1	Resistor, 50 Ω, 0.1 W, 0603	Various	–
R <sub>D2</sub>	1	Resistor, 200 Ω, 0.1 W, 0603	Various	–
R <sub>D3</sub>	1	Resistor, 698 Ω, 0.1 W, 0603	Various	–
R <sub>G</sub>	1	Resistor, 1.5 kΩ, 0.1 W, 0603	Various	–
U <sub>1</sub>	1	TPSF12C3-Q1 common-mode AEF IC for three-phase AC power systems	Texas Instruments	TPSF12C3QDYRQ1

(1) See the [Third-Party Products Disclaimer](#).

(2) Check the effective capacitance value based on the applied voltage and operating temperature.

More generally, the TPSF12C3-Q1 AEF IC is designed to operate with a wide range of passive filter components and system parameters.

#### 9.2.1.2.1 Sense Capacitors

The sense pins of the TPSF12C3-Q1 feed into a high-pass filter and signal combiner within the IC, which rejects the line-frequency and DM components of the power line voltages, extracting the high-frequency CM component.

The sense pins externally interface to the power lines using Y-rated capacitors, designated as C<sub>SEN1</sub>, C<sub>SEN2</sub>, C<sub>SEN3</sub> and C<sub>SEN4</sub> in Figure 9-2. Choose Y2-rated sense capacitors of 680 pF, 300 VAC in this application to establish voltages at the SENSE pins of less than 1-V peak-to-peak when operating at maximum line voltage.

#### 9.2.1.2.2 Inject Capacitor

The INJ node interfaces to a power line using a Y-rated capacitor, designated as C<sub>INJ</sub> in Figure 9-2. Choose a Y2-rated inject capacitor of 4.7 nF, 300 VAC in this design to accommodate an AC voltage swing at INJ with at least a 2.5-V margin of headroom from the positive and negative supply rails. The INJ pin biases at half the VDD supply voltage. Assuming a 12-V supply rail and allowing 2.5 V of upper and lower headroom, this implies that a swing of ±3.5 V is available around the DC operating midpoint.

#### Note

Many commercially available Y-rated capacitors yield an effective capacitance that derates significantly with operating temperature. The effective capacitance value can be much lower than the nameplate capacitance, particularly when operating near the boundaries of the rated operating temperature range. Select the dielectric of the sense and inject capacitors to meet the required temperature range. Depending on the implementation, lower than expected sense and inject capacitances can affect the stability performance.



where the term  $G_{AEF}$  is the gain from the power lines to the INJ node (see the TPSF12C3-Q1 [quickstart calculator](#) for related detail).

Equation 1 shows that the impedance  $Z_{INJ}$  appears in series with  $Z_{D3}$  and a parallel combination of  $Z_{D1}$  and  $Z_{D2}$ . Furthermore, the gain  $G_{AEF}$  is reduced by the voltage divider ratio between  $Z_{D2}$  and  $Z_{D1}$ . These effects combine to increase the effective impedance of the AEF and hence reduce its attenuation performance, thus illustrating a trade-off between performance and stability.

So while an injection network is needed for stability, it also adds impedance in series with the inject capacitor, thus compromising EMI mitigation. As shown below, the user can minimize the impact on performance with careful and appropriate design.

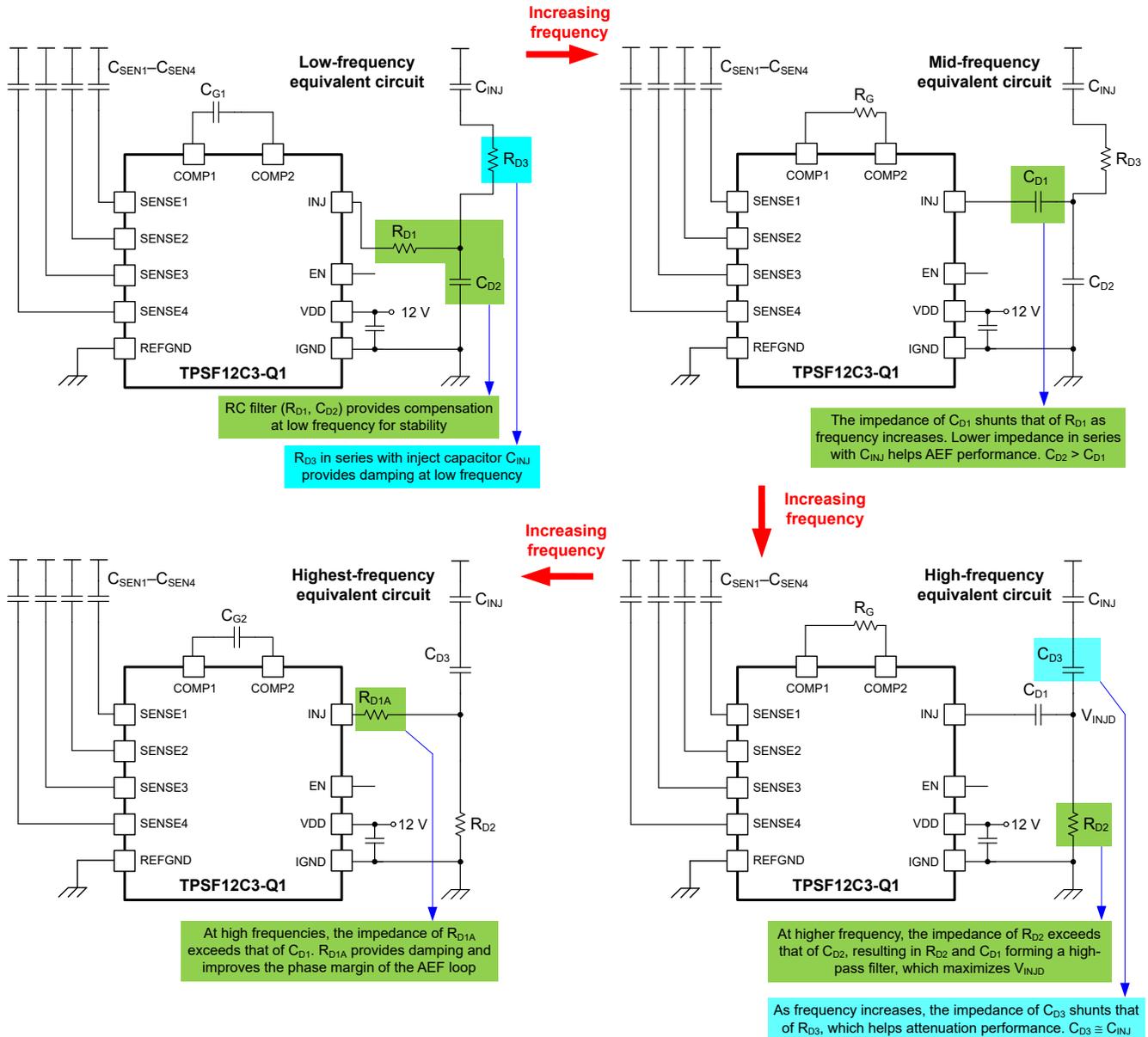


Figure 9-4. Dominant Components of the Injection Network vs Frequency

Illustrated in Figure 9-4, at low frequencies in the range of 5 kHz to 50 kHz, components  $R_{D1}$  and  $C_{D2}$  provide compensation and  $R_{D3}$  damps the effects of LC resonance. At higher frequencies (above 10 kHz), the dominant component impedance of each branch transitions to enable better attenuation performance:

- $R_{D1}$  transitions to  $C_{D1}$

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- $C_{D2}$  transitions to  $R_{D2}$
- $R_{D3}$  transitions to  $C_{D3}$

Finally,  $C_{D1}$  transitions to  $R_{D1A}$  if needed for phase margin of the AEF loop at high frequencies, typically above 100 kHz. When viewed in a clockwise direction, [Figure 9-4](#) shows these transitions in sequence as frequency increases.

Below are basic guidelines to select the component values for the injection network:

1. The undamped loop gain characteristic is likely to be unstable within the range of 5 kHz to 50 kHz, which, as mentioned previously, relates to an LC resonance between CM choke inductance and inject capacitance. Observe from circuit simulation – or by using the TPSF12C3-Q1 [quickstart calculator](#) – the frequency,  $f_{LFstability}$ , at which the phase crosses  $-180^\circ$  with positive gain, indicating negative gain margin.
2. Choose a corner frequency with  $R_{D1}$  and  $C_{D2}$  equal to one fifth of the instability frequency:

$$\frac{1}{2\pi \cdot R_{D1} \cdot C_{D2}} = \frac{f_{LFstability}}{5} \quad (2)$$

Assigning  $R_{D1} = 1 \text{ k}\Omega$  and assuming instability at 35 kHz, use [Equation 3](#) to find a value for the capacitance of  $C_{D2}$ :

$$C_{D2} [\text{nF}] = \frac{5000}{2\pi \cdot R_{D1} [\text{k}\Omega] \cdot f_{LFstability} [\text{kHz}]} = \frac{5000}{2\pi \cdot 1 \cdot 35} = 22 \text{ nF} \quad (3)$$

3. Select  $C_{D1} < C_{D2}$ , where a typical choice is  $C_{D1} = C_{D2}/5 = 4.7 \text{ nF}$ .
4. Choose the resistance of  $R_{D2}$  such that the  $R_{D2}, C_{D2}$  corner frequency is equal to that of  $R_{D1}, C_{D1}$ :

$$R_{D2} [\Omega] = \frac{R_{D1} [\Omega] \cdot C_{D1} [\text{nF}]}{C_{D2} [\text{nF}]} = \frac{R_{D1} [\Omega]}{5} = \frac{1000}{5} = 200 \Omega \quad (4)$$

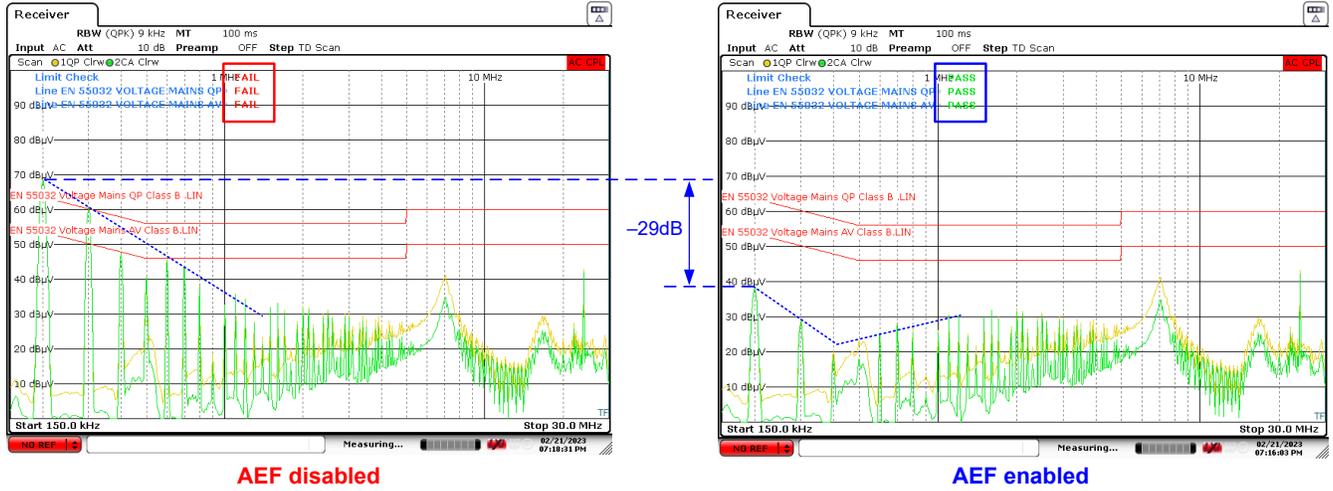
5. Select the resistance of  $R_{D3}$  to damp the resonance around the instability frequency,  $f_{LFstability}$ .
  - A typical choice for  $R_{D3}$  is 500  $\Omega$  to 1 k $\Omega$ .
  - Assign  $C_{D3}$  equal to  $C_{INJ}$  or a suitable value such that the  $R_{D3}, C_{D3}$  corner frequency is less than switching frequency.
  - A lower resistance for  $R_{D3}$  results in more damping but at the penalty of reduced high-frequency attenuation (or forces a higher value for  $C_{D3}$  to maintain the applicable corner frequency below the switching frequency).
6. Select a resistance for  $R_{D1A}$  of 50  $\Omega$  to improve the phase margin of the AEF loop (if needed).

#### 9.2.1.2.5 Surge Protection

EMI filter designs, both passive and active, typically use MOVs connected from the power lines to chassis ground to clamp surge voltage transients. While the sense pins of the TPSF12C3-Q1 have internal clamp protection, the higher value of inject capacitance produces larger currents during surge events and thus requires external protection. Place a bidirectional TVS diode on the low-voltage side of the inject capacitor with standoff voltage of 24 V. Using the SOD-323 packaged device given in [Table 9-2](#), clamping occurs at 40 V and 50 V with surge currents of 1 A and 8 A, respectively.

### 9.2.1.3 Application Curves

Unless otherwise indicated,  $V_{DD} = V_{EN} = 12\text{ V}$ .



#### Note

A high DM noise signature may mask improvement in CM noise performance related to AEF. A reduction of CM choke inductance may also reduce leakage inductance, which could impact DM noise attenuation. Install higher X-capacitance or a discrete DM filter inductor to manage DM attenuation as needed. Also, use a DM-CM noise splitter to isolate the CM component of the measured total noise.

Figure 9-5. EMI Mitigation Result with AEF On and Off (EN Tied High and Low)

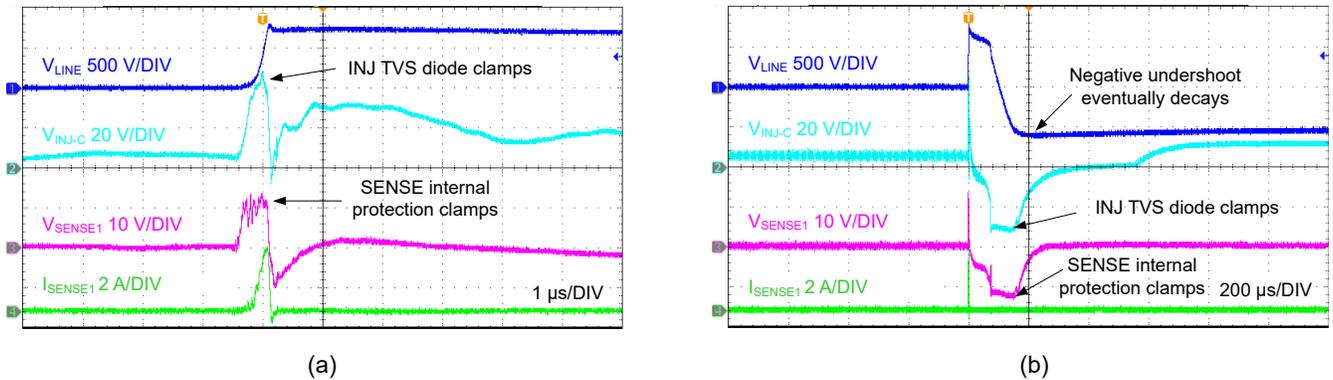


Figure 9-6. IEC 61000-4-5 Positive Surge, 5-kV Single Strike – 1 μs/div (a), 200 μs/div (b)

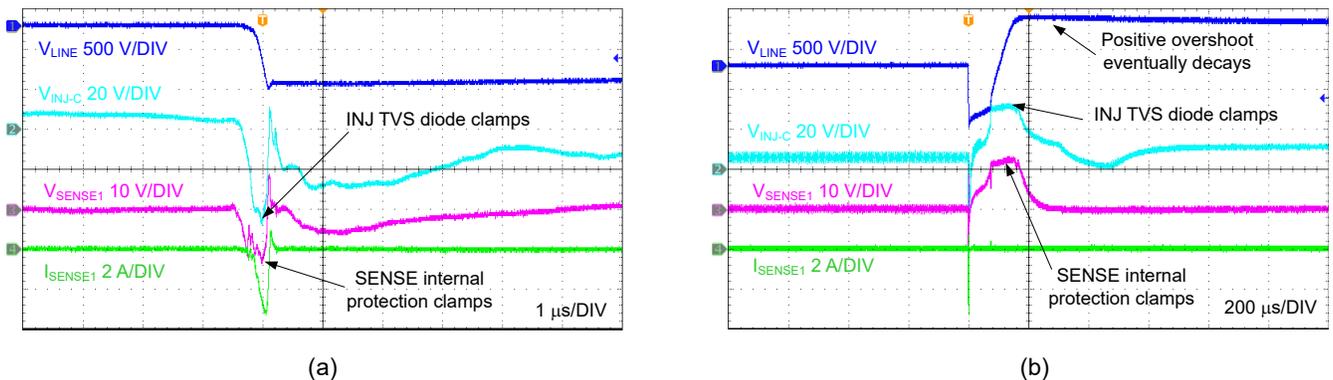
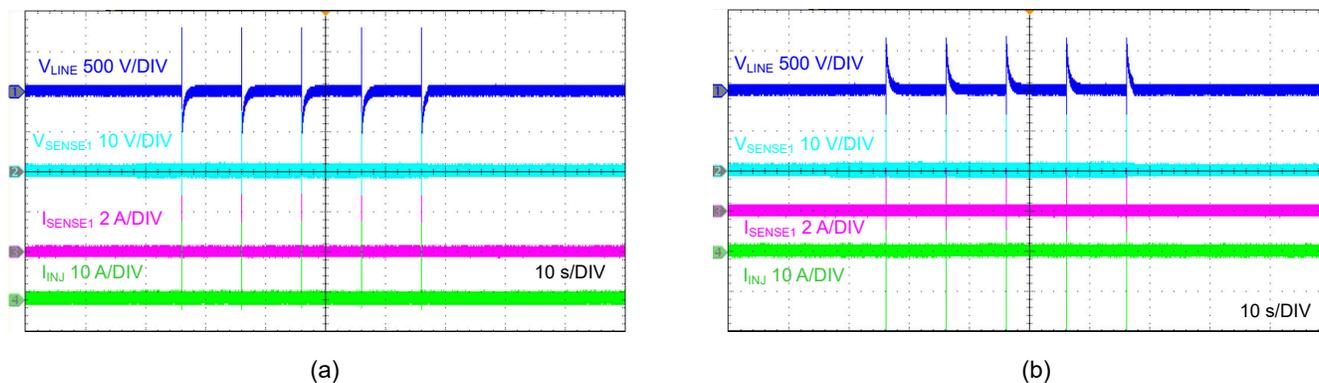


Figure 9-7. IEC 61000-4-5 Negative Surge, 5-kV Single Strike – 1 μs/div (a), 200 μs/div (b)



**Figure 9-8. IEC 61000-4-5 Surge, 5-kV Repetitive Strike at 10-Second Intervals – Positive (a), Negative (b)**

#### Note

The surge test circuit used MOVs (Littelfuse V20E300P) connected from line and neutral filter inputs to chassis ground. See [Figure 9-11](#).

### 9.3 Power Supply Recommendations

The TPSF12C3-Q1 AEF IC operates over a wide supply voltage range of 8 V to 16 V (typically 12 V) and is referenced to chassis ground of the system. The characteristics of this VDD bias supply must be compatible with the [Absolute Maximum Ratings](#) and [Recommended Operating Conditions](#) in this data sheet. In addition, the VDD supply must be capable of delivering the required supply current to the loaded AEF circuit.

The supply rail can already be present in the system or can be derived using a low-cost solution with an auxiliary winding from an isolated flyback regulator. Connect a ceramic capacitor of at least 1  $\mu\text{F}$  close to the VDD and IGND pins of the TPSF12C3-Q1. Ensure that the ripple voltage at VDD is less than 20 mV peak-to-peak to avoid low-frequency noise amplification.

### 9.4 Layout

Proper PCB design and layout is important in active EMI circuits (where high regulator voltage and current slew rates exist) to achieve reliable device operation and design robustness. Furthermore, the EMI performance of the design depends to a large extent on PCB layout.

#### 9.4.1 Layout Guidelines

The following list summarizes the essential guidelines for PCB layout and component placement to optimize AEF performance. [Figure 9-9](#) and [Figure 9-10](#) show a recommended layout for the TPSF12C3-Q1 circuit specifically with optimized placement and routing of the IC and small-signal components. [Figure 9-11](#) shows an example of a three-phase, four-wire filter board design with CM chokes, X-capacitors, Y-capacitors, protection components (varistors and X-capacitor discharge resistors), and AEF circuit.

- *Position the sense and inject capacitors between the CM chokes near the X-capacitor that couples the injected signal to the other power lines. Avoid placement close to the CM choke windings that may result in parasitic coupling to the sense and inject capacitors.*
- *Maintain adequate clearance spacing between high-voltage and low-voltage traces. As an example, [Figure 9-11](#) has 150 mils (3.8 mm) copper-to-copper spacing from power lines (lives and neutral) to chassis ground.*
- *Route the sense lines S1, S2, S3 and S4 away from the INJ line. Avoid coupling between the sense and inject traces.*
- *Use a solid ground connection between the TPSF12C3-Q1 and the filter board. Minimize parasitic inductance from the AEF circuit return to the chassis ground connections on the board.*
- *Place a ceramic capacitor close to VDD and IGND. Minimize the loop area to the VDD and IGND pins.*
- *Place the compensation network components close to the COMP1 and COMP2 pins. Reduce noise sensitivity of the feedback compensation network path by placing components  $R_G$ ,  $C_{G1}$  and  $C_{G2}$  close to the COMP pins. COMP2 is the inverting input to the AEF amplifier and represents a high-impedance node sensitive to noise.*

- Provide enough PCB area for proper heatsinking. Use sufficient copper area to achieve a low thermal impedance. Provide adequate heatsinking for the TPSF12C3-Q1 to keep the junction temperature below 150°C. A top-side ground plane is an important heat-dissipating area. Use several heat-sinking vias to connect REFGND (pin 9) and IGND (pin 14) to ground copper on other layers.

### 9.4.2 Layout Example

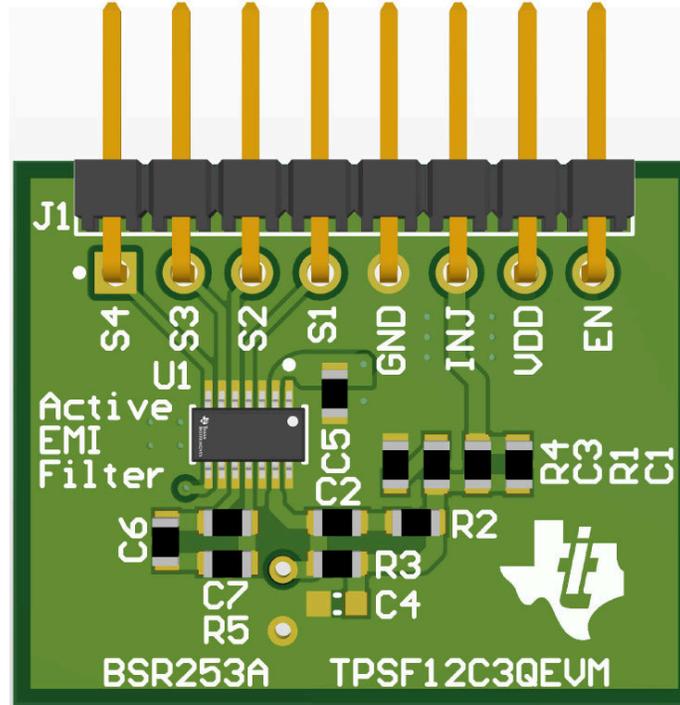


Figure 9-9. Typical Layout

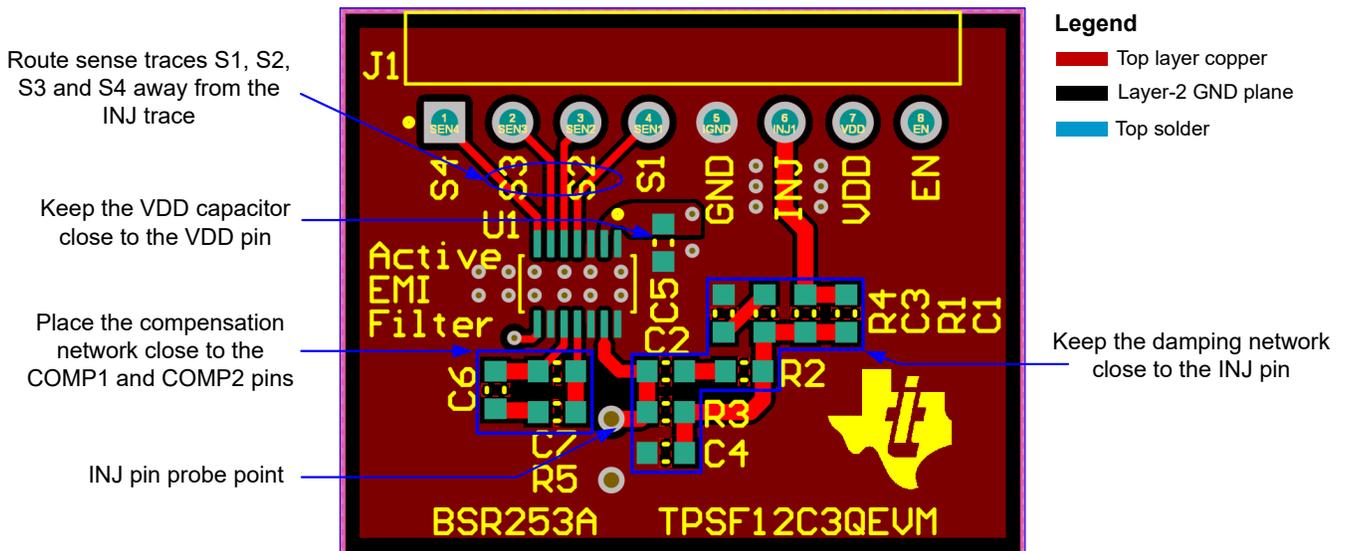


Figure 9-10. Typical Top-Layer Design



**Legend**

- █ Top layer copper
- █ Bottom layer copper
- █ Top solder

**Figure 9-11. Typical Three-Phase Filter Board Design With AEF**

## 10 Device and Documentation Support

### 10.1 Device Support

#### 10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 10.1.2 Development Support

All AEF devices from the family shown in [Table 10-1](#) are rated for a maximum junction temperature of 150°C and are [functional safety-capable](#). See the Texas Instruments power-supply filter ICs [landing page](#) for more detail.

**Table 10-1. Common-mode AEF IC Family**

DEVICE	ORDERABLE PART NUMBER	PHASES	GRADE	JUNCTION TEMPERATURE RANGE
<a href="#">TPSF12C3-Q1</a>	TPSF12C3QDYRQ1	3	Automotive	-40°C to 150°C
<a href="#">TPSF12C1-Q1</a>	TPSF12C1QDYRQ1	1	Automotive	-40°C to 150°C
<a href="#">TPSF12C3</a>	TPSF12C3DYR	3	Commercial	-40°C to 150°C
<a href="#">TPSF12C1</a>	TPSF12C1DYR	1	Commercial	-40°C to 150°C

For development support see the following:

- [TPSF12C3-Q1 quickstart calculator](#)
- [TPSF12C3-Q1 EVM Altium layout source files](#)
- [TPSF12C3-Q1 PSPIICE for TI and SIMPLIS simulation models](#)
- [TPSF12C3-Q1 EVM user's guide](#)
- For TI's reference design library, visit [TI Reference Design library](#)
- To design a low-EMI power supply, review TI's comprehensive [EMI Training Series](#)
- TI Reference Designs:
  - [3-kW, 180-W/in<sup>3</sup> single-phase totem-pole bridgeless PFC reference design with 16-A max input](#)
  - [1-kW reference design with CCM totem pole PFC and current-mode LLC realized by C2000™ and GaN](#)
  - [7.4-kW on-board charger reference design with CCM totem pole PFC and CLLLC DC/DC using C2000™ MCU](#)
  - [GaN-based, 6.6-kW, bidirectional, onboard charger reference design](#)
  - [10-kW, bidirectional three-phase three-level \(T-type\) inverter and PFC reference design](#)
- Technical Articles:
  - Texas Instruments, [How a stand-alone active EMI filter IC shrinks common-mode filter size](#)
  - Texas Instruments, [How device-level features and package options can help minimize EMI in automotive designs](#)
  - Texas Instruments, [How to use slew rate for EMI control](#)
- White Papers:
  - Texas Instruments, [How Active EMI Filter ICs Mitigate Common-Mode Emissions and Save PCB Space in Single- and Three-Phase Systems](#)
  - Texas Instruments, [An Overview of Conducted EMI Specifications for Power Supplies](#)
  - Texas Instruments, [An Overview of Radiated EMI Specifications for Power Supplies](#)
- Video:
  - Texas Instruments, [Single- and three-phase active EMI filter ICs mitigate common-mode EMI, save space and reduce cost](#)
- To view a related device of this product, see the [TPSF12C1-Q1](#) single-phase active EMI filter for common-mode noise mitigation or refer to the Texas Instruments power-supply filter ICs [landing page](#)

## 10.2 Documentation Support

### 10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [TI pioneers the industry's first stand-alone active EMI filter ICs, supporting high-density power supply designs](#) press release
- Texas Instruments, [An Engineer's Guide To EMI In DC/DC Regulators](#) e-book
- Texas Instruments, [Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics](#) ADJ article
- Texas Instruments, [Designing High Performance, Low-EMI, Automotive Power Supplies](#) application report
- Texas Instruments, [EMI Filter Components And Their Nonidealities For Automotive DC/DC Regulators](#) technical brief

### 10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on [Subscribe to updates](#) to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSF12C3QDYRQ1	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	TPSF12C3Q1
TPSF12C3QDYRQ1.A	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	TPSF12C3Q1

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TPSF12C3-Q1 :**

- Catalog : [TPSF12C3](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

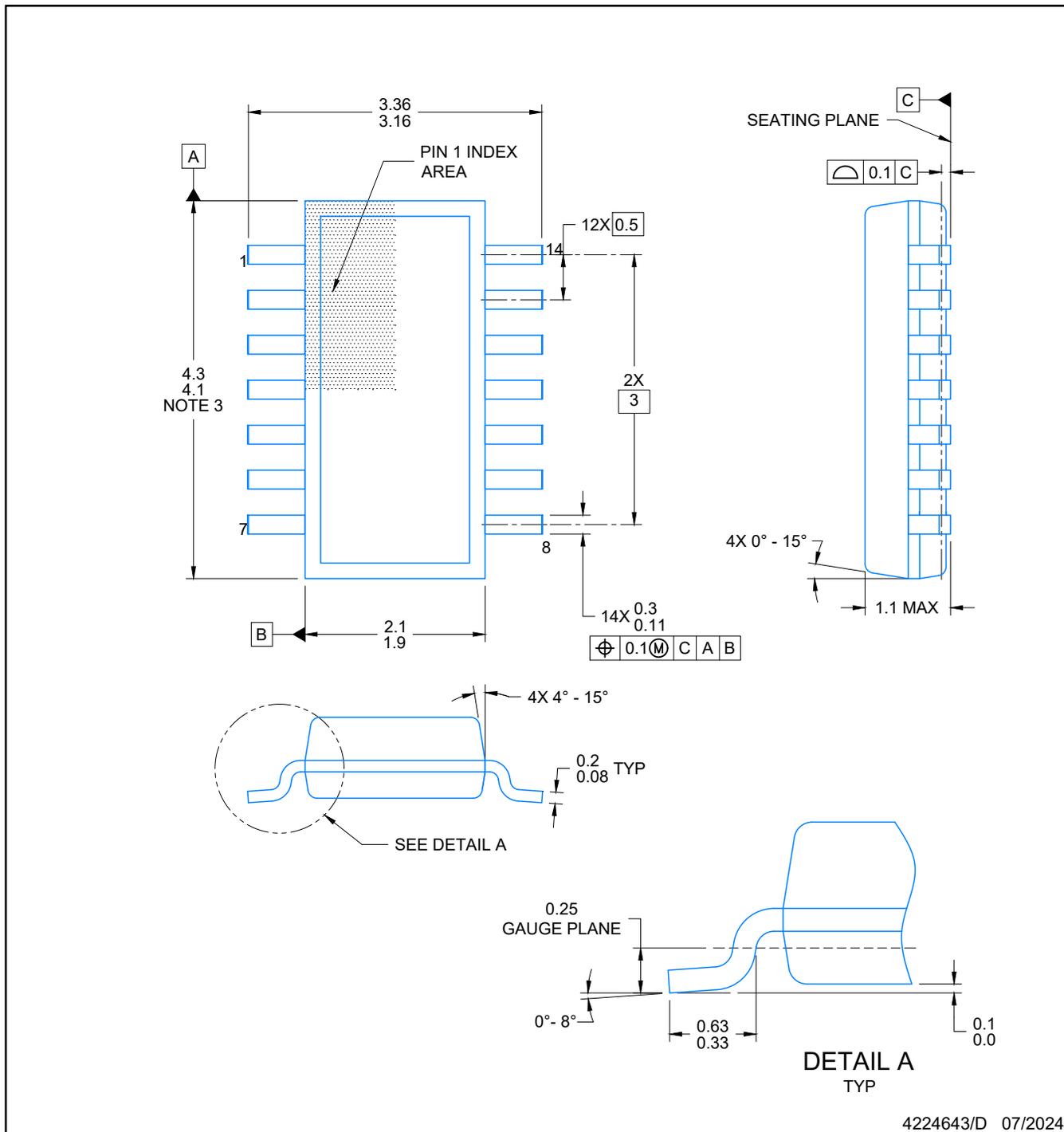

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSF12C3QDYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

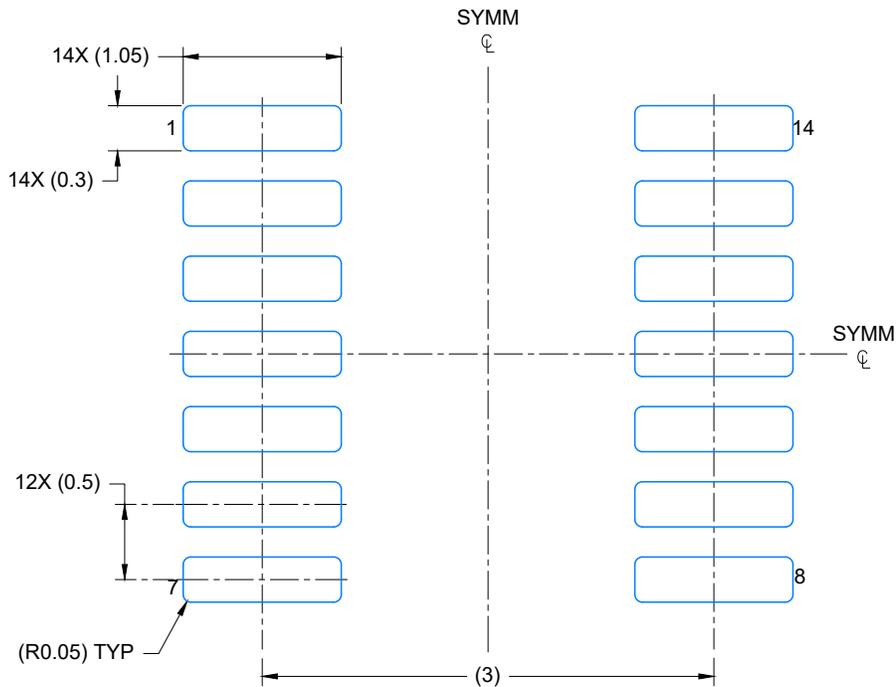
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSF12C3QDYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8



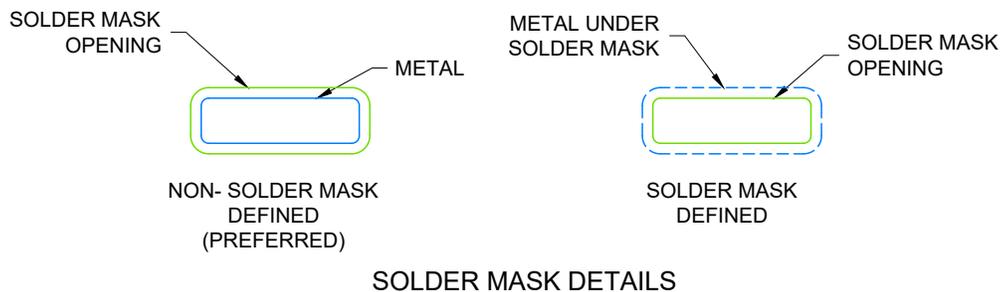
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



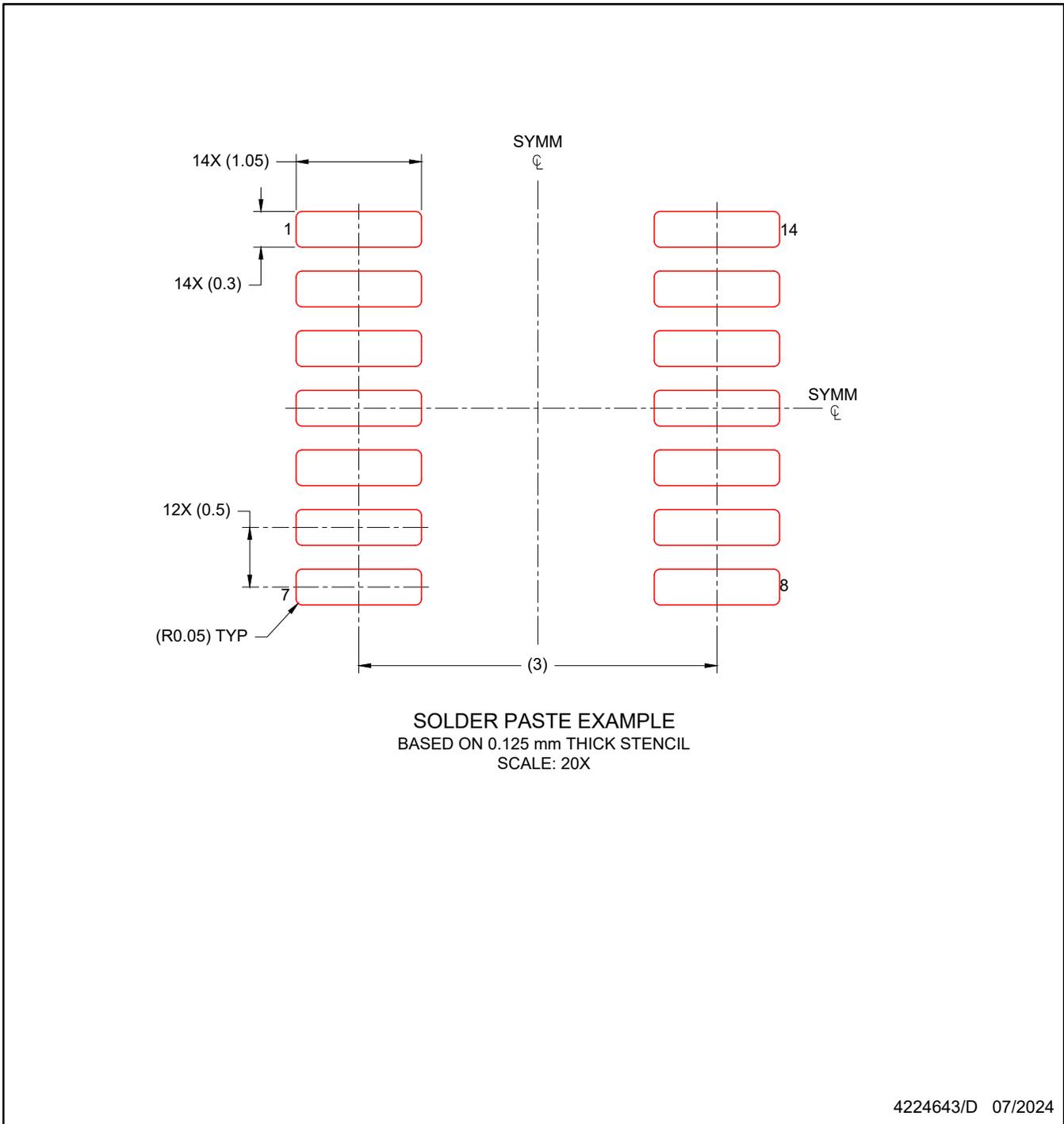
LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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