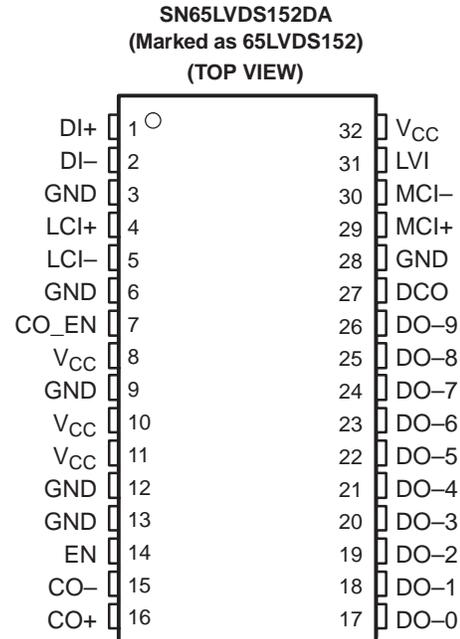


MuxIt™ RECEIVER-DESERIALIZER

Check for Samples: [SN65LVDS152](#)

FEATURES

- **A Member of the MuxIt™ Serializer-Deserializer Building-Block Chip Family**
- **Supports Deserialization of One Serial Link Data Channel Input at Rates up to 200 Mbps**
- **PLL Lock/Valid Input Provided to Enable Parallel Data and Clock Outputs**
- **Cascadable With Additional SN65LVDS152 MuxIt Receiver-Deserializers for Wider Parallel Output Data Channel Widths**
- **LVDS Compatible Differential Inputs and Outputs Meet or Exceed the Requirements of ANSI TIA/EIA-644-A**
- **LVDS Input and Output ESD Protection Exceeds 12 kV HBM**
- **LVTTL Compatible Inputs for Lock/Valid and Enables Are 5-V Tolerant**
- **Operates With 3.3-V Supply**
- **Packaged in 32-Pin DA Thin Shrink Small-Outline Package With 26-Mil Terminal Pitch**



DESCRIPTION

MuxIt is a family of general-purpose, multiple-chip building blocks for implementing parallel data serializers and deserializers. The system allows for wide parallel data to be transmitted through a reduced number of transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) data interface. The number of bits multiplexed per transmission line is user selectable, allowing for higher transmission efficiencies than with other existing fixed ratio solutions. MuxIt utilizes the LVDS (TIA/EIA-644-A) low voltage differential signaling technology for communications between the data source and data destination.

The MuxIt family initially includes three devices supporting simplex communications: the SN65LVDS150 phase locked loop frequency multiplier, the SN65LVDS151 serializer-transmitter, and the SN65LVDS152 receiver-deserializer.

The SN65LVDS152 consists of three LVDS differential transmission line receivers, an LVDS differential transmission line driver, a 10-bit serial-in/parallel-out shift register, plus associated input and output buffers. It receives serialized data over an LVDS transmission line link, deserializes (demultiplexes) it, and delivers it on parallel data outputs, DO-0 through DO-9. Data received over the link is clocked at a factor of M times the original parallel data frequency. The multiplexing ratio M, or number of bits per data clock cycle, is programmed with configuration pins (M1 → M5) on the companion SN65LVDS150 MuxIt programmable PLL frequency multiplier. Up to 10 bits of data may be deserialized and output by each SN65LVDS152. Two or more SN65LVDS152 units may be connected in series (cascaded) to accommodate wider parallel data paths for higher serialization values. The range of multiplexing ratio M supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier is between 4 and 40. [Table 1](#) shows some of the combinations of LCI and MCI supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MuxIt is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Data is serially shifted into the SN65LVDS152 shift register on the falling edges of the M-clock input (MCI). The data is latched out in parallel from the SN65LVDS152 shift register on the second rising edge after the first falling edge of the M-clock following a rising edge of the link clock input (LCI). The SN65LVDS152 includes LVDS differential line receivers for both the serialized link data stream (DI) and link clock (LCI). High-speed signals from the SN65LVDS150 MuxIt programmable frequency multiplier (MCI), plus the input and output for cascaded data (DI, CO) are carried over differential connections to minimize skew and jitter. Examples of operating waveforms for values of $M = 4$ and $M = 10$ are provided in [Figure 1](#).

The enable input (EN) along with internal power-on reset (POR) controls the outputs. When V_{CC} is below 1.5 volts, or when EN is low, outputs are disabled. When V_{CC} is above 3 V and EN is high, outputs are enabled and operating to specifications.

Parallel data bits are output from DO-n outputs in an order dependent on the value of the multiplexing ratio (frequency multiplier value) M . For values of M from 4 through 10, the cascade output (CO_{\pm}) is not used, and only the top M parallel outputs (DO-9 through DO-[10-M]) are used. The data bit output on DO-9 corresponds to the data bit input on DI-[$M-1$] of the SN65LVDS151 serializer. Likewise, the data bit output on DO-[10-M] will correspond to the data bit input on DI-0 of the SN65LVDS151 serializer.

For values of M greater than 10, the cascade output (CO_{\pm}) is used to connect multiple SN65LVDS152 deserializers. In this case the higher-order unit(s) output 10 bits each of the highest numbered bits that are input into the SN65LVDS151 serializer(s). The lowest numbered input bits are output on the lowest-order SN65LVDS152 deserializer in descending order from output DO-9. The number of bits is equal to $M \bmod(10)$. [Table 2](#) reflects this information, where $X = M \bmod(10)$.

Table 1. Example Combinations of LCI and MCI Supported by the SN65LVDS150 MuxIt Programmable PLL Frequency Multiplier

| M | LCI, MHz | | MCI, MHz | |
|----|----------|---------|----------|---------|
| | MINIMUM | MAXIMUM | MINIMUM | MAXIMUM |
| 4 | 5 | 50 | 20 | 200 |
| 10 | 5 | 20 | 50 | 200 |
| 20 | 5 | 10 | 100 | 200 |
| 40 | 5 | 5 | 200 | 200 |

Table 2. Output Data Bits as a Function of Multiplier Value M

| | X = 1 | X = 2 | X = 3 | X = 4 | X = 5 | X = 6 | X = 7 | X = 8 | X = 9 | X = 0 |
|-----------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|-------|
| DO-9 output bit | DI-0 | DI-1 | DI-2 | DI-3 | DI-4 | DI-5 | DI-6 | DI-7 | DI-8 | DI-9 |
| DO-8 output bit | Invalid | DI-0 | DI-1 | DI-2 | DI-3 | DI-4 | DI-5 | DI-6 | DI-7 | DI-8 |
| DO-7 output bit | Invalid | Invalid | DI-0 | DI-1 | DI-2 | DI-3 | DI-4 | DI-5 | DI-6 | DI-7 |
| DO-6 output bit | Invalid | Invalid | Invalid | DI-0 | DI-1 | DI-2 | DI-3 | DI-4 | DI-5 | DI-6 |
| DO-5 output bit | Invalid | Invalid | Invalid | Invalid | DI-0 | DI-1 | DI-2 | DI-3 | DI-4 | DI-5 |
| DO-4 output bit | Invalid | Invalid | Invalid | Invalid | Invalid | DI-0 | DI-1 | DI-2 | DI-3 | DI-4 |
| DO-3 output bit | Invalid | Invalid | Invalid | Invalid | Invalid | Invalid | DI-0 | DI-1 | DI-2 | DI-3 |
| DO-2 output bit | Invalid | DI-0 | DI-1 | DI-2 |
| DO-1 output bit | Invalid | DI-0 | DI-1 |
| DO-0 output bit | Invalid | DI-0 |

Additional information on output bit ordering in cascaded applications can be found in the MuxIt Application Report.

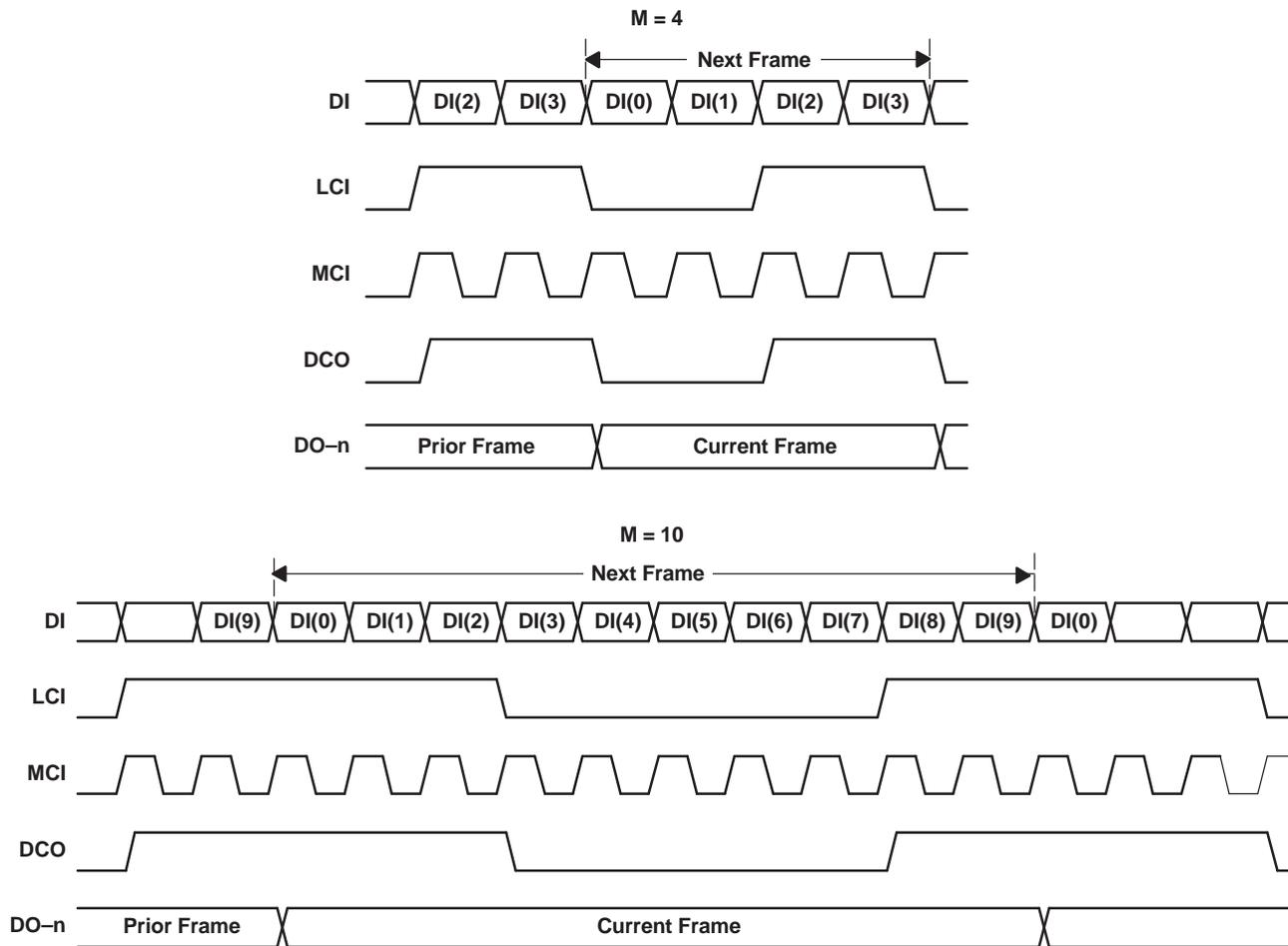
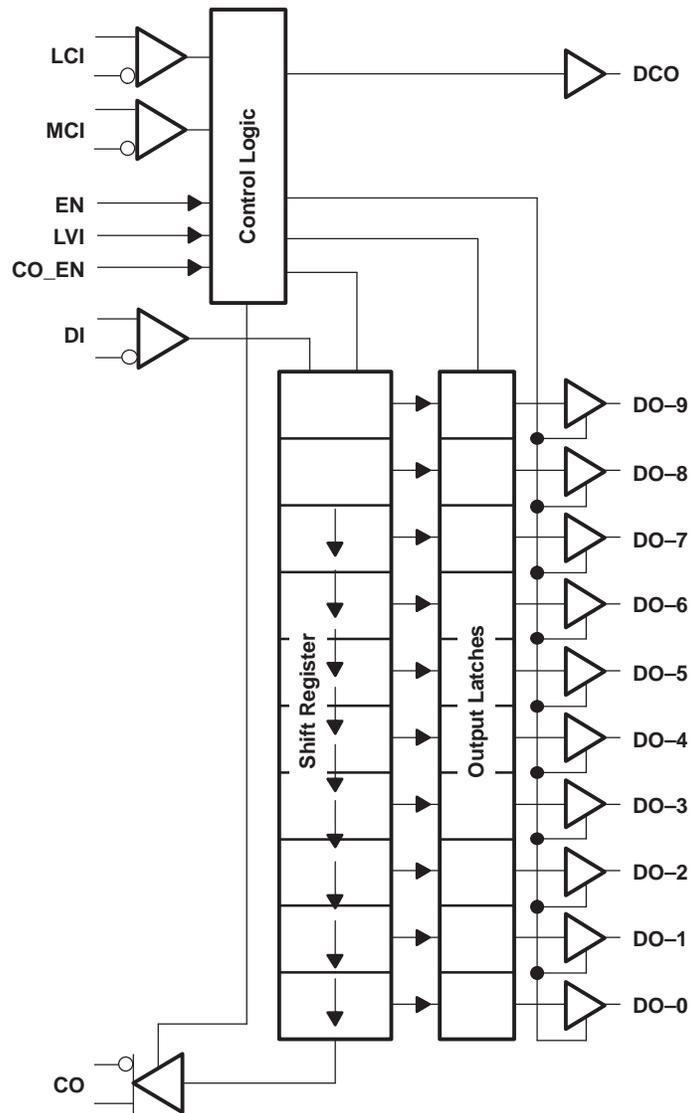
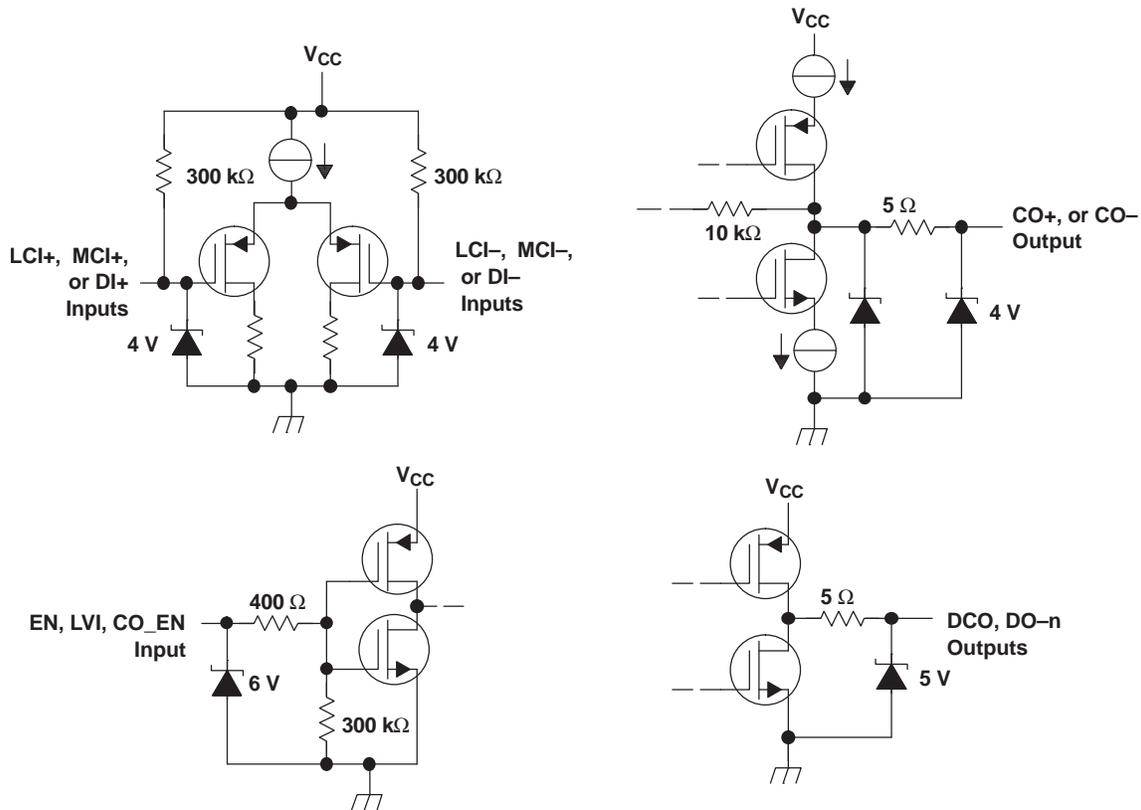


Figure 1. Operating Waveform Examples

FUNCTIONAL BLOCK DIAGRAM



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | LEVEL | DESCRIPTION |
|-----------------|---------------------|--------|--------|---|
| CO-, CO+ | 15, 16 | Output | LVDS | Cascade output. This is used to connect to additional SN65LVDS152 units when the multiplexing ratio M (and M-clock) value is greater than 10. |
| CO_EN | 7 | Input | LVTTTL | Cascade output enable. Used to control the CO output. A high-level input enables the CO output, a low-level input disables the CO output. |
| DCO | 27 | Output | LVTTTL | Data clock output. This is the recovered (original frequency) clock that is synchronized to the deserialized parallel data. |
| DI+, DI- | 1, 2 | Input | LVDS | Link data input. This is the data being received from the source end of the serialized link. Also used for cascade data input from additional SN65LVDS152 units when the multiplexing ratio M value is greater than 10. |
| EN | 14 | Input | LVTTTL | Enable. Used to control overall device operation. A high-level input enables the device. A low-level input disables the device by resetting the internal latches and forcing the CO and LVTTTL outputs to a high-impedance state. |
| GND | 3, 6, 9, 12, 13, 28 | Power | NA | Circuit ground |
| LCI+, LCI- | 4, 5 | Input | LVDS | Link clock input. This is the data block synchronization clock received from the source end of the serialized link. |
| LVI | 31 | Input | LVTTTL | Lock/valid input. This is a signal required for proper MuxIt system operation. It is to be directly connected to the LVO output of an SN65LVDS150. It is used to inhibit the operation of this device until after the PLL has stabilized. A low level input disables the data and clock outputs, a high level input enables the outputs |
| MCI+, MCII- | 29,30 | Input | LVDS | M-clock input. This is the high frequency multiplied clock input from the local PLL frequency multiplier. It synchronizes the reception of the link data |
| DOI-0I-DOI-9 | 17-26 | Output | LVTTTL | Parallel data outputs. Data from the serial shift register is transferred to the output data latches in synchronization with the rising edge of LCI. |
| V _{CC} | 8, 10, 11, 32 | Power | NA | Supply voltage |

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | UNIT |
|--|-------------------------------|------------------------------|
| Supply voltage range, V_{CC} ⁽²⁾ | | –0.5 V to 4 V |
| Input voltage range | EN, LVI, CO_EN | –0.5 V to 5.5 V |
| | LCl±, MCl±, DI±, CO± | –0.5 V to 4 V |
| Electrostatic discharge, human body model ⁽³⁾ | LCl±, MCl±, DI±, CO±, and GND | ±12 kV |
| | All pins | ±2 kV |
| Charged-device model ⁽⁴⁾ | All pins | ±500 V |
| Continuous power dissipation | | See Dissipation Rating Table |
| Storage temperature range | | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260°C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---|---|--|
| DA | 1453 mW | 11.6 mW/°C | 756 mW |

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|------------|---|-----|-----|----------------------|------|
| V_{CC} | Supply voltage | 3 | 3.3 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | V_{CC} | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| $ V_{ID} $ | Magnitude of differential input voltage | 0.1 | | 0.6 | V |
| V_{IC} | Common-mode input voltage | | | $\frac{ V_{ID} }{2}$ | V |
| | | | | $V_{CC} - 0.8$ | V |
| T_A | Operating free-air temperature | 40 | | 85 | °C |

TIMING REQUIREMENTS

| PARAMETERS | | TEST CONDITIONS | MIN | MAX | UNIT |
|-------------|--------------------------------------|------------------------------|-----|-----|------|
| $t_{su(1)}$ | Clock setup time, MCl↓ before LCl↑ | See Figure 2 | 0 | | ns |
| $t_{su(2)}$ | Clock setup time, LCl↑ before MCl↓ | | 1 | | ns |
| $t_{su(3)}$ | Link data setup time, DI before MCl↓ | See Figure 3 | 0.3 | | ns |
| $t_{h(3)}$ | Link data hold time, DI after MCl↓ | | 0.5 | | ns |

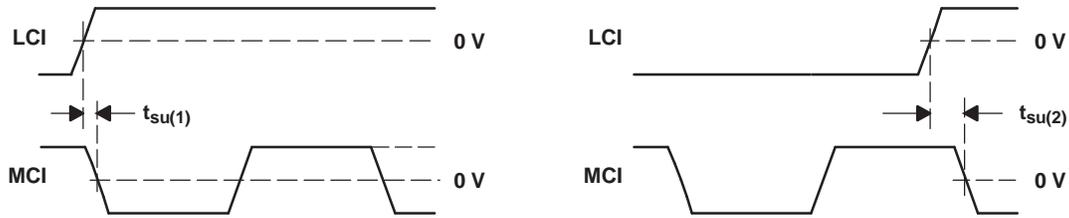


Figure 2. Link Clock Input and M-Clock Setup Time Waveforms

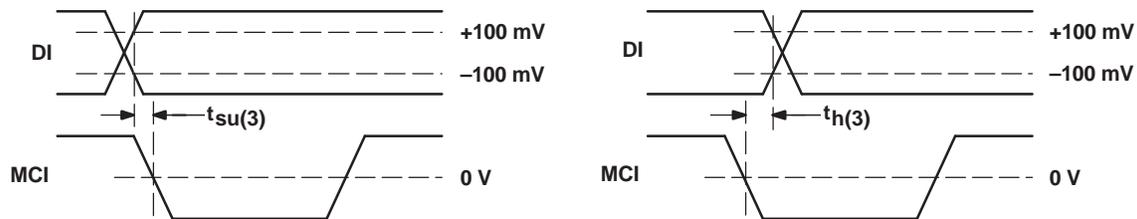


Figure 3. Input Data and M-Clock Setup and Hold Time Waveforms

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|-----------------------|---|--|--|--------------------|-------|------|----|
| V _{ITH+} | Positive-going differential input voltage threshold | See Figure 4 | | | 100 | mV | |
| V _{ITH-} | Negative-going differential input voltage threshold | | -100 | | | | |
| V _{OD(SS)} | Steady-state differential output voltage magnitude | R _L = 100 Ω, V _{ID} = ±100 mV, See Figure 5 and Figure 6 | 247 | 340 | 454 | mV | |
| Δ V _{OD(SS)} | Change in steady-state differential output voltage magnitude between logic states | | -50 | | 50 | | |
| V _{OC(SS)} | Steady-state common-mode output voltage | See Figure 7 | 1.125 | | 1.375 | V | |
| ΔV _{OC(SS)} | Change in steady-state common-mode output voltage between logic states | | -50 | | 50 | | |
| V _{OC(PP)} | Peak-to-peak change common-mode output voltage | | | 50 | 150 | | |
| V _{OH} | High-level output voltage | DO-n, DCO | I _{OH} = -8 mA | 2.4 | | V | |
| V _{OL} | Low-level output voltage | | I _{OL} = 8 mA | | 0.4 | | |
| I _{CC} | Supply current | Enabled, R _L = 100 Ω, | | 14 | 25 | mA | |
| | | Disabled | | 0.5 | 1 | | |
| | | f _(MCI) = 200 MHz, f _(LCI) = 20 MHz, R _L = 100 Ω, DI-n = 1010101010 at 200 Mbit/s | | 35 | 60 | | |
| I _I | Input current | LCI, MCI, DI inputs | V _I = 0 V | -2 | | μA | |
| | | | V _I = 2.4 V | -1.2 | | | |
| I _{ID} | Differential input current | LCI, MCI, DI inputs | V _{IC} = 0.05 V to 2.35 V, V _{ID} = ±0.1 V | | -2 | 2 | μA |
| I _{I(OFF)} | Power-off input current | LCI, MCI, DI inputs | V _{CC} = 0 V, V _I = 3.6 V | | | 20 | μA |
| I _{IH} | High-level input current | EN, LVI, CO_EN | V _{IH} = 2 V | | | 20 | μA |
| I _{IL} | Low-level input current | EN, LVI, CO_EN | V _{IL} = 0.8 V | | | 10 | μA |
| I _{OS} | Short-circuit output current | CO | V _{O+} or V _{O-} = 0 V | -10 | | 10 | mA |
| | | | V _{OD} = 0 V | -10 | | 10 | |
| I _{OZ} | High-impedance output current | CO | V _O = 0 V or V _{CC} | | -5 | 5 | μA |
| | | DO-n, DCO | | | -5 | 5 | |
| I _{O(OFF)} | Power-off output current | CO | V _{CC} = 1.5 V, V _O = 3.6 V | | -5 | 5 | μA |
| C _I | Input capacitance | LCI, MCI, DI inputs | V _{ID} = (0.4sin(4E6πt) + 0.5) V | | | 3 | pF |

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|--|---|-----|-----|-----|------|
| $t_{d(1)}$ | Propagation delay time, LCI \uparrow to DCO \uparrow | See Figure 8 | | 2 | 3 | ns |
| $t_{d(2)}$ | Delay time, MCI \uparrow to DO-n | | | 3.3 | 5.5 | |
| $t_{su(4)}$ | Set-up time, DO-n valid to DCO \uparrow | | 5 | | | |
| $t_h(4)$ | Hold time, DCO \uparrow to DO-n valid | | 5 | | | |
| $t_{d(3)}$ | Delay time, MCI \downarrow to CO | See Figure 9 | | 2.9 | 4.5 | ns |
| t_r | Differential output signal rise time, CO | $R_L = 100 \Omega$, $C_L = 10 \text{ pF}$, See Figure 10 | 0.3 | 0.8 | 1.5 | ns |
| | Output signal rise time, DCO, DO-n | $C_L = 10 \text{ pF}$, See Figure 11 | | 0.6 | 1.5 | |
| t_f | Differential output signal fall time, CO | $R_L = 100 \Omega$, $C_L = 10 \text{ pF}$, See Figure 10 | 0.3 | 0.8 | 1.5 | ns |
| | Output signal fall time, DCO, DO-n | $C_L = 10 \text{ pF}$, See Figure 11 | | 0.6 | 1.5 | |
| $t_{sk(p)}$ | Pulse skew ($ t_{PHL} - t_{PLH} $), CO | $R_L = 100 \Omega$, $C_L = 10 \text{ pF}$, See Figure 10 | | 0 | 300 | ps |
| t_{PZH} | Propagation delay time, high-impedance to high-level output (DCO only) | EN to DCO, DO-n, $C_L = 10 \text{ pF}$, See Figure 12 | | 5 | 15 | ns |
| t_{PZL} | Propagation delay time, high-impedance to low-level output | | | 5 | 15 | |
| t_{PHZ} | Propagation delay time, high-level to high-impedance output | | | 5 | 15 | |
| t_{PLZ} | Propagation delay time, low-level to high-impedance output | | | 6 | 15 | |
| t_{PZH} | Propagation delay time, high-impedance to high-level output (DCO only) | LVI to DCO, DO-n $C_L = 10 \text{ pF}$, See Figure 12 | | 5 | 15 | ns |
| t_{PZL} | Propagation delay time, high-impedance to low-level output | | | 5 | 15 | |
| t_{PHZ} | Propagation delay time, high-level to high-impedance output | | | 5 | 15 | |
| t_{PLZ} | Propagation delay time, low-level to high-impedance output | | | 5 | 15 | |

PARAMETER MEASUREMENT INFORMATION

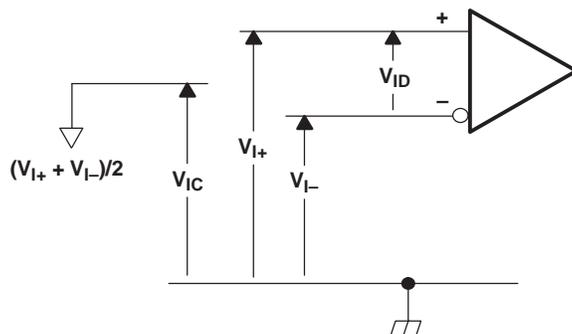


Figure 4. Receiver Voltage Definitions

Table 3. Receiver Minimum and Maximum Input Threshold Test Voltages

| APPLIED VOLTAGES | | RESULTING DIFFERENTIAL INPUT VOLTAGE | RESULTING COMMON-MODE INPUT VOLTAGE |
|------------------|----------|--------------------------------------|-------------------------------------|
| V_{I+} | V_{I-} | V_{ID} | V_{IC} |
| 1.25 V | 1.15 V | 100 mV | 1.2 V |
| 1.15 V | 1.25 V | -100 mV | 1.2 V |
| 2.4 V | 2.3 V | 100 mV | 2.35 V |
| 2.3 V | 2.4 V | -100 mV | 2.35 V |
| 0.1 V | 0 V | 100 mV | 0.05 V |
| 0 V | 0.1 V | -100 mV | 0.05 V |
| 1.5 V | 0.9 V | 600 mV | 1.2 V |
| 0.9 V | 1.5 V | -600 mV | 1.2 V |
| 2.4 V | 1.8 V | 600 mV | 2.1 V |
| 1.8 V | 2.4 V | -600 mV | 2.1 V |
| 0.6 V | 0 V | 600 mV | 0.3 V |
| 0 V | 0.6 V | -600 mV | 0.3 V |

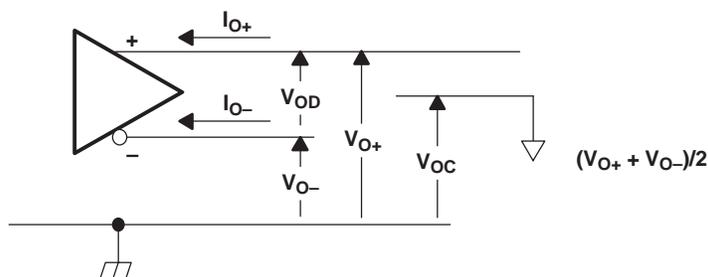


Figure 5. Driver Voltage and Current Definitions

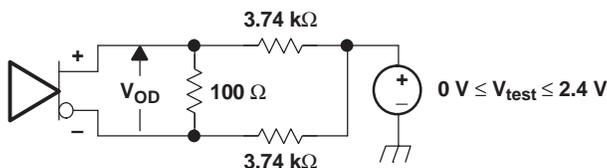
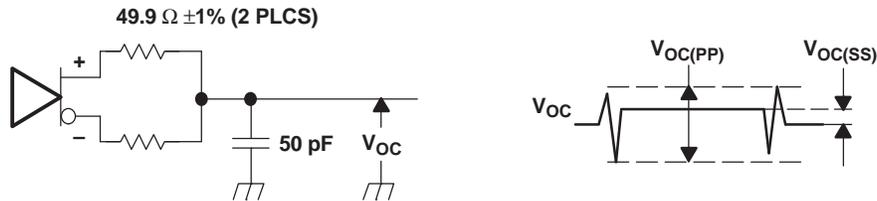


Figure 6. V_{OD} Test Circuit



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, Pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 5 GHz.

Figure 7. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

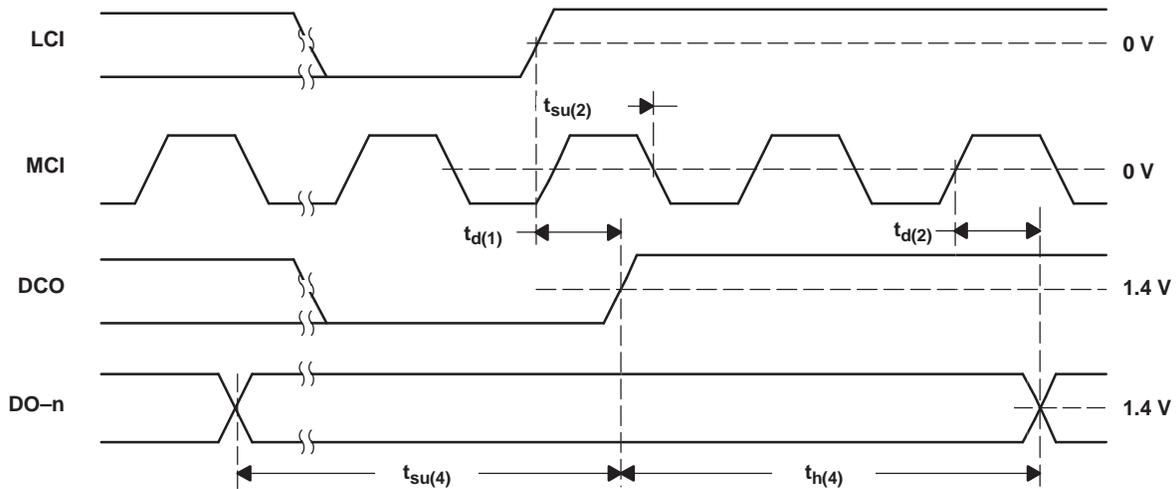


Figure 8. Data Clock and Data Output Timing Waveforms

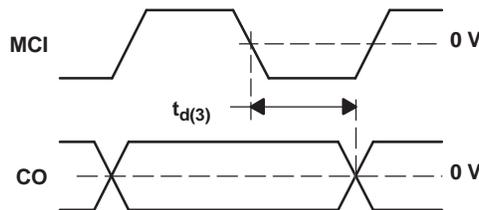
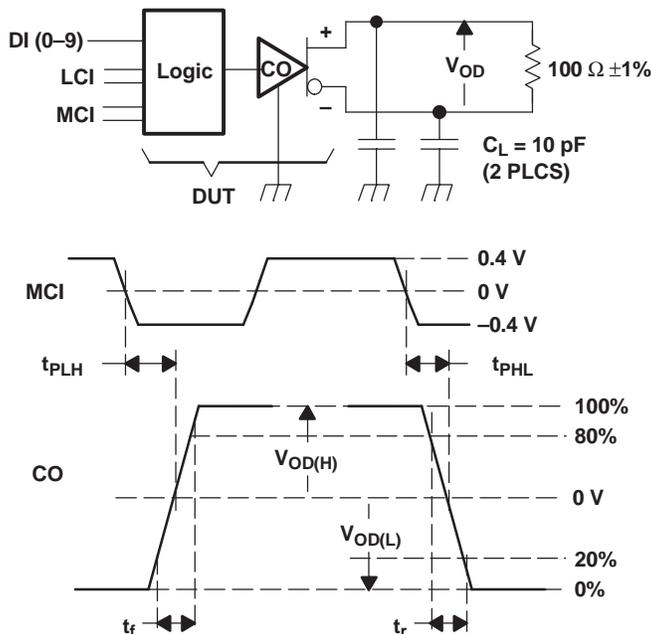
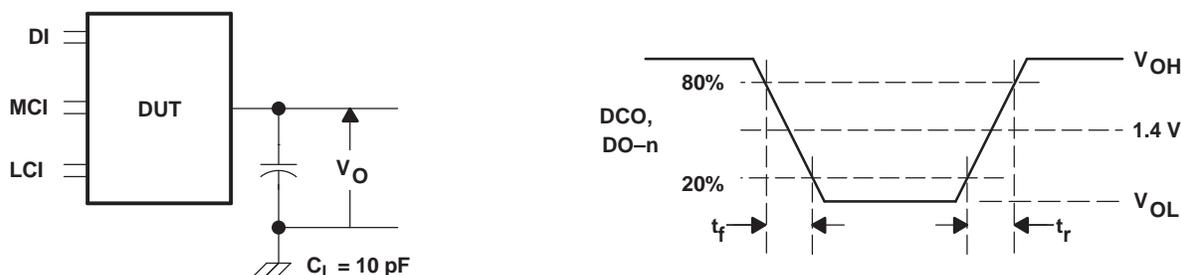


Figure 9. MCI to CO Timing Waveforms



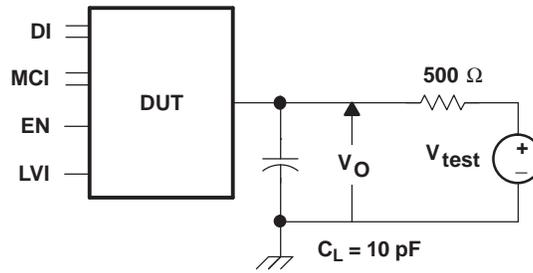
- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 100 Mpps, Pulse width = 5 ± 0.1 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 10. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, MCI pulse repetition rate (PRR) = 50 Mpps, Pulse width = 10 ± 0.2 ns. LCI pulse repetition rate (PRR) = 5 Mpps, pulsewidth = 100 ± 2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 11. Timing Test Circuit and Waveforms



NOTE: $V_{TEST} = 2.5\text{ V}$ for t_{PZL} or t_{PLZ} , $V_{TEST} = 0\text{ V}$ for t_{PZH} or t_{PHZ} . All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1\text{ ns}$, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = $500 \pm 10\text{ ns}$. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

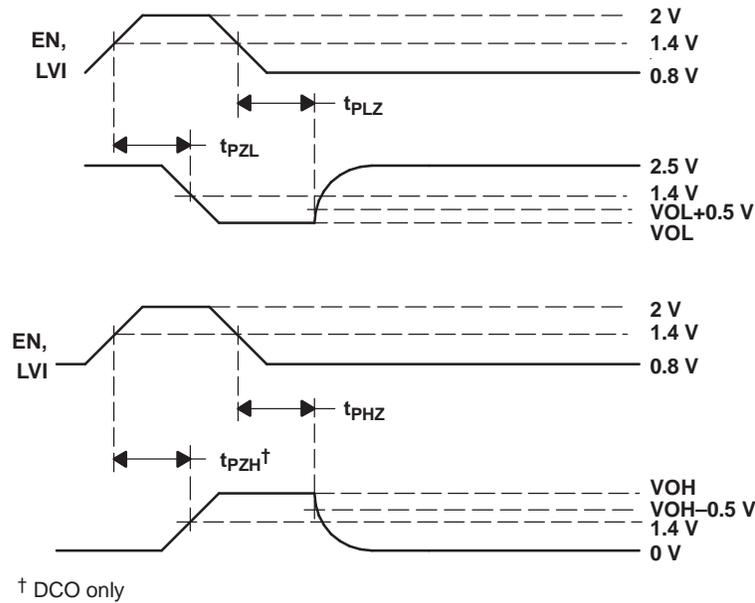
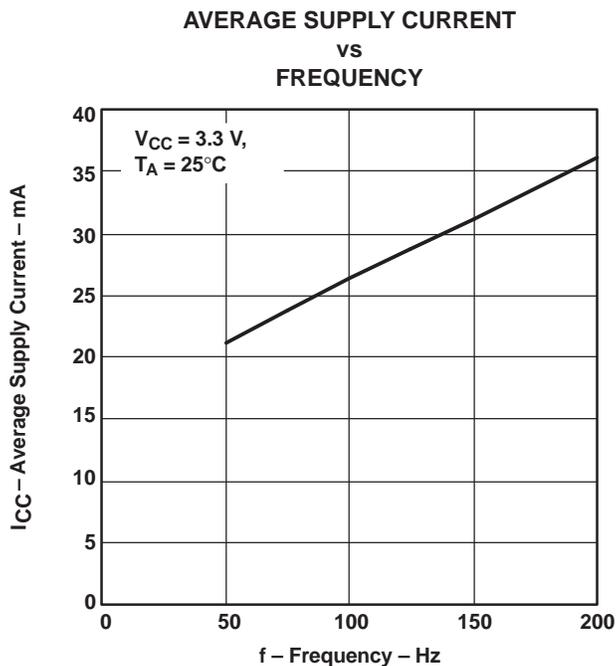


Figure 12. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS



REVISION HISTORY

| Changes from Original (December 2000) to Revision A | Page |
|---|------|
| • Changed Figure 2 title From: THIS NEEDS A TITLE To: Link Clock Input and M-Clock Setup Time Waveforms | 7 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN65LVDS152DA | Last Time Buy | Production | TSSOP (DA) 32 | 46 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 65LVDS152 |
| SN65LVDS152DA.B | Last Time Buy | Production | TSSOP (DA) 32 | 46 TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 65LVDS152 |
| SN65LVDS152DAR | Last Time Buy | Production | TSSOP (DA) 32 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 65LVDS152 |
| SN65LVDS152DAR.B | Last Time Buy | Production | TSSOP (DA) 32 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 65LVDS152 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

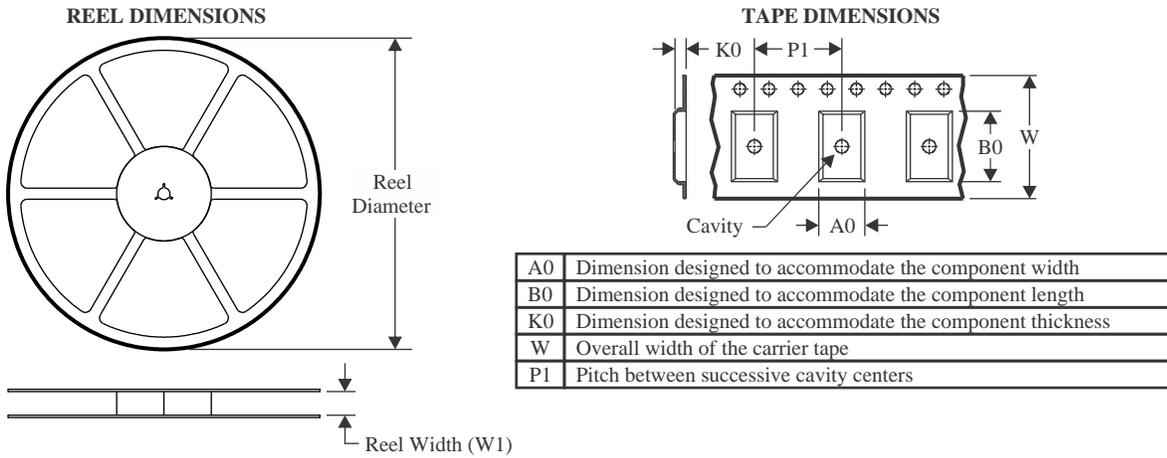
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

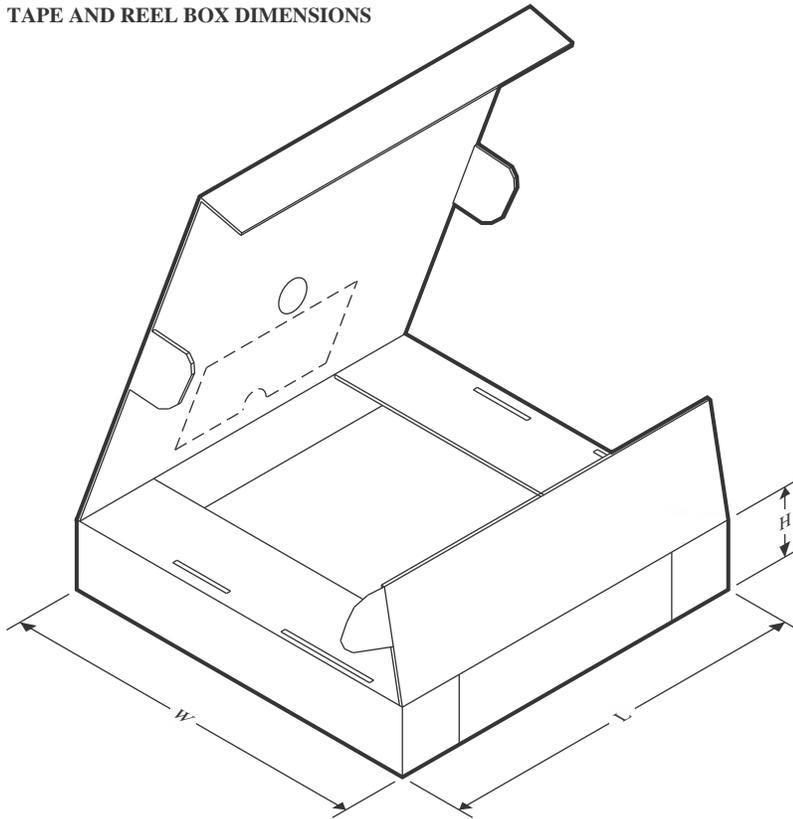
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

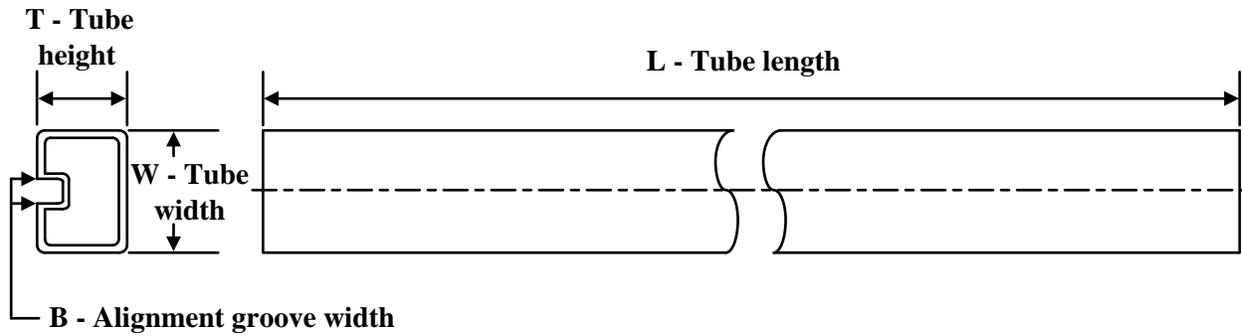

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LVDS152DAR | TSSOP | DA | 32 | 2000 | 330.0 | 24.4 | 8.6 | 11.5 | 1.6 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LVDS152DAR | TSSOP | DA | 32 | 2000 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65LVDS152DA | DA | TSSOP | 32 | 46 | 530 | 11.89 | 3600 | 4.9 |
| SN65LVDS152DA.B | DA | TSSOP | 32 | 46 | 530 | 11.89 | 3600 | 4.9 |

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated