

# TUSB1142 USB Type-C® 10Gbps USB 3.2 2:1/1:2 Mux/DeMux Adaptive Linear Redriver

## 1 Features

- USB Type-C 2:1 redriver MUX
- USB 3.2 5Gbps and 10Gbps support
- Advanced USB power management
  - Active: 550mW (typical)
  - Disconnect: 1.5mW
  - Disabled (EN = L): 0.130mW
- 16 EQ settings up to 12dB at 5GHz
- Choice between adaptive or fixed receiver equalization for ports facing USB connector
- Choice between linear or limited redriver for port facing the system (SSRX transmitter)
- Less than 1V  $V_{TX-CM}$  and  $V_{RX-CM}$
- Configuration through I<sup>2</sup>C or pin-strap
- Selection between 1.8V or 3.3V I<sup>2</sup>C levels
- Operates from a single 3.3V supply

## 2 Applications

- [Notebooks and desktops](#)
- [Docking stations](#)
- [Data storage](#)
- [Connected peripherals and printers](#)

## 3 Description

The TUSB1142 is a 10Gbps USB 3.2 linear redriver with 1:2 DeMUX or 2:1 Mux function for USB-C® applications. The TUSB1142 is intended to reside between a Host and a USB-C receptacle or between a USB device and a USB-C receptacle. The TUSB1142 supports both USB 3.2 Gen2 (10Gbps) and Gen1 (5Gbps) as well as USB 3.2 low power states (Disconnect, U1, U2, and U3).

The TUSB1142 incorporates an adaptive receiver equalization (AEQ) feature. The AEQ feature automatically determines what the best ISI compensation settings are between the TUSB1142 and USB device plugged into the USB connector resulting in improved interoperability.

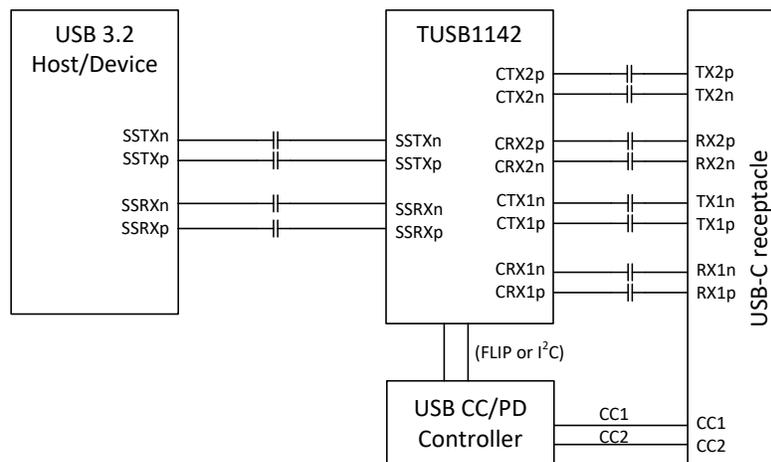
The TUSB1142 operates from a single 3.3V supply and is available in a 40-pin WQFN package.

### Package Information

| PART NUMBER | TEMPERATURE                    | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|--------------------------------|------------------------|-----------------------------|
| TUSB1142    | T <sub>A</sub> = 0°C to 70°C   | RNQ (WQFN, 40)         | 6mm × 4mm                   |
| TUSB1142I   | T <sub>A</sub> = -40°C to 85°C | RNQ (WQFN, 40)         | 6mm × 4mm                   |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Simplified Schematic**



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## 4 Pin Configuration and Functions

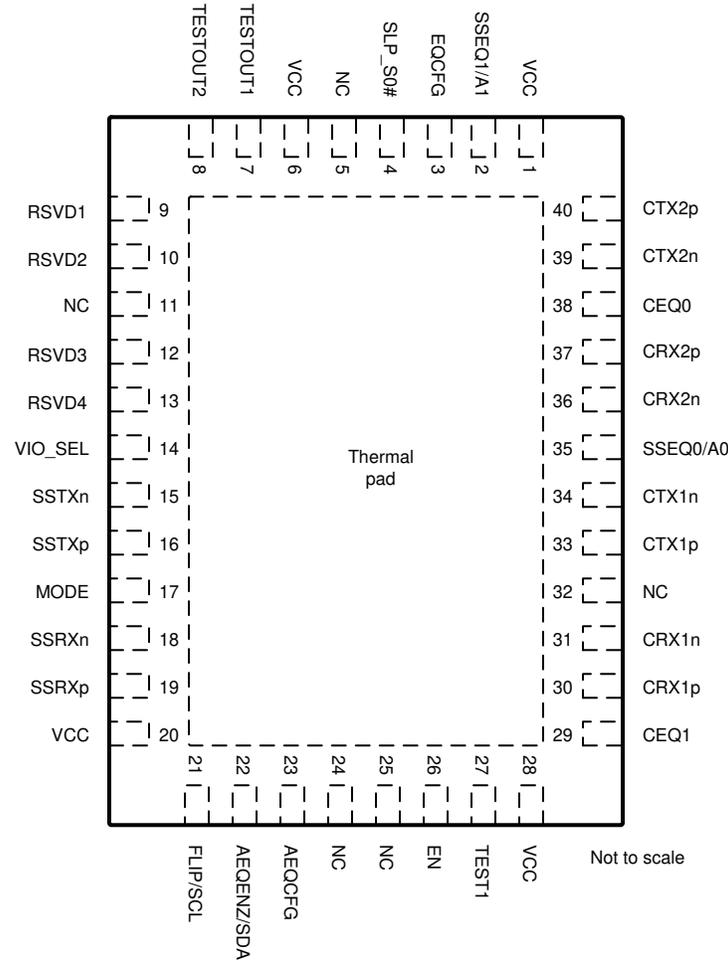


Figure 4-1. TUSB1142 RNQ Package, 40-Pin WQFN (Top View)

Table 4-1. Pin Functions

| PIN      |     | TYPE <sup>(1)</sup> | DESCRIPTION  |
|----------|-----|---------------------|--|
| NAME     | NO. |                     |  |
| VCC      | 1   | P                   | 3.3 V supply   |
| SSEQ1/A1 | 2   | 4-level I (PU/PD)   | In I <sup>2</sup> C mode, this pin along with A0 pin selects the 7-bit I2C target address (refer to <a href="#">Table 7-8</a> ). In pin-strap mode, this pin along with SSEQ0 selects the receiver EQ for SSTX and/or SSTX (refer to <a href="#">Table 7-3</a> ).                                    |
| EQCFG    | 3   | 4-level I (PU/PD)   | In pin-strap mode, this controls how CEQ[1:0] pins and SSEQ[1:0] are used. Refer to <a href="#">Rx EQ Configuration in Pin-Strap Mode</a> for details. In I <sup>2</sup> C mode, this pin is for TI internal test and must be left floating for normal operation.                                    |
| SLP_S0#  | 4   | I (PU)              | SLP_S0#. This pin will control whether or not Rx.Detect function is enabled. If this pin is low and device is in Disconnect state, Rx termination will be disabled. If this pin is low and device is U2/U3 state, Rx termination will be enabled.<br>1: Rx.Detect Enabled.<br>0: Rx.Detect Disabled. |
| NC       | 5   |                     | No internal connection.  |
| VCC      | 6   | P                   | 3.3 V supply   |
| TESTOUT1 | 7   | O                   | For internal TI test only. For normal operation this pin should be left unconnected.   |
| TESTOUT2 | 8   | O                   | For internal TI test only. For normal operation this pin should be left unconnected.   |

**Table 4-1. Pin Functions (continued)**

| PIN        |     | TYPE <sup>(1)</sup> | DESCRIPTION   |
|------------|-----|---------------------|---|
| NAME       | NO. |                     |   |
| RSVD1      | 9   | I                   | Reserved. Leave pin unconnected   |
| RSVD2      | 10  | I                   | Reserved. Leave pin unconnected   |
| NC         | 11  |                     | No internal connection.   |
| RSVD3      | 12  | O                   | Reserved. Leave pin unconnected   |
| RSVD4      | 13  | O                   | Reserved. Leave pin unconnected.  |
| VIO_SEL    | 14  | 4-level I (PU/PD)   | Selects the input thresholds for I2C (SDA and SCL).<br>"0": I2C 3.3 V<br>"R": I2C 1.8 V<br>"F": I2C 3.3 V.<br>"1": I2C 1.8 V.   |
| SSTXn      | 15  | I                   | Differential negative input for USB port. Should be connected to USB 3.2 Host transmit port through an external 220 nF AC-coupling capacitor.   |
| SSTXp      | 16  | I                   | Differential positive input for USB port. Should be connected to USB 3.2 Host transmit port through an external 220 nF AC-coupling capacitor.   |
| MODE       | 17  | 4-level I (PU/PD)   | This pin selects whether device is in I <sup>2</sup> C mode or pin-strap mode. Refer to <a href="#">Table 7-5</a> for details.  |
| SSRXn      | 18  | O                   | Differential negative output for USB port. Should be connected to USB 3.2 Host receiver port through an external 220 nF AC-coupling capacitor.  |
| SSRXp      | 19  | O                   | Differential positive output for USB port. Should be connected to USB 3.2 Host receiver port through an external 220 nF AC-coupling capacitor.  |
| VCC        | 20  | P                   | 3.3 V supply  |
| FLIP/SCL   | 21  | I                   | In I <sup>2</sup> C mode, this pin functions as I2C clock. In pin-strap mode, this pin controls the orientation of the MUX (Refer to <a href="#">Table 7-4</a> ).   |
| AEQENZ/SDA | 22  | I/O                 | In I <sup>2</sup> C mode, this pin functions as I2C data. In pin-strap mode, this pin controls whether or not AEQ is enabled.<br>0: AEQ enabled<br>1: AEQ disabled  |
| AEQCFG     | 23  | 4-level I (PU/PD)   | In pin-strap mode, this pin controls the FULLAEQ_UPPER_EQ limit. In I <sup>2</sup> C mode, this function is controlled by the FULLAEQ_UPPER_EQ register.<br>"0": FULLAEQ_UPPER_EQ = Ah<br>"R": FULLAEQ_UPPER_EQ = Fh<br>"F": FULLAEQ_UPPER_EQ = 8h<br>"1": FULLAEQ_UPPER_EQ = Ch  |
| NC         | 24  |                     | No internal connection  |
| NC         | 25  |                     | No internal connection  |
| EN         | 26  | I (PU)              | When low, the differential receiver's termination will be disabled and differential drivers will be disabled. On rising edge of EN, device will sample four-level inputs and function based on the sampled state of the pins. This pin has an internal 500k pullup to VCC. Please note this pin will also reset internal configuration registers. |
| TEST1      | 27  | I                   | TI Test1. Under normal operations, this pin shall be connected directly or pulldown to GND.   |
| VCC        | 28  | P                   | 3.3 V supply  |
| CEQ1       | 29  | 4-level I (PU/PD)   | In pin-strap mode, this pin along with CEQ0 selects the receiver EQ for CRX1 and/or CRX2 (Refer to <a href="#">Table 7-2</a> ).   |
| CRX1p      | 30  | I                   | Differential positive input for USB port 1. Should be connected to RX1p pin of USB connector. Connection can be DC-coupled to USB connector. Optionally, connection can be through an external 330 nF AC-coupling capacitor.  |
| CRX1n      | 31  | I                   | Differential negative input for USB port 1. Should be connected to RX1n pin of USB connector. Connection can be DC-coupled to USB connector. Optionally, connection can be through an external 330 nF AC-coupling capacitor.  |
| NC         | 32  |                     | No internal connection.   |

**Table 4-1. Pin Functions (continued)**

| PIN         |     | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-------------|-----|---------------------|---|
| NAME        | NO. |                     |   |
| CTX1p       | 33  | O                   | Differential positive output for USB port 1. Should be connected to TX1p pin of USB connector through an external 220 nF AC-coupling capacitor.   |
| CTX1n       | 34  | O                   | Differential negative output for USB port 1. Should be connected to TX1n pin of USB connector through an external 220 nF AC-coupling capacitor.   |
| SSEQ0/A0    | 35  | 4-level I (PU/PD)   | In I <sup>2</sup> C mode, this pin along with A1 pin selects the 7-bit I2C target address (refer to <a href="#">Table 7-8</a> ). In pin-strap mode, this pin along with SSEQ1 selects the receiver EQ for SSTX and/or SSTX (refer to <a href="#">Table 7-3</a> ). |
| CRX2n       | 36  | I                   | Differential negative input for USB port 2. Should be connected to RX2n pin of USB connector. Connection can be DC-coupled to USB connector. Optionally, connection can be through an external 330 nF AC-coupling capacitor.                                      |
| CRX2p       | 37  | I                   | Differential positive input for USB port 2. Should be connected to RX2p pin of USB connector. Connection can be DC-coupled to USB connector. Optionally, connection can be through an external 330 nF AC-coupling capacitor.                                      |
| CEQ0        | 38  | 4-level I (PU/PD)   | In pin-strap mode, this pin along with CEQ1 selects the receiver EQ for CRX1 and/or CRX2 (Refer to <a href="#">Table 7-2</a> ).   |
| CTX2n       | 39  | O                   | Differential negative output for USB port 2. Should be connected to TX2n pin of USB connector through an external 220 nF AC-coupling capacitor.   |
| CTX2p       | 40  | O                   | Differential positive output for USB port 2. Should be connected to TX2p pin of USB connector through an external 220 nF AC-coupling capacitor.   |
| Thermal Pad |     | G                   | Thermal pad. Connect to a solid ground plane.   |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, PD = Internal Pulldown, PU = Internal Pullup.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|  |   | MIN  | MAX | UNIT |
|--|---|------|-----|------|
| Supply Voltage Range                         | V <sub>CC</sub>   | -0.3 | 4   | V    |
| Voltage Range at any input or output pin     | Differential voltage between positive and negative inputs | -2.5 | 2.5 | V    |
|  | Voltage at differential inputs                            | -0.5 | 4   | V    |
|  | CMOS Inputs   | -0.5 | 4   | V    |
| Maximum junction temperature, T <sub>J</sub> | TUSB1142  |      | 105 | °C   |
|  | TUSB1142I   |      | 125 | °C   |
| Storage temperature, T <sub>stg</sub>        |   | -65  | 150 | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±1500 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                    |   | MIN | NOM | MAX | UNIT |
|--------------------|---|-----|-----|-----|------|
| V <sub>CC</sub>    | Main power supply   | 3.0 | 3.3 | 3.6 | V    |
|                    | Main supply ramp requirement  | 0.1 |     | 50  | ms   |
| V <sub>(I2C)</sub> | Supply that external resistors are pulled up to for both SDA and SCL pins | 1.7 |     | 3.6 | V    |
| V <sub>(PSN)</sub> | Supply Noise on V <sub>CC</sub> pins (less than 4MHz)                     |     |     | 50  | mVpp |
| T <sub>A</sub>     | TUSB1142 Operating free-air temperature                                   | 0   |     | 70  | °C   |
|                    | TUSB1142I Operating free-air temperature                                  | -40 |     | 85  | °C   |

### 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TUSB1142   | UNIT |
|-------------------------------|--|------------|------|
|                               |  | RNQ (WQFN) |      |
|                               |  | 40 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 31.4       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 21.8       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 12.2       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.3        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 12.2       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 4.3        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER              |   | TEST CONDITIONS  | MIN | TYP   | MAX | UNIT |
|------------------------|---|--|-----|-------|-----|------|
| $P_{ACTIVE-USB-1Port}$ | Average active power<br>USB Only for single port. | Link in U0 with GEN2 data transmission;<br>EQ control pins = NC; PRBS7 pattern at<br>10 Gbps, $V_{ID} = 1000\text{ mV}_{PP}$ ; LINR_L3;<br>EN = H; |     | 275   |     | mW   |
| $P_{NC-USB-SLP\#}$     | Average power with no connection<br>with SLP_S0#  | No USB3.2 GEN2 device is connected to<br>CTX1; EN = H; SLP_S0#;  |     | 0.13  |     | mW   |
| $P_{NC-USB-1Port}$     | Average power with no connection                  | No USB3.2 GEN2 device is connected to<br>CTX1;<br>EN = H;  |     | 1.5   |     | mW   |
| $P_{U2U3-SLP\#}$       | Average power in U2/U3 with<br>SLP_S0#            | Link in U2 or U3; EN = H; SLP_S0# = L;   |     | 0.24  |     | mW   |
| $P_{U2U3-1Port}$       | Average power in U2/U3                            | Link in U2 or U3; EN = H;  |     | 1.9   |     | mW   |
| $P_{DISABLED-I2C}$     | Device Disabled power in I <sup>2</sup> C Mode    | MODE = "F"; EN = H; CTLSEL = 0h;   |     | 0.108 |     | mW   |
| $P_{DISABLED}$         | Device Disabled power in pin-strap                | MODE != "F"; EN = L;   |     | 0.130 |     | mW   |

## 5.6 Control I/O DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                     |  | TEST CONDITIONS   | MIN  | TYP  | MAX | UNIT          |
|---|--|---|------|------|-----|---------------|
| <b>4-level Inputs</b>                         |  |   |      |      |     |               |
| 4-Level $V_{TH}$                              | Threshold 0 / R  | $V_{CC} = 3.3\text{ V}$   |      | 0.55 |     | V             |
| 4-Level $V_{TH}$                              | Threshold R/ Float   | $V_{CC} = 3.3\text{ V}$   |      | 1.65 |     | V             |
| 4-Level $V_{TH}$                              | Threshold Float / 1  | $V_{CC33} = 3.3\text{ V}$   |      | 2.7  |     | V             |
| $I_{IH}$                                      | High level input current with internal<br>resistors disabled.  | $V_{CC} = 3.6\text{ V}$ ; $V_{IN} = 3.6\text{ V}$                                       | -5   |      | 5   | $\mu\text{A}$ |
| $I_{IL}$                                      | Low level input current with internal<br>resistors disabled    | $V_{CC} = 3.6\text{ V}$ ; $V_{IN} = 0\text{ V}$   | -1   |      | 1   | $\mu\text{A}$ |
| $I_{IH-REN}$                                  | High level input current with internal<br>resistors enabled.   | $V_{CC} = 3.6\text{ V}$ ; $V_{IN} = 3.6\text{ V}$                                       | 20   |      | 60  | $\mu\text{A}$ |
| $I_{IL-REN}$                                  | Low level input current with internal<br>resistors enabled.    | $V_{CC} = 3.6\text{ V}$ ; $V_{IN} = 0\text{ V}$   | -100 |      | -40 | $\mu\text{A}$ |
| $R_{PU}$                                      | Internal pullup resistance                                     |   |      | 48   |     | k $\Omega$    |
| $R_{PD}$                                      | Internal pulldown resistance                                   |   |      | 98   |     | k $\Omega$    |
| <b>2-State CMOS Input (EN, SLP_S0#)</b>       |  |   |      |      |     |               |
| $V_{IH}$                                      | High-level input voltage                                       |   | 1.2  |      | 3.6 | V             |
| $V_{IL}$                                      | Low-level input voltage  |   | -0.3 |      | 0.6 | V             |
| $R_{PU}$                                      | Internal pullup resistance (EN, SLP_S0#)                       |   | 250  | 400  | 550 | k $\Omega$    |
| $I_{IH}$                                      | High-level input current (EN, SLP_S0#)                         | $V_{IN} = 3.6\text{ V}$ ; MODE != "F"; VIO_SEL = "0"<br>or "R";                         | -5   |      | 5   | $\mu\text{A}$ |
| $I_{IL}$                                      | Low-level input current (EN, SLP_S0#)                          | $V_{IN} = \text{GND}$ , $V_{CC} = 3.6\text{ V}$ ; MODE !=<br>"F"; VIO_SEL = "0" or "R"; | -11  |      | 11  | $\mu\text{A}$ |
| <b>I<sup>2</sup>C Control Pins (SCL, SDA)</b> |  |   |      |      |     |               |
| $V_{IH\_1p8V}$                                | High-level input voltage when configured<br>for 1.8V I2C level | MODE = "F"; VIO_SEL = "R" or "1";   | 1.2  |      | 3.6 | V             |
| $V_{IL\_1p8V}$                                | Low-level input voltage when configured<br>for 1.8V I2C level  | MODE = "F"; VIO_SEL = "R" or "1";   | -0.3 |      | 0.6 | V             |
| $V_{IH\_3p3V}$                                | High-level input voltage when configured<br>for 3.3V I2C level | MODE = "F"; VIO_SEL = "0" or "F";   | 2.0  |      | 3.6 | V             |
| $V_{IL\_3p3V}$                                | Low-level input voltage when configured<br>for 3.3V I2C level  | MODE = "F"; VIO_SEL = "0" or "F";   | -0.3 |      | 0.8 | V             |
| $V_{OL}$                                      | Low-level output voltage                                       | MODE = "F"; $I_{OL} = 6\text{ mA}$  | 0    |      | 0.4 | V             |
| $I_{OL}$                                      | Low-level output current                                       | MODE = "F"; $V_{OL} = 0.4\text{ V}$   | 20   |      |     | mA            |
| $I_{I(I2C)}$                                  | Input current  | $0.1 \times V_{(I2C)} < \text{Input voltage} < 3.3\text{ V}$                            | -1   |      | 1   | $\mu\text{A}$ |
| $C_{I(I2C)}$                                  | Input capacitance  |   |      |      | 10  | pF            |

## 5.6 Control I/O DC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER             |   | TEST CONDITIONS                | MIN | TYP  | MAX  | UNIT |
|-----------------------|---|--------------------------------|-----|------|------|------|
| $C_{(I2C\_FM+\_BUS)}$ | I <sup>2</sup> C bus capacitance for FM+ (1MHz)                       |                                |     |      | 150  | pF   |
| $C_{(I2C\_FM\_BUS)}$  | I <sup>2</sup> C bus capacitance for FM (400kHz)                      |                                |     |      | 150  | pF   |
| $R_{(EXT\_I2C\_FM+)}$ | External resistors on both SDA and SCL when operating at FM+ (1MHz)   | $C_{(I2C\_FM+\_BUS)} = 150$ pF | 620 | 820  | 910  | Ω    |
| $R_{(EXT\_I2C\_FM)}$  | External resistors on both SDA and SCL when operating at FM (400 kHz) | $C_{(I2C\_FM\_BUS)} = 150$ pF  | 620 | 1500 | 2200 | Ω    |

## 5.7 USB Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER  |  | TEST CONDITIONS   | MIN  | TYP  | MAX | UNIT |
|--|--|---|------|------|-----|------|
| <b>USB Gen 2 Differential Receiver (CRX1p/n, CRX2p/n, SSTX)</b>    |  |   |      |      |     |      |
| $V_{(RX-DIFF-PP)}$   | Input differential peak-peak voltage swing linear dynamic range  | AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel                      |      | 1200 |     | mVpp |
| $V_{(RX-DC-CM)}$   | Common-mode voltage bias in the receiver (DC)  |   |      | 0    |     | V    |
| $V_{RX-CM-INST}$   | Max Instantaneous RX DC common-mode voltage change under all operating conditions (OFF to ON, Disabled to USB, and so forth)                                 | Measured at non-device side of AC coupling capacitor with 200-kΩ load.  | -300 |      | 500 | mV   |
| $R_{(RX-DIFF-DC)}$   | Differential input impedance (DC)  | Present after a GEN2 device is detected.  | 72   | 90   | 120 | Ω    |
| $R_{(RX-CM-DC)}$   | Receiver DC common mode impedance  | Present after a GEN2 device is detected.  | 18   |      | 30  | Ω    |
| $Z_{(RX-HIGH-IMP-DC-POS)}$   | Common-mode input impedance with termination disabled (DC)   | Present when no GEN2 device is detected on transmitter. Measured over the range of 0-500mV with respect to GND. | 25   |      |     | kΩ   |
| $V_{(SIGNAL-DET-DIFF-PP)}$   | Input differential peak-to-peak signal detect assert level   | At 10 Gbps, no input loss, PRBS7 pattern  |      | 75   |     | mV   |
| $V_{(RX-IDLE-DET-DIFF-PP)}$  | Input differential peak-to-peak signal detect deassert Level   | At 10 Gbps, no input loss, PRBS7 pattern  |      | 55   |     | mV   |
| $V_{(RX-LFPS-DET-DIFF-PP)}$  | Low frequency periodic signaling (LFPS) detect threshold   | Below the minimum is squelched  | 100  |      | 300 | mV   |
| $V_{(RX-CM-AC-P)}$   | Peak RX AC common-mode voltage   | Measured at package pin   |      |      | 150 | mV   |
| $C_{(RX)}$   | RX input capacitance to GND  | At 5 GHz;   |      |      | 1   | pF   |
| $R_{L(RX-DIFF)}$   | Differential return Loss   | 50 MHz – 1.25 GHz at 85 Ω;  |      | -22  |     | dB   |
|  |  | 5 GHz at 85 Ω;  |      | -20  |     | dB   |
| $R_{L(RX-CM)}$   | Common-mode return loss  | 50 MHz – 5 GHz at 85 Ω;   |      | -12  |     | dB   |
| $E_{Q\_SSTX15}$  | SSTX->CTX1 Receiver equalization at 5 GHz  | SSEQ1_SEL = 15; Gain at 5GHz minus Gain at 10MHz;   |      | 13.6 |     | dB   |
| $E_{Q\_RX15}$  | CRX1 -> SSRX Receiver equalization at 5 GHz  | CEQ1_SEL = 15; Gain at 5GHz minus Gain at 10MHz;  |      | 12.7 |     | dB   |
| $C_{AC-USB1}$  | Required external AC capacitor on SSTX   |   | 75   |      | 265 | nF   |
| $C_{AC-USB2}$  | Optional external AC capacitor on CRX1 and CRX2.   |   | 297  |      | 363 | nF   |
| <b>USB Gen 2 Differential Transmitter (CTX1p/n, CTX2p/n, SSRX)</b> |  |   |      |      |     |      |
| $V_{TX(DIFF-PP)}$  | Transmitter dynamic differential voltage swing range.  | EQ15; VID = 1Vpp; LINR_L3   |      | 1200 |     | mVpp |
| $V_{TX(RCV-DETECT)}$   | Amount of voltage change allowed during receiver detection   |   |      |      | 600 | mV   |
| $V_{TX-CM-INST-ONOFF}$   | Max Instantaneous TX DC common-mode voltage change under operating condition: OFF to ON, ON to OFF, during Rx.Detect; Disconnect to U0, U2/U3 to Disconnect. | Measured single-ended at non-device side of AC coupling capacitor with 200-kΩ load.                             | -500 |      | 800 | mV   |
| $V_{TX(CM-IDLE-DELTA)}$  | Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS  |   | -300 |      | 600 | mV   |
| $V_{TX(DC-CM)}$  | Common-mode voltage bias in the transmitter (DC)   |   | 0.5  | 0.76 | 1   | V    |
| $V_{TX(CM-AC-PP-ACTIVE)}$  | Tx AC common-mode voltage active   | Max mismatch from Txp + Txn for both time and amplitude   |      |      | 100 | mVpp |
| $V_{TX(IDLE-DIFF-AC-PP)}$  | AC electrical idle differential peak-to-peak output voltage  | At package pins   | 0    |      | 10  | mV   |
| $V_{TX(CM-DC-ACTIVE-IDLE-DELTA)}$                                  | Absolute DC common-mode voltage between U1 and U0  | At package pin  |      |      | 200 | mV   |

## 5.7 USB Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER                       |   | TEST CONDITIONS   | MIN | TYP  | MAX  | UNIT |
|---------------------------------|---|---|-----|------|------|------|
| R <sub>TX(DIFF)</sub>           | Differential impedance of the driver  |   | 80  | 90   | 120  | Ω    |
| R <sub>TX(CM)</sub>             | Common-mode impedance of the driver   | Measured with respect to AC ground over 0–500 mV  | 18  |      | 30   | Ω    |
| V <sub>SSRX-LIMITED-VODL0</sub> | SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L0 | TX_PRESHOOT_EN = 0;<br>TX_DEEMPHASIS_EN = 0;  |     | 750  |      | mVpp |
| V <sub>SSRX-LIMITED-VODL1</sub> | SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L1 | TX_PRESHOOT_EN = 0;<br>TX_DEEMPHASIS_EN = 0;  |     | 900  |      | mVpp |
| V <sub>SSRX-LIMITED-VODL2</sub> | SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L2 | TX_PRESHOOT_EN = 0;<br>TX_DEEMPHASIS_EN = 0;  |     | 1000 |      | mVpp |
| V <sub>SSRX-LIMITED-VODL3</sub> | SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L3 | TX_PRESHOOT_EN = 0;<br>TX_DEEMPHASIS_EN = 0;  |     | 1100 |      | mVpp |
| V <sub>SSRX-DE-RATIO0</sub>     | SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.          | TX_PRESHOOT_EN = 0;<br>TX_DEEMPHASIS_EN = 1;<br>TX_DEEPHASIS = 2'b00;<br>USB_SSRX_VOD = 2'b00 (LINR_L3);<br>Refer to <a href="#">Figure 6-7</a> |     | –1.8 |      | dB   |
| V <sub>SSRX-DE-RATIO1</sub>     | SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.          | TX_PRESHOOT_EN = 0;<br>TX_DEEMPHASIS_EN = 1;<br>TX_DEEPHASIS = 2'b01;<br>USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to <a href="#">Figure 6-7</a>    |     | –2.1 |      | dB   |
| V <sub>SSRX-DE-RATIO2</sub>     | SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.          | TX_PRESHOOT_EN = 0;<br>TX_DEEMPHASIS_EN = 1;<br>TX_DEEPHASIS = 2'b10;<br>USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to <a href="#">Figure 6-7</a>    |     | –3.2 |      | dB   |
| V <sub>SSRX-DE-RATIO3</sub>     | SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.          | TX_PRESHOOT_EN = 0;<br>TX_DEEMPHASIS_EN = 1;<br>TX_DEEPHASIS = 2'b11;<br>USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to <a href="#">Figure 6-7</a>    |     | –3.8 |      | dB   |
| V <sub>SSRX-PRESH-RATIO0</sub>  | SSRX preshoot level when configured for limited redriver and preshoot enabled.          | TX_PRESHOOT_EN = 1;<br>TX_DEEMPHASIS_EN = 0;<br>TX_PRESHOOT = 2'b00;<br>USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to <a href="#">Figure 6-6</a>     |     | 1.6  |      | dB   |
| V <sub>SSRX-PRESH-RATIO1</sub>  | SSRX preshoot level when configured for limited redriver and preshoot enabled.          | TX_PRESHOOT_EN = 1;<br>TX_DEEMPHASIS_EN = 0;<br>TX_PRESHOOT = 2'b01;<br>USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to <a href="#">Figure 6-6</a>     |     | 2.1  |      | dB   |
| V <sub>SSRX-PRESH-RATIO2</sub>  | SSRX preshoot level when configured for limited redriver and preshoot enabled.          | TX_PRESHOOT_EN = 1;<br>TX_DEEMPHASIS_EN = 0;<br>TX_PRESHOOT = 2'b10;<br>USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to <a href="#">Figure 6-6</a>     |     | 2.5  |      | dB   |
| V <sub>SSRX-PRESH-RATIO3</sub>  | SSRX preshoot level when configured for limited redriver and preshoot enabled.          | TX_PRESHOOT_EN = 1;<br>TX_DEEMPHASIS_EN = 0;<br>TX_PRESHOOT = 2'b11;<br>USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to <a href="#">Figure 6-6</a>     |     | 3.0  |      | dB   |
| I <sub>TX(SHORT)</sub>          | TX short circuit current  | TX± shorted to GND  |     |      | 60   | mA   |
| C <sub>TX(PARASITIC)</sub>      | TX input capacitance for return loss  | At package pins, at 5 GHz   |     |      | 1.25 | pF   |
| R <sub>LTX(DIFF)</sub>          | Differential return loss  | 50 MHz – 1.25 GHz at 85 Ω   |     | –28  |      | dB   |
| R <sub>LTX(CM)</sub>            | Common-mode return loss   | 50 MHz – 5 GHz at 85 Ω  |     | –12  |      | dB   |
| C <sub>TX-AC(COUPLING)</sub>    | External required AC coupling capacitor   |   | 75  |      | 265  | nF   |
| <b>AC Characteristics</b>       |   |   |     |      |      |      |

## 5.7 USB Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER                     |   | TEST CONDITIONS  | MIN | TYP  | MAX | UNIT |
|-------------------------------|---|--|-----|------|-----|------|
| Crosstalk_CRXTX               | Differential crosstalk between CTX1/2 and CRX1/2 signal pairs | 85 Ω; At 5 GHz; SSEQ[1:0] = 0; CEQ[1:0] = 0;   |     |      | -40 | dB   |
| CP <sub>LF-LINRL0</sub>       | Low-frequency -1dB compression point at LINR_L0 setting.      | 20 MHz clock pattern; VID is 200mV to 1200mV in 10mV steps;  |     | 750  |     | mVpp |
| CP <sub>HF-LINRL0</sub>       | High-frequency -1dB compression point at LINR_L0 setting.     | 5 GHz clock pattern; VID is 200mV to 1200mV in 10mV steps;   |     | 650  |     | mVpp |
| CP <sub>LF-LINRL1</sub>       | Low-frequency -1dB compression point at LINR_L1 setting.      | 20 MHz clock pattern; VID is 200mV to 1200mV in 10mV steps;  |     | 850  |     | mVpp |
| CP <sub>HF-LINRL1</sub>       | High-frequency -1dB compression point at LINR_L1 setting.     | 5 GHz clock pattern; VID is 200mV to 1200mV in 10mV steps;   |     | 750  |     | mVpp |
| CP <sub>LF-LINRL2</sub>       | Low-frequency -1dB compression point at LINR_L2 setting.      | 20 MHz clock pattern; VID is 200mV to 1200mV in 10mV steps;  |     | 950  |     | mVpp |
| CP <sub>HF-LINRL2</sub>       | High-frequency -1dB compression point at LINR_L2 setting.     | 5 GHz clock pattern; VID is 200mV to 1200mV in 10mV steps;   |     | 850  |     | mVpp |
| CP <sub>LF-LINRL3</sub>       | Low-frequency -1dB compression point at LINR_L3 setting.      | 20 MHz clock pattern; VID is 200mV to 1200mV in 10mV steps;  |     | 1050 |     | mVpp |
| CP <sub>HF-LINRL3</sub>       | High-frequency -1dB compression point at LINR_L3 setting.     | 5 GHz clock pattern; VID is 200mV to 1200mV in 10mV steps;   |     | 900  |     | mVpp |
| f <sub>LF</sub>               | Low frequency cutoff  | 200 mV <sub>pp</sub> < V <sub>ID</sub> < 1200 mV <sub>pp</sub>   |     | 20   | 50  | kHz  |
| t <sub>TX_DJ_SSTX1-CTX1</sub> | TX output deterministic residual jitter SSTX-> CTX.           | Optimal EQ setting; 12-in prechannel (SDD21 = -11.2dB); 1.6-in post channel (SDD21 = -1.8dB); PRBS7; 10 Gbps |     | .05  |     | UI   |

## 5.8 Timing Requirements

|                                 |   |  | MIN | NOM | MAX  | UNIT |
|---------------------------------|---|--|-----|-----|------|------|
| <b>USB3.1</b>                   |   |  |     |     |      |      |
| t <sub>DLEEntry</sub>           | Delay from U0 to electrical idle  | Refer to <a href="#">Figure 6-4</a> .  |     |     | 10   | ns   |
| t <sub>DELExit_U1</sub>         | U1 exit time: break in electrical idle to the transmission of LFPS                | Refer to <a href="#">Figure 6-4</a> .  |     |     | 1    | ns   |
| t <sub>DLEExit_U2U3</sub>       | U2/U3 exit time: break in electrical idle to transmission of LFPS                 | Refer to <a href="#">Figure 6-4</a> .  |     | 10  |      | μs   |
| t <sub>RXDET_INTVL</sub>        | RX detect interval while in Disconnect  |  |     |     | 12   | ms   |
| t <sub>DLEExit_DISC</sub>       | Disconnect Exit Time  |  |     | 10  |      | μs   |
| t <sub>Exit_SHTDN</sub>         | Shutdown Exit Time  |  |     |     | 0.75 | ms   |
| t <sub>AEQ_FULL_DONE</sub>      | Maximum time to obtain optimum EQ setting when operating in Full AEQ mode.        |  |     |     | 400  | μs   |
| t <sub>AEQ_FAST_DONE</sub>      | Maximum time to determine appropriate EQ setting when operating in Fast AEQ mode. |  |     |     | 60   | μs   |
| t <sub>DIFF_DLY</sub>           | Differential Propagation Delay  | Refer to <a href="#">Figure 6-3</a> .  |     |     | 300  | ps   |
| t <sub>R</sub> , t <sub>F</sub> | Output Rise/Fall time   | 20%-80% of differential voltage measured 1.7 inch from the output pin; Refer to <a href="#">Figure 6-5</a> . | 30  |     |      | ps   |
| t <sub>RF_MM</sub>              | Output Rise/Fall time mismatch  | 20%-80% of differential voltage measured 1.7 inch from the output pin  |     |     | 2.6  | ps   |
| <b>Power-up</b>                 |   |  |     |     |      |      |
| t <sub>EN_LOW</sub>             | EN pin held low after supply reaches VCC(min)                                     | Refer to <a href="#">Figure 6-1</a>  | 5   |     |      | ms   |
| t <sub>CFG_SU</sub>             | CFG <sup>(1)</sup> high   | Refer to <a href="#">Figure 6-1</a>  | 250 |     |      | μs   |
| t <sub>CFG_HD</sub>             | CFG <sup>(1)</sup> high   | Refer to <a href="#">Figure 6-1</a>  | 500 |     |      | μs   |

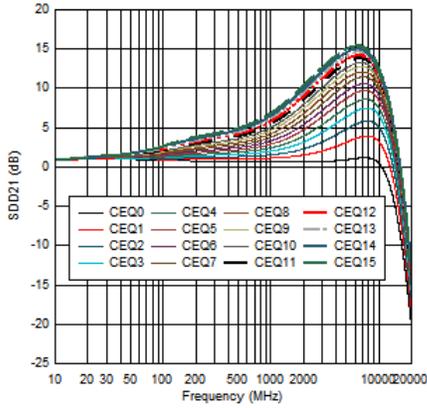
(1) Following pins comprise CFG pins: MODE, CEQ[1:0], SSEQ[1:0], EQCFG, AEQCFG

## 5.9 Switching Characteristics

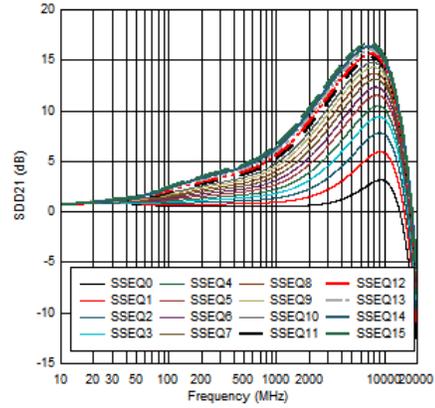
over operating free-air temperature range (unless otherwise noted)

| PARAMETER             |   | TEST CONDITIONS                     | MIN                            | TYP | MAX | UNIT |
|-----------------------|---|-------------------------------------|--------------------------------|-----|-----|------|
| <b>I<sup>2</sup>C</b> |   |                                     |                                |     |     |      |
| f <sub>SCL</sub>      | I <sup>2</sup> C clock frequency  |                                     |                                |     | 1   | MHz  |
| t <sub>BUF</sub>      | Bus free time between START and STOP conditions   | Refer to <a href="#">Figure 6-2</a> | 0.5                            |     |     | μs   |
| t <sub>HD_STA</sub>   | Hold time after repeated START condition. After this period, the first clock pulse is generated | Refer to <a href="#">Figure 6-2</a> | 0.26                           |     |     | μs   |
| t <sub>LOW</sub>      | Low period of the I <sup>2</sup> C clock  | Refer to <a href="#">Figure 6-2</a> | 0.5                            |     |     | μs   |
| t <sub>HIGH</sub>     | High period of the I <sup>2</sup> C clock   | Refer to <a href="#">Figure 6-2</a> | 0.26                           |     |     | μs   |
| t <sub>SU_STA</sub>   | Setup time for a repeated START condition   | Refer to <a href="#">Figure 6-2</a> | 0.26                           |     |     | μs   |
| t <sub>HD_DAT</sub>   | Data hold time  | Refer to <a href="#">Figure 6-2</a> | 0                              |     |     | μs   |
| t <sub>SU_DAT</sub>   | Data setup time   | Refer to <a href="#">Figure 6-2</a> | 50                             |     |     | ns   |
| t <sub>R</sub>        | Rise time of both SDA and SCL signals   | Refer to <a href="#">Figure 6-2</a> |                                |     | 120 | ns   |
| t <sub>F</sub>        | Fall time of both SDA and SCL signals   | Refer to <a href="#">Figure 6-2</a> | 20 × (V <sub>I2C</sub> /5.5 V) |     | 120 | ns   |
| t <sub>SU_STO</sub>   | Setup time for STOP condition   | Refer to <a href="#">Figure 6-2</a> | 0.26                           |     |     | μs   |
| C <sub>b</sub>        | Capacitive load for each bus line   |                                     |                                |     | 150 | pF   |

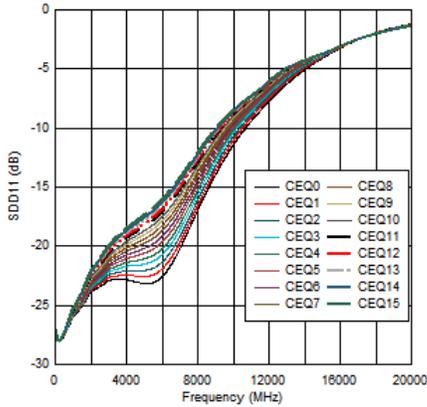
### 5.10 Typical Characteristics



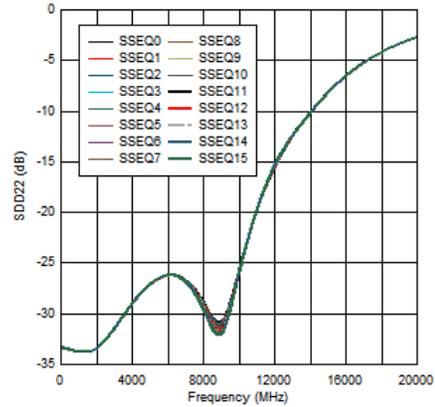
**Figure 5-1. USB CRX1 EQ Settings Curves at 85 Ω (from simulation)**



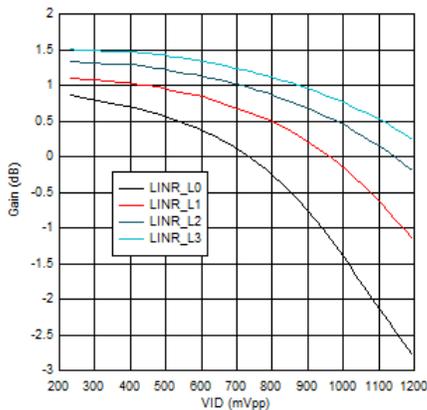
**Figure 5-2. USB SSTX EQ Settings Curves at 85 Ω (from simulation)**



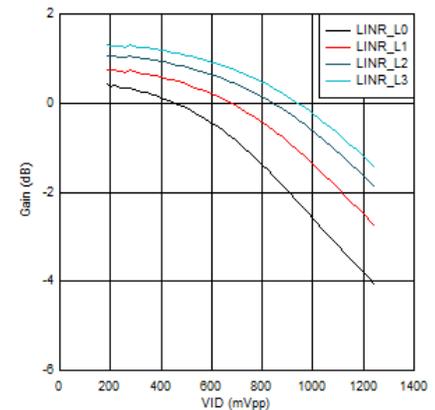
**Figure 5-3. CRX1 Input Return Loss Performance at 85 Ω (from simulation)**



**Figure 5-4. CTX1 Output Return Loss Performance at 85 Ω (from simulation)**

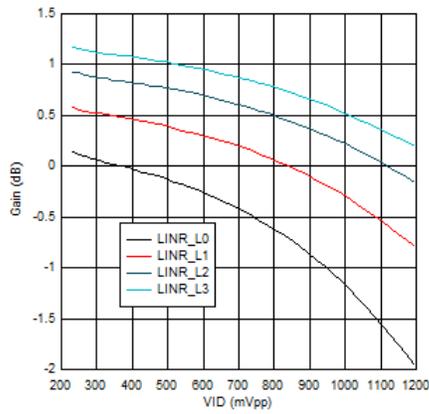


**Figure 5-5. USB SSRX VOD Linearity Settings at 20 MHz and EQ = 0**

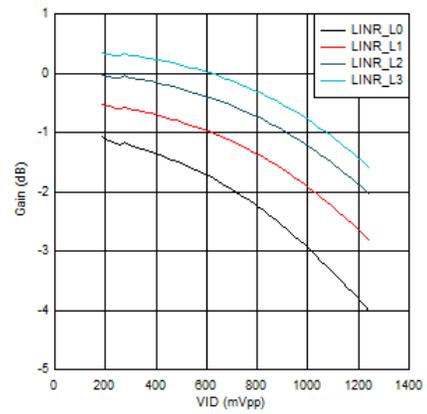


**Figure 5-6. USB SSRX VOD Linearity Settings at 5 GHz and EQ = 0**

### 5.10 Typical Characteristics (continued)

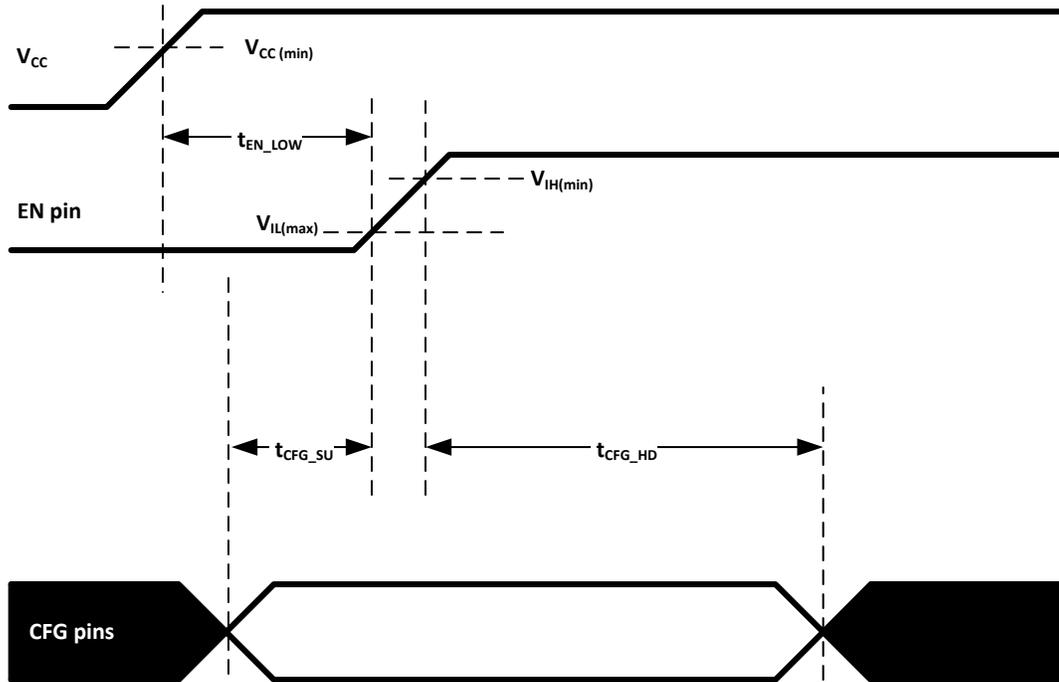


**Figure 5-7. USB CTX1 VOD Linearity Settings at 20 MHz and EQ = 0**

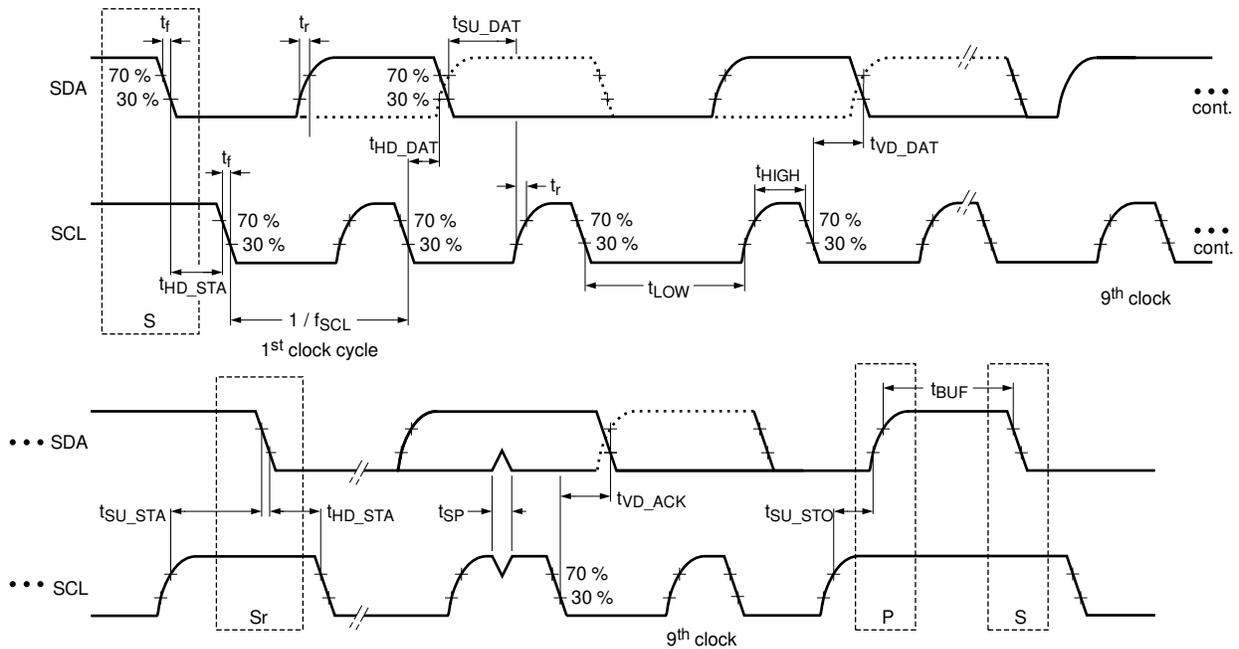


**Figure 5-8. USB CTX1 VOD Linearity Settings at 5 GHz and EQ = 0**

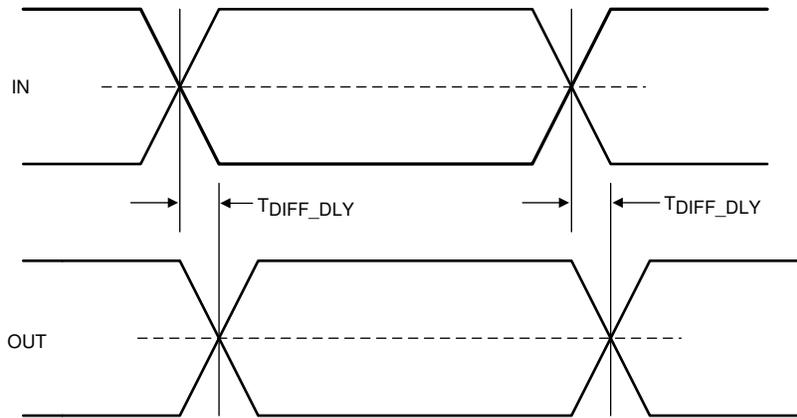
## 6 Parameter Measurement Information



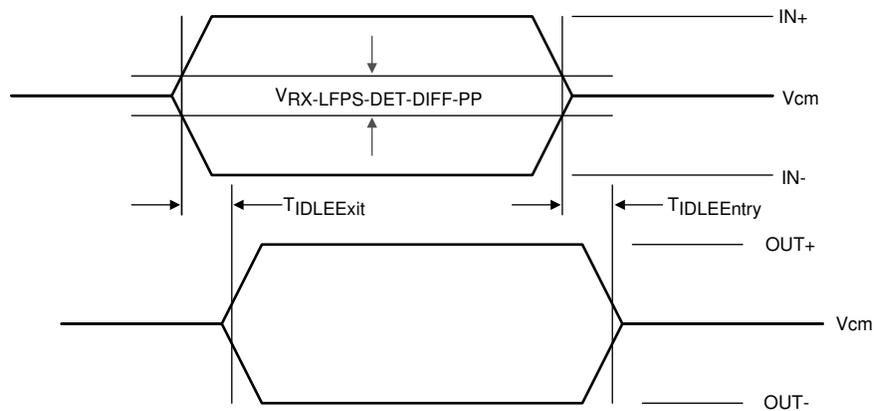
**Figure 6-1. Power-On Timing Requirements**



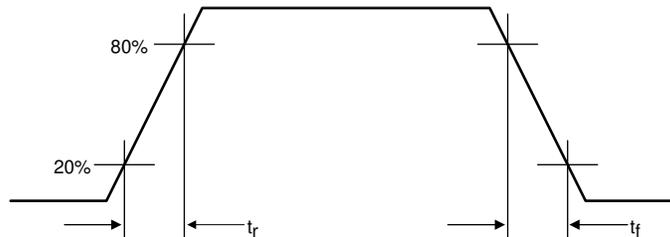
**Figure 6-2. I2C Timing Diagram Definitions**



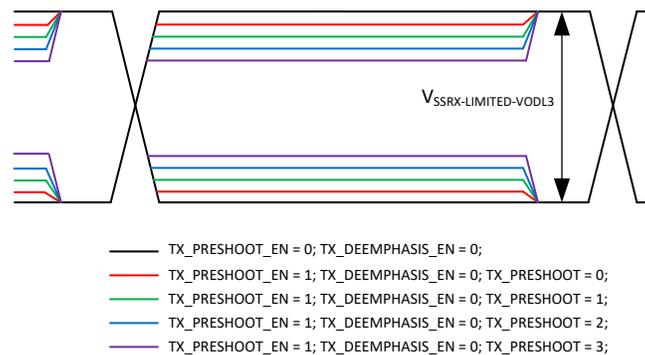
**Figure 6-3. USB Propagation Delay**



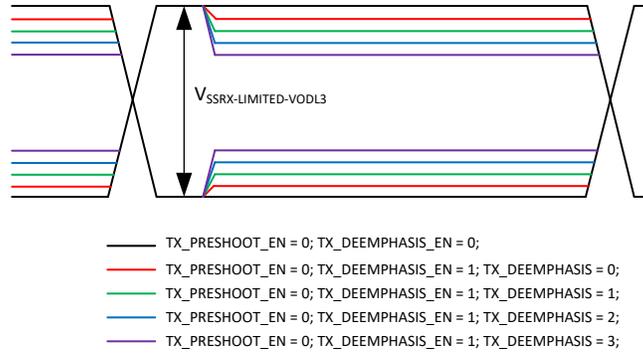
**Figure 6-4. Electrical Idle Exit and Entry Delay**



**Figure 6-5. Output Rise and Fall Times**



**Figure 6-6. SSRX Limited Preshoot Only**



**Figure 6-7. SSRX Limited De-Emphasis Only**

## 7 Detailed Description

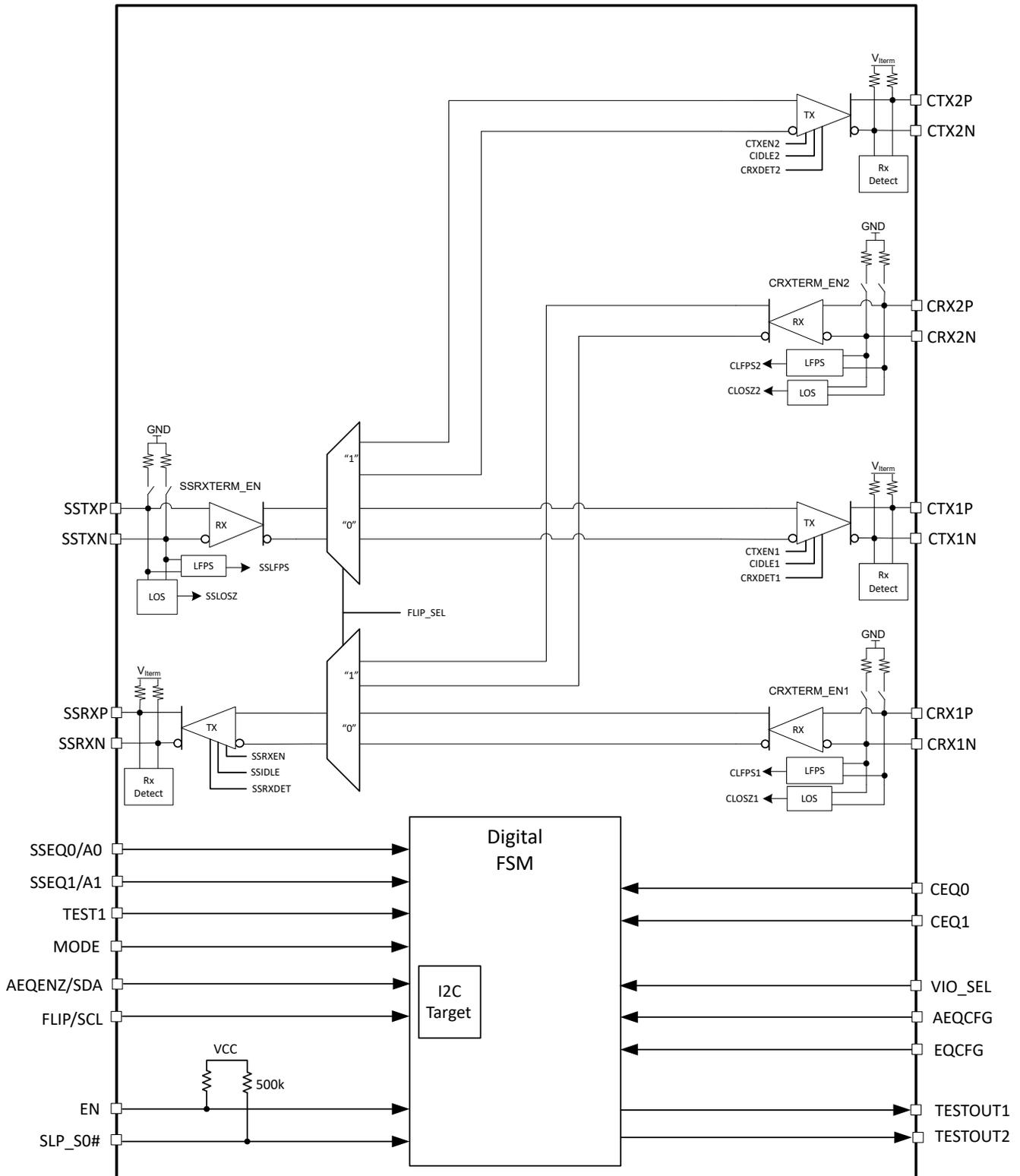
### 7.1 Overview

The TUSB1142 is a 10 Gbps USB 3.2 linear redriver with 1:2 DeMUX or 2:1 Mux function for USB-C applications. The TUSB1142 is intended to reside between a Host and a USB-C receptacle or between a USB device and a USB-C receptacle. The TUSB1142 supports both USB 3.2 Gen2 (10 Gbps) and Gen1 (5 Gbps) as well as USB 3.2 low power states (Disconnect, U1, U2, and U3).

The TUSB1142 supports up to 16 receiver equalization settings controlled by either pin-strap pins or through I2C registers. The USB connector facing receivers (CRX1 and CRX2) support three equalization modes: Fixed EQ, Fast AEQ, and Full AEQ. Selection between these modes is done through either pin-strap pins or through I2C registers. The other receivers (SSTX) only support Fixed EQ.

The TUSB1142 operates as a linear redriver for signals traversing from the SSTX receivers towards CTX1/2 transmitters. It can operate as either a linear redriver or limited redriver for signals traversing from CRX1/2 receivers towards SSRX transmitters. TUSB1142 defaults to linear redriver but can be enabled for limited redriver by I2C register. When enabled for limited redriver, the SSRX transmitter support four levels of preshoot and four-levels of de-emphasis.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 4-Level Inputs

The TUSB1142 has 4-level inputs pins that are used to control the receiver equalization gain, transmitter voltage swing, and place TUSB1142 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There are internal pullup and pulldown resistors. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

**Table 7-1. 4-Level Control Pin Settings**

| LEVEL | SETTINGS                                 |
|-------|--|
| 0     | Tie 1-k $\Omega$ 5% to GND.              |
| R     | Tie 20-k $\Omega$ 5% to GND.             |
| F     | Float (leave pin open)                   |
| 1     | Tie 1-k $\Omega$ 5% to V <sub>CC</sub> . |

---

#### Note

All 4-level inputs are latched after the rising edge of EN pin. After these pins are sampled, the internal pullup and pulldown resistors will be isolated in order to save power.

---

### 7.3.2 USB Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TUSB1142. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss before the input of the TUSB1142 receivers. Two 4-level inputs pins enable up to 16 possible equalization settings when in pin-strap mode. The TUSB1142's USB 3.2 host, hub, and device receivers (SSTX) and USB 3.2 USB connector receivers (CRX1/2) each have their own two 4-level inputs. The TUSB1142 also provides the flexibility of adjusting settings through I<sup>2</sup>C registers.

The TUSB1142's USB host, hub, and device facing port receiver (SSTX) only support Fixed EQ (FEQ). The TUSB1142 implements three different equalizer features for the USB connector facing port receivers (CRX1 and CRX2): Fixed EQ (FEQ), Fast Adaptive EQ (Fast AEQ), and Full Adaptive EQ (Full AEQ). In Fixed EQ operation, a single setting is used for all possible devices (with and without cable) inserted into the USB receptacle. The Fast AEQ feature will distinguish between a short channel and a long channel. A short channel represents a low loss use case of a USB 3.2 device plugged directly into USB receptacle without a cable. A long channel represents the high loss use case of the USB 3.2 device plugged into the receptacle through a USB cable. In Fast AEQ mode, TUSB1142 will select between two pre-determined settings based on whether or not channel is short or long. When TUSB1142 is configured for Full AEQ, the TUSB1142 will automatically determine what it believes is the best equalization setting each time a USB device is inserted into the USB receptacle. In Full AEQ mode, the TUSB1142 will attempt to determine the best settings regardless if the channel is short, long, or somewhere in between.

---

#### Note

Adaptive EQ is only supported on CRX1 and CRX2. Adaptive EQ must only be used when CRX1 and CRX2 is connected to a USB receptacle. If CRX1 and CRX2 is connected directly (not through a USB receptacle) to a USB Host, USB Hub or USB Device, then adaptive EQ must be disabled. AEQ should never be enabled in a active cable application. If daisy chaining multiple TUSB1142, AEQ should only be enabled on the TUSB1142 that is near the USB receptacle.

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### 7.3.2.1 Linear EQ Configuration

Each of the TUSB1142 receiver lanes have individual controls for receiver equalization. The receiver equalization gain value can be controlled either through I<sup>2</sup>C registers or through pin-straps. [Table 7-2](#) and [Table 7-3](#) details the gain value for each available combination when TUSB1142 is in pin-strap mode. These same options are also available in I<sup>2</sup>C mode by updating registers CEQ1\_SEL, CEQ2\_SEL, and SSEQ1\_SEL.

**Table 7-2. USB Connector Facing Port Receiver (CRX1 and CRX2 pins) Equalization Control**

| Register(s): CEQ1_SEL or CEQ2_SEL<br>Equalization Setting # | CEQ1 PIN Level | CEQ0 PIN Level | EQ Gain at 5 GHz minus Gain at 100 MHz (dB) |
|---|----------------|----------------|---|
| 0   | 0              | 0              | -0.4  |
| 1   | 0              | R              | 1.9   |
| 2   | 0              | F              | 3.5   |
| 3   | 0              | 1              | 5.0   |
| 4   | R              | 0              | 6.1   |
| 5   | R              | R              | 7.2   |
| 6   | R              | F              | 8.0   |
| 7   | R              | 1              | 8.8   |
| 8   | F              | 0              | 9.6   |
| 9   | F              | R              | 10.2  |
| 10  | F              | F              | 10.7  |
| 11  | F              | 1              | 11.2  |
| 12  | 1              | 0              | 11.6  |
| 13  | 1              | R              | 12.0  |
| 14  | 1              | F              | 12.4  |
| 15  | 1              | 1              | 12.7  |

**Table 7-3. USB Host Facing Port Receiver (SSTX) Equalization Control**

| Register(s): SSEQ1_SEL<br>Equalization Setting # | SSEQ1 PIN LEVEL | SSEQ0 PIN LEVEL | EQ Gain at 5 GHz minus Gain at 100 MHz (dB) |
|--|-----------------|-----------------|---|
| 0  | 0               | 0               | 0.6   |
| 1  | 0               | R               | 2.8   |
| 2  | 0               | F               | 4.5   |
| 3  | 0               | 1               | 6.0   |
| 4  | R               | 0               | 7.0   |
| 5  | R               | R               | 8.0   |
| 6  | R               | F               | 9.0   |
| 7  | R               | 1               | 10.0  |
| 8  | F               | 0               | 10.6  |
| 9  | F               | R               | 11.2  |
| 10   | F               | F               | 11.7  |
| 11   | F               | 1               | 12.2  |
| 12   | 1               | 0               | 12.5  |
| 13   | 1               | R               | 13.0  |
| 14   | 1               | F               | 13.3  |
| 15   | 1               | 1               | 13.6  |

### 7.3.2.2 Full Adaptive Equalization

The Full AEQ mode attempts to find what it believes is the best equalization value for CRX1 and CRX2 receivers by starting at the lowest EQ value and sweeping through all EQ combinations up to the value programmed into FULLAEQ\_UPPER\_EQ field. The default is to sweep through nine EQ values (zero to eight). The number of EQ combinations can be adjusted by programming FULLAEQ\_UPPER\_EQ register. The TUSB1142 also provides the ability to add or subtract some over/under equalization to compensate for channel in front of TUSB1142 by programming OVER\_EQ\_CTRL field to a non-zero value. If OVER\_EQ\_SIGN = 0, the TUSB1142 will add the value programmed into OVER\_EQ\_CTRL to the EQ value determined by the full adaptation. If OVER\_EQ\_SIGN = 1, the TUSB1142 will subtract the value programmed into OVER\_EQ\_CTRL from the EQ value determined by the full adaptation. For example, if full adaptation determines the best equalization value to be 4 and OVER\_EQ\_CTRL is 2 and OVER\_EQ\_SIGN = 0, the EQ setting used by TUSB1142 will be 6. The TUSB1142 hardware will always limit the sum of OVER\_EQ\_CTRL and the determined optimal EQ from full adaptation to be less than or equal to 15.

---

#### Note

Full AEQ is supported in both pin-strap and I<sup>2</sup>C mode. In pin-strap mode, enable or disable of Full AEQ is determined by the state of AEQENZ pin.

---

### 7.3.2.3 Fast Adaptive Equalization

The Fast AEQ mode is used to distinguish two channels (short channel and a long channel) and choose the appropriate receiver equalization setting for that channel. Because Fast AEQ only distinguishes between two choices, the AEQ time is a lot shorter than Full AEQ mode which minimizes impact to USB link training.

When Fast AEQ is enabled and channel is determined to be short, the TUSB1142 will use the value programmed into the CEQx\_SEL, where x = 1 or 2. If the TUSB1142 determines channel is not short, the TUSB1142 will switch to EQ value programmed into LONG\_EQx register, where x = 1 or 2. During initial system evaluation, it is recommended to perform both short and long channel USB 3.1 RX JTOL Gen2 testing and program CEQx\_SEL and LONG\_EQx to the value which produced the best results for each channel configuration.

The TUSB1142 will determine short and long based on the estimate eye height. The value programmed into FASTAEQ\_LIMITS register will determine the eye height limits. Software can change the defaults of this register to lower or raise the limits.

---

#### Note

Fast AEQ is only supported in I<sup>2</sup>C mode.

EQ\_OVERRIDE field must be set for values programmed into CEQx\_SEL and LONG\_EQx to be used.

---

## 7.3.3 USB Transmitter

### 7.3.3.1 Linearity VOD

Linearity VOD defines the linearity range of the TUSB1142. When TUSB1142 is in linear VOD mode, the output VOD is a linear function of the input VID. For example, if the signal at TUSB1142's input (VID) is at 600 mVpp then the TUSB1142's output VOD will be around 600 mVpp. Linearity VOD mode is the default operation of the TUSB1142. Linear VOD mode is supported on SSRX and CTX1/2 transmitters.

The TUSB1142 provides four different linearity VOD settings. All four settings are available in I<sup>2</sup>C mode through register control. In pin-strap mode, the linearity is fixed at the highest setting.

### 7.3.3.2 Limited VOD

Limited VOD mode is used to set the actual VOD level and is used when TUSB1142 is configured in limited redriver mode. In this mode the VOD is no longer a linear function of the input VID. For example, if the signal at TUSB1142's input (VID) is at 600 mVpp then the TUSB1142's output VOD will be around 1000 mVpp (assuming LINR\_L3 is selected). The limited redriver mode is only supported on the SSRX transmitter. The TUSB1142 provides four different limited VOD settings. All four settings are available through register control.

#### Note

Limited redriver mode is disabled by default and can only be enabled by setting the SSRX\_LIMIT\_ENABLE register. Once enabled, the VOD level for SSRX transmitters is controlled by the USB\_SSRX\_VOD register

### 7.3.3.3 Transmit Equalization (Limited Redriver Mode Only)

The TUSB1142 in limited redriver mode offers preshoot and de-emphasis controls for SSRX transmitter. The TUSB1142 offers four preshoot levels and four de-emphasis levels. These levels can be changed by modifying I<sup>2</sup>C registers.

SSRX transmitter equalization is controlled by TX\_PRESHOOT and TX\_DEEMPHASIS fields. When SSRX\_LIMIT\_ENABLE = 1 and TX\_PRESHOOT\_EN = 1, the TX\_PRESHOOT field selects between four different preshoot levels. When SSRX\_LIMIT\_ENABLE = 1 and TX\_DEEMPHASIS\_EN = 1, the TX\_DEEMPHASIS field selects between four different de-emphasis levels.

#### Note

Transmitter equalization control is not supported in pin-strap mode.

### 7.3.4 USB 3.2 2:1 MUX Description

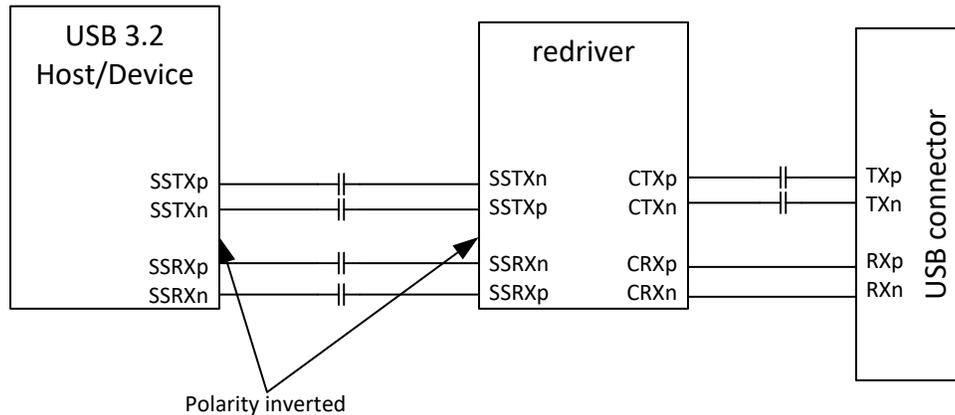
The TUSB1142 implements a 2:1 MUX between the USB-C receptacle and the USB 3.2 Host, Hub or device. In pin-strap mode the selection of MUX path is controlled from the FLIP pin. In I<sup>2</sup>C mode, the MUX is controlled by FLIP\_SEL register. Refer to [Table 7-4](#) for details.

**Table 7-4. USB 3.2 MUX Control**

| FLIP pin or FLIP_SEL register | EN pin or CTLSEL register | USB Path     |
|-------------------------------|---------------------------|--------------|
| X                             | 0                         | Disabled     |
| 0                             | 1                         | CRX1 -> SSRX |
|                               |                           | SSTX -> CTX1 |
| 1                             | 1                         | CRX2 -> SSRX |
|                               |                           | SSTX -> CTX2 |

### 7.3.5 USB Polarity Inversion

The USB 3.2 standard requires all host, hubs, and devices support USB polarity inversion detection and correction. For this reason, polarity between TUSB1142 and USB connector as well as between USB Host/Device and TUSB1142 does not have to be maintained. Not maintaining polarity will simplify layout by eliminating the need to swap P and N in the layout. The [Figure 7-1](#) shows example in which polarity between USB host and redriver is not maintained.



**Figure 7-1. Polarity Inversion Example**

### 7.3.6 Receiver Detect Control

The SLP\_S0# pin offers system designers the ability to control the TUSB1142 Rx.Detect functionality during Disconnect and U2/U3 states and therefore achieving lower consumption in these states. When the system is in a low power state (Sx where x = 1, 2, 3, 4, or 5), system can assert SLP\_S0# low to disable TUSB1142 receiver detect functionality. While SLP\_S0# is asserted low and USB 3.2 interface is in U3, the TUSB1142 keeps receiver termination active. The TUSB1142 will not respond to any LFPS signaling while in this state. This means that system wake from U3 is not supported while SLP\_S0# is asserted low. If the TUSB1142 is in Disconnect state when SLP\_S0# is asserted low, then TUSB1142 disables all channels receiver termination and disables receiver detect functionality. When SLP\_S0# is asserted high, the TUSB1142 resumes normal operation of performing far-end receiver termination detection.

## 7.4 Device Functional Modes

### 7.4.1 MODE Pin

The MODE pin selects between I<sup>2</sup>C mode and pin-strap mode. Refer to [Table 7-5](#) for details.

In I<sup>2</sup>C mode, the TUSB1142 supports either 1.8-V LVCMOS or 3.3-V LVCMOS signaling based on the sampled state of VIO\_SEL pin.

**Table 7-5. MODE Pin Function**

| MODE PIN LEVEL | DESCRIPTION           |
|----------------|-----------------------|
| 0              | Pin-strap mode.       |
| R              | Reserved              |
| F              | I <sup>2</sup> C Mode |
| 1              | Reserved.             |

### 7.4.2 Rx EQ Configuration in Pin-Strap Mode

The TUSB1142 configured in pin-strap mode uses the follow pins to control the EQ setting for each of its receivers: EQCFG pin, SSEQ[1:0] pins, CEQ[1:0] pins.

**Table 7-6. Pin-strap: SSTX Receiver EQ Configuration**

| SSTX Receiver | SSEQ[1:0] pin level                           | Gain at 5 GHz                        | EQCFG pin level |
|---------------|---|--------------------------------------|-----------------|
| SSTX          | SSEQ0 = "0"                                   | 3 dB                                 | "1" or "R"      |
|               | SSEQ0 = "R"                                   | 6 dB                                 | "1" or "R"      |
|               | SSEQ0 = "F"                                   | 9 dB                                 | "1" or "R"      |
|               | SSEQ0 = "1"                                   | 12 dB                                | "1" or "R"      |
|               | 16 possible settings based on SSEQ0 and SSEQ1 | Refer to <a href="#">Table 7-3</a> . | "0" or "F"      |

The following table describes receiver equalization controls for the receivers facing the USB connector.

**Table 7-7. Pin Strap: CRX1 and CRX2 EQ Configuration with AEQ Disabled**

| CRX Receiver | CEQ[1:0] pin level                          | Gain at 5 GHz                        | EQCFG pin level |
|--------------|---|--------------------------------------|-----------------|
| CRX1         | CEQ0 = "0"                                  | 3 dB                                 | "0" or "R"      |
|              | CEQ0 = "R"                                  | 6 dB                                 | "0" or "R"      |
|              | CEQ0 = "F"                                  | 9 dB                                 | "0" or "R"      |
|              | CEQ0 = "1"                                  | 12 dB                                | "0" or "R"      |
|              | 16 possible settings based on CEQ0 and CEQ1 | Refer to <a href="#">Table 7-2</a> . | "F" or "1"      |
| CRX2         | CEQ1 = "0"                                  | 3 dB                                 | "0" or "R"      |
|              | CEQ1 = "R"                                  | 6 dB                                 | "0" or "R"      |
|              | CEQ1 = "F"                                  | 9 dB                                 | "0" or "R"      |
|              | CEQ1 = "1"                                  | 12 dB                                | "0" or "R"      |
|              | 16 possible settings based on CEQ0 and CEQ1 | Refer to <a href="#">Table 7-2</a> . | "F" or "1"      |

### 7.4.3 USB 3.2 Power States

The TUSB1142 monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB 3.1 interface. Depending on the state of the USB 3.2 interface, the TUSB1142 can be in one of four primary modes of operation when USB 3.1 is enabled: Disconnect, U2/U3, U1, and U0 (Active).

The *Disconnect* state is the state in which TUSB1142 has not detected far-end termination on both upstream facing port (UFP) or downstream facing port (DFP). The disconnect mode is the lowest power mode of each of the four states. The TUSB1142 remains in this state until far-end receiver termination has been detected on both UFP (SSRX) and DFP (CTX). The TUSB1142 immediately exits this mode and enters U0 once far-end termination is detected.

Once in U0 state, the TUSB1142 will redrive all traffic received on the port in both directions. U0 is the highest power mode of all USB 3.2 power states. The TUSB1142 remains in U0 state until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB1142 immediately transitions to U1.

The U1 state is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB1142 UFP and DFP receiver termination remains enabled. The UFP and DFP transmitter DC common mode is maintained. The power consumption in U1 is similar to power consumption of U0.

Next to the disconnect state, the U2/U3 state is next lowest power state. While in this state, the TUSB1142 periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB1142 leaves the U2/U3 state and transitions to the Disconnect state. It also monitors for a valid LFPS. Upon detection of a valid LFPS, the TUSB1142 immediately transitions to the U0 state. In U2/U3 state, the TUSB1142 receiver terminations remain enabled but the TX DC common mode voltage is not maintained.

### 7.4.4 Disabling U1 and U2

In systems which have U1 and U2 disabled, it may be necessary to disable U1 and U2 in TUSB1142. In I<sup>2</sup>C mode this can be accomplished by setting the USB3\_U1\_DISABLE field. In pin-strap mode U1 and U2 is enabled by default and can't be disabled.

## 7.5 Programming

### 7.5.1 Pseudocode Examples

#### 7.5.1.1 Fixed EQ with Linear Redriver Mode

```
// (address, data)
// Initial power-on configuration.

(0x0A, 0x11), // Linear redriver, EQ_OVERRIDE and USB 3.2
(0x1C, 0x80), // Disable AEQ enable.
(0x32, 0xC0), // VOD control
(0x20, 0x44), // USB connector CRX1/CRX2 EQ setting
(0x21, 0x05), // SSTX receiver EQ.
```

```
// Controls when selecting between normal and flip orientation.
If (USBonly_normal) // USB-C connected and normal orientation.
{ (0x0A, 0x11); }
Else if (USBonly_flip) // USB-C connected and Flip orientation.
{ (0x0A, 0x15); }
Else // Nothing connected to USB-C connector. Disable USB 3.2.
{ (0x0A, 0x10); }
```

### 7.5.1.2 Fixed EQ with Limited Redriver Mode

```
// (address, data)
// Initial power-on configuration.

(0x0A, 0x91), // Limited redriver, EQ_OVERRIDE and USB 3.2
(0x0B, 0x6F), // SSRX limited. Preshoot and de-emphasis.

(0x1C, 0x80), // Disable AEQ enable.
(0x32, 0xC0), // VOD control
(0x20, 0x44), // USB connector CRx1/CRx2 EQ setting
(0x21, 0x05), // SSTX receiver EQ.
```

```
// Controls when selecting between normal and flip orientation.
If (USBonly_normal) // USB-C connected and normal orientation.
{ (0x0A,0x91); }
Else if (USBonly_flip) // USB-C connected and Flip orientation.
{ (0x0A, 0x95); }
Else // Nothing connected to USB-C connector. Disable USB 3.2.
{ (0x0A, 0x90); }
```

### 7.5.1.3 Fast AEQ with Linear Redriver Mode

```
// (address, data)
// Initial power-on configuration.

(0x0A, 0x11), // Linear redriver, EQ_OVERRIDE and USB 3.2
(0x1C, 0x81), // Fast AEQ enable.
(0x32, 0xC0), // VOD control
(0x1D, 0x10), // Over EQ adjustment
(0x1E, 0x77), // USB connector CRx1/CRx2 long channel EQ setting
(0x20, 0x11), // USB connector CRx1/CRx2 short channel EQ setting
(0x21, 0x05), // SSTX receiver EQ.
```

```
// Controls when selecting between normal and flip orientation.
If (USBonly_normal) // USB-C connected and normal orientation.
{ (0x0A,0x11); }
Else if (USBonly_flip) // USB-C connected and Flip orientation.
{ (0x0A, 0x15); }
Else // Nothing connected to USB-C connector. Disable USB 3.2.
{ (0x0A, 0x10); }
```

### 7.5.1.4 Fast AEQ with Limited Redriver Mode

```
// (address, data)
// Initial power-on configuration.

(0x0A, 0x91), // Limited redriver, EQ_OVERRIDE and USB 3.2
(0x0B, 0x6F), // SSRX limited. Preshoot and de-emphasis.

(0x32, 0xC0), // VOD control
(0x1C, 0x81), // Fast AEQ enable.
(0x1D, 0x10), // Over EQ adjustment
(0x1E, 0x77), // USB connector CRx1/CRx2 long channel EQ setting
(0x20, 0x11), // USB connector CRx1/CRx2 short channel EQ setting
(0x21, 0x05), // SSTX receiver EQ.
```

```
// Controls when selecting between normal and flip orientation.
If (USBonly_normal) // USB-C connected and normal orientation.
{ (0x0A,0x91); }
```

```
Else if (USBonly_flip) // USB-C connected and Flip orientation.
{ (0x0A, 0x95); }
Else // Nothing connected to USB-C connector. Disable USB 3.2.
{ (0x0A, 0x90); }
```

### 7.5.1.5 Full AEQ with Linear Redriver Mode

```
// (address, data)
// Initial power-on configuration.

(0x0A, 0x11), // Linear redriver, EQ_OVERRIDE and USB 3.2
(0x32, 0xC0), // VOD control
(0x1C, 0x85), // Full AEQ enable. Set upper EQ limit to 0x8.
(0x1D, 0x10), // Over EQ adjustment
(0x20, 0x11), // USB connector CRx1/CRx2 EQ. Not used in Full AEQ.
(0x21, 0x05), // SSTX receiver EQ.
```

```
// Controls when selecting between normal and flip orientation.
If (USBonly_normal) // USB-C connected and normal orientation.
{ (0x0A, 0x11); }
Else if (USBonly_flip) // USB-C connected and Flip orientation.
{ (0x0A, 0x15); }
Else // Nothing connected to Type-C. Disable USB 3.2.
{ (0x0A, 0x10); }
```

### 7.5.1.6 Full AEQ with Limited Redriver Mode

```
// (address, data)
// Initial power-on configuration.

(0x0A, 0x91), // Limited redriver, EQ_OVERRIDE and USB 3.2
(0x0B, 0x6F), // SSRX limited. Preshoot and de-emphasis.

(0x32, 0xC0), // VOD control
(0x1C, 0x85), // Full AEQ enable.
(0x1D, 0x10), // Over EQ adjustment
(0x20, 0x11), // USB connector CRx1/CRx2 short channel EQ setting. Not used for Full AEQ.
(0x21, 0x05), // SSTX receiver EQ.
```

```
// Controls when selecting between normal and flip orientation.
If (USBonly_normal) // USB-C connected and normal orientation.
{ (0x0A, 0x91); }
Else if (USBonly_flip) // USB-C connected and Flip orientation.
{ (0x0A, 0x95); }
Else // Nothing connected to USB-C connector. Disable USB 3.2.
{ (0x0A, 0x90); }
```

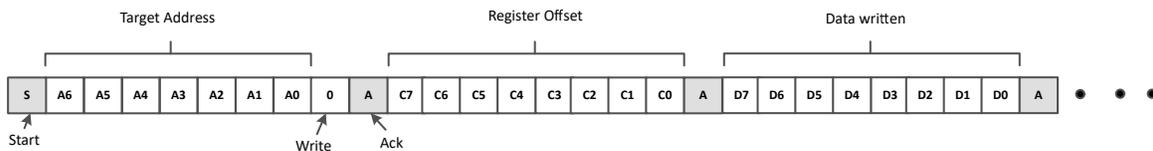
### 7.5.2 TUSB1142 I<sup>2</sup>C Address Options

For further programmability, the TUSB1142 can be controlled using I<sup>2</sup>C. The SCL and SDA pins are used for I<sup>2</sup>C clock and I<sup>2</sup>C data respectively.

**Table 7-8. TUSB1142 I<sup>2</sup>C Target Address**

| SSEQ1/A1<br>PIN LEVEL | SSEQ0/A0<br>PIN LEVEL | 7-bit Address | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0<br>(W/R) |
|-----------------------|-----------------------|---------------|-------------|-------|-------|-------|-------|-------|-------|----------------|
| 0                     | 0                     | 44h           | 1           | 0     | 0     | 0     | 1     | 0     | 0     | 0/1            |
| 0                     | R                     | 45h           | 1           | 0     | 0     | 0     | 1     | 0     | 1     | 0/1            |
| 0                     | F                     | 46h           | 1           | 0     | 0     | 0     | 1     | 1     | 0     | 0/1            |
| 0                     | 1                     | 47h           | 1           | 0     | 0     | 0     | 1     | 1     | 1     | 0/1            |
| R                     | 0                     | 20h           | 0           | 1     | 0     | 0     | 0     | 0     | 0     | 0/1            |
| R                     | R                     | 21h           | 0           | 1     | 0     | 0     | 0     | 0     | 1     | 0/1            |
| R                     | F                     | 22h           | 0           | 1     | 0     | 0     | 0     | 1     | 0     | 0/1            |
| R                     | 1                     | 23h           | 0           | 1     | 0     | 0     | 0     | 1     | 1     | 0/1            |
| F                     | 0                     | 10h           | 0           | 0     | 1     | 0     | 0     | 0     | 0     | 0/1            |
| F                     | R                     | 11h           | 0           | 0     | 1     | 0     | 0     | 0     | 1     | 0/1            |
| F                     | F                     | 12h           | 0           | 0     | 1     | 0     | 0     | 1     | 0     | 0/1            |
| F                     | 1                     | 13h           | 0           | 0     | 1     | 0     | 0     | 1     | 1     | 0/1            |
| 1                     | 0                     | Ch            | 0           | 0     | 0     | 1     | 1     | 0     | 0     | 0/1            |
| 1                     | R                     | Dh            | 0           | 0     | 0     | 1     | 1     | 0     | 1     | 0/1            |
| 1                     | F                     | Eh            | 0           | 0     | 0     | 1     | 1     | 1     | 0     | 0/1            |
| 1                     | 1                     | Fh            | 0           | 0     | 0     | 1     | 1     | 1     | 1     | 0/1            |

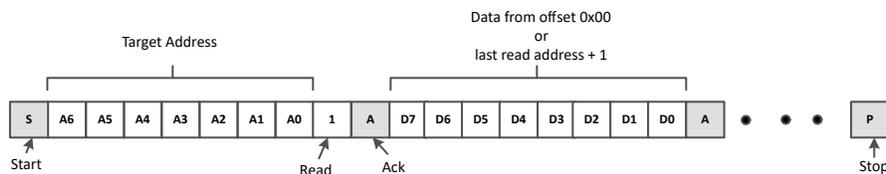
### 7.5.3 TUSB1142 I<sup>2</sup>C Target Behavior



**Figure 7-2. I2C Write with Data**

The following procedure should be followed to write data to TUSB1142 I<sup>2</sup>C registers (refer to [Figure 7-2](#)):

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB1142 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1142 acknowledges the address cycle.
3. The controller presents the register offset within TUSB1142 to be written, consisting of one byte of data, MSB-first.
4. The TUSB1142 acknowledges the sub-address cycle.
5. The controller presents the first byte of data to be written to the I<sup>2</sup>C register.
6. The TUSB1142 acknowledges the byte transfer.
7. The controller may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB1142.
8. The controller terminates the write operation by generating a stop condition (P).



**Figure 7-3. I2C Read Without Repeated Start**

The following procedure should be followed to read the TUSB1142 I<sup>2</sup>C registers without a repeated Start (refer [Figure 7-3](#)).

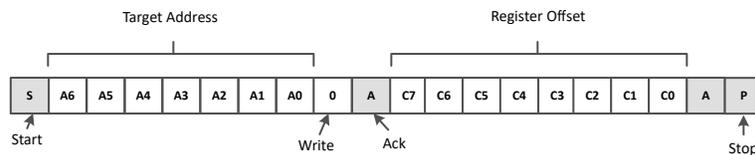
1. The controller initiates a read operation by generating a start condition (S), followed by the TUSB1142 7-bit address and a zero-value “W/R” bit to indicate a read cycle.
2. The TUSB1142 acknowledges the 7-bit address cycle.
3. Following the acknowledge the controller continues sending clock.
4. The TUSB1142 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I<sup>2</sup>C register occurred prior to the read, then the TUSB1142 shall start at the register offset specified in the write.
5. The TUSB1142 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I<sup>2</sup>C controller acknowledges reception of each data byte transfer.
6. If an ACK is received, the TUSB1142 transmits the next byte of data as long as controller provides the clock. If a NAK is received, the TUSB1142 stops providing data and waits for a stop condition (P).
7. The controller terminates the write operation by generating a stop condition (P).



**Figure 7-4. I2C Read with Repeated Start**

The following procedure should be followed to read the TUSB1142 I<sup>2</sup>C registers with a repeated Start (refer [Figure 7-4](#)).

1. The controller initiates a read operation by generating a start condition (S), followed by the TUSB1142 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1142 acknowledges the 7-bit address cycle.
3. The controller presents the register offset within TUSB1142 to be written, consisting of one byte of data, MSB-first.
4. The TUSB1142 acknowledges the register offset cycle.
5. The controller presents a repeated start condition (Sr).
6. The controller initiates a read operation by generating a start condition (S), followed by the TUSB1142 7-bit address and a one-value “W/R” bit to indicate a read cycle.
7. The TUSB1142 acknowledges the 7-bit address cycle.
8. The TUSB1142 transmit the contents of the memory registers MSB-first starting at the register offset.
9. The TUSB1142 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I<sup>2</sup>C controller acknowledges reception of each data byte transfer.
10. If an ACK is received, the TUSB1142 transmits the next byte of data as long as controller provides the clock. If a NAK is received, the TUSB1142 stops providing data and waits for a stop condition (P).
11. The controller terminates the read operation by generating a stop condition (P).



**Figure 7-5. I2C Write Without Data**

The following procedure should be followed for setting a starting sub-address for I<sup>2</sup>C reads (refer to [Figure 7-5](#)).

1. The controller initiates a write operation by generating a start condition (S), followed by the TUSB1142 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1142 acknowledges the address cycle.
3. The controller presents the register offset within TUSB1142 to be written, consisting of one byte of data, MSB-first.
4. The TUSB1142 acknowledges the register offset cycle.
5. The controller terminates the write operation by generating a stop condition (P).

### Note

After initial power-up, if no register offset is included for the read procedure (refer to [Figure 7-3](#)), then reads start at register offset 00h and continue byte by byte through the registers until the I<sup>2</sup>C controller terminates the read operation. During a read operation, the TUSB1142 auto-increments the I<sup>2</sup>C internal register address of the last byte transferred independent of whether or not an ACK was received from the I2C controller.

## 7.6 Register Map

### 7.6.1 TUSB1142 Registers

[Table 7-9](#) lists the memory-mapped registers for the TUSB1142 registers. All register offset addresses not listed in [Table 7-9](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-9. TUSB1142 Registers**

| Offset | Acronym          | Register Name                          | Section            |
|--------|------------------|--|--------------------|
| 8h     | Rev_ID           | Revision ID Register                   | <a href="#">Go</a> |
| Ah     | General_1        | General Register                       | <a href="#">Go</a> |
| Bh     | TX1EQ_CTRL       | TX1 EQ Control                         | <a href="#">Go</a> |
| 1Ch    | AEQ_CONTROL1     | AEQ Controls                           | <a href="#">Go</a> |
| 1Dh    | AEQ_CONTROL2     | AEQ Controls                           | <a href="#">Go</a> |
| 1Eh    | AEQ_LONG         | AEQ setting for Long channel           | <a href="#">Go</a> |
| 20h    | USBC_EQ          | EQ control for CRX1 and CRX2 receivers | <a href="#">Go</a> |
| 21h    | SS_EQ            | EQ Control for SSTX receiver           | <a href="#">Go</a> |
| 22h    | USB3_MISC        | Misc USB3 Controls                     | <a href="#">Go</a> |
| 24h    | USB1_STATUS      | USB1 state machine status              | <a href="#">Go</a> |
| 25h    | USB2_STATUS      | USB2 state machine status              | <a href="#">Go</a> |
| 32h    | VOD_CTRL         | VOD Linearity and AEQ Controls         | <a href="#">Go</a> |
| 3Bh    | AEQ1_STATUS      | Full and Fast AEQ status               | <a href="#">Go</a> |
| 3Ch    | AEQ2_STATUS      | Full and Fast AEQ status               | <a href="#">Go</a> |
| 50h    | AEQ_CONTROL_AUX1 |  | <a href="#">Go</a> |
| 51h    | AEQ_CONTROL_AUX2 |  | <a href="#">Go</a> |
| 52h    | AEQ_CONTROL_AUX3 |  | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. [Table 7-10](#) shows the codes that are used for access types in this section.

**Table 7-10. TUSB1142 Access Type Codes**

| Access Type | Code      | Description                        |
|-------------|-----------|------------------------------------|
| Read Type   |           |                                    |
| R           | R         | Read                               |
| RH          | R<br>H    | Read<br>Set or cleared by hardware |
| Write Type  |           |                                    |
| W           | W         | Write                              |
| W1C         | W<br>1C   | Write<br>1 to clear                |
| W1S         | W<br>1S   | Write<br>1 to set                  |
| WtoPH       | W<br>toPH | Write<br>Pulse high                |

**Table 7-10. TUSB1142 Access Type Codes  
(continued)**

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Reset or Default Value |      |  |
| -n                     |      | Value after reset or the default value |

### 7.6.1.1 Rev\_ID Register (Offset = 8h) [Reset = 01h]

Rev\_ID is shown in [Table 7-11](#).

Return to the [Summary Table](#).

**Table 7-11. Rev\_ID Register Field Descriptions**

| Bit | Field       | Type | Reset | Description     |
|-----|-------------|------|-------|-----------------|
| 7-0 | REVISION_ID | RH   | 1h    | Device Revision |

### 7.6.1.2 General\_1 Register (Offset = Ah) [Reset = 00h]

General\_1 is shown in [Table 7-12](#).

Return to the [Summary Table](#).

This register is used to enable USB as well as selecting the orientation of the MUX. Software should set EQ\_OVERRIDE bit in order for EQ registers to be used instead of pins.

**Table 7-12. General\_1 Register Field Descriptions**

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 7   | SSRX_LIMIT_ENABLE | R/W  | 0h    | Limited redriver mode enable for SSRX transmitter.<br>0h = Linear Redriver<br>1h = Limited Redriver  |
| 6   | RESERVED          | R    | 0h    | Reserved   |
| 5   | RESERVED          | R    | 0h    | Reserved   |
| 4   | EQ_OVERRIDE       | R/W  | 0h    | Setting this field will allow software to use EQ settings from registers instead of value sampled from pins.<br>0h = EQ settings based on sampled state of EQ pins.<br>1h = EQ settings based on programmed value of each of the EQ registers. |
| 3   | RESERVED          | R    | 0h    | Reserved   |
| 2   | FLIP_SEL          | R/W  | 0h    | This field controls the orientation.<br>0h = Normal Orientation<br>1h = Flip orientation.  |
| 1-0 | CTLSEL            | R/W  | 0h    | Controls whether USB is enabled or not.<br>0h = Disabled<br>1h = USB enabled.<br>2h = Disabled<br>3h = USB enabled   |

### 7.6.1.3 TX1EQ\_CTRL Register (Offset = Bh) [Reset = 6Fh]

TX1EQ\_CTRL is shown in [Table 7-13](#).

Return to the [Summary Table](#).

This register controls the preshoot and de-emphasis levels for SSRX when limited redriver mode is enabled.

**Table 7-13. TX1EQ\_CTRL Register Field Descriptions**

| Bit | Field              | Type | Reset | Description   |
|-----|--------------------|------|-------|---|
| 7-6 | SSRX_PRESHOOT      | R/W  | 1h    | SSRX TX preshoot level (pre-cursor).<br>0h = 1.5dB<br>1h = 2dB<br>2h = 2.3dB<br>3h = 2.8dB                              |
| 5   | SSRX_PRESHOOT_EN   | R/W  | 1h    | SSRX TX preshoot (pre-cursor) enabled. Valid only when SSRX_LIMIT_ENABLE = 1.<br>0h = Disabled (0dB)<br>1h = Enabled    |
| 4-3 | SSRX_DEEMPHASIS    | R/W  | 1h    | SSRX TX de-emphasis level (post-cursor)<br>0h = -1.5dB<br>1h = -2.1dB<br>2h = -3.2dB<br>3h = -3.8dB                     |
| 2   | SSRX_DEEMPHASIS_EN | R/W  | 1h    | SSRX TX de-emphasis (post-cursor) enable. Valid only when SSRX_LIMIT_ENABLE = 1.<br>0h = Disabled (0dB)<br>1h = Enabled |
| 1-0 | RESERVED           | R/W  | 3h    | Reserved  |

**7.6.1.4 AEQ\_CONTROL1 Register (Offset = 1Ch) [Reset = 85h]**

AEQ\_CONTROL1 is shown in [Table 7-14](#).

Return to the [Summary Table](#).

This register is used to enable adaptive EQ and select between Fast and Full adaptive EQ.

**Table 7-14. AEQ\_CONTROL1 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 7-4 | FULLAEQ_UPPER_EQ | R/W  | 8h    | This field sets the maximum EQ value to check for full AEQ mode when in I2C mode.   |
| 3   | USB3_U1_DISABLE  | R/W  | 0h    | This field when set will cause entry to U3 instead of U1 when electrical idle is detected.<br>0h = U1 entry after electrical idle.<br>1h = U3 entry after electrical idle.  |
| 2-1 | AEQ_MODE         | R/W  | 2h    | Selects Adaption mode (Fast, or one of three Full modes).<br>0h = Fast AEQ.<br>1h = Full AEQ, with hits counted at mideye for every EQ iteration (using current EQ setting).<br>2h = Full AEQ, algorithm II.<br>3h = Full AEQ, with hits counted at mideye only for first EQ iteration (using EQ set to the MID_HC_EQ value). |
| 0   | AEQ_EN           | R/W  | 1h    | Controls whether or not adaptive EQ for USB downstream facing port is enabled.<br>0h = AEQ disabled<br>1h = AEQ enabled   |

**7.6.1.5 AEQ\_CONTROL2 Register (Offset = 1Dh) [Reset = 10h]**

AEQ\_CONTROL2 is shown in [Table 7-15](#).

Return to the [Summary Table](#).

This register allows for controls for the Fast AEQ limits as well as adding or reducing final EQ value used by the Full AEQ function.

**Table 7-15. AEQ\_CONTROL2 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 7   | OVER_EQ_SIGN   | R/W  | 0h    | Selects the sign for OVER_EQ_CTRL field.<br>0h = positive<br>1h = negative   |
| 6   | RESERVED       | R    | 0h    | Reserved   |
| 5-3 | FASTAEQ_LIMITS | R/W  | 2h    | Selects the upper/lower limits of DAC for determining short vs long channel.<br>0h = +/- 0mV<br>1h = +/- 40mV<br>2h = +/- 80mV<br>3h = +/- 120mV<br>4h = +/- 160mV<br>5h = +/- 200mV<br>6h = +/- 240mV<br>7h = +/- 280mV   |
| 2-0 | OVER_EQ_CTRL   | R/W  | 0h    | This field will increase or decrease the AEQ by value programmed into this field. For example, full AEQ value is 6 and this field is programmed to 2 and OVER_EQ_SIGN = 0, then EQ value used will be 8. This field is only used in Full AEQ mode.<br>0h = 0 or -8<br>1h = 1 or -7<br>2h = 2 or -6<br>3h = 3 or -5<br>4h = 4 or -4<br>5h = 5 or -3<br>6h = 6 or -2<br>7h = 7 or -1 |

#### 7.6.1.6 AEQ\_LONG Register (Offset = 1Eh) [Reset = 77h]

AEQ\_LONG is shown in [Table 7-16](#).

Return to the [Summary Table](#).

This register is used to program the EQ used for long channel setting when Fast AEQ is enabled.

**Table 7-16. AEQ\_LONG Register Field Descriptions**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7-4 | LONG_CEQ2 | R/W  | 7h    | When AEQ_EN = 1 and AEQ_MODE = x0 (that is, Fast), selects EQ setting for USB connector port2 (CRX2) when long channel is detected. The user should program this field with the value that provides the best Rx JTOL results for a long channel configuration. |
| 3-0 | LONG_CEQ1 | R/W  | 7h    | When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB connector port1 (CRX1) when long channel is detected. The user should program this field with the value that provides the best Rx JTOL results for a long channel configuration.                 |

#### 7.6.1.7 USBC\_EQ Register (Offset = 20h) [Reset = 00h]

USBC\_EQ is shown in [Table 7-17](#).

Return to the [Summary Table](#).

This register controls the receiver equalization setting for the connector receiver (CRX1 and CRX2).

**Table 7-17. USBC\_EQ Register Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7-4 | CEQ2_SEL | RH/W | 0h    | If AEQ_EN = 0, this field selects EQ for USB CRX2 receiver which faces the USB-C receptacle. When EQ_OVERRIDE = 0b, this field reflects the sampled state of CEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for CRX2p/n pins based on value written to this field. When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB connector port2 (CRX2) when short channel is detected. The user should program this field with the value that provides the best Rx JTOL results for a short channel configuration. |
| 3-0 | CEQ1_SEL | RH/W | 0h    | If AEQ_EN = 0, this field selects EQ for USB CRX1 receiver which faces the USB-C receptacle. When EQ_OVERRIDE = 0b, this field reflects the sampled state of CEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for CRX1p/n pins based on value written to this field. When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB connector port1 (CRX1) when short channel is detected. The user should program this field with the value that provides the best Rx JTOL results for a short channel configuration. |

**7.6.1.8 SS\_EQ Register (Offset = 21h) [Reset = 00h]**

SS\_EQ is shown in [Table 7-18](#).

Return to the [Summary Table](#).

This register controls the receiver equalization setting for the SSTX.

**Table 7-18. SS\_EQ Register Field Descriptions**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7-4 | RESERVED  | RH/W | 0h    | Reserved   |
| 3-0 | SSEQ1_SEL | RH/W | 0h    | This field selects EQ for USB SSTX receiver which faces the USB host. When EQ_OVERRIDE = 0b, this field reflects the sampled state of SSEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for SSTXp/n pins based on value written to this field. |

**7.6.1.9 USB3\_MISC Register (Offset = 22h) [Reset = 04h]**

USB3\_MISC is shown in [Table 7-19](#).

Return to the [Summary Table](#).

**Table 7-19. USB3\_MISC Register Field Descriptions**

| Bit | Field              | Type | Reset | Description   |
|-----|--------------------|------|-------|---|
| 7   | RXD_START_TERM     | R/W  | 0h    | Termination setting at start of RX detection following warm reset and at entry to SS.Inactive.<br>0h = Maintain termination.<br>1h = Turn off termination. Avoid compliance failures due to race between local and remote rxd in case of disconnect. If connection remains next state was polling regardless. |
| 6-5 | U23_RXDET_INTERVAL | R/W  | 0h    | This field controls the Rx.Detect interval for the downstream facing port (CTX1P/N and CTX2P/N) when in U2/U3.<br>0h = 48ms<br>1h = 84ms<br>2h = 120ms<br>3h = 156ms  |
| 4   | DISABLE_U2U3_RXDET | R/W  | 0h    | Controls whether or not Rx.Detect is performed in U2/U3 state.<br>0h = Rx.Detect in U2/U3 enabled.<br>1h = Rx.Detect in U2/U3 disabled.   |

**Table 7-19. USB3\_MISC Register Field Descriptions (continued)**

| Bit | Field                   | Type | Reset | Description  |
|-----|-------------------------|------|-------|--|
| 3-2 | DFP_RXDET_INTERVAL      | R/W  | 1h    | This field controls the Rx.Detect interval for the downstream facing port (CTX1P/N and CTX2P/N).<br>0h = 4ms<br>1h = 6ms<br>2h = 36ms<br>3h = 84ms   |
| 1   | DIS_WARM_RESET_RXD      | R/W  | 0h    | Disables receiver detection following warm reset if device starts polling during warm reset.<br>0h = whether receiver detection is done following warm reset depends on other settings.<br>1h = if USB FSM detects that device started polling during warm reset, it will not do receiver detection. |
| 0   | USB_COMPLIANCE_CTR<br>L | R/W  | 0h    | Controls whether compliance mode detection is determined by FSM or disabled<br>0h = Compliance mode determined by FSM.<br>1h = Compliance mode disabled.   |

#### 7.6.1.10 USB1\_STATUS Register (Offset = 24h) [Reset = 01h]

USB1\_STATUS is shown in [Table 7-20](#).

Return to the [Summary Table](#).

**Table 7-20. USB1\_STATUS Register Field Descriptions**

| Bit | Field             | Type   | Reset | Description  |
|-----|-------------------|--------|-------|--|
| 7   | USB1_FASTAEQ_STAT | RH     | 0h    | When AEQ_EN = 1 and AEQ_MODE = x0, this status field indicates whether short or long EQ setting is used. When AEQ_EN = 0, this field will always default to 0h.<br>0h = Short channel EQ used.<br>1h = Long channel EQ used. |
| 6   | RESERVED          | RH/W1C | 0h    | Reserved   |
| 5   | RESERVED          | RH     | 0h    | Reserved   |
| 4   | RESERVED          | RH     | 0h    | Reserved   |
| 3   | CM_ACTIVE1        | RH     | 0h    | Compliance mode status.<br>0h = Not in USB3.1 compliance mode.<br>1h = In USB3.1 compliance mode.  |
| 2   | U0_STAT1          | RH     | 0h    | U0 Status. Set if enters U0 state.   |
| 1   | U2U3_STAT1        | RH     | 0h    | U2/U3 Status. Set if enters U2/U3 state.   |
| 0   | DISC_STAT1        | RH     | 1h    | Disconnect Status. Set if enters Disconnect state.   |

#### 7.6.1.11 USB2\_STATUS Register (Offset = 25h) [Reset = 01h]

USB2\_STATUS is shown in [Table 7-21](#).

Return to the [Summary Table](#).

**Table 7-21. USB2\_STATUS Register Field Descriptions**

| Bit | Field             | Type   | Reset | Description  |
|-----|-------------------|--------|-------|--|
| 7   | USB2_FASTAEQ_STAT | RH     | 0h    | When AEQ_EN = 1 and AEQ_MODE = x0, this status field indicates whether short or long EQ setting is used. When AEQ_EN = 0, this field will always default to 0h.<br>0h = Short channel EQ used.<br>1h = Long channel EQ used. |
| 6   | RESERVED          | RH/W1C | 0h    | Reserved   |
| 5   | RESERVED          | RH     | 0h    | Reserved   |

**Table 7-21. USB2\_STATUS Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 4   | RESERVED   | RH   | 0h    | Reserved  |
| 3   | CM_ACTIVE2 | RH   | 0h    | Compliance mode status.<br>0h = Not in USB3.1 compliance mode.<br>1h = In USB3.1 compliance mode. |
| 2   | U0_STAT2   | RH   | 0h    | U0 Status. Set if enters U0 state.  |
| 1   | U2U3_STAT2 | RH   | 0h    | U2/U3 Status. Set if enters U2/U3 state.  |
| 0   | DISC_STAT2 | RH   | 1h    | Disconnect Status. Set if enters Disconnect state.  |

**7.6.1.12 VOD\_CTRL Register (Offset = 32h) [Reset = C0h]**

VOD\_CTRL is shown in [Table 7-22](#).

Return to the [Summary Table](#).

This register controls the transmitters output linearity range for both UFP and DFP. When device is configured for limited redriver (SSRX\_LIMIT\_ENABLE field is set), USB\_SSRX\_VOD controls the VOD level for SSRX limited driver.

**Table 7-22. VOD\_CTRL Register Field Descriptions**

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 7-6 | LFPS_VOD       | R/W  | 3h    | VOD linearity control for SSRX, CTX1, and CTX2 when LFPS is being transmitted.<br>0h = LINR_L3 (highest)<br>1h = LINR_L2<br>2h = LINR_L1<br>3h = LINR_L0 (lowest)  |
| 5-4 | RESERVED       | R    | 0h    | Reserved   |
| 3-2 | USB_CTX12_VOD  | R/W  | 0h    | VOD linearity control for USB connector facing ports (CTX1 and CTX2).<br>0h = LINR_L3 (highest)<br>1h = LINR_L2<br>2h = LINR_L1<br>3h = LINR_L0 (lowest)   |
| 1-0 | USB_SSRX12_VOD | R/W  | 0h    | VOD linearity control for USB upstream facing port (SSRX). When SSRX_LIMIT_ENABLE = 1, then this field controls the limited VOD for SSRX.<br>0h = LINR_L3 (highest)<br>1h = LINR_L2<br>2h = LINR_L1<br>3h = LINR_L0 (lowest) |

**7.6.1.13 AEQ1\_STATUS Register (Offset = 3Bh) [Reset = 00h]**

AEQ1\_STATUS is shown in [Table 7-23](#).

Return to the [Summary Table](#).

This register provides the status of AEQ function.

**Table 7-23. AEQ1\_STATUS Register Field Descriptions**

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 7-5 | RESERVED     | R    | 0h    | Reserved   |
| 4   | RESERVED     | RH   | 0h    | Reserved   |
| 3-0 | AEQ1_EQ_STAT | RH   | 0h    | Optimal EQ determined by FSM after the completion of Full AEQ. This field will also indicate EQ used for Fast AEQ. This field will include the value programmed into OVER_EQ_CTRL field. |

### 7.6.1.14 AEQ2\_STATUS Register (Offset = 3Ch) [Reset = 00h]

AEQ2\_STATUS is shown in [Table 7-24](#).

Return to the [Summary Table](#).

This register provides the status of AEQ function.

**Table 7-24. AEQ2\_STATUS Register Field Descriptions**

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 7-5 | RESERVED     | R    | 0h    | Reserved   |
| 4   | RESERVED     | RH   | 0h    | Reserved   |
| 3-0 | AEQ2_EQ_STAT | RH   | 0h    | Optimal EQ determined by FSM after the completion of Full AEQ. This field will also indicate EQ used for Fast AEQ. This field will include the value programmed into OVER_EQ_CTRL field. |

### 7.6.1.15 AEQ\_CONTROL\_AUX1 Register (Offset = 50h) [Reset = 00h]

AEQ\_CONTROL\_AUX1 is shown in [Table 7-25](#).

Return to the [Summary Table](#).

**Table 7-25. AEQ\_CONTROL\_AUX1 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-6 | RESERVED | R    | 0h    | Reserved    |
| 5-2 | RESERVED | R    | 0h    | Reserved    |
| 1-0 | RESERVED | R    | 0h    | Reserved    |

### 7.6.1.16 AEQ\_CONTROL\_AUX2 Register (Offset = 51h) [Reset = 07h]

AEQ\_CONTROL\_AUX2 is shown in [Table 7-26](#).

Return to the [Summary Table](#).

**Table 7-26. AEQ\_CONTROL\_AUX2 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 7-5 | RESERVED  | R    | 0h    | Reserved  |
| 4   | EQ_MERGE  | R/W  | 0h    | Initial EQ result merge control. This field controls how the EQ results from the positive and negative VOD offsets steps are merged to produce the initial EQ value. This field is applicable only when the AEQ_MODE field is set to 2'b10.<br>0h = Use max of pos/neg VOD EQs<br>1h = Use min of pos/neg VOD EQs |
| 3-0 | MID_HC_EQ | R/W  | 7h    | Sets EQ value during the mid-eye hit-count capture step. This field is applicable only when the AEQ_MODE field is set to 2'b10 or 2'b11.  |

### 7.6.1.17 AEQ\_CONTROL\_AUX3 Register (Offset = 52h) [Reset = 86h]

AEQ\_CONTROL\_AUX3 is shown in [Table 7-27](#).

Return to the [Summary Table](#).

**Table 7-27. AEQ\_CONTROL\_AUX3 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 7-5 | HC_EQ_THR  | R/W  | 4h    | Sets the hit-count threshold during the EQ search steps. The algorithm will find the minimum EQ setting such that the hit-count is at or above value $N_{eq}$ , where: $N_{eq} = HC_{me} * (128 - HC\_EQ\_THR) / 128$ and $HC_{me}$ is the mid-eye hit-count. This field is applicable only when the AEQ_MODE field is set to 2'b10.                |
| 4   | RESERVED   | R    | 0h    | Reserved  |
| 3-0 | HC_VOD_THR | R/W  | 6h    | Sets the hit-count threshold during the VOD search steps. The algorithm will find the maximum DAC VOD setting such that the hit-count is at or above the threshold value $N_{vod}$ , where: $N_{vod} = HC_{me} * HC\_VOD\_THR / 128$ and $HC_{me}$ is the mid-eye hit-count. This field is applicable only when the AEQ_MODE field is set to 2'b10. |

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The TUSB1142 is a linear redriver designed specifically to compensate for intersymbol interference (ISI) jitter causes by signal attenuation through a passive medium like PCB traces or cables. Placing the TUSB1142 between the USB connector and a USB 3.2 host, hub, and device can correct signal integrity issues resulting in a more robust system.

### 8.2 Typical Application

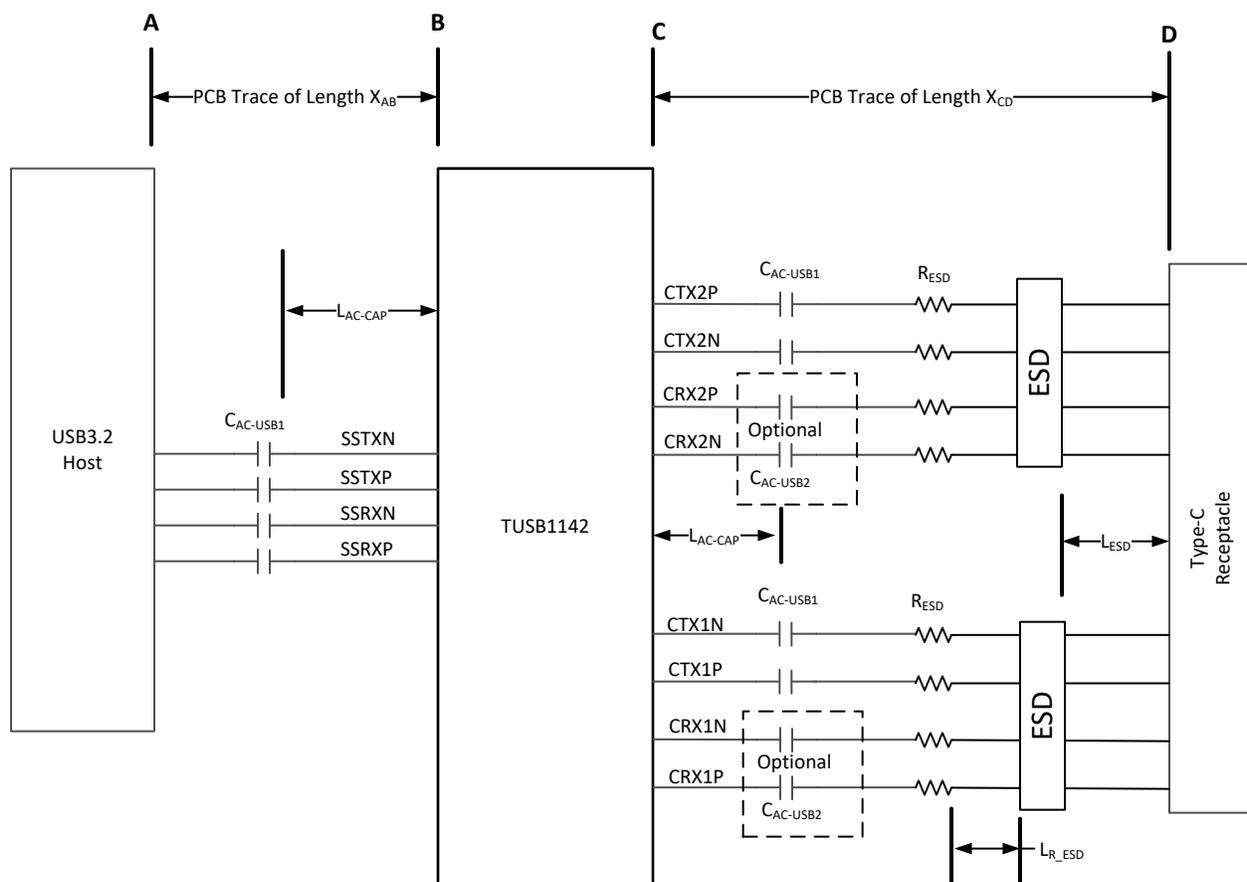


Figure 8-1. Typical USB Host Application

### 8.2.1 Design Requirements

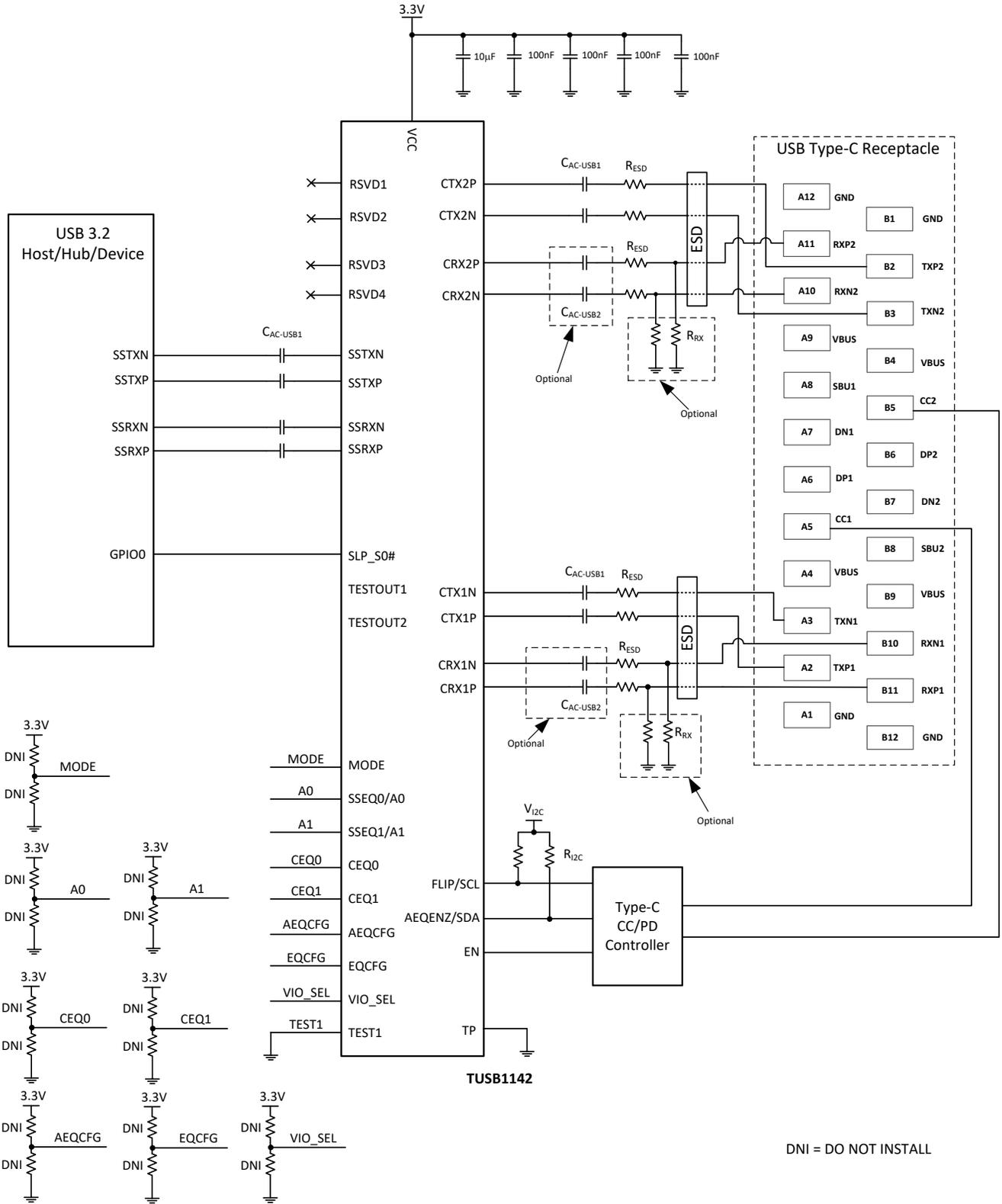
For this design example, use the parameters shown in [Table 8-1](#).

**Table 8-1. Design Parameters**

| PARAMETER  | VALUE   |
|--|---|
| 10 Gbps USB 3.2 pre-channel A to B PCB trace length, $X_{AB}$ .<br>Refer to <a href="#">Figure 8-1</a> . | 2 inches $\leq X_{AB} \leq$ 12 inches - $X_{CD}$  |
| 10 Gbps USB post-channel C to D PCB trace length, $X_{CD}$ .<br>Refer to <a href="#">Figure 8-1</a> .    | up to 4 inches  |
| Minimum distance of the AC capacitors from TUSB1142, $L_{AC-CAP}$  | 0.4 inches  |
| Maximum distance of ESD component from the USB receptacle, $L_{ESD}$                                     | 1.0 inches  |
| Maximum distance of series resistor ( $R_{ESD}$ ) from ESD component, $L_{R\_ESD}$ .                     | 0.25 inches   |
| $C_{AC-USB1}$ AC-coupling capacitor (75 nF to 265 nF)  | 220 nF  |
| $C_{AC-USB2}$ AC-coupling capacitor (297 nF to 363 nF)   | Options: <ul style="list-style-type: none"> <li>• RX1 and RX2 are DC-coupled to USB receptacle</li> <li>• 330 nF AC-couple with <math>R_{RX}</math> resistor</li> </ul> |
| Optional $R_{RX}$ resistor (220-k $\Omega$ $\pm$ 5%)   | No used   |
| $R_{ESD}$ (0- $\Omega$ to 2.2- $\Omega$ )  | 1- $\Omega$   |
| $V_{CC}$ supply (3-V to 3.6-V)   | 3.3-V   |
| I <sup>2</sup> C Mode or Pin-strap Mode  | I <sup>2</sup> C Mode. (MODE = "F")   |
| 1.8-V or 3.3-V I <sup>2</sup> C Interface  | 3.3-V I <sup>2</sup> C. VIO_SEL pin to Float "F".   |

### 8.2.2 Detailed Design Procedure

A typical usage of the TUSB1142 device is shown in [Figure 8-2](#). The device can be configured either through its GPIO pins or through its I<sup>2</sup>C interface. In the following example, a Type-C PD controller or microcontroller is used to configure the device through the I<sup>2</sup>C interface. In I<sup>2</sup>C mode, the equalization settings for each receiver can be independently controlled through I<sup>2</sup>C registers. For this reason, all of the equalization pins (SSEQ[1:0], and CEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB1142 7-bit I<sup>2</sup>C target address will be 0x12 because both SSEQ1/A1 and SSEQ0/A0 will be at pin level F. If a different I<sup>2</sup>C target address is desired, SSEQ1/A1 and SSEQ0/A0 pins should be set to a level which produces the desired I<sup>2</sup>C target address.



DNI = DO NOT INSTALL

Figure 8-2. Application Circuit

### 8.2.2.1 USB SSTX Receiver Configuration

Configuring the TUSB1142 involves understanding the insertion loss (SDD21) of the pre-channel ( $X_{AB}$ ). The TUSB1142's SSEQ[1:0] pins if pin-strap mode, or if I<sup>2</sup>C mode, SSEQ1\_SEL registers should be set to the level of the pre-channel insertion loss at 5 GHz. A good rule for FR4 trace insertion loss at 5 GHz is  $\approx -1$  dB per inch. Using this rule, if the pre-channel for USB ( $X_{AB}$ ) is 8-inches, the TUSB1142 SSEQ should be programmed to -8 dB.

### 8.2.2.2 USB CRX1/2 Receiver Configuration

#### 8.2.2.2.1 Fixed Equalization

In Fixed EQ operation, a single EQ setting is used for all possible devices inserted into the USB receptacle (with or without an USB cable). It is recommended to set TUSB1142 CEQ[1:0] pins if pin-strap mode, or CEQ1\_SEL and CEQ2\_SEL if I<sup>2</sup>C mode to about 4 dB to 5 dB greater than loss of the post channel ( $X_{CD}$ ). For example, if post channel is 0.5 inches, then assuming -1 dB per inch at 5 GHz, CEQ1\_SEL and CEQ2\_SEL should be programmed to 4.5 to 5.5 dB. It is recommended to perform USB 3.1 Rx JTOL long and short channel tests to optimize the setting. Depending of the USB 3.2 Host, a single EQ setting which satisfies both the long and short channel tests may not be possible. If this is the case, then it is recommended to use AEQ mode.

#### 8.2.2.2.2 Full Adaptive Equalization

In Full AEQ mode, the TUSB1142 will determine the best settings regardless if the channel is short, long or somewhere in between. In pin-strap mode, the Full AEQ is enabled based on the state of AEQENZ pin. In I<sup>2</sup>C mode, the Full AEQ feature is enabled by default. Full AEQ is enabled when AEQ\_MODE = 1, 2, or 3, and AEQ\_EN = 0x1.

#### 8.2.2.2.3 Fast Adaptive Equalization

Fast Adaptive EQ will distinguish between a short and long channel and select a pre-determined EQ setting based on which channel is detected. Fast AEQ is available only I<sup>2</sup>C mode. Fast AEQ is enabled when AEQ\_MODE = 0 and AEQ\_EN = 1.

The EQ setting used for short channel should be programmed into CEQ1\_SEL and CEQ2\_SEL registers. It is recommended to program these registers about 1 dB to 2 dB more than the loss of post channel ( $X_{CD}$ ). For example, if post channel is 0.5 inches, then assuming -1dB insertion loss per inch at 5 GHz, CEQ1\_SEL and CEQ2\_SEL should be programmed to 1.5 to 2.5 dB. It is recommended to perform USB 3.2 Rx JTOL Short channel test to find the optimal short channel setting.

The EQ setting used for long channel should be programmed into LONG\_CEQ1 and LONG\_CEQ2. It is recommended to program these registers about 4 to 5 dB more than the loss of post channel ( $X_{CD}$ ). For example, if post channel is 0.5 inches, then assuming -1 dB per inch at 5 GHz, LONG\_CEQ1 and LONG\_CEQ2 should be programmed to 4.5 to 5.5 dB. It is recommended to perform USB 3.2 Rx JTOL Long channel test to find the optimal long channel setting.

### 8.2.2.3 ESD Protection

It may be necessary to incorporate an ESD component to protect the TUSB1142 from electrostatic discharge (ESD). TI recommends following the ESD protection recommendations listed in [Table 8-2](#). A clamp voltage greater than value specified in [Table 8-2](#) may require a  $R_{ESD}$  on each differential pin. Place the ESD component near the USB connector.

**Table 8-2. ESD Diodes Recommended Characteristics**

| Parameter  | Recommendation                           |
|--|--|
| Breakdown voltage  | $\geq 3.5$ V                             |
| I/O line capacitance                                     | Data rates $\leq 5$ Gbps: $\leq 0.50$ pF |
|  | Data rates $> 5$ Gbps: $\leq 0.35$ pF    |
| Delta capacitance between any P and N I/O pins           | $\leq 0.07$ pF                           |
| Clamping voltage at 8A $I_{PP}$ IO to GND <sup>(1)</sup> | $\leq 4.5$ V                             |

**Table 8-2. ESD Diodes Recommended Characteristics (continued)**

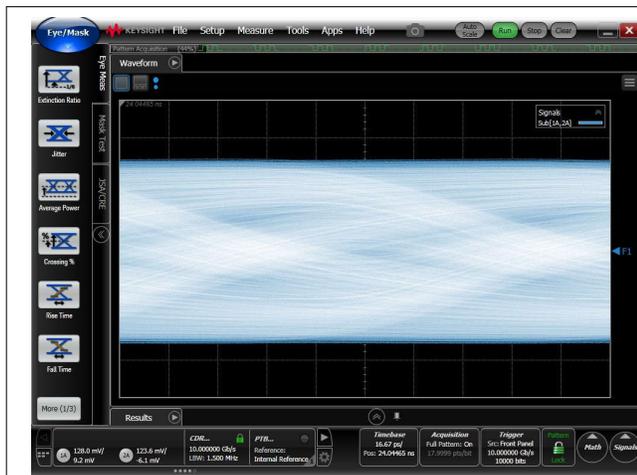
| Parameter                  | Recommendation |
|----------------------------|----------------|
| Typical dynamic resistance | ≤ 30 mΩ        |

(1) According to IEC 61000-4-5 (8/20μs current waveform)

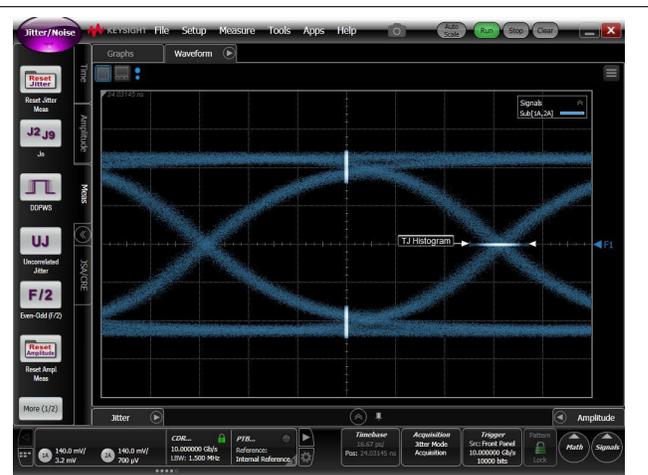
**Table 8-3. Recommended ESD Protection Component**

| Manufacturer      | Part Number    | R <sub>ESD</sub> to support IEC 61000-4-2 Contact ±8 kV |
|-------------------|----------------|---|
| Nexperia          | PUSB3FR4       | 1 Ω   |
| Nexperia          | PESD2V8Y1BSF   | 1 Ω   |
| Texas Instruments | TPD1E04U04DPLR | 2 Ω   |
| Texas Instruments | TPD4E02B04DQAR | 2 Ω   |

### 8.2.3 Application Curves



**Figure 8-3. 10 Gbps Input Eye At SSTX After 12.5 dB at 5 GHz Pre-channel**



**Figure 8-4. 10 Gbps Output Eye at CTX1 After 1.2 dB at 5 GHz Post-Channel**

### 8.3 Power Supply Recommendations

The TUSB1142 is designed to operate with a 3.3 V power supply. Levels above those listed in the *Absolute Maximum Ratings* table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors should be used to reduce noise and improve power supply integrity. A 0.1 μF de-coupling capacitor should be used on each power pin. The de-coupling capacitor should be placed close as possible to the power pin. It is also recommended to have a single bulk capacitor of 1 μF to 10 μF.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

1. SSTXP/N, SSRXP/N, CRX1P/N, CRX2PN, CTX1P/N, and CTX2P/N pairs should be routed with controlled 90-Ω differential impedance (±10%).
2. There is no inter-pair length match requirement.
3. Keep away from other high speed signals.
4. Intra-pair routing (between P and N) should be kept to less than 5 mils.
5. Length matching should be near the location of mismatch.
6. Each pair should be separated at least by 3 times the signal trace width.
7. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This

will minimize any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.

8. Route all differential pairs on the same of layer.
9. The number of vias should be kept to a minimum. It is recommended to keep the vias count to 2 or less.
10. Keep traces on layers adjacent to ground plane.
11. Do not route differential pairs over any plane split.
12. Adding test points will cause impedance discontinuity, and therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.
13. Highly recommended to have reference plane void under USB-C receptacle's super speed pins to minimize the capacitance effect of the receptacle.
14. Highly recommended to have reference plane void under the AC-coupling capacitances.

### 8.4.2 Layout Example

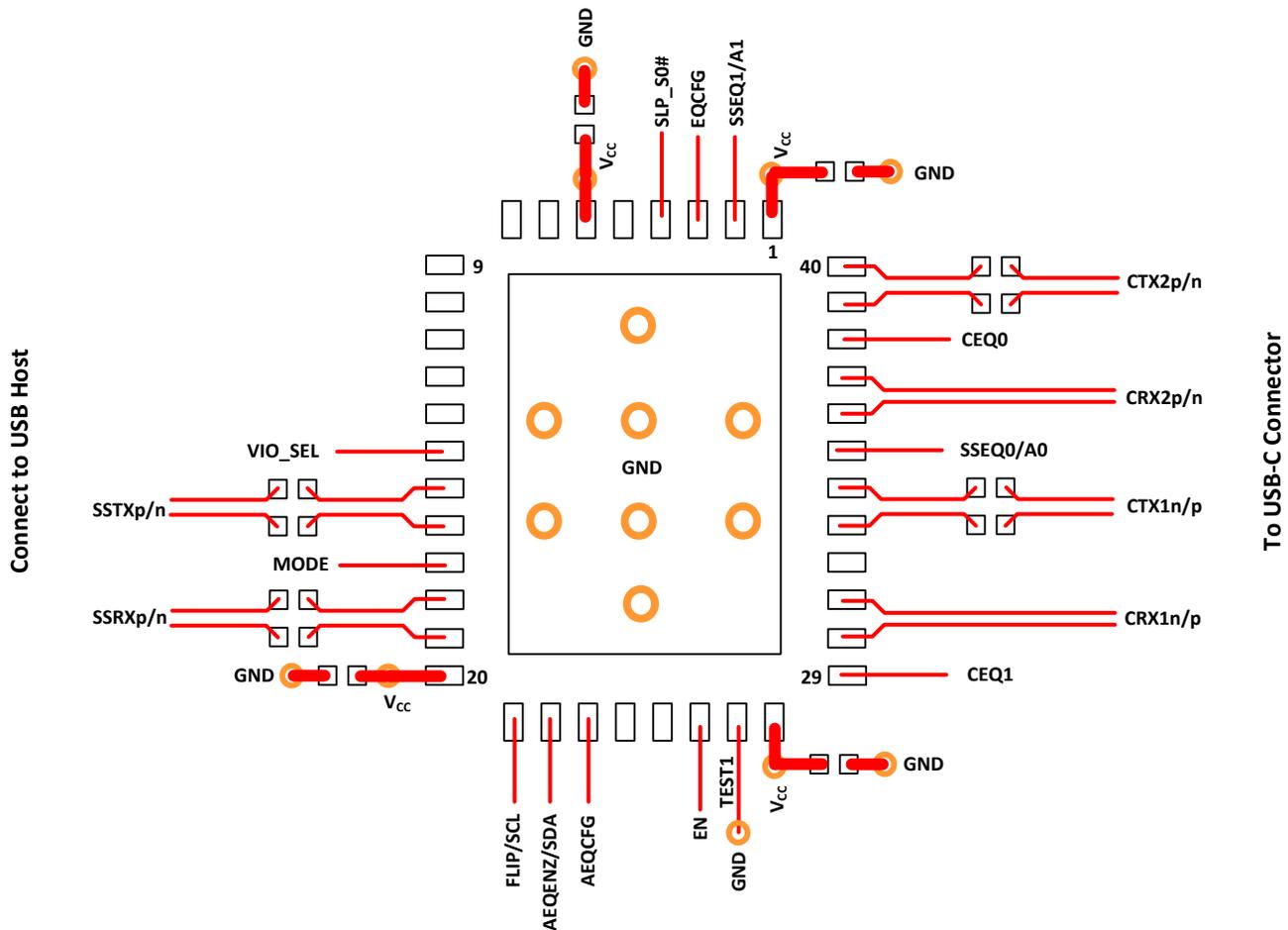


Figure 8-5. Layout Example

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.3 Trademarks

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### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

| Changes from Revision * (April 2022) to Revision A (May 2024)   | Page |
|---|------|
| • Added temperature ranges to the Device Information table..... | 1    |
| • Added section on ESD protection recommendations.....          | 44   |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TUSB1142IRNQR</a> | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TSB04               |
| TUSB1142IRNQR.B               | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TSB04               |
| <a href="#">TUSB1142IRNQT</a> | Active        | Production           | WQFN (RNQ)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TSB04               |
| TUSB1142IRNQT.B               | Active        | Production           | WQFN (RNQ)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TSB04               |
| <a href="#">TUSB1142RNQR</a>  | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TSB04               |
| TUSB1142RNQR.B                | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TSB04               |
| <a href="#">TUSB1142RNQT</a>  | Active        | Production           | WQFN (RNQ)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TSB04               |
| TUSB1142RNQT.B                | Active        | Production           | WQFN (RNQ)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TSB04               |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

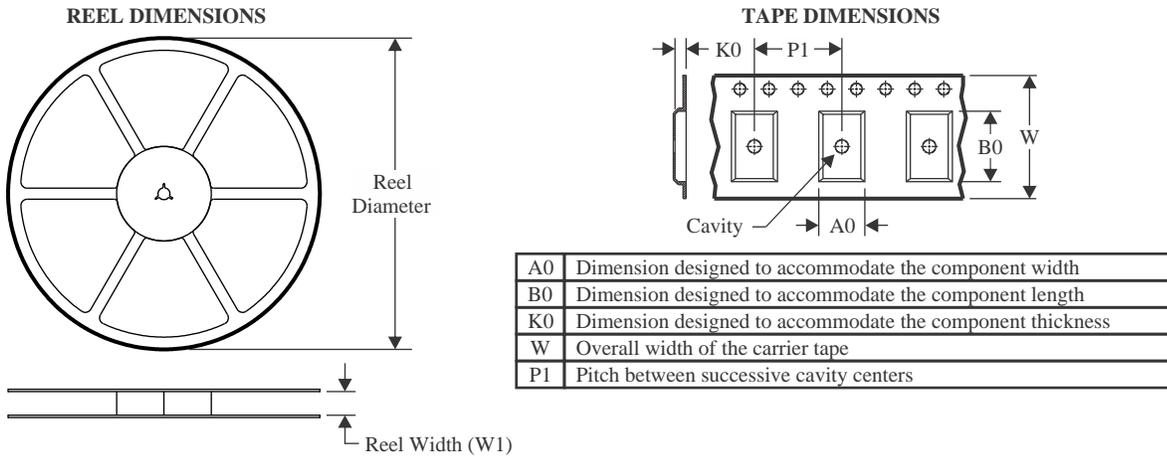
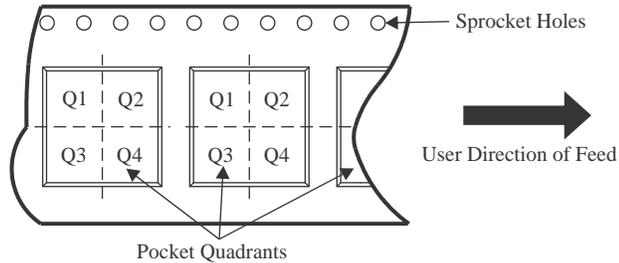
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TUSB1142IRNQR | WQFN         | RNQ             | 40   | 3000 | 330.0              | 12.4               | 4.3     | 6.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TUSB1142IRNQT | WQFN         | RNQ             | 40   | 250  | 180.0              | 12.4               | 4.3     | 6.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TUSB1142RNQR  | WQFN         | RNQ             | 40   | 3000 | 330.0              | 12.4               | 4.3     | 6.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TUSB1142RNQT  | WQFN         | RNQ             | 40   | 250  | 180.0              | 12.4               | 4.3     | 6.3     | 1.1     | 8.0     | 12.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TUSB1142IRNQR | WQFN         | RNQ             | 40   | 3000 | 367.0       | 367.0      | 35.0        |
| TUSB1142IRNQT | WQFN         | RNQ             | 40   | 250  | 210.0       | 185.0      | 35.0        |
| TUSB1142RNQR  | WQFN         | RNQ             | 40   | 3000 | 367.0       | 367.0      | 35.0        |
| TUSB1142RNQT  | WQFN         | RNQ             | 40   | 250  | 210.0       | 185.0      | 35.0        |

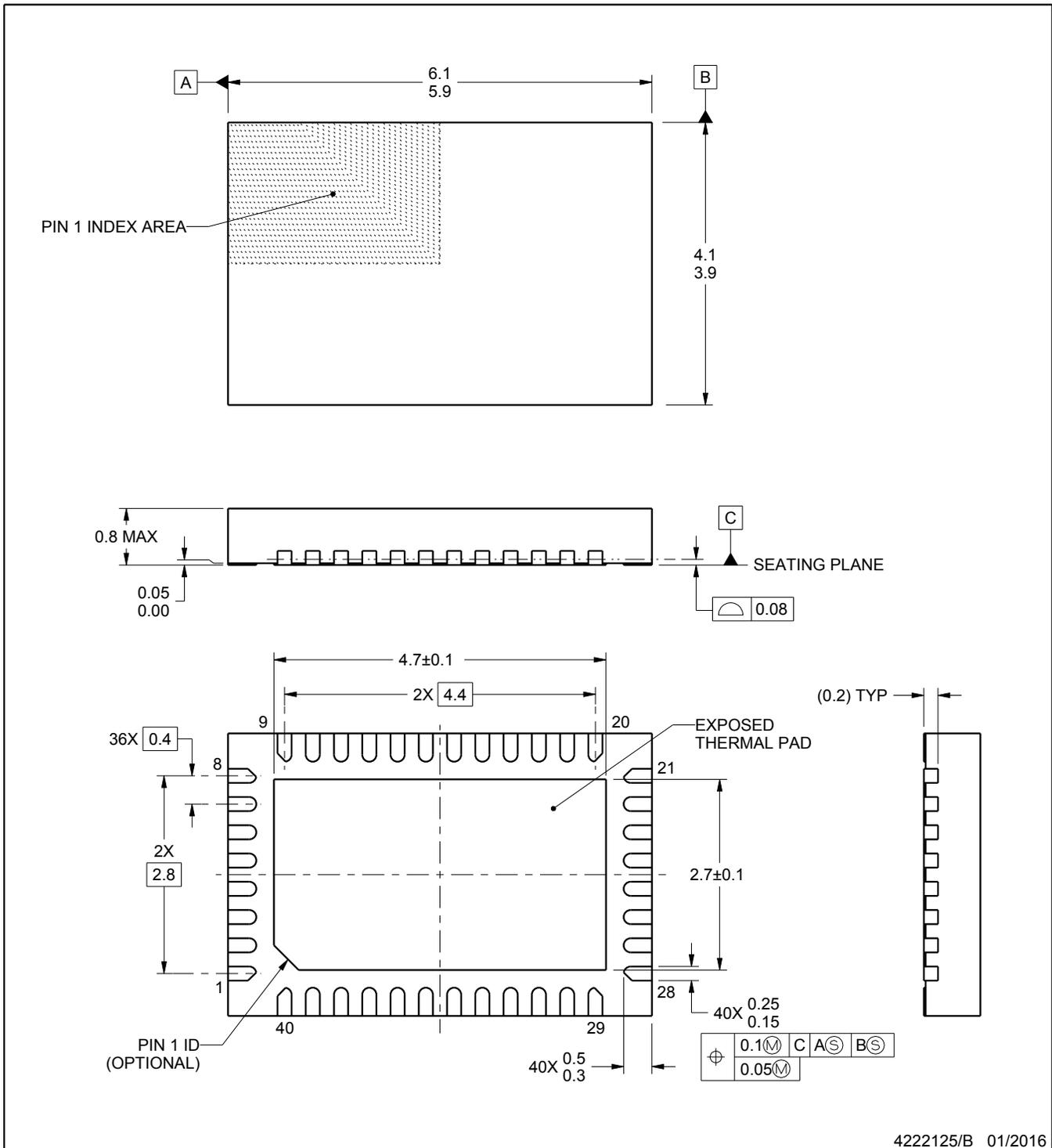
# RNQ0040A



# PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4222125/B 01/2016

**NOTES:**

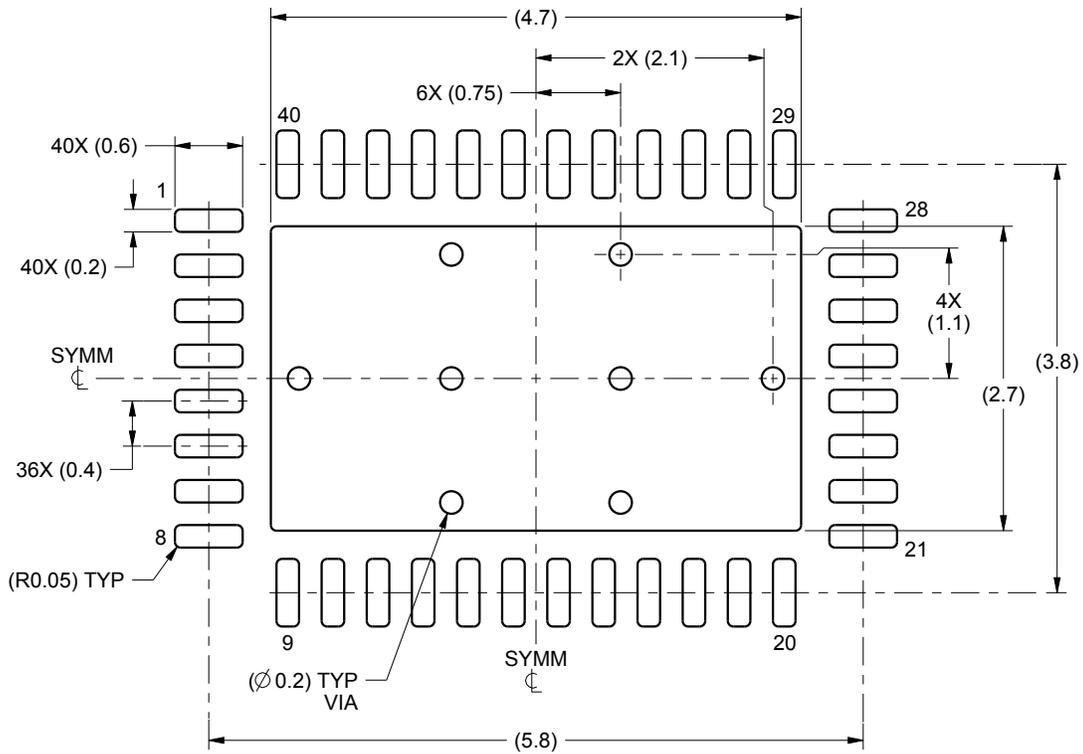
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

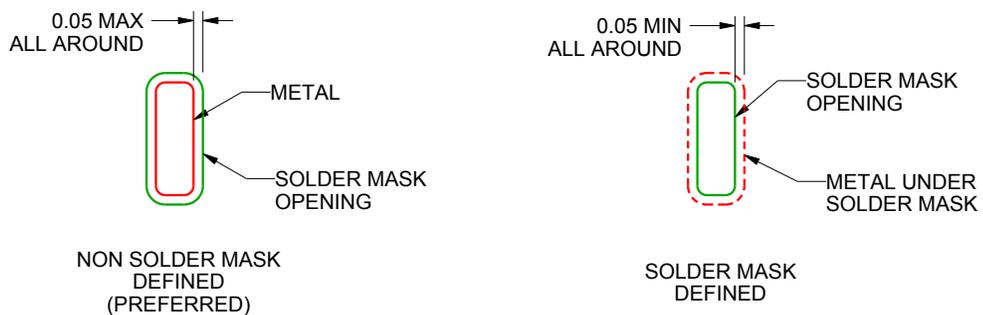
**RNQ0040A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4222125/B 01/2016

NOTES: (continued)

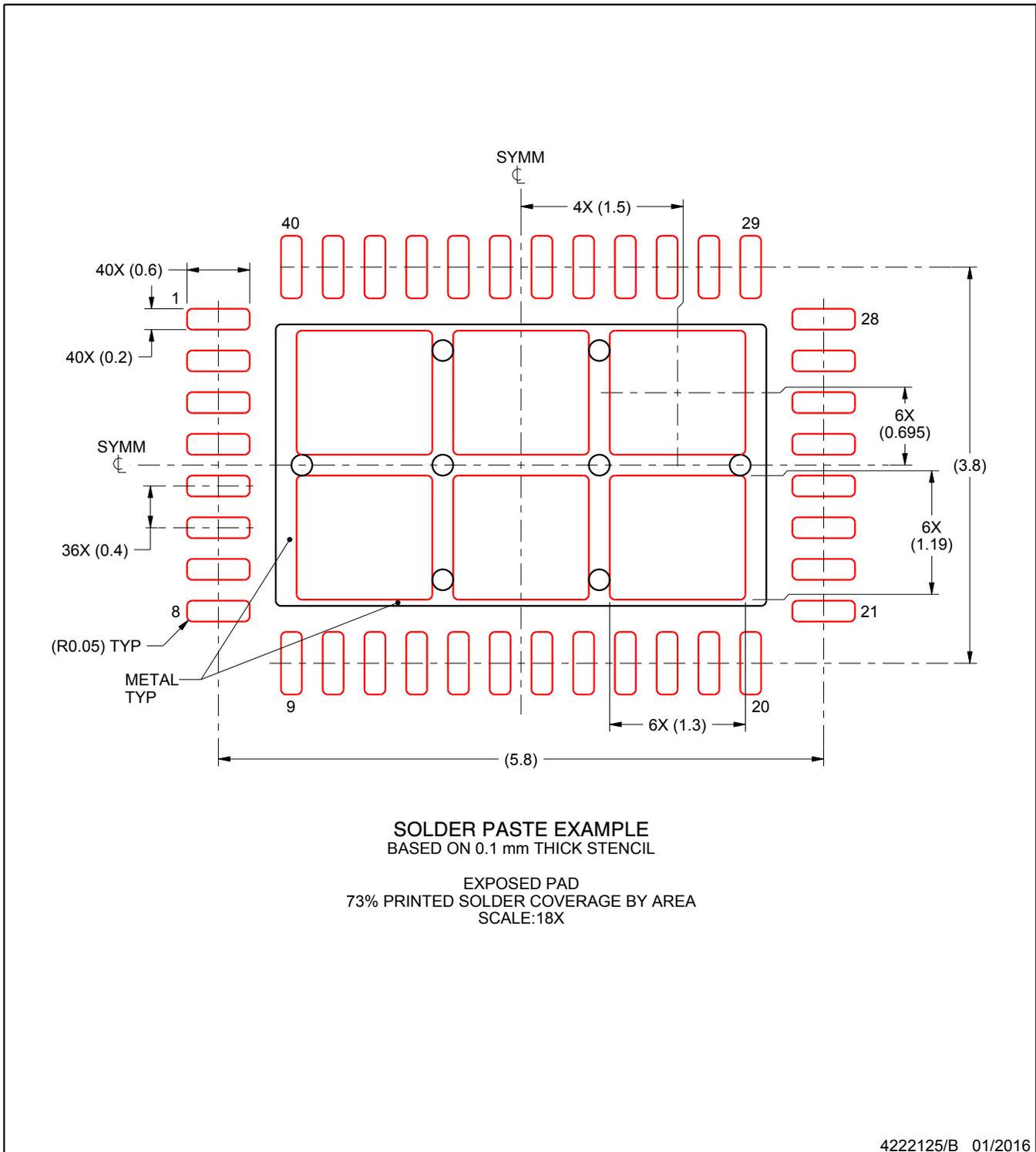
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RNQ0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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