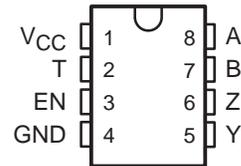


# SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

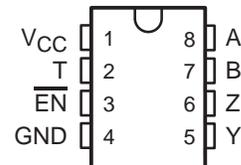
SLLS002C – D2606, JULY 1985 – REVISED FEBRUARY 1993

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Bus Voltage Range . . .  $-7\text{ V}$  to  $12\text{ V}$
- Positive and Negative Current Limiting
- Driver Output Capability . . .  $60\text{ mA}$  Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . .  $12\text{ k}\Omega$  Min
- Receiver Input Sensitivity . . .  $\pm 200\text{ mV}$
- Receiver Input Hysteresis . . .  $50\text{ mV}$  Typ
- Operates From Single  $5\text{-V}$  Supply
- Low Power Requirements

SN75177B . . . D OR P PACKAGE  
(TOP VIEW)



SN75178B . . . P PACKAGE  
(TOP VIEW)



**THE SN75177B IS NOT  
RECOMMENDED FOR NEW DESIGN**

## description

The SN75177B and SN75178B differential bus repeaters are monolithic integrated devices each designed for one-way data communication on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. Each device is designed to improve the performance of the data communication over long bus lines. The SN75177B and SN75178B are identical except for the complementary enable inputs, which allow the devices to be used in pairs for bidirectional communication.

The SN75177B and SN75178B feature positive- and negative-current limiting 3-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of  $\pm 200\text{ mV}$  over a common-mode input voltage range of  $-7\text{ V}$  to  $12\text{ V}$ . The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately  $150^\circ\text{C}$ . The driver is designed to drive current loads up to  $60\text{ mA}$  maximum.

The SN75177B and SN75178B are designed for optimum performance when used on transmission buses employing the SN75172 and SN75174 differential line drivers, SN75173 and SN75175 differential line receivers, or SN75176B bus transceiver.

## Function Tables

SN75177B

DIFFERENTIAL INPUTS A – B	ENABLE EN	OUTPUTS		
		T	Y	Z
$V_{ID} \geq 0.2\text{ V}$	H	H	H	L
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	H	?	?	?
$V_{ID} \leq 0.2\text{ V}$	H	L	L	H
X	L	Z	Z	Z

SN75178B

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{\text{EN}}$	OUTPUTS		
		T	Y	Z
$V_{ID} \geq 0.2\text{ V}$	L	H	H	L
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?	?	?
$V_{ID} \leq 0.2\text{ V}$	L	L	L	H
X	H	Z	Z	Z

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = impedance (off)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

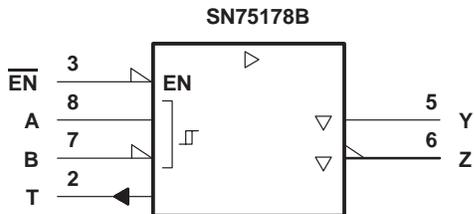
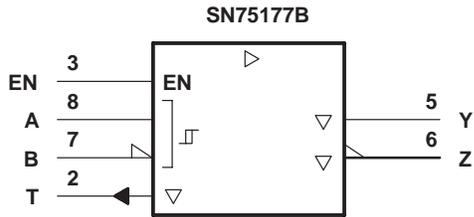
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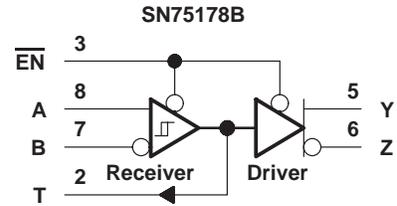
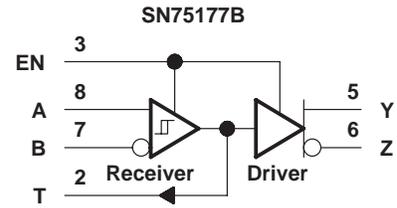
# SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

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## logic symbols†

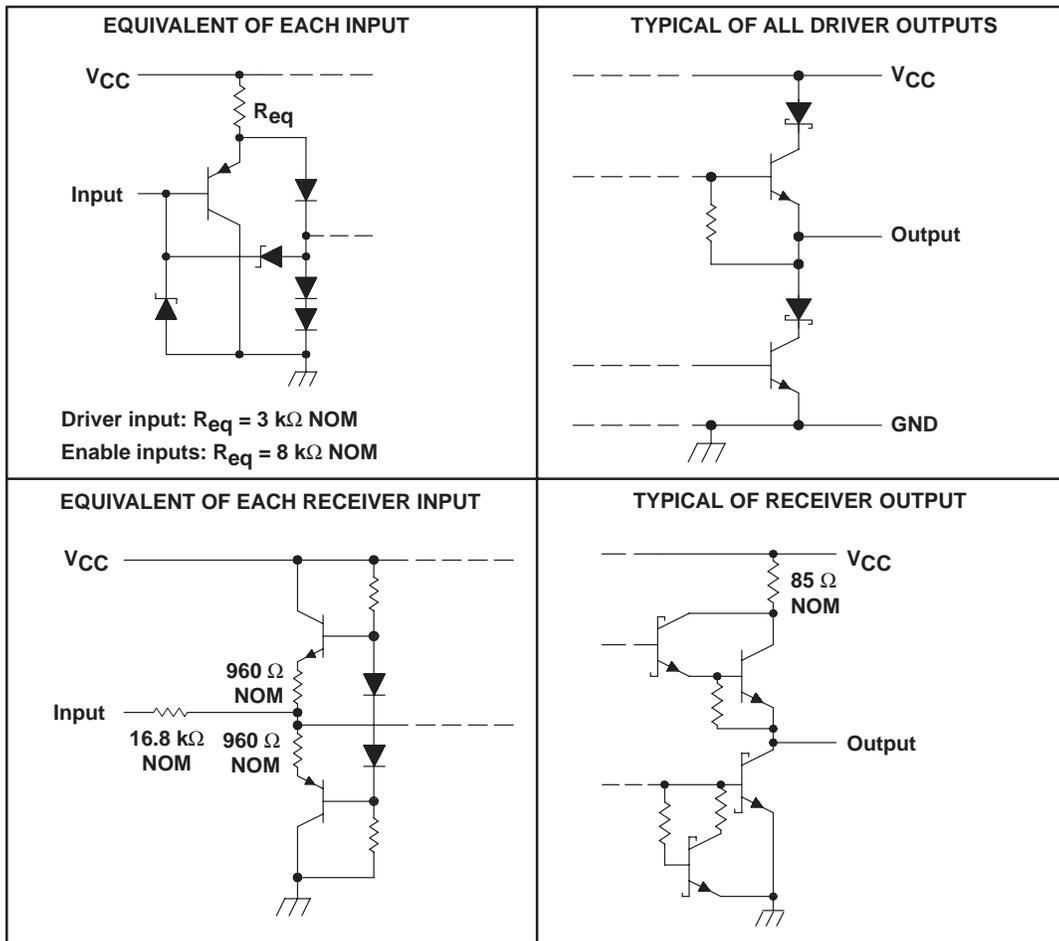


## logic diagrams (positive logic)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## schematics of inputs and outputs



# SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Voltage range at any bus terminal .....	–10 V to 15 V
Differential input voltage (see Note 2) .....	$\pm 25$ V
Enable input voltage .....	5.5 V
Continuous total dissipation .....	See Dissipation Rating Table
Operating free-air temperature range .....	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range .....	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	$260^{\circ}\text{C}$

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.  
 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^{\circ}\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^{\circ}\text{C}$	$T_A = 70^{\circ}\text{C}$ POWER RATING
D	725 mW	5.8 mW/ $^{\circ}\text{C}$	464 mW
P	1000 mW	8.0 mW/ $^{\circ}\text{C}$	640 mW

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
High-level input voltage, $V_{IH}$	EN or $\overline{\text{EN}}$	2			V
low-level input voltage, $V_{IL}$	EN or $\overline{\text{EN}}$			0.8	V
Common-mode input voltage, $V_{IC}$		$-7^{\dagger}$		12	V
Differential input voltage, $V_{ID}$				$\pm 12$	V
High-level output current, $I_{OH}$	Driver			–60	mA
	Receiver			–400	$\mu\text{A}$
Low-level output current, $I_{OL}$	Driver			60	mA
	Receiver			8	mA
Operating free-air temperature, $T_A$		0		70	$^{\circ}\text{C}$

$\dagger$  The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.



# SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

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## DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$ Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
$V_O$ Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$ , See Figure 1	$1/2 V_{OD1}$ or $2\text{§}$			V
	$R_L = 54 \Omega$ , See Figure 1	1.5	2.5	5	
$ V_{OD3} $ Differential output voltage	See Note 3	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage‡	$R_L = 54 \Omega$ or $100 \Omega$ , See Figure 1			$\pm 0.2$	V
$V_{OC}$ Common-mode output voltage				3 -1	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage‡				$\pm 0.2$	V
$I_O$ Output current	$V_{CC} = 0$ , $V_O = -7 \text{ V to } 12 \text{ V}$			$\pm 100$	$\mu\text{A}$
$I_{OZ}$ High-impedance-state output current	$V_O = -7 \text{ V to } 12 \text{ V}$			$\pm 100$	$\mu\text{A}$
$I_{IH}$ High-level input current	$V_I = 2.4 \text{ V}$			20	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_I = 0.4 \text{ V}$			-400	$\mu\text{A}$
$I_{OS}$ Short-circuit output current	$V_O = -7 \text{ V}$			-250	mA
	$V_O = V_{CC}$			250	
	$V_O = 12 \text{ V}$			250	
$I_{CC}$ Supply current (total package)	No load	Outputs enabled	57	70	mA
		Outputs disabled	26	35	

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level.

§ The minimum  $V_{OD2}$  with a  $100\text{-}\Omega$  load is either  $1/2 V_{OD1}$  or 2, whichever is greater.

NOTE 3: See Figure 3.5 of EIA Standard RS-485.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dD}$ Differential-output delay time	$R_L = 54 \Omega$ , See Figure 3		15	20	ns
$t_{tD}$ Differential-output transition time			20	30	ns
$t_{PZH}$ Output enable time to high level	$R_L = 110 \Omega$ , See Figure 4		85	120	ns
$t_{PZL}$ Output enable time to low level	$R_L = 110 \Omega$ , See Figure 5		40	60	ns
$t_{PHZ}$ Output disable time from high level	$R_L = 110 \Omega$ , See Figure 4		150	250	ns
$t_{PLZ}$ Output disable time from low level	$R_L = 110 \Omega$ , See Figure 5		20	30	ns



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# SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

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## SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
$V_O$	$V_{oa}, V_{ob}$	$V_{oa}, V_{ob}$
$ V_{OD1} $	$V_o$	$V_o$
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $		$V_t$ (Test Termination Measurement 2)
$\Delta V_{OD} $	$  V_t  -  \bar{V}_t  $	$  V_t  -  \bar{V}_t  $
$V_{OC}$	$ V_{OS} $	$ V_{OS} $
$\Delta V_{OC} $	$ V_{OS} - \bar{V}_{OS} $	$ V_{OS} - \bar{V}_{OS} $
$I_{OS}$	$ I_{sa} ,  I_{sb} $	
$I_O$	$ I_{xa} ,  I_{xb} $	$I_{ia}, I_{ib}$

## RECEIVER SECTION

**electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{T+}$	Positive-going input threshold voltage	$V_O = 2.7 \text{ V}$ ,	$I_O = -0.4 \text{ mA}$			0.2	V
$V_{T-}$	Negative-going input threshold voltage	$V_O = 0.5 \text{ V}$ ,	$I_O = 8 \text{ mA}$	-0.2‡			V
$V_{hys}$	Input hysteresis ( $V_{T+} - V_{T-}$ )				50		mV
$V_{IK}$	Input clamp voltage at EN		$I_I = -18 \text{ mA}$			-1.5	V
$V_{OH}$	High-level output voltage	$V_{ID} = 200 \text{ mV}$ , See Figure 2	$I_{OH} = -400 \mu\text{A}$ ,	2.7			V
$V_{OL}$	Low-level output voltage	$V_{ID} = -200 \text{ mV}$ , See Figure 2	$I_{OL} = 8 \text{ mA}$ ,			0.45	V
$I_{OZ}$	High-impedance-state output current	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$				20	$\mu\text{A}$
						-400	
$I_I$	Line input current	Other input at 0 V, See Note 4	$V_I = 12 \text{ V}$			1	mA
			$V_I = -7 \text{ V}$			-0.8	
$I_{IH}$	High-level enable-input current	$V_{IH} = 2.7 \text{ V}$				20	$\mu\text{A}$
$I_{IL}$	Low-level enable-input current	$V_{IL} = 0.4 \text{ V}$				-200	$\mu\text{A}$
$r_i$	Input resistance			12			$\text{k}\Omega$
$I_{OS}$	Short-circuit output current			-15		-85	mA
$I_{CC}$	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: Refer to EIA Standard RS-422 for exact conditions.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high level output	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V}$ , $C_L = 15 \text{ pF}$ , See Figure 6			19	35	ns
$t_{PHL}$	Propagation delay time, high-to-low level output				30	40	
$t_{PZH}$	Output enable time to high level	$C_L = 15 \text{ pF}$ , See Figure 7			10	20	ns
$t_{PZL}$	Output enable time to low level				12	20	
$t_{PHZ}$	Output disable time from high level	$C_L = 15 \text{ pF}$ , See Figure 8			25	35	ns
$t_{PLZ}$	Output disable time from low level				17	25	



# SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

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## PARAMETER MEASUREMENT INFORMATION

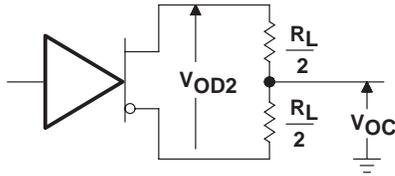


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

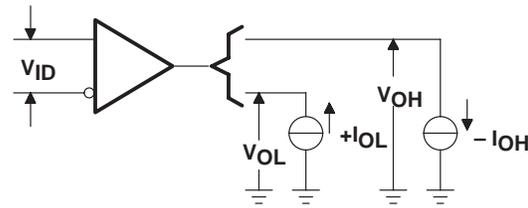
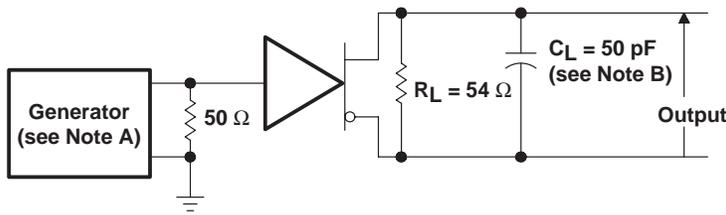
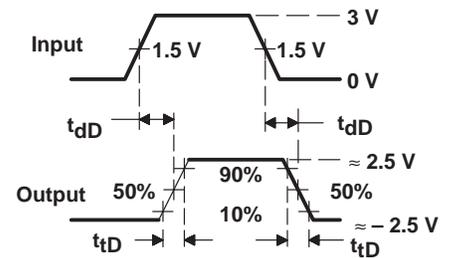


Figure 2. Receiver  $V_{OH}$  and  $V_{OL}$

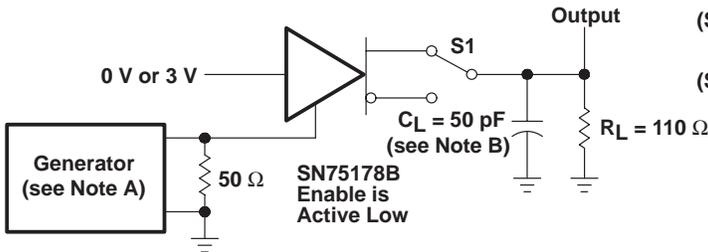


TEST CIRCUIT

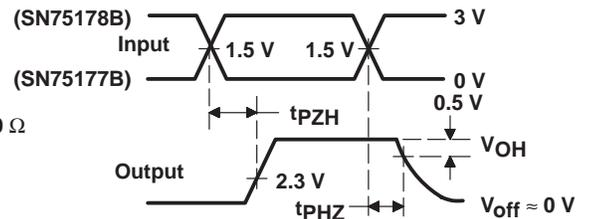


VOLTAGE WAVEFORMS

Figure 3. Driver Differential-Output Test Circuit and Voltage Waveforms

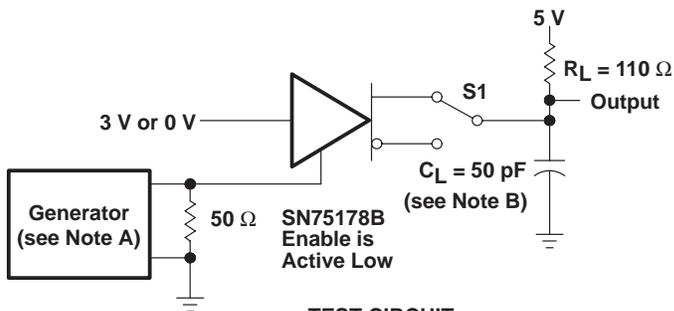


TEST CIRCUIT

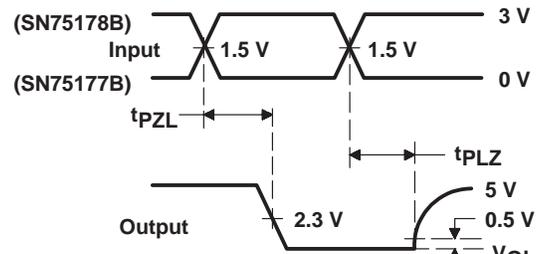


VOLTAGE WAVEFORMS

Figure 4. Driver Enable and Disable Times



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Driver Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_0 = 50 \Omega$ .

B.  $C_L$  includes probe and jig capacitance.

## PARAMETER MEASUREMENT INFORMATION

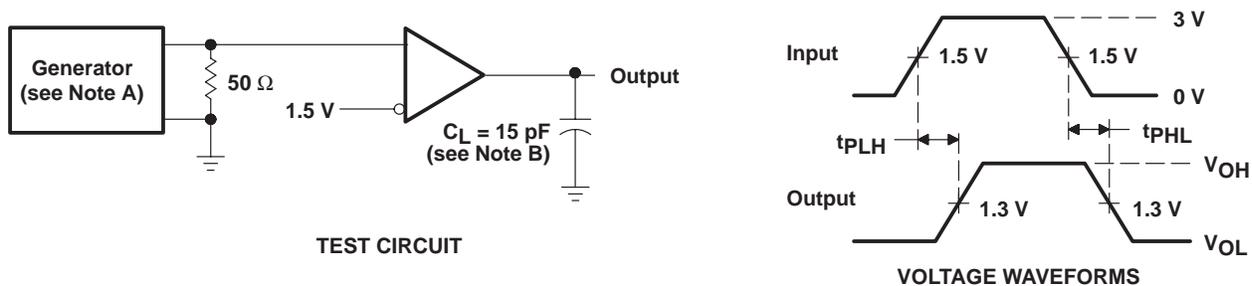


Figure 6. Receiver Propagation Delay Times

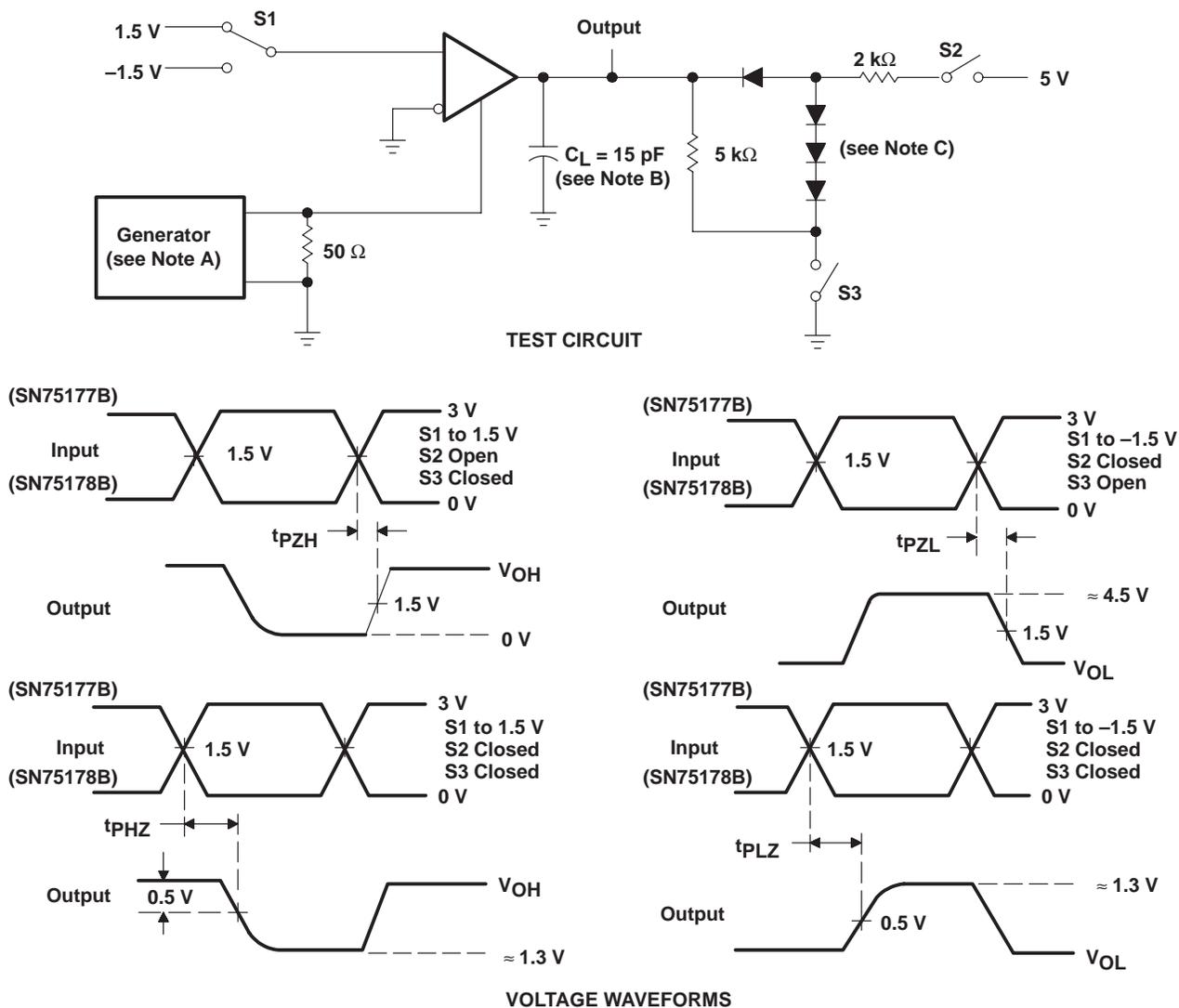


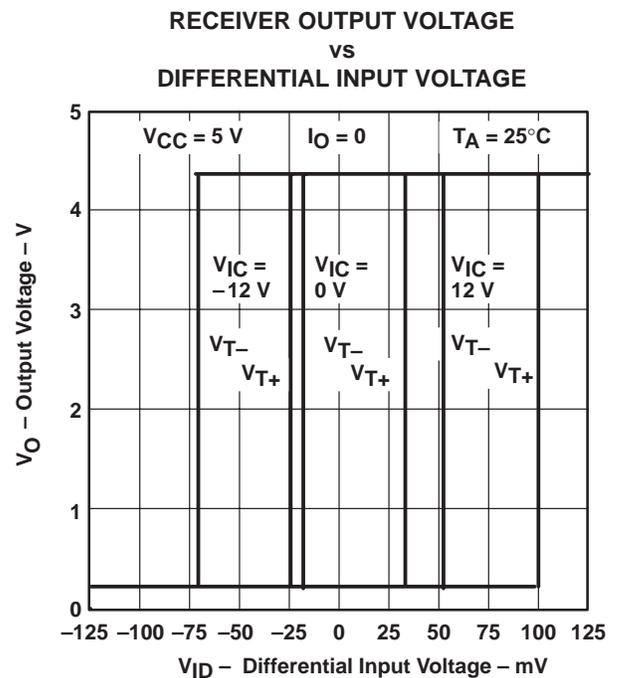
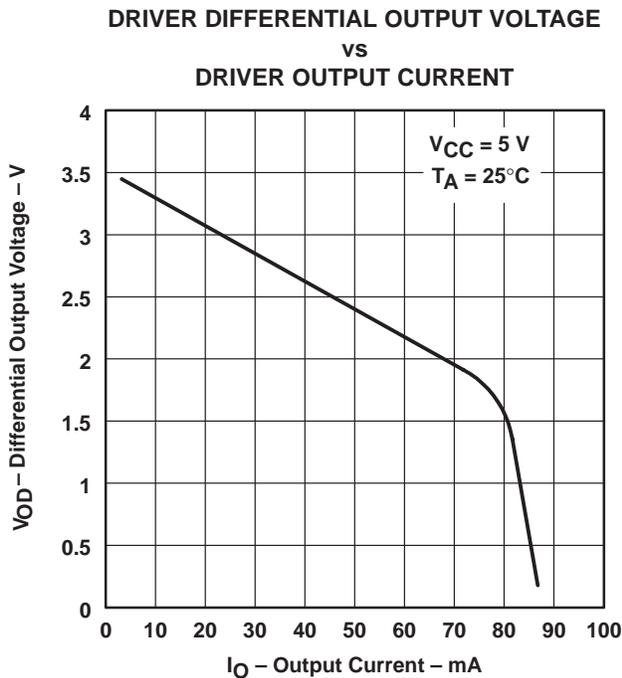
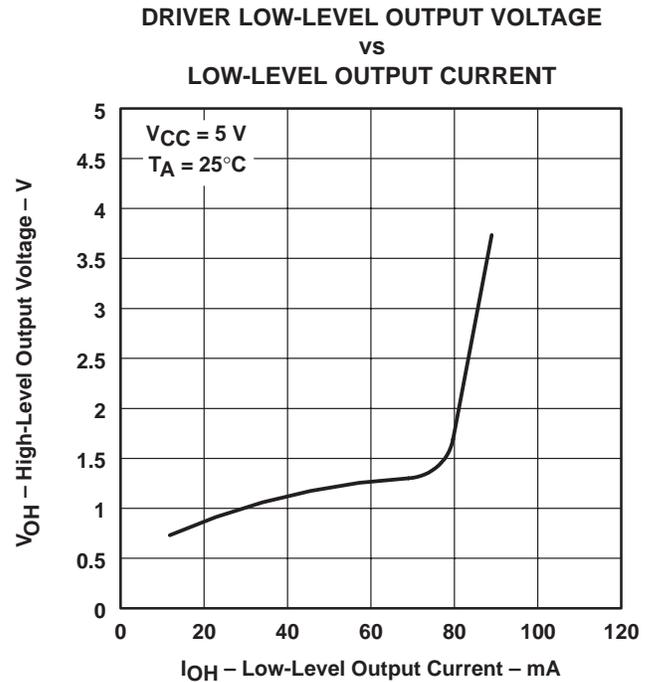
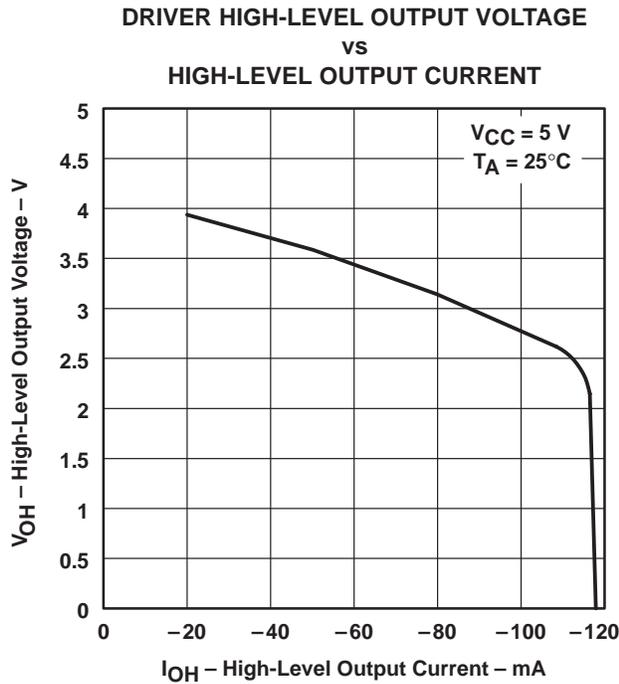
Figure 7. Receiver Output Enable and Disable Times

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_0 = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N916 or equivalent.

# SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

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## TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

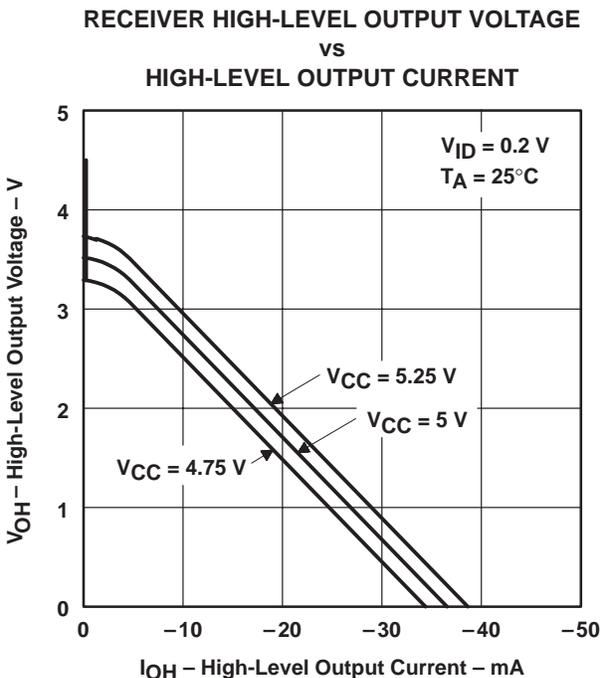


Figure 12

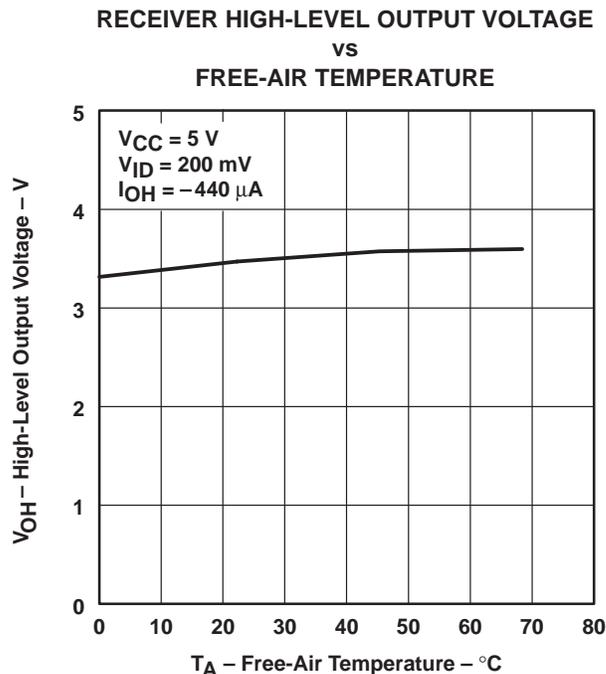


Figure 13

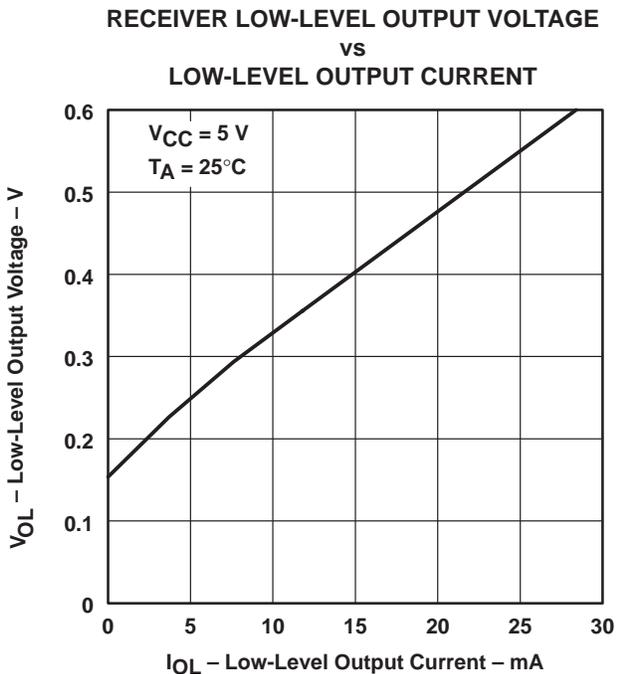


Figure 14

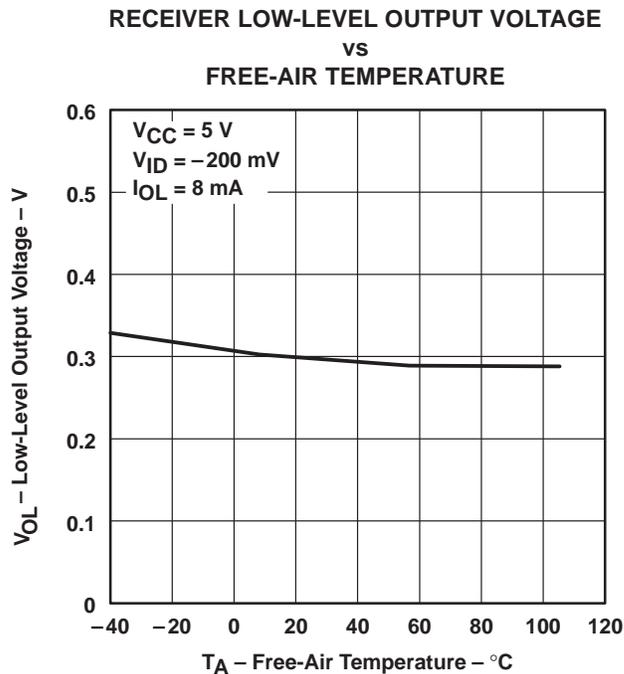
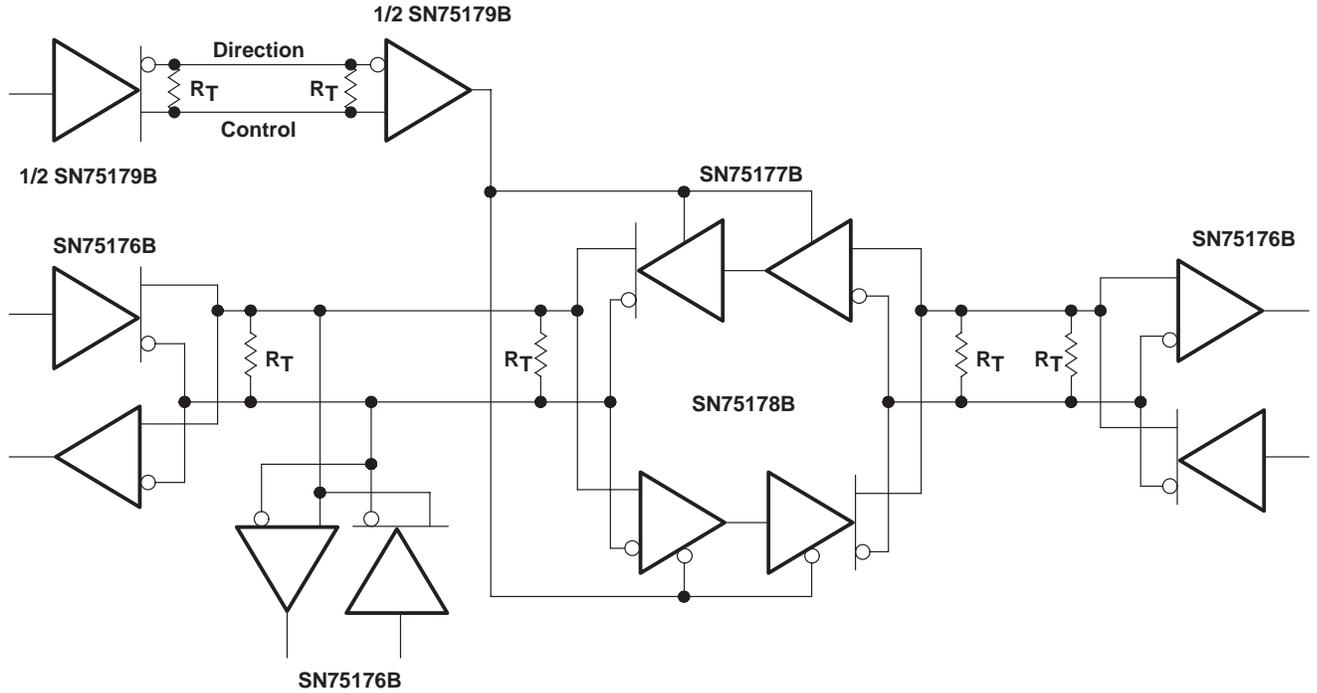


Figure 15

# SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

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## APPLICATION INFORMATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 16. Typical Application Circuit

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN75178BP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75178BP
SN75178BP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75178BP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75178BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75178BP.A	P	PDIP	8	50	506	13.97	11230	4.32

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