AK4601

Audio HUB CODEC with Digital Mixer

1. General Description

The AK4601 is an Audio HUB CODEC including 5ch ADC, 6ch DAC and digital mixers. The analog input block consists of a 24-bit stereo ADC, a 24-bit stereo ADC with input selector and a monaural ADC, and the analog output block consists of 32-bit 6ch DAC. The transfer block for digital signals integrates a serial interface that supports Data BUS and TDM format, realizing an audio HUB function. It gives scalability to the device for both analog and digital signals.
A car audio system that is capable of processing both sound and voice such as for hands-free function simultaneously can be realized by using the AK4601 with AKM's multi-core DSP, the AK7707. The AK4601 is available in a space saving 48-pin LQFP package.

2. Features

□ **ADC1: 24-bit Stereo ADC with MIC Gain Amplifiers**
- **Sampling Frequency: fs=8kHz to 192kHz**
- **Channel Independent Analog Gain Amplifiers (0 to 18dB(2dB Step), 18 to 36dB(3dB step))**
- **Differential Input or Single-ended Input**
- **ADC Characteristics S/N: 106dB (fs=48kHz, Differential Input, MIC Gain=0dB,)**
- **Channel Independent Digital Volume Control (+24 to -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **Low Noise MIC Power Output: 2ch**
- **4 types of Digital Filter for Sound Color Selection**

□ **ADC2: 24-bit Stereo ADC with Input Selector**
- **Sampling Frequency: fs=8kHz to 192kHz**
- **Analog Input Selector: Differential Input x1 or Single-ended Input x2, Semi-Differential Input x1**
- **ADC Characteristics S/N: 106dB (fs=48kHz, Differential Input)**
- **Channel Independent Digital Volume (+24 to -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **4 types of Digital Filter for Sound Color Selection**

□ **ADCM: 24-bit Monaural ADC**
- **Sampling Frequency: fs=8kHz to 192kHz**
- **Differential Input or Single-ended Input**
- **ADC Characteristics S/N: 106dB (fs=48kHz, Differential Input)**
- **Channel Independent Digital Volume (+24 to -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **4 types of Digital Filter for Sound Color Selection**

□ **DAC: Advanced 32-bit DAC**
- **2ch x3**
- **Sampling Frequency: fs=8kHz to 192kHz**
- **Single-ended Output**
- **DAC Characteristics S/N: 108dB (fs=48kHz)**
- **Channel Independent Digital Volume Control (+12 to -115dB, 0.5dB Step, Mute)**
- **4 types of Digital Filter for Sound Color Selection**

□ **Digital Interface:**
- **Digital Input Port: max 20ch(16ch x 1Port, 2ch x 2Port) when TDM mode**
- **Digital Output Port: max 20ch(16ch x 1Port, 2ch x 2Port) when TDM mode**
- **Independent LRCK/BICK Input port x 2 Lines**
- **Data Format: MSB 32,24-bit / LSB 24,20,16-bit / I^2S**
- **PCM Short / Long Frame Supported**
- **TDM Format Supported**

□ **Digital Mixer Circuit**
□ **Independent Digital Volume (+12 to -115dB, 0.5dB Step, Mute)**
□ **PLL Circuit**
□ **µP Interface: SPI(7MHz max), I^2C-bus (max 1MHz, Fast Mode Plus)**
□ **Power Supply:**
- **Analog AVDD: 3.0 to 3.6V (typ. 3.3V)**
- **Digital LVDD: 3.0 to 3.6V (typ. 3.3V) (3.3V → 1.2V regulator integrated)**
- **I/F TVDD: 1.7 to 3.6V (typ. 3.3V)**

□ **Operating Temperature Range: -40°C to 85°C**
□ **Package: 48-pin LQFP (7mm x 7mm, 0.5mm pitch)**

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4. Block Diagram and Functions

■ Device Block Diagram

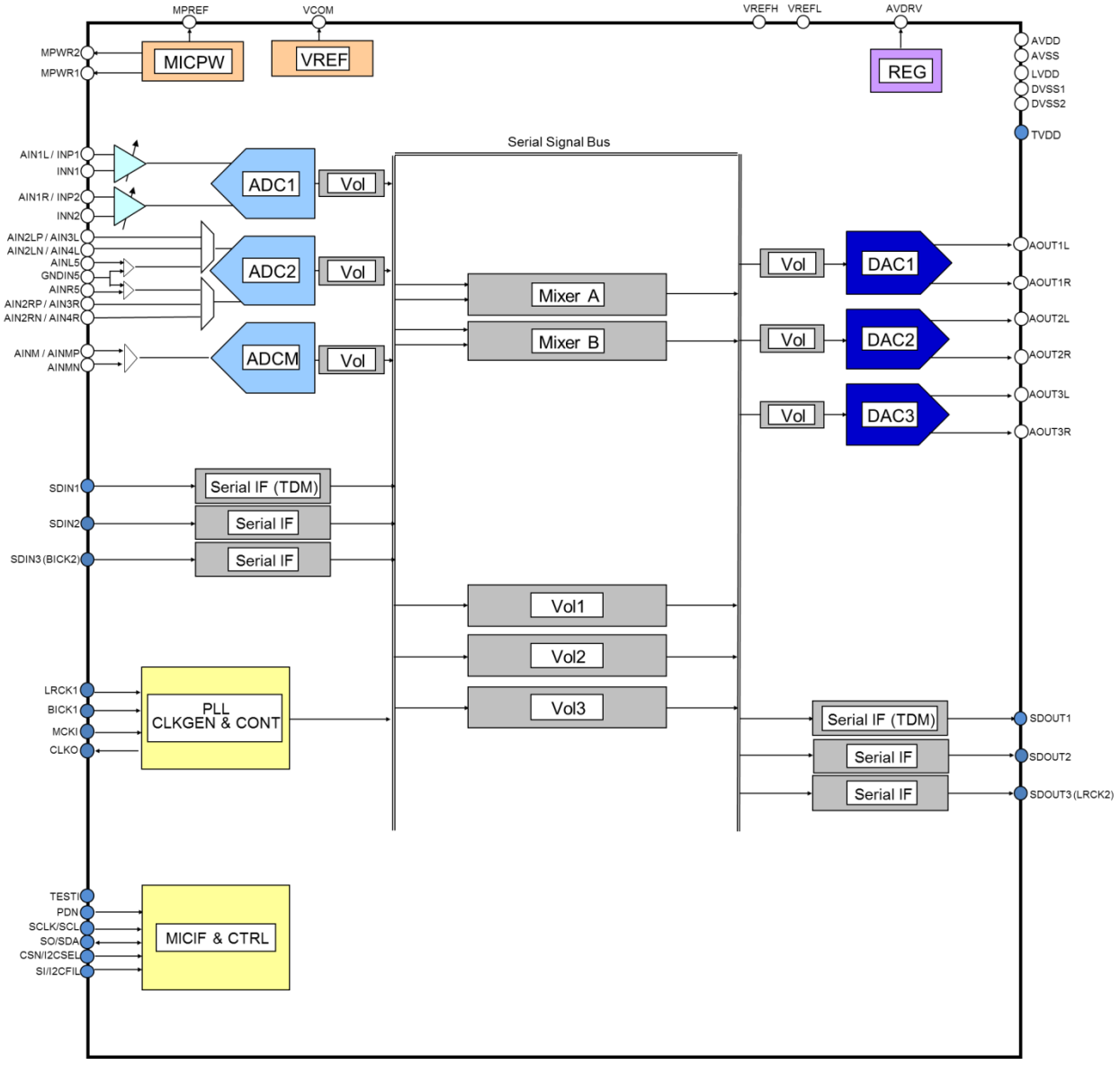
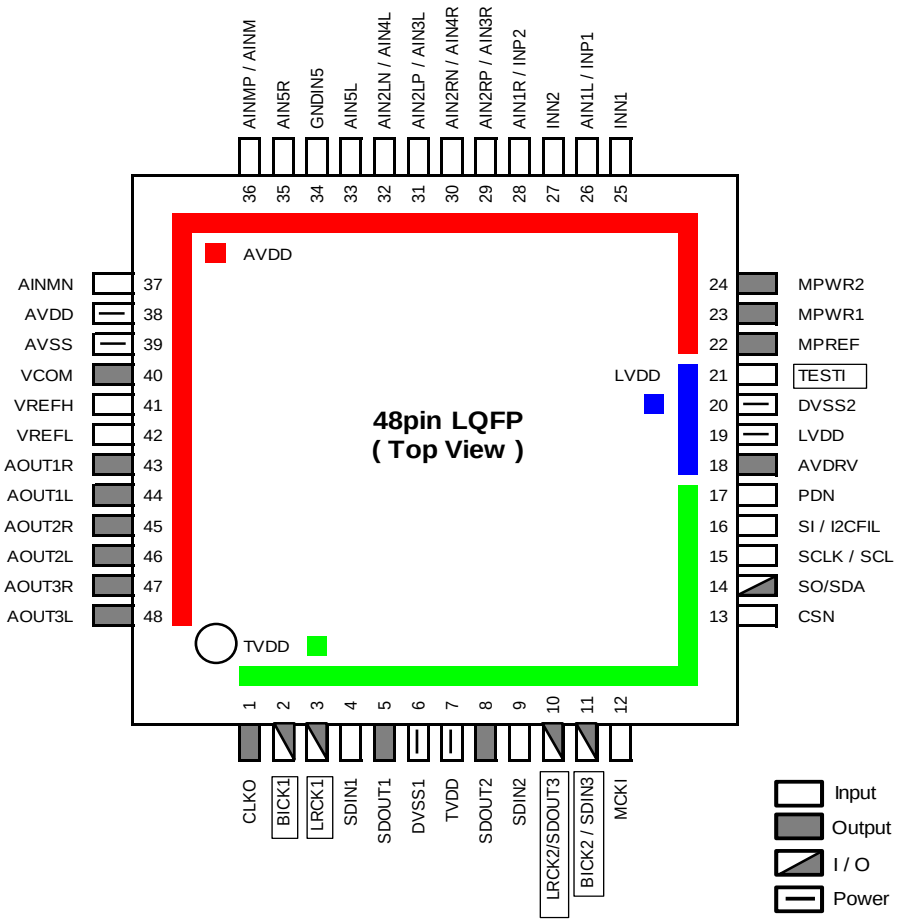


Figure 1. Block Diagram

5. Pin Configuration and Functions

■ Pin Layout



*** Pins with framed name are pulled down internally.

■ Pin Functions

No.	Pin Name	I/O	Function
1	CLKO	O	Master Clock Output Pin
2	BICK1	I/O	Serial Bit Clock 1 Pin
3	LRCK1	I/O	LR Channel Select Clock 1 Pin
4	SDIN1	I	Serial Digital Data Input 1 Pin
5	SDOUT1	O	Serial Digital Data Output 1 Pin
6	DVSS1	-	Digital Ground 1 Pin 0V
7	TVDD	-	Digital I/F Power Supply Pin 1.7~3.6V (typ.3.3V)
8	SDOUT2	O	Serial Data Output 2 Pin
9	SDIN2	I	Serial Data Input 2 Pin
10	LRCK2	I/O	LR Channel Select Clock 2 Pin (MSELN bit = "L", default)
	SDOUT3		Serial Data Output 3 Pin (MSELN bit = "H")
11	BICK2	I/O	Serial Bit Clock 2 Pin (MSELN bit = "L", default)
	SDIN3		Serial Data Input 3 Pin (MSELN bit = "H")
12	MCKI	I	Master Clock Pin
13	CSN	I	SPI I/F Chip Select N Pin During power-down state or when µP I/F are not in use, leave this pin "H" level.
14	SO	O	Serial Data Output Pin for SPI I/F This pin outputs "Hi-Z" during power-down state.
	SDA	I/O	Serial Data In/Output Pin for I^2C I/F This pin outputs "Hi-Z" during power-down state.
15	SCLK	I	Serial Data Clock Input Pin for SPI I/F
	SCL	I	Serial Data Clock Input Pin for I^2C I/F
16	SI	I	Serial Data Input Pin for SPI I/F
	I2CFIL	I	I^2C I/F Mode Select Input Pin I2CFIL = "L": Fast Mode (400kHz) I2CFIL = "H": Fast Mode Plus (1MHz) (should be fixed to TVDD)
17	PDN	I	Power-down N Pin Use this pin to power down the AK4601. The PDN pin should be held "L" when power is supplied.

No.	Pin Name	I/O	Function
18	AVDRV	O	LDO Output Pin Connect a 2.2uF ceramic capacitor between this pin and DVSS2. Do not connect this pin to an external circuit.
19	LVDD	-	Digital Core Power Supply Pin 3.0~3.6V (typ.3.3V)
20	DVSS2	-	Digital Ground 2 Pin 0V
21	TESTI	I	Test Input Pin It must be tied “L”.
22	MPREF	O	Ripple Filter Pin for Microphone Power Supply Connect a 1uF ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit.
23	MPWR1	O	Power Supply Output 1 Pin for Microphone This pin outputs “Hi-Z” during power-down state.
24	MPWR2	O	Power Supply Output 2 Pin for Microphone This pin outputs “Hi-Z” during power-down state.
25	INN1	I	MIC Lch Inverted Differential Input 1 Pin
26	AIN1L	I	MIC Lch Single-ended Input 1 Pin
	INP1	I	MIC Lch Non-inverted Differential Input 1 Pin
27	INN2	I	MIC Rch Inverted Differential Input 2 Pin
28	AIN1R	I	MIC Rch Single-ended Input 1 Pin
	INP2	I	MIC Rch Non-inverted Differential Input 2 Pin
29	AIN2RP	I	ADC2 Rch Non-inverted Differential Input 2 Pin
	AIN3R	I	ADC2 Rch Single-ended Input 3 Pin
30	AIN2RN	I	ADC2 Rch Inverted Differential Input 2 Pin
	AIN4R	I	ADC2 Rch Single-ended Input 4 Pin
31	AIN2LP	I	ADC2 Lch Non-inverted Differential Input 2 Pin
	AIN3L	I	ADC2 Lch Single-ended Input 3 Pin
32	AIN2LN	I	ADC2 Lch Inverted Differential Input 2 Pin
	AIN4L	I	ADC2 Lch Single-ended Input 4 Pin
33	AIN5L	I	ADC2 Lch Pseudo Differential Input 5 Pin
34	GNDIN5	I	ADC2 Pseudo Differential Ground Input 5 Pin
35	AIN5R	I	ADC2 Rch Pseudo Differential Input 5 Pin
36	AINMP	I	ADCM Non-inverted Differential Input Pin
	AINM	I	ADCM Single-ended Input Pin
37	AINMN	I	ADCM Inverted Differential Input Pin
38	AVDD	-	Analog Power Supply Pin 3.0~3.6V (typ.3.3V)
39	AVSS	-	Analog Ground Pin 0V
40	VCOM	O	Analog Common Voltage Output Pin Connect a 2.2uF ceramic capacitor between this pin and AVSS. Do not connect this pin to an external circuit. This pin outputs “L” during power-down state.

No.	Pin Name	I/O	Function
41	VREFH	I	Analog High-level Reference Voltage Input Pin Connect this pin to AVDD.
42	VREFL	I	Analog Low-level Reference Voltage Input Pin Connect this pin to AVSS.
43	AOUT1R	O	DAC1 Rch Analog Output Pin This pin outputs “Hi-Z” during power-down state.
44	AOUT1L	O	DAC1 Lch Analog Output Pin This pin outputs “Hi-Z” during power-down state.
45	AOUT2R	O	DAC2 Rch Analog Output Pin This pin outputs “Hi-Z” during power-down state.
46	AOUT2L	O	DAC2 Lch Analog Output Pin This pin outputs “Hi-Z” during power-down state.
47	AOUT3R	O	DAC3 Rch Analog Output Pin This pin outputs “Hi-Z” during power-down state.
48	AOUT3L	O	DAC3 Lch Analog Output Pin This pin outputs “Hi-Z” during power-down state.

■ Handling of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	MPREF, MPWR1, MPWR2, AIN1L/INP1, INN1, AIN1R/INP2, INN2, AIN2LP/AIN3L, AIN2LN/AIN4L, AIN2RP/AIN3R, AIN2RN/AIN4R, AIN5L, GNDIN5, AIN5R, AINMP/AINM, AINMN, AOUT1L, AOUT1R AOUT2L, AOUT2R, AOUT3L, AOUT3R	Open
Digital	SDOUT1, SDOUT2, CLKO	Open
	BICK2/SDIN3, SDIN2, SDIN1, LRCK1, BICK1, LRCK2/SDOUT3, MCKI, TESTI	Connect to DVSS1 ~ 2

Table 1. Handling of Unused Pins

■ Pull-down Pin Statuses

Pin No.	Pin	Power-down PDN pin = "L"	Power-down Release PDN pin = "H" (Slave Mode, MSNx bit = "0")		Power-down Release PDN pin = "H" (Master Mode MSNx bit = "1")
			PSWxN bit = "1"	PSWxN bit = "0"	
1	CLKO	Pulled-down (50K)	Output	Output	Output
2	BICK1	Pulled-down (50K)	Input HiZ	Input Pulled-down (46K)	Output
3	LRCK1	Pulled-down (50K)	Input HiZ	Input Pulled-down (46K)	Output
5	SDOUT1	Pulled-down (50K)	Output	Output	Output
8	SDOUT2	Pulled-down (50K)	Output	Output	Output
10	LRCK2/SDOUT3	Pulled-down (50K)	-		-
	LRCK2 (MSELN bit = "L")	-	Input HiZ	Input Pulled-down (46K)	Output
	SDOUT3 (MSELN bit = "H")	-	Output	Output	Output
11	BICK2/SDIN3	Pulled-down (50K)	-		-
	BICK2 (MSELN bit = "L")	-	Input HiZ	Input Pulled-down (46K)	Output
	SDIN3 (MSELN bit = "H")	-	Input HiZ	Input HiZ	Input
18	AVDRV	Pulled-down (70Ω)	Output	Output	Output
21	TESTI	Pulled-down (25K)	Pulled-down (25K)	Pulled-down (25K)	Pulled-down (25K)

Table 2. Pull-down Pin Statuses (x=1~2)

■ Power-down Status of Output Pins

No	Pin Name	I/O	Power-down Status	No	Pin Name	I/O	Power-down Status
1	CLKO	O	“L” Output	23	MPWR1	O	“Hi-Z” Output
2	BICK1	I/O	Input	24	MPWR2	O	“Hi-Z” Output
3	LRCK1	I/O	Input	40	VCOM	O	“L” Output
5	SDOUT1	O	“L” Output	43	AOUT1R	O	“Hi-Z” Output
8	SDOUT2	O	“L” Output	44	AOUT1L	O	“Hi-Z” Output
10	LRCK2/ SDOUT3	I/O	Input	45	AOUT2R	O	“Hi-Z” Output
11	BICK2/SDIN3	I/O	Input	46	AOUT2L	O	“Hi-Z” Output
14	SO/SDA	I/O	“Hi-Z” Output	47	AOUT3R	O	“Hi-Z” Output
18	AVDRV	O	“L” Output	48	AOUT3L	O	“Hi-Z” Output
22	MPREF	O	“L” Output				

Table 3. Power-down Status of Output Pins

6. Absolute Maximum Ratings

(AVSS=DVSS1=DVSS2=0V; Note 1)

Parameter	Symbol	Min.	Max.	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(Core)	LVDD	-0.3	4.3	V
Digital2(I/F)	TVDD	-0.3	4.3	V
Difference (AVSS, DVSS1 ~ 2) (Note 1)	ΔGND	-0.3	0.3	V
Input Current (except power supply pins)	IIN	—	±10	mA
Analog Input Voltage (Note 2)	VINA	-0.3	(AVDD+0.3) or 4.3	V
Digital Input Voltage (Note 3)	VIND1	-0.3	(TVDD+0.3) or 4.3	V
Ambient Temperature (Power applied)	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages are with respect to ground. AVSS and DVSS1-2 must be connected to the same ground.

Note 2. The maximum analog input voltage is a smaller value between (AVDD+0.3)V and 4.3V.

Note 3. The maximum digital input voltage of SDIN1, SDIN2, BICK2/SDIN3, LRCK1, BICK1, MCKI, LRCK2/SDOUT3, PDN, SCLK/SCL, SO/SDA, CSN, SI/I2CFIL pins is a smaller value between (TVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS1=DVSS2=0V; Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supplies					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(Core)	LVDD	3.0	3.3	3.6	V
Digital2(I/F)	TVDD	1.7	3.3	3.6	V
Difference1	AVDD – LVDD	-0.1	0	+0.1	V
Difference2	LVDD – TVDD	-0.1	-	-	V

Note 4. The power-up sequence with AVDD, LVDD, TVDD is not critical. The PDN pin should be held “L” when power is supplied. The PDN pin is allowed to be “H” after all power supplies are applied and settled.

Note 5. Do not turn off the power supply of the AK4601 with the power supply of the peripheral device turned on when using the I^2C interface. Pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC AMP Gain

(Ta=25°C; AVDD=VREFH=LVDD=TVDD=3.3V; AVSS=VREFL=DVSS1=DVSS2=0V, ADC1VL/R bit = "0")

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP	Input Impedance		14	20	26	kΩ
	Gain	MGNL[3:0]bits=0h, MGNR[3:0]bits=0h	-1	0	1	dB
		MGNL[3:0]bits=1h, MGNR[3:0]bits=1h	1	2	3	
		MGNL[3:0]bits=2h, MGNR[3:0]bits=2h	3	4	5	
		MGNL[3:0]bits=3h, MGNR[3:0]bits=3h	5	6	7	
		MGNL[3:0]bits=4h, MGNR[3:0]bits=4h	7	8	9	
		MGNL[3:0]bits=5h, MGNR[3:0]bits=5h	9	10	11	
		MGNL[3:0]bits=6h, MGNR[3:0]bits=6h	11	12	13	
		MGNL[3:0]bits=7h, MGNR[3:0]bits=7h	13	14	15	
		MGNL[3:0]bits=8h, MGNR[3:0]bits=8h	15	16	17	
		MGNL[3:0]bits=9h, MGNR[3:0]bits=9h	17	18	19	
		MGNL[3:0]bits=Ah, MGNR[3:0]bits=Ah	20	21	22	
		MGNL[3:0]bits=Bh, MGNR[3:0]bits=Bh	23	24	25	
		MGNL[3:0]bits=Ch, MGNR[3:0]bits=Ch	26	27	28	
		MGNL[3:0]bits=Dh, MGNR[3:0]bits=Dh	29	30	31	
		MGNL[3:0]bits=Eh, MGNR[3:0]bits=Eh	32	33	34	
		MGNL[3:0]bits=Fh, MGNR[3:0]bits=Fh	35	36	37	

2. MIC Bias Output

(Ta=25°C; AVDD=VREFH=LVDD=TVDD =3.3V; AVSS=VREFL=DVSS1=DVSS2=0V; Measurement Frequency = 20Hz~20kHz)

	Parameter	Min.	Typ.	Max.	Unit
MIC Bias	Output Voltage	2.3	2.5	2.7	V
	Load Resistance	2			kΩ
	Load Capaitance			30	pF
	Output Noise (A-weighted)		-114	-108	dBV

3. MIC AMP + ADC1

(Ta=25°C; AVDD=VREFH=LVDD=TVDD=3.3V; AVSS=VREFL= DVSS1= DVSS2 =0V; Signal Frequency =1kHz; 24bit Data; BICK=64fs; Measurement Frequency BW=20Hz ~ 20kHz @fs=48kHz; Measurement Frequency BW=20Hz ~ 40kHz @fs=96kHz,192kHz; ADC1VL/R bit =”0”; MGNL/R[3:0] bits = 0h (0dB))

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP + ADC1	Resolution				24	bit
	Differential Input					
	Full-scale Input Voltage	(Note 7)	±2.1	±2.3	±2.5	Vpp
		(Note 8)	±0.264	±0.290	±0.315	
		(Note 9)	±2.55	±2.83	±3.11	
	S/(N+D) (-1dBFS)	fs=48kHz (Note 7)	85	95		dB
		fs=48kHz (Note 8)		87		
		fs=96kHz (Note 7)		92		
		fs=96kHz (Note 8)		84		
		fs=192kHz (Note 7)		92		
		fs=192kHz (Note 8)		84		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted) (Note 7)	98	106		dB
		fs=48kHz (A-weighted) (Note 8)		95		
		fs=96kHz (Note 7)		99		
		fs=96kHz (Note 8)		89		
		fs=192kHz (Note 7)		99		
		fs=192kHz (Note 8)		89		
	S/N	fs=48kHz (A-weighted) (Note 7)	98	106		dB
		fs=48kHz (A-weighted) (Note 8)		95		
		fs=96kHz (Note 7)		99		
		fs=96kHz (Note 8)		89		
		fs=192kHz (Note 7)		99		
		fs=192kHz (Note 8)		89		
	Inter-Channel Isolation	(Note 6)	90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	PSRR	(Note 7, Note 10)		50		dB
	CMRR	(Note 11)	60	80		dB

Parameter		Min.	Typ.	Max.	Unit
Single-ended Input					
Full-scale Input Voltage	(Note 7)	2.1	2.3	2.5	Vpp
	(Note 8)	0.264	0.290	0.315	
	(Note 9)	2.55	2.83	3.11	
S/(N+D) (-1dBFS)	fs=48kHz (Note 7)	85	95		dB
	fs=48kHz (Note 8)		87		
	fs=96kHz (Note 7)		92		
	fs=96kHz (Note 8)		84		
	fs=192kHz (Note 7)		92		
	fs=192kHz (Note 8)		84		
Dynamic Range (-60dBFS)	fs=48kHz (A-weighted) (Note 7)	96	104		dB
	fs=48kHz (A-weighted) (Note 8)		92		
	fs=96kHz (Note 7)		97		
	fs=96kHz (Note 8)		86		
	fs=192kHz (Note 7)		97		
	fs=192kHz (Note 8)		86		
S/N	fs=48kHz (A-weighted) (Note 7)	96	104		dB
	fs=48kHz (A-weighted) (Note 8)		92		
	fs=96kHz (Note 7)		97		
	fs=96kHz (Note 8)		86		
	fs=192kHz (Note 7)		97		
	fs=192kHz (Note 8)		86		
Inter-Channel Isolation (Note 6)		90	105		dB
Channel Gain Mismatch			0.0	0.3	dB
PSRR (Note 7, Note 10)			50		dB

Note 6. Inter-channel isolation with -1dBFS signal input between Lch and Rch.
Note 7. ADC1VL/R bit = “0”,MGNL/R[3:0] bits = 0h (0dB). Input full-scale voltage is propotional to AVDD (0.7 x AVDD).
Note 8. ADC1VL/R bit = “0”,MGNL/R[3:0] bits = 9h (+18dB). Input full-scale voltage is propotional to AVDD (0.088 x AVDD).
Note 9. ADC1VL/R bit = “1”, MGNL/R[3:0] bits = 0h (0dB). Input full-scale voltage is propotional to AVDD (0.86 x AVDD).
Note 10. PSRR is applied to AVDD and VREFH with 1kHz, 50mVpp.
Note 11. Common mode rejection ratio is applied 1kHz and 100mVpp sine waves to both differential input pins. It is defined as a reference value when appling 1kHz and ±100mVpp sine waves to the differential input.

4. ADC2

(Ta=25°C; AVDD=VREFH=LVDD=TVDD=3.3V; AVSS=VREFL=DVSS1= DVSS2=0V; Signal Frequency=1kHz; 24bit Data; BICK=64fs; Measurement Frequency BW=20Hz ~ 20kHz @fs=48kHz; Measurement Frequency BW=20Hz~40kHz @fs=96kHz,192kHz; ADC2VL/R bit =”0”)

	Parameter		Min.	Typ.	Max.	Unit
ADC2	Resolution				24	bit
	Input Impedance		14	20	26	kΩ
	Differential Input					
	Full-scale Input Voltage (Note 12)	(Note 13)	±2.1	±2.3	±2.5	Vpp
		(Note 14)	±2.55	±2.83	±3.11	
	S/(N+D) (-1dBFS)	fs=48kHz	85	95		dB
		fs=96kHz		92		
		fs=192kHz		92		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	98	106		dB
		fs=96kHz		99		
		fs=192kHz		99		
	S/N	fs=48kHz (A-weighted)	98	106		dB
		fs=96kHz		99		
		fs=192kHz		99		
	Inter-Channel Isolation	(Note 6)	90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	PSRR	(Note 10)		50		dB
	CMRR	(Note 11)	60	80		dB
	Single-ended Input, Pseudo-differential Input					
	Full-scale Input Voltage (Note 15)	(Note 13)	2.1	2.3	2.5	Vpp
		(Note 14)	2.55	2.83	3.11	
	S/(N+D) (-1dBFS)	fs=48kHz	85	95		dB
		fs=96kHz		92		
		fs=192kHz		92		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	96	104		dB
		fs=96kHz		97		
		fs=192kHz		97		
	S/N	fs=48kHz (A-weighted)	96	104		dB
		fs=96kHz		97		
		fs=192kHz		97		
	Inter-Channel Isolation	(Note 6)	90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	PSRR	(Note 10)		50		dB
	CMRR (Pseudo-differential)	(Note 16)	55	75		dB

Note 12. AIN2LP, AIN2LN, AIN2RP and AIN2RN pins.
Note 13. ADC2VL/R bit = “0”. Input full-scale voltage is propotional to AVDD (0.7 x AVDD).
Note 14. ADC2VL/R bit = “0”. Input full-scale voltage is propotional to AVDD (0.86 x AVDD).
Note 15. AIN3L, AIN3R, AIN4L, AIN4R, AIN5L and AIN5R pins.
Note 16. Common mode rejection ratio is applied 1kHz and 100mVpp sine waves to both Pseudo-differential input and Pseudo-differential ground input pins. It is defined as a reference value when appling 100mVpp sine wave to the Pseudo-differential input.

5. ADCM

(Ta=25°C; AVDD=VREFH=LVDD=TVDD=3.3V; AVSS=VREFL=DVSS1=DVSS2=0V; Signal Frequency=1kHz; 24bit Data; BICK=64fs; Measurement Frequency BW=20Hz ~ 20kHz @fs=48kHz; Measurement Frequency BW=20Hz ~ 40kHz @fs=96kHz,192kHz; ADCMV bit =”0”)

	Parameter		Min.	Typ.	Max.	Unit
ADCM	Resolution				24	bit
	Input Impedance		14	20	26	kΩ
	Differential Input					
	Full-scale Input Voltage (Note 17)	(Note 18)	±2.1	±2.3	±2.5	Vpp
		(Note 19)	±2.55	±2.83	±3.11	
	S/(N+D) (-1dBFS)	fs=48kHz	85	95		dB
		fs=96kHz		92		
		fs=192kHz		92		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	98	106		dB
		fs=96kHz		99		
		fs=192kHz		99		
	S/N	fs=48kHz (A-weighted)	98	106		dB
		fs=96kHz		99		
		fs=192kHz		99		
	PSRR	(Note 10)		50		dB
	CMRR	(Note 11)	60	80		dB
	Single-ended Input					
	Full-scale Input Voltage (Note 20)	(Note 18)	2.1	2.3	2.5	Vpp
		(Note 19)	2.55	2.83	3.11	
	S/(N+D) (-1dBFS)	fs=48kHz	85	95		dB
		fs=96kHz		92		
		fs=192kHz		92		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	96	104		dB
		fs=96kHz		97		
		fs=192kHz		97		
	S/N	fs=48kHz (A-weighted)	96	104		dB
		fs=96kHz		97		
		fs=192kHz		97		
	PSRR	(Note 10)		50		dB

Note 17. AINMP and AINMN pins.
Note 18. ADCMV bit = “0”. Input full-scale voltage is propotional to AVDD (0.7 x AVDD).
Note 19. ADCMV bit = “1”. Input full-scale voltage is propotional to AVDD (0.86 x AVDD).
Note 20. AINM pin

6. DAC

(Ta=25°C; AVDD=VREFH=LVDD=TVDD=3.3V; AVSS=VREFL=DVSS1= DVSS2=0V;
SignalFrequency=1kHz; 32bit Data; BICK=64fs; Measurement Frequency BW=20Hz ~ 20kHz @fs=48kHz;Measurement Frequency BW=20Hz ~ 40kHz @fs=96kHz,192kHz)

	Parameter		Min.	Typ.	Max.	Unit
DAC1 DAC2 DAC3	Resolution				32	bit
	Output Voltage (Note 21)		2.55	2.83	3.11	Vpp
	S/(N+D) (0dBFS)	fs=48kHz	80	91		dB
		fs=96kHz		89		
		fs=192kHz		89		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
		fs=192kHz		101		
	S/N	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
		fs=192kHz		101		
	Inter-Channel Isolation (fin=1kHz) (Note 22)		90	110		dB
	Channel Gain Mismatch			0.0	0.7	dB
	Load Resistance (Note 23)		10			kΩ
	Load Capacitance				30	pF
	PSRR (Note 10)			50		dB

Note 21. Full-scale output Voltage. Output full-scale voltage is propotional to AVDD (0.86 x AVDD).
Note 22. Inter-channel isolation between each DAC of Lch and Rch with 0dBFS signal input. (AOUT1L and AOUT1R, AOUT2L and AOUT2R and AOUT3L and AOUT3R)
Note 23. to AC Load.

■ Power Consumption

(Ta=25°C; AVDD=VREFH=3.0~3.6V(typ=3.3V, max=3.6V); LVDD=3.0~3.6V(typ=3.3V, max=3.6V); TVDD=1.7~3.6V(typ=3.3V, max=3.6V); AVSS=VREFL=DVSS1=DVSS2=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operation Current Consumption (Note 24) (PDN pin= "H")	AVDD		30	43	mA
	LVDD		13.5	30	mA
	TVDD		5	8	mA
Power-down Current (PDN pin= "L")	AVDD		0.01		mA
	LVDD		0.01		mA
	TVDD		0.01		mA

Note 24. The current consumption of LVDD varies depending on the system frequency.

9. Digital Filter Characteristics

1. ADC Block

(Ta= 25°C; AVDD=VREFH=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=VREFL=DVSS1 =DVSS2=0V)

1-1 Sharp Roll-Off Filter (ADSD bit = "0", ADSL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 25)	0dB/-0.06dB	PB	0	-	22.1	kHz
	-3.0dB	PB	-	23.7	-	kHz
Stopband (Note 25)		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~20kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	20	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.0	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 25)	0dB/-0.06dB	PB	0	-	44.2	kHz
	-3.0dB	PB	-	47.5	-	kHz
Stopband (Note 25)		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	20	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 25)	0dB/-0.04dB	PB	0	-	83.7	kHz
	-3.0dB	PB	-	96.0	-	kHz
Stopband (Note 25)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	16	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.9	-	Hz

1-2 Slow Roll-Off Filter (ADSD bit = "0", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 25)	0dB/-0.074dB	PB	0	-	12.5	kHz
	-3.0dB		-	19.2	-	kHz
Stopband (Note 25)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~20kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	8	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.0	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 25)	0dB/-0.074dB	PB	0	-	25	kHz
	-3.0dB		-	38.5	-	kHz
Stopband (Note 25)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	8	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 25)	0dB/-0.1dB	PB	0	-	31.1	kHz
	-3.0dB		-	62.3	-	kHz
Stopband (Note 25)		SB	145.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 26)		GD	-	9	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.88	-	Hz

1-3 Short Delay Sharp Roll-Off Filter (ADSD bit = "1", ADSL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 25)	0dB/-0.06dB	PB	0	-	22.1	kHz
	-3.0dB		-	23.7	-	kHz
Stopband (Note 25)		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~20kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 26)		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.0	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 25)	0dB/-0.06dB	PB	0	-	44.2	kHz
	-3.0dB		-	47.5	-	kHz
Stopband (Note 25)		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 26)		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 25)	0dB/-0.04dB	PB	0	-	83.7	kHz
	-3.0dB		-	96.0	-	kHz
Stopband (Note 25)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	0	0.2	1/fs
Group Delay (Note 26)		GD	-	7	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.88	-	Hz

1-4 Short Delay Slow Roll-Off Filter (ADSD bit = "1", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 25)	0dB/-0.074dB	PB	0	-	12.5	kHz
	-3.0dB		-	19.2	-	kHz
Stopband (Note 25)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~20kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 26)		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.0	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 25)	0dB/-0.074dB	PB	0	-	25	kHz
	-3.0dB		-	38.5	-	kHz
Stopband (Note 25)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 26)		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 25)	0db/-0.1dB	PB	0	-	31.1	kHz
	-3.0dB		-	63.2	-	kHz
Stopband (Note 25)		SB	145.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion : 0Hz~40kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 26)		GD	-	7	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.88	-	Hz

Note 25. The passband and stopband frequencies are proportional to fs (sampling rate). High-pass filter characteristics are not included. A reference value of each passband and stopband frequency is the maximum value of frequency response.

Note 26. Delay time caused by the digital filter calculation. This time is measured from an impulse signal input until impulse data are set into the output register. It includes group delay by HPF.

2. DAC Block

(Ta=25°C; AVDD=VREFH=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=VREFL=DVSS1=DVSS2=0V)

2-1 Sharp Roll-Off Filter (DASD bit = "0", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 27)	±0.05dB	PB	0		21.7	kHz
	−3.0dB	PB		23.4		kHz
Passband Ripple (Note 28)		PR	-0.0032		0.0032	dB
Stopband (Note 27)		SB	26.3			kHz
Stopband Attenuation (Note 30, Note 31)		SA	80			dB
Group Delay (Note 29)		GD	-	27.3	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 20.0kHz			-0.3		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 27)	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Passband Ripple (Note 28)		PR	-0.0032		0.0032	dB
Stopband (Note 27)		SB	52.5	0		kHz
Stopband Attenuation (Note 30, Note 31)		SA	80			dB
Group Delay (Note 29)		GD	-	27.3	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 40.0kHz			-0.5		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 27)	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Passband Ripple (Note 28)		PR	-0.0032		0.0032	dB
Stopband (Note 27)		SB	105			kHz
Stopband Attenuation (Note 30, Note 31)		SA	80			dB
Group Delay (Note 29)		GD	-	27.3	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 80.0kHz			-1.9		0.1	dB

Note 27. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB=0.4535 × fs, SB=0.546 × fs"

Note 28. Pass-band gain amplitude of double seep over sampling filter at the first step of Interpolator.

Note 29. Delay time caused by the digital filter calculation. This time is measured from setting of the 16/20/24/32-bit impulse data to the input registers to output of the analog peak signal.

Note 30. The output level with a 1kHz, 0dB sine wave input is defined as 0dB.

Note 31. Band width of Stopband Attenuation ranges from 0kHz to fs.

2-2 Slow Roll-Off Filter (DASD bit = "0", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 32)	±0.05dB	PB	0		8.8	kHz
	−3.0dB	PB		19.8		kHz
Passband Ripple (Note 28)		PR	-0.043		0.043	dB
Stopband (Note 32)		SB	42.7			kHz
Stopband Attenuation (Note 30, Note 31)		SA	73			dB
Group Delay (Note 29)		GD	-	6.8	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 20.0kHz			-5.0		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 32)	±0.05dB	PB	0		17.7	kHz
	−3.0dB	PB		39.5		kHz
Passband Ripple (Note 28)		PR	-0.043		0.043	dB
Stopband (Note 32)		SB	85.3			kHz
Stopband Attenuation (Note 30, Note 31)		SA	73			dB
Group Delay (Note 29)		GD	-	6.8	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 40.0kHz			-5.2		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband (Note 32)	±0.05dB	PB	0		35.5	kHz
	−3.0dB	PB		79.0		kHz
Passband Ripple (Note 28)		PR	-0.043		0.043	dB
Stopband (Note 32)		SB	171			kHz
Stopband Attenuation (Note 30, Note 31)		SA	73			dB
Group Delay (Note 29)		GD	-	6.8	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 80.0kHz			-5.90		0.1	dB

Note 32. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB=0.185 × fs, SB=0.888 × fs"

2-3 Short Delay Sharp Roll-Off Filter (DASD bit = "1", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 27)	±0.05dB	PB	0		21.7	kHz
	–3.0dB	PB		23.4		kHz
Passband Ripple (Note 28)		PR	-0.0031		0.0031	dB
Stopband (Note 27)		SB	26.3			kHz
Stopband Attenuation (Note 30, Note 31)		SA	80			dB
Group Delay (Note 29)		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 20.0kHz			-0.3		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 27)	±0.05dB	PB	0		43.5	kHz
	–3.0dB	PB		46.8		kHz
Passband Ripple (Note 28)		PR	-0.0031		0.0031	dB
Stopband (Note 27)		SB	52.5	0		kHz
Stopband Attenuation (Note 30, Note 31)		SA	80			dB
Group Delay (Note 29)		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 40.0kHz			-0.5		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband (Note 27)	±0.05dB	PB	0		87.0	kHz
	–3.0dB	PB		93.6		kHz
Passband Ripple (Note 28)		PR	-0.0031		0.0031	dB
Stopband (Note 27)		SB	105			kHz
Stopband Attenuation (Note 30, Note 31)		SA	80			dB
Group Delay (Note 29)		GD	-	6.3	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 80.0kHz			-1.9		0.1	dB

9.4 Short Delay Slow Roll-Off Filter (DASD bit = "1", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 33)	±0.05dB	PB	0		12.0	kHz
	−3.0dB	PB		21.1		kHz
Passband Ripple (Note 28)		PR	-0.05		0.05	dB
Stopband (Note 33)		SB	41.5			kHz
Stopband Attenuation (Note 30, Note 31)		SA	82			dB
Group Delay (Note 29)		GD	-	5.3	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 20.0kHz			-4.8		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 33)	±0.05dB	PB	0		24.2	kHz
	−3.0dB	PB		42.1		kHz
Passband Ripple (Note 28)		PR	-0.05		0.05	dB
Stopband (Note 33)		SB	83.0			kHz
Stopband Attenuation (Note 30, Note 31)		SA	82			dB
Group Delay (Note 29)		GD	-	5.3	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 40.0kHz			-5.0		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband (Note 33)	±0.05dB	PB	0		48.4	kHz
	−3.0dB	PB		84.3		kHz
Passband Ripple (Note 28)		PR	-0.05		0.05	dB
Stopband (Note 33)		SB	165.9			kHz
Stopband Attenuation (Note 30, Note 31)		SA	82			dB
Group Delay (Note 29)		GD	-	5.3	-	1/fs
Digital Filter + SCF + SMF (Note 30)						
Frequency Response: 0 ~ 80.0kHz			-5.7		0.1	dB

Note 33. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB=0.252 × fs, SB=0.864 × fs"

10. DC Characteristics

■ **DC Characteristics**

(Ta=-40~85°C; AVDD=VREFH=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=VREFL=DVSS1=DVSS2=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage 1 (Note 34)		VIH1	80%TVDD			V
Low-Level Input Voltage 1 (Note 34)		VIL1			20%TVDD	V
High-Level Input Voltage 2 (Note 35)		VIH2	70%TVDD			V
Low-Level Input Voltage 2 (Note 35)		VIL2			30%TVDD	V
High-Level Output Voltage Iout= -100μA (Note 34)		VOH1	TVDD-0.3			V
Low-Level Output Voltage Iout=100μA (Note 34)		VOL1			0.3	V
SDA Low Level Output Voltage	Fast Mode					
	TVDD ≥ 2.0V (Iout=3mA)	VOL2			0.4	V
	TVDD < 2.0V (Iout=3mA)	VOL2			20%TVDD	V
	Fast Mode Plus					
	TVDD ≥ 2.0V (Iout=20mA)	VOL2			0.4	V
	TVDD < 2.0V (Iout=3mA)	VOL2			20%TVDD	V
Input Leak Current (Note 36)		Iin			±10	μA

Note 34. CLKO, SDIN1, SDIN2, BICK2/SDIN3, SDOUT1, SDOUT2, LRCK2/SDOUT3, LRCK1, BICK1, PDN, SCLK, SO, CSN and SI/I2CFIL pins.

Note 35. SCL and SDA pins.

Note 36. SDIN1, SDIN2, SDIN3, PDN, SCLK/SCL, SO/SDA, CSN and SI/I2CFIL pins.

11. Switching Characteristics

1. System Clock

(Ta=-40~85°C; AVDD=VREFH=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=VREFL=DVSS1=DVSS2=0V; CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCKI Input Timing					
Duty Cycle	Duty	40	50	60	%
Input Frequency	fCLK	0.256		24.576	MHz
CLKO Output Timing					
Output Frequency	fCLKO	2.048		24.576	MHz
Duty Cycle	dCLKO		50		%
LRCK/BICK Input Timing (Slave Mode)					
LRCK Input Timing					
Frequency	fs	8		192	kHz
BICK Input Timing					
Frequency (Note 37)	fBCLK	0.256		24.576	MHz
Pulse Width Low	tBCLKL	0.4 / fBCLK			ns
Pulse Width High	tBCLKH	0.4 / fBCLK			ns
LRCK/BICK Output Timing (Master Mode)					
LRCK Output Timing					
Frequency	fs	8		192	kHz
Pulse Width High PCM Short/Long Frame I^2S/DSP Mode	 tLRCKH tLRCKH		 1/fBCLK 50		 ns %
BICK Output Timing					
Frequency (Note 37)	fBCLK	0.256		24.576	MHz
Duty	dBCLK		50		%

Note 37. Required to meet the following expression: “fBCLK ≥ 2 x fs x (Input/Output Data Length)”

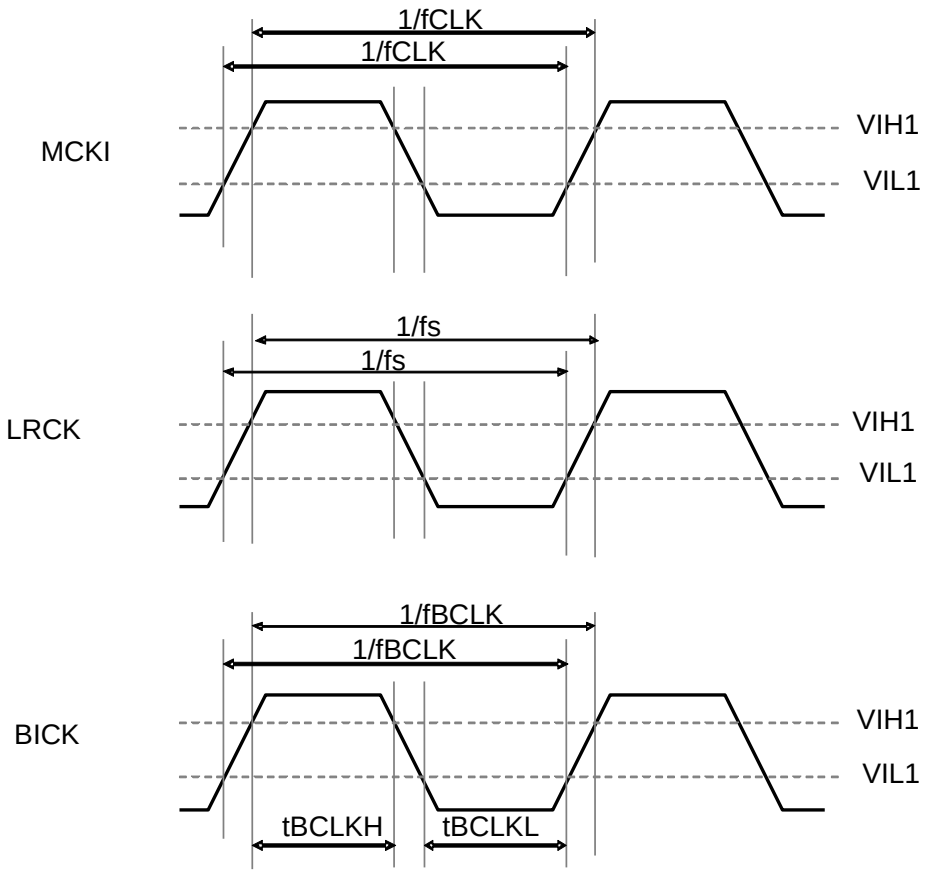


Figure 2. System Clock Timing

2. Power Down

(Ta=-40~85°C; AVDD=VREFH=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=VREFL=DVSS1=DVSS2=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width (Note 38)	tRST	600			ns

Note 38. The PDN pin must be “L” when power up the AK4601.

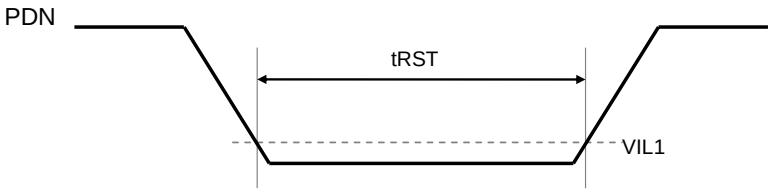


Figure 3. Reset Timing

3. Serial Data Interface (SDINx, SDOUTx)

(Ta=-40~85°C; AVDD=VREFH=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=VREFL=DVSS1=DVSS2=0V; CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK (Note 39)	tBLRD	10			ns
Delay Time from LRCK to BICK "↑" (Note 39)	tLRBD	10			ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	5			ns
Delay Time from BICK"↓"to Serial Data Output (Note 40)	tBSOD1			20	ns
Delay Time from BICK "↑"to Serial Data Output (Note 39, Note 41)	tBSOD2	5		30	ns
Master Mode					
BICK Frequency	fBCLK		32, 48, 64, 128, 256, 512		fs
BICK Duty Cycle	Duty		50		%
Delay Time from BICK "↓" to LRCK (Note 40)	tMBL	-10		10	ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	10			ns
Delay Time from BICK"↓"to Serial Data Output (Note 40, Note 41)	tBSOD			10	ns

Note 39. It is measured from BICK "↓" when the BICK polarity is inverted by setting BCKPx bit = "1".
Note 40. It is measured from BICK "↑" when the BICK polarity is inverted by setting BCKPx bit = "1".
Note 41. Set SDOPHx bit to "1" and the data from SDOUTx pin should be output based on BICK "↑" when BICKx speed is more than 12.288MHz such as TDM512 mode with 48kHz sampling frequency, TDM256 mode with 96kHz sampling frequency or TDM128 mode with 192kHz sampling frequency in slave mode. SDOPHx bit must be set to "0" in master mode.

3-1. Slave Mode

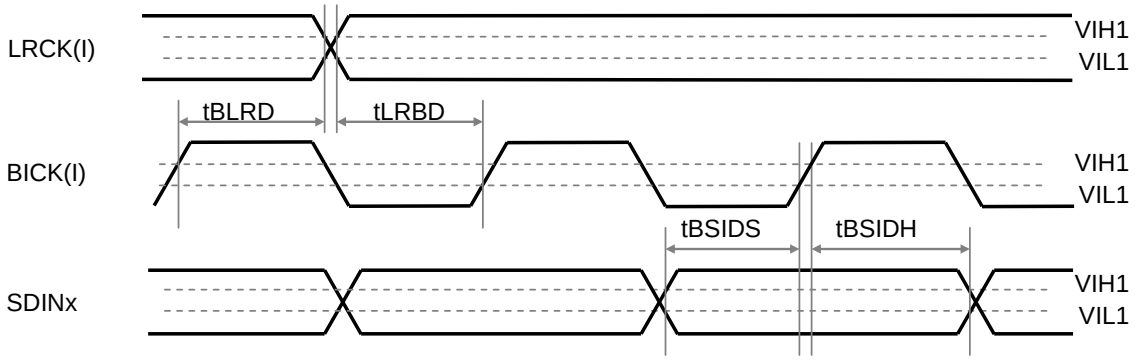


Figure 4. Serial Interface Input Timing in Slave Mode

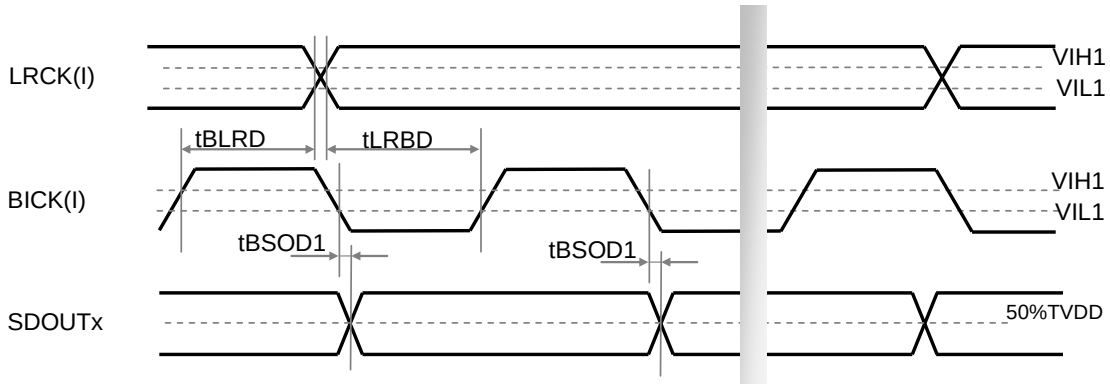


Figure 5. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “0”)

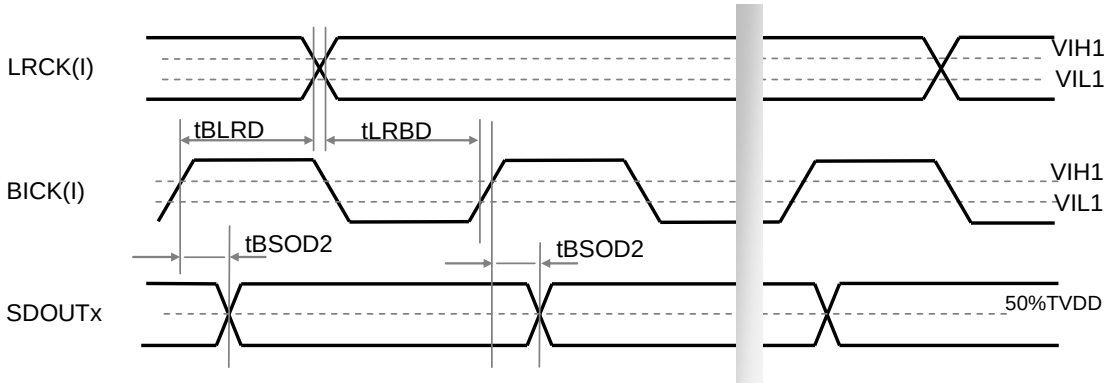


Figure 6. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “1”)

3-2. Master Mode

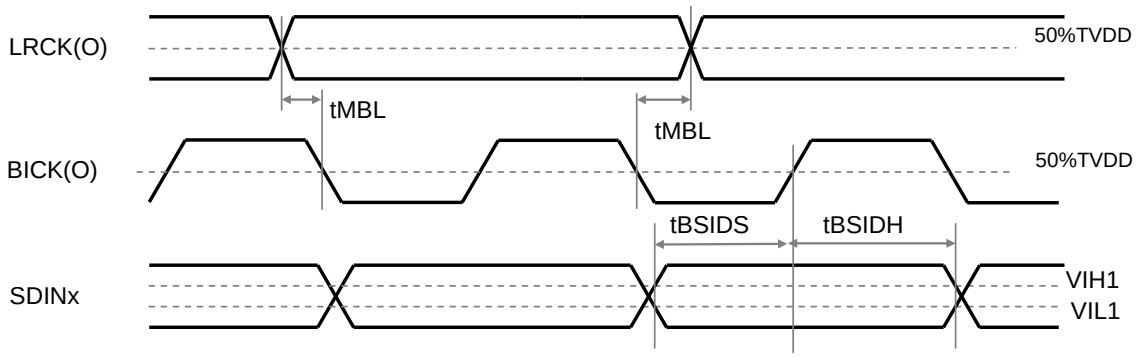


Figure 7. Serial Interface Input Timing in Master Mode

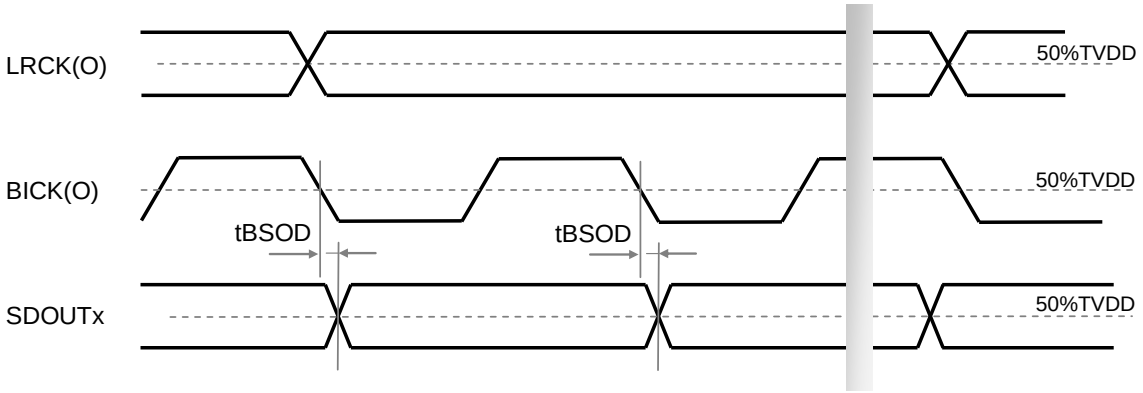


Figure 8. Serial Interface Output Timing in Master Mode

4. SPI Interface

(Ta=-40~85°C; AVDD=VREFH=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=VREFL=DVSS1=DVSS2=0V; CL=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency	fSCLK			7	MHz
SCLK Low-level Width	tSCLKL	60			ns
SCLK High-level Width	tSCLKH	60			ns
Microcontroller → AK4601					
CSN High-level Width	tWRQH	150			ns
From CSN "↑" to PDN "↑"	tRST	180			ns
From PDN "↑" to CSN "↓"	tIRRQ	1			ms
From CSN "↓" to SCLK "↓"	tWSC	150			ns
From SCLK "↑" to CSN "↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	20			ns
SI Latch Hold Time	tSIH	20			ns
AK4601 → Microcontroller					
Delay Time from SCLK "↓" to SO Output	tSOS			40	ns

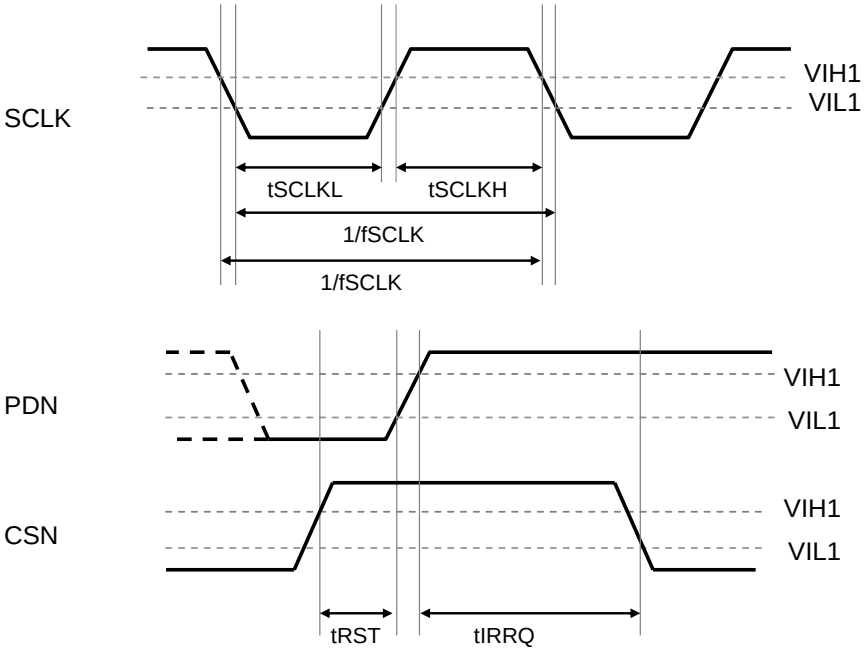


Figure 9. SPI Interface Timing1

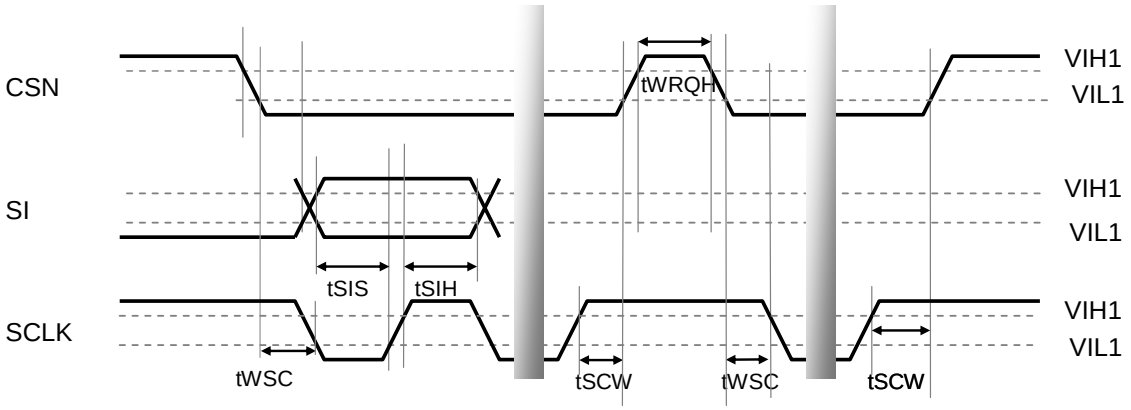


Figure 10. SPI Interface Timing 2 (Microcontroller→ AK4601)

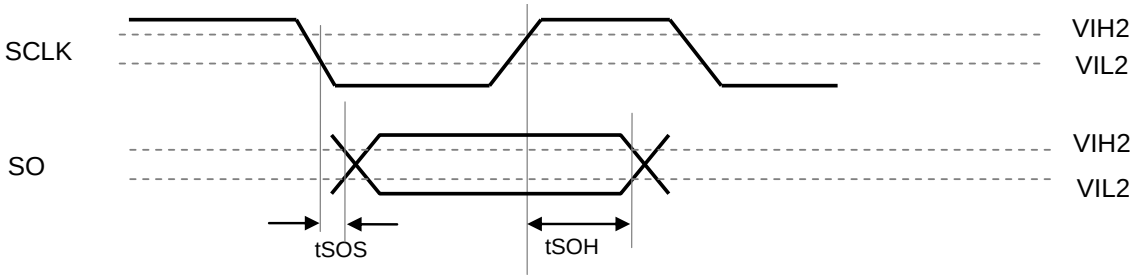


Figure 11. SPI Interface Timing 3 (AK4601 → Microcontroller)

5. I²C Interface

(Ta=-40~85°C; AVDD=VREFH=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=VREFL=DVSS1 =DVSS2=0V)

<I²C: Fast Mode>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0			µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

<I²C: Fast Mode Plus>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL			1	MHz
Bus Free Time Between Transmissions	tBUF	0.5			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.26			µs
Clock Low Time	tLOW	0.5			µs
Clock High Time	tHIGH	0.26			µs
Setup Time for Repeated Start Condition	tSU:STA	0.26			µs
SDA Hold Time from SCL Falling	tHD:DAT	0			µs
SDA Setup Time from SCL Rising	tSU:DAT	0.05			µs
Rise Time of Both SDA and SCL Lines	tR			0.12	µs
Fall Time of Both SDA and SCL Lines	tF			0.12	µs
Setup Time for Stop Condition	tSU:STO	0.26			µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			550	pF

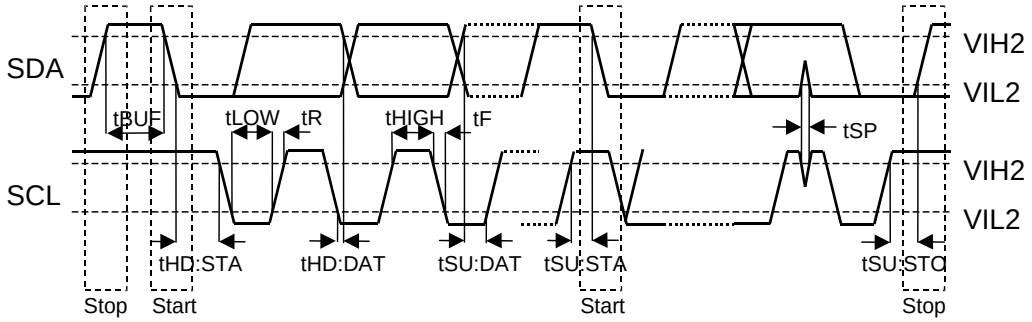


Figure 12. I²C BUS Interface Timing

12. Functional Descriptions

■ System Clock

1. Clock Mode

The AK4601 has a PLL circuit to generate an internal operation clock. An input pin for the PLL reference clock is selected by REFSEL[2:0] bits (Table 4). REFMODE[4:0] bits set the frequency of the reference clock (Table 5). A reference clock input pin and the reference clock frequency must be changed during clock reset.

REFSEL[2:0] bits	Reference Clock	
000	MCKI pin	(default)
001	BICK1 pin	
010	BICK2 pin	
Others	N/A	

Table 4. PLL Reference Clock Frequency Setting

REFMODE[4:0] bits	Input Frequency (kHz)		
	48kHz base	44.1kHz base	
00000	256	235.2	(default)
00001	384	352.8	
00010	512	470.4	
00011	768	705.6	
00100	1,024	940.8	
00101	1,152	1,058.4	
00110	1,536	1,411.2	
00111	2,048	1,881.6	
01000	2,304	2,116.8	
01001	3,072	2,822.4	
01010	4,096	3,763.2	
01011	4,608	4,233.6	
01100	6,144	5,644.8	
01101	8,192	7,526.4	
01110	9,216	8,467.2	
01111	12,288	11,289.6	
10000	18,432	16,934.4	
10001	24,576	22,579.2	
Others	N/A	N/A	

Table 5. Reference Clock Frequency Setting

The PLL block multiplies a input clock which is set by REFMODE[4:0] bits directly and generates a 122.88MHz/112.896MHz master clock (PLL_MCLK) for internal operation (Table 6).

Master Clock (PLL_MCLK)	48kHz base	44.1kHz base
	122.88MHz	112.896MHz

Table 6. Internal Operation Master Clock

A stable BICK is required when using clock input from BICKx (x=1~2) pin as reference clock. A clock with two different frequencies cannot be used. The MCKI pin must be put to “L” (DVSS1) if the system does not need the MCKI pin.

2. Audio HUB

2-1 Audio HUB

Audio HUB provides simultaneous data transmitting and flexible path configuration for various audio sources by setting sample rate converters, Input/Output port that supports TDM mode and registers. Therefore the AK4601 is able to support to various use cases of car-audio systems.

Figure 13 shows an example of when using audio play-back and hands-free talk at the same time in a car audio system.
With the AK7707, AKM's multi-core DSP, the AK4601 realizes simultaneous processing of data in different sampling rates such as microphone input ADC data and Radio tuner audio data.

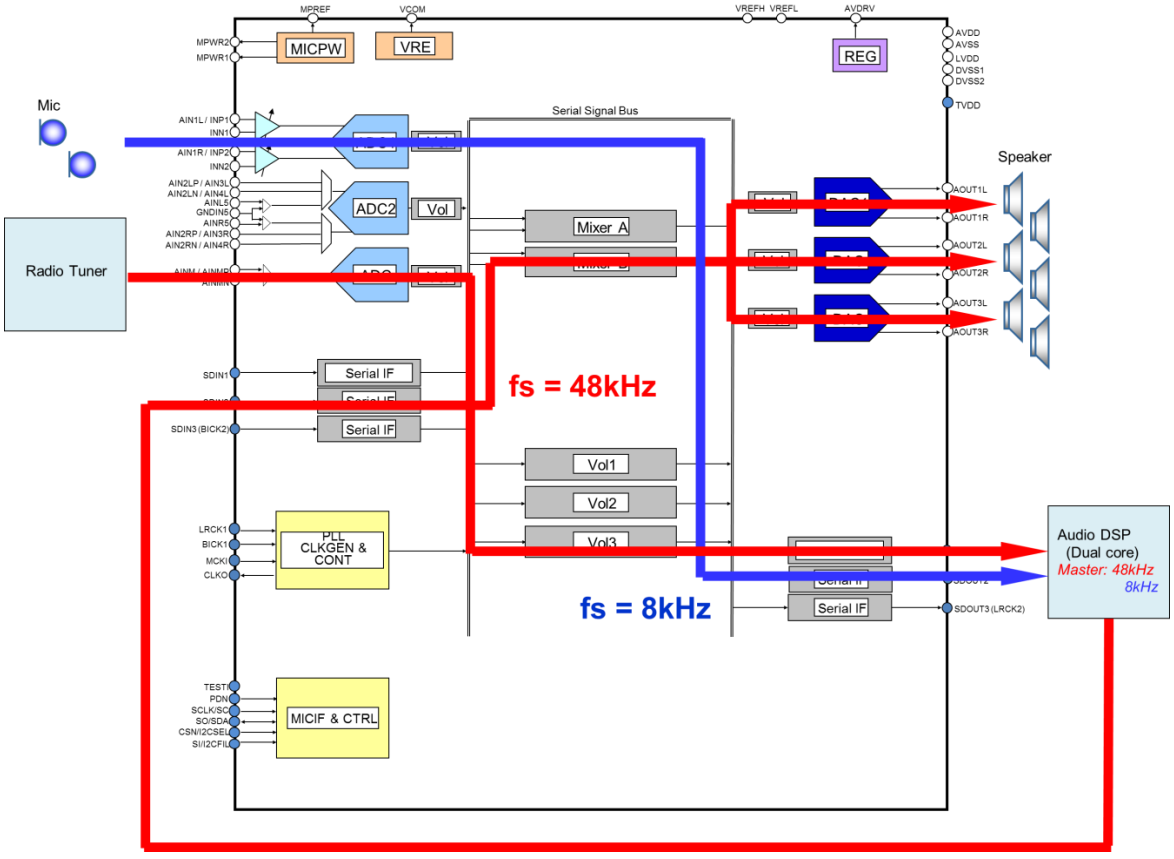


Figure 13. Audio HUB Example

2-2. Clock Sync Domain

The AK4601 has two Clock Sync Domains (SD1-2). Reference clocks (LRCKSDx, BICKSDx, x=1~2)are output according to each register settings for SD1-2 (Figure 14). The internal audio data and input/output data of the AK4601 must be synchronized with one of these two Clock Sync Domains.

When MSNx bit =“0”, input pins (LRCKx pin/BICKx pin) are selected for the clock sync reference clock. When MSNx bit = “1”, internal dividing clocks (MLRCKx/MBICKx) are selected for the clock sync reference clock (Table 7).

MSNx bit	Reference Clock (LRCKSDx/BICKSDx)
0	Input Pin (LRCKx pin/BICKx pin)
1	Internal Dividing Clock (MLRCKx/MBICKx) Reference clock is generated internally by CKSx[2:0], BDVx[8:0] and SDVx[2:0] bits settings.

Table 7. Reference Clock of Clock Sync Domain

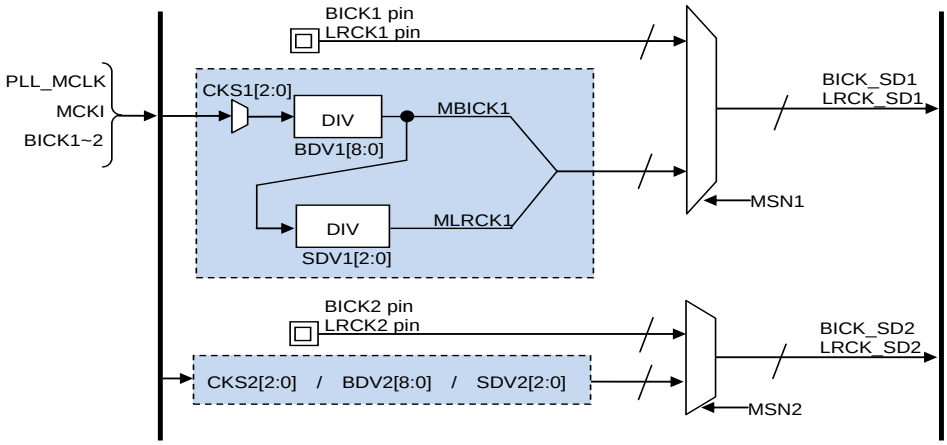


Figure 14. Clock Sync Domain

The clock source of Internal dividing clock MBICKx is selected by CKSx[2:0] bits (Table 8). MBICKx is generated by dividing the selected clock source according to the BDVx[8:0] bits setting (Table 9). Additionally, MLRCKx is generated by dividing this MBICKx by setting SDVx[2:0] bits (Table 8).

CKSx[2:0] bits	Clock Source	
000	TieLow	(default)
001	PLL MCLK	
010	MCKI	
011	BICK1	
100	BICK2	
Others	N/A	

Table 8. Clock Source of Internal Dividing Clock

BDVx[8:0] bits	Divide by	
0x00	1	(default)
0x01 – 0xFF	BDVx+1	

Table 9. MBICKx Setting

SDVx[2:0] bits	Divide by	
000	64	(default)
001	48	
010	32	
011	128	
100	256	
101	N/A	
110	N/A	
111	512	

Table 10. MLRCKx Setting (N/A: Not available)

Clock Sync Domain settings when PLL MCLK is selected as the clock source are shown in Table 11.

PLL MCLK = 122.88MHz (48kHz base) / 112.896MHz (44.1kHz base)
MBICKx = PLL MCLK dvided by BDVx[8:0] bits setting
MLRCKx = MBICKx divided by SDVx[2:0] bits setting

e.g.) MBICKx= 122.88MHz/240= 0.512MHz, MLRCKx= 0.512MHz/64= 8kHz when PLL_MCLK = 122.88MHz (fs=48kHz), BDVx[8:0] bits= “0xEF”(divide by 240) and SDVx[2:0] bits = “000” (divide by 64).

When PLL_MCLK is selected as the clock source, frequency settings other than shown in Table 11 are not available.

BDVx[8:0] bits	BDVx[8:0] bits Dividing	MBICKx(MHz)		SDVx[2:0] bits	SDVx[2:0] bits Dividing	MLRCKx(kHz)	
		48kHz base	44.1kHz base			48kHz base	44.1kHz base
0x1DF	480	0.256	0.2352	010	32	8	-
0x13F	320	0.384	0.3528	001	48	8	-
0x0EF	240	0.512	0.4704	000	64	8	-
0x077	120	1.024	0.9408	011	128	8	-
0x03B	60	2.048	1.8816	100	256	8	-
0x01D	30	4.096	3.7632	111	512	8	-
0x13F	320	0.384	0.3528	010	32	12	11.025
0x09F	160	0.768	0.7056	000	64	12	11.025
0x04F	80	1.536	1.4112	011	128	12	11.025
0x027	40	3.072	2.8224	100	256	12	11.025
0x013	20	6.144	5.6448	111	512	12	11.025
0x0EF	240	0.512	0.4704	010	32	16	14.7
0x09F	160	0.768	0.7056	001	48	16	14.7
0x077	120	1.024	0.9408	000	64	16	14.7
0x03B	60	2.048	1.8816	011	128	16	14.7
0x01D	30	4.096	3.7632	100	256	16	14.7
0x00E	15	8.192	7.5264	111	512	16	14.7
0x09F	160	0.768	0.7056	010	32	24	22.050
0x04F	80	1.536	1.4112	000	64	24	22.050
0x027	40	3.072	2.8224	011	128	24	22.050
0x013	20	6.144	5.6448	100	256	24	22.050
0x009	10	12.288	11.2896	111	512	24	22.050
0x077	120	1.024	0.9408	010	32	32	29.4
0x04F	80	1.536	1.4112	001	48	32	29.4
0x03B	60	2.048	1.8816	000	64	32	29.4
0x01D	30	4.096	3.7632	011	128	32	29.4
0x00E	15	8.192	7.5264	100	256	32	29.4
0x04F	80	1.536	1.4112	010	32	48	44.1
0x027	40	3.072	2.8224	000	64	48	44.1
0x013	20	6.144	5.6448	011	128	48	44.1
0x009	10	12.288	11.2896	100	256	48	44.1
0x004	5	24.576	22.5792	111	512	48	44.1
0x027	40	3.072	2.8224	010	32	96	88.2
0x013	20	6.144	5.6448	000	64	96	88.2
0x009	10	12.288	11.2896	011	128	96	88.2
0x004	5	24.576	22.5792	100	256	96	88.2
0x013	20	6.144	5.6448	010	32	192	176.4
0x009	10	12.288	11.2896	000	64	192	176.4
0x004	5	24.576	22.5792	011	128	192	176.4

Table 11. Clock Sync Domain Setting when PLL MCLK is Clock Source

For Clock Sync Domain, set BDVx[8:0] bits and SDVx[2:0] bits according to the input clock frequency when the MCKI or BICK pin input is selected as the clock source, as well as the PLL MCLK.

MBICKx= MCKI pin or BICKx pin frequency divided by BDVx[8:0] bits setting
MLRCKx= MBICKx divided by SDVx[2:0] bits setting

2-3. Sampling Frequency Setting of ADC, DAC Blocks

The ADC, DAC blocks of the AK4601 are operated by a master clock generated by dividing PLL MCLK. Sampling frequencies of the ADC1, and the ADC2, ADCM, DAC1, DAC2 and DAC3 (hereinafter called CODEC) are set by FSMODE[4:0] bits (Table 12).

Mode	FSMODE[4:0] bits	ADC2, ADCM DAC1, DAC2, DAC3	ADC1	
0	00000	8kHz	8kHz	(default)
1	00001	12kHz	12kHz	
2	00010	16kHz	16kHz	
3	00011	24kHz	24kHz	
4	00100	32kHz	32kHz	
5	00101	32kHz	16kHz	
6	00110	32kHz	8kHz	
7	00111	48kHz	48kHz	
8	01000	48kHz	24kHz	
9	01001	48kHz	16kHz	
10	01010	48kHz	8kHz	
11	01011	96kHz	96kHz	
12	01100	96kHz	48kHz	
13	01101	96kHz	32kHz	
14	01110	96kHz	24kHz	
15	01111	96kHz	16kHz	
16	10000	96kHz	8kHz	
17	10001	192kHz	192kHz	
18	10010	192kHz	96kHz	
19	10011	192kHz	48kHz	
20	10100	192kHz	32kHz	
21	10101	192kHz	16kHz	

Table 12. Sampling Frequency Settings of Internal Blocks (fs=48kHz base)

Clock Sync Domain of the ADC1 (SDADC1) is selected by SDADC1[2:0] bits and Clock Sync Domain of the CODEC (SDCODEC) is selected by SDCODEC[2:0] bits (Figure 20). SDADC1 and SDCODEC must be synchronized with PLL MCLK. The sampling frequency of LRCK SDx for SDADC1 and the sampling frequency of the ADC1 should be the same. The sampling frequency of LRCK SDx for SDCODEC and the sampling frequency of the CODEC should also be the same.

Set SDADC1[2:0] bits = “000” (Reference Clocks are Low) when not using the ADC1. In the same manner, SDCODEC[2:0] bits must be set to “000” (Reference Clocks are Low) when not using the CODEC.

e.g.) Input pin is selected for PLL Reference Clock.

• PLL Setting
REFSEL[2:0] bits = “010” (PLL Reference Clock is set to BICK2 pin=3.072MHz)

• Clock Sync Domain Setting
SDADC1[2:0] bits = “001”, SDCODEC[2:0] bits = “002”, MSN1 bit = MSN2 bit = “0”,
BICK_SD1 = BICK1 pin = 64fs (0.512MHz), LRCK_SD1 = LRCK1 pin = 8kHz
BICK_SD2 = BICK2 pin = 64fs (3.072MHz),LRCK_SD2 = LRCK2 pin = 48kHz

• ADC1 and CODEC Setting
FSMODE[4:0] bits=” 01010” (Set fs = 8kHz for ADC1, Set CODEC, fs = 48kHz)

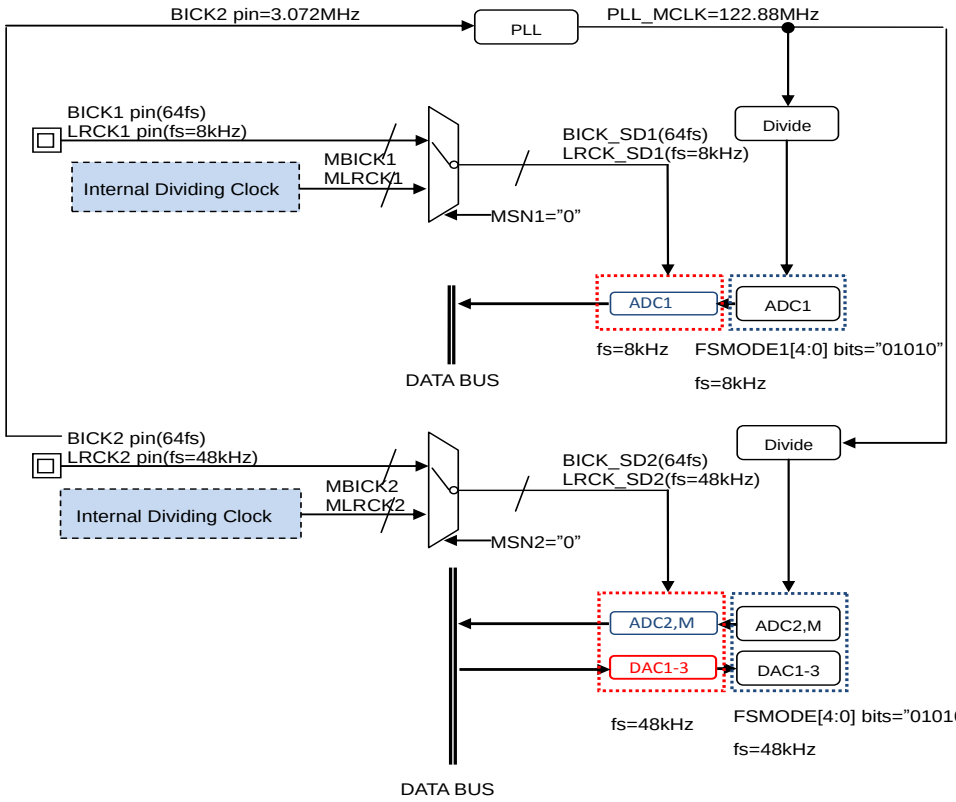


Figure 15. ADC, DAC Setting Example (MSNx bit = “0”: Input pin is selected as PLL Reference Clock)

Note 42. BICK1/LRCK1 and BICK2/LRCK2 must be synchronized.

e.g.) Internal Dividing Clock is Selected as PLL Reference Clock

• PLL Setting
REFSEL[2:0] bits = “000” (PLL Reference Clock is MCKI pin = 3.072MHz), PLL MCLK = 122.88MHz

• Clock Sync Domain Setting
SDADC[2:0] bits = “001”, SDCODEC[2:0] bits = “002”, MSN1 bit = MSN2 bit = “1”,
CKS1[2:0] = “001” (PLL MCLK is set as the reference clock of Clock Sync Domain 1)
BDV1[8:0] = “0x0EF” (BICK SD1 = MBICK1 = 122.88MHz/240 = 0.512MHz)
SDV1[2:0] = “000” (LRCK SD1 = MLRCK1 = 0.512MHz/64 = 8kHz)
CKS2[2:0] = “001” (PLL MCLK is set as the reference clock of Clock Sync Domain 2)
BDV2[8:0] = “0x027” (BICK SD2 = MBICK2 = 122.88MHz/40 = 3.072MHz)
SDV2[2:0] = “000” (LRCK SD2 = MLRCK2 = 3.072MHz/64 = 48kHz)

• ADC1 and CODEC Setting
FSMODE[4:0] bits= “01010” (Set fs = 8kHz for ADC1, Set CODEC, fs = 48kHz)

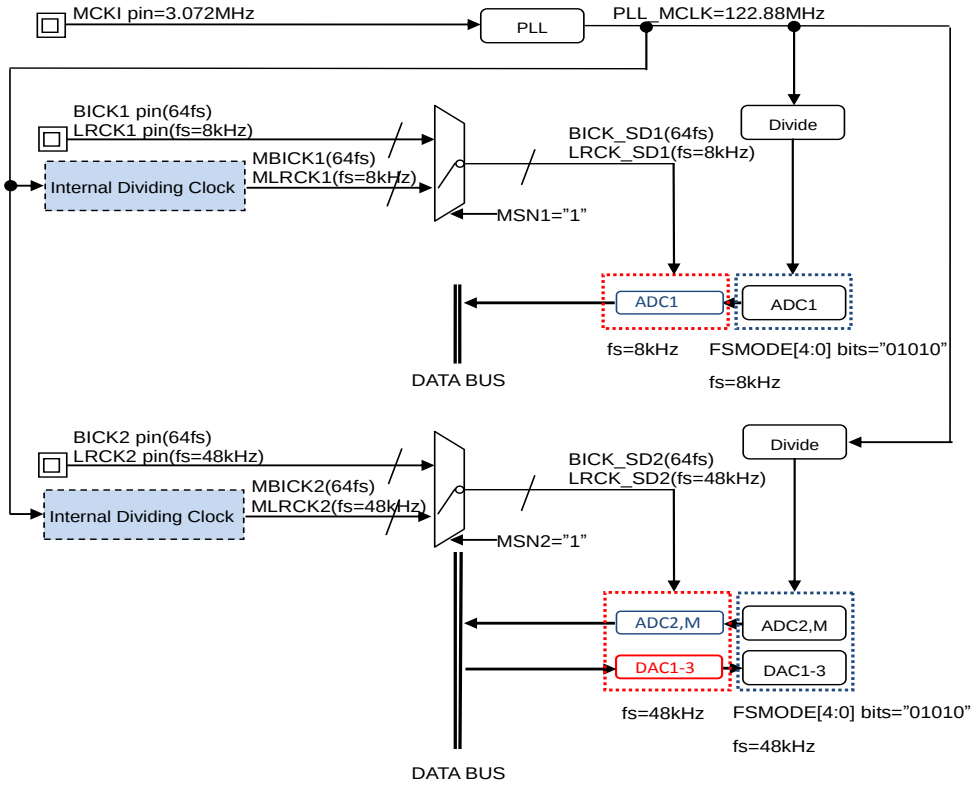


Figure 16. ADC, DAC, Setting Example
(MSNx bit = “1”: Internal Dividing Clock is Selected as PLL Reference Clock)

2-4. CLKO Pin Output Clock

The CLKO pin of the AK4601 outputs a divided clock of PLL MCLK. The output frequency setting of the CLKO pin is controlled by CLKOSEL[2:0] bits (Table 13).

CLKOSEL[2:0] bits	Output Frequency (fs=48kHz base)	Output Frequency (fs=44.1kHz base)	
000	12.288MHz	11.2896MHz	(default)
001	24.576MHz	22.5792MHz	
010	8.192MHz	7.5264MHz	
011	6.144MHz	5.6448MHz	
100	4.096MHz	3.7632MHz	
101	2.048MHz	1.8816MHz	

Table 13. CLKO Pin Setting

2-5. BICK2/SDIN3 pin and LRCK2/SDOUT3 pin Settings

Pin functions of the BICK2/SDIN3 pin and the LRCK2/SDOUT3 pin are selected by MSELN bit. When MSELN bit is “0”, the BICK2/SDIN3 pin works as the BICK2 pin and the LRCK2/SDOUT3 pin works as the LRCK2 pin. When MSELN bit is “1”, the BICK2/SDIN3 pin works as the SDIN3 pin and the LRCK2/SDOUT3 pin works as the SDOUT3 pin.

MSELN bit	Function	
0	BICK2	(default)
1	SDIN3	

Table 14. BICK2/SDIN3 Pin Setting 1

2-6. SDINx/BICKx/LRCKx Pin Setting

The AK4601 has three SDIN pins and two BICK/LRCK pins. They are independent each other. Synchronized channel of the SDINx pin can be selected by EXBCKx[2:0] bits from BICKx pin and LRCKx pin (Table 15).

EXBCKx[2:0] bits	BICK and LRCK pins that synchronizes to SDINx pin	
000	TieLow	(default)
001	BICK1 pin, LRCK1 pin	
010	BICK2 pin, LRCK2 pin	
011	N/A	
100		
101		
110		
111		

Table 15. BICKx/LRCKx pin Setting for Synchronization to SDINx pin

MSNx bit selects Master/Slave mode of the BICKx pin and the LRCKx pin. (Table 16)

MSNx bit	BICKx pin, LRCKx pin	
0	Slave Mode (Input)	(default)
1	Master Mode (Output)	

Table 16. BICKx pin/LRCKx pin Mode Select

Note 43. Set MSNx bit to “0” when using the BICKx pin as PLL reference clock input pin.

When MSELN bit = “1”, the BICK2/SDIN3 pin works as SDIN3 (Input) even setting MSN2 bit to “1”, and the LRCK2/SDOUT3 pin works as SDOUT3 (Output) even setting MSN2 bit to “0”.

MSELN bit	MSN2 bit	Function		
0	0	BICK2 (Slave mode, Input)	LRCK2 (Slave mode, Input)	(default)
0	1	BICK2 (Master mode, Output)	LRCK2 (Master mode, Output)	
1	0	SDIN3 (Input)	SDOUT3 (Output)	
1	1			

Table 17. BICK2/SDIN3 Pin Setting 2

When BICKx/LRCKx (x=1~2) pin is set to Slave mode, the reference clock of Clock Sync Domain x is the BICKx/LRCKx pin (Table 7).When BICKx/LRCKx pin is set to Master mode, the output clock of the BICKx/LRCKx pin can be selected from two Sync Domains by SDBCKx[2:0] bits (x= 1~2). (Table 18)

MSNx bit	SDBCKx[2:0] bits	BICKx pin/LRCKx pin	
1	000	TieLow	
1	001	BICK SD1, LRCK SD1	
1	010	BICK SD2, LRCK SD2	
1	011	N/A	
1	100		
1	101		
1	110		
1	111		
0	xxx	Input	(default)

Table 18. Clock Sync Domain Setting of BICKx/LRCKx Pin

■ Data Path Setting

1. Data Bus, In/Output Port

The AK4601 has a 32-bit serial audio stereo data bus (Figure 17). Inputs and outputs of each internal block and all input/output pins of the AK4601 are connected to this serial audio data bus. The port that data is input to this serial audio data bus is defined as “input port” and the port that data is output from the audio data bus is defined as “output port”. Each port selects Clock Sync Domain and inputs (outputs) audio data that synchronized to the reference clock of the Clock Sync domain to the data bus (Figure 17).

A stereo data on each port is defined as “data source”. All data sources are connected to the serial audio bus and a data source on any input port can be output from any output port. Data connection of the data bus and a data port with the same sampling frequency is defined as “data path”. Input and output ports on the same data path should have the same Clock Sync Domain. If these ports have different Clock Sync Domains, reference clocks (BICK SDx, LRCK SDx) must be synchronized and the sampling frequency must be the same. Phase synchronization of reference clocks is not necessary if the frequency of these clocks are synchronized. However, frequencies of BICK SDx can be different.
An SRC is necessary for data transmission between two ports that have clock sync domain with different sampling frequencies or different reference clocks.

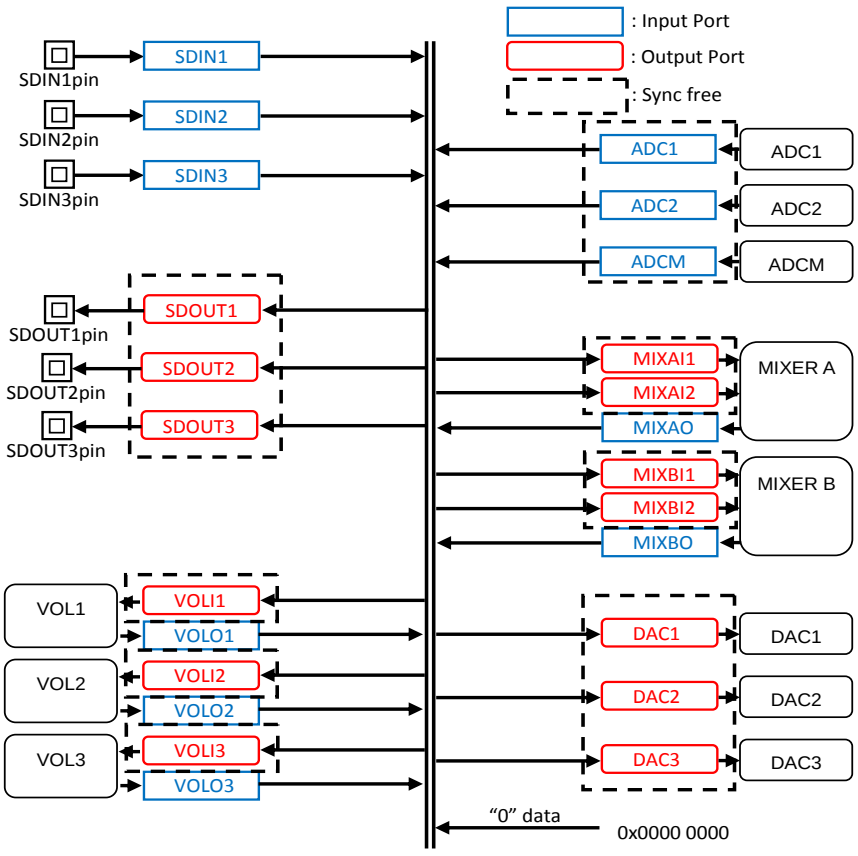


Figure 17. Data Path, Input/Output Port

1-1. Data BUS Group Delay

2*(1/fs) group delay occurs in total as audio data will have group delay of 1*(1/fs) at each input and output port of the data bus that have the same sync domain. Therefore, this group delay will increase as the number of times that the data go through the data path increases.

2. Clock Sync Domain Setting for Input/Output Port

Domain numbers are assigned to each Clock Sync Domain (Table 19). Each input/output port has setting registers for Clock Sync Domain (Figure 20).

Set a domain number to clock sync domain setting registers for each input/output port. (Table 20, Table 21)

Domain Number	Clock Sync Domain	
0x0	Reference Clocks are Low	(default)
0x1	SD1 (BICK SD1, LRCK SD1)	
0x2	SD2 (BICK SD2, LRCK SD2)	

Table 19. Clock Sync Domain Number

If the output port sync domain setting is in auto mode, an audio data port inherits the sync domain of the input data.

Clock Sync Domain of the SDINx pin is automatically selected by setting EXBCKx[2:0] bits, MSN bit and SDBCKx[2:0] bits (Table 15, Table 16, Table 18).

e.g.)
SD2 are selected for Clock Sync Domain of the SDIN2 pin when EXBCK2[2:0] bits = “010” and MSN2 bit =“0” (Figure 18).

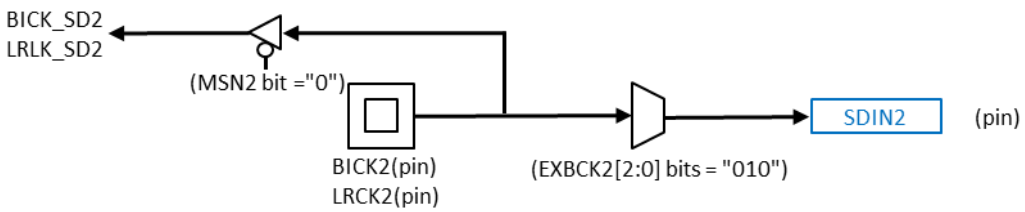


Figure 18. Clock Sync Domain Setting Example1 of SDINx Pin

e.g.)
SD2 are selected for Clock Sync Domain of the SDIN1 pin when EXBCK1[2:0] bits = “001”, MSN1 bit =“1” and SDBCK1[2:0] bits = “010” (Figure 19).

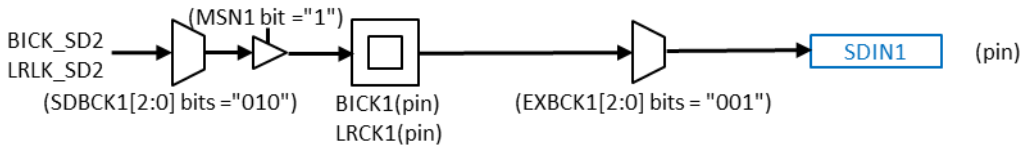


Figure 19. Clock Sync Domain Setting Example2 of SDINx Pin

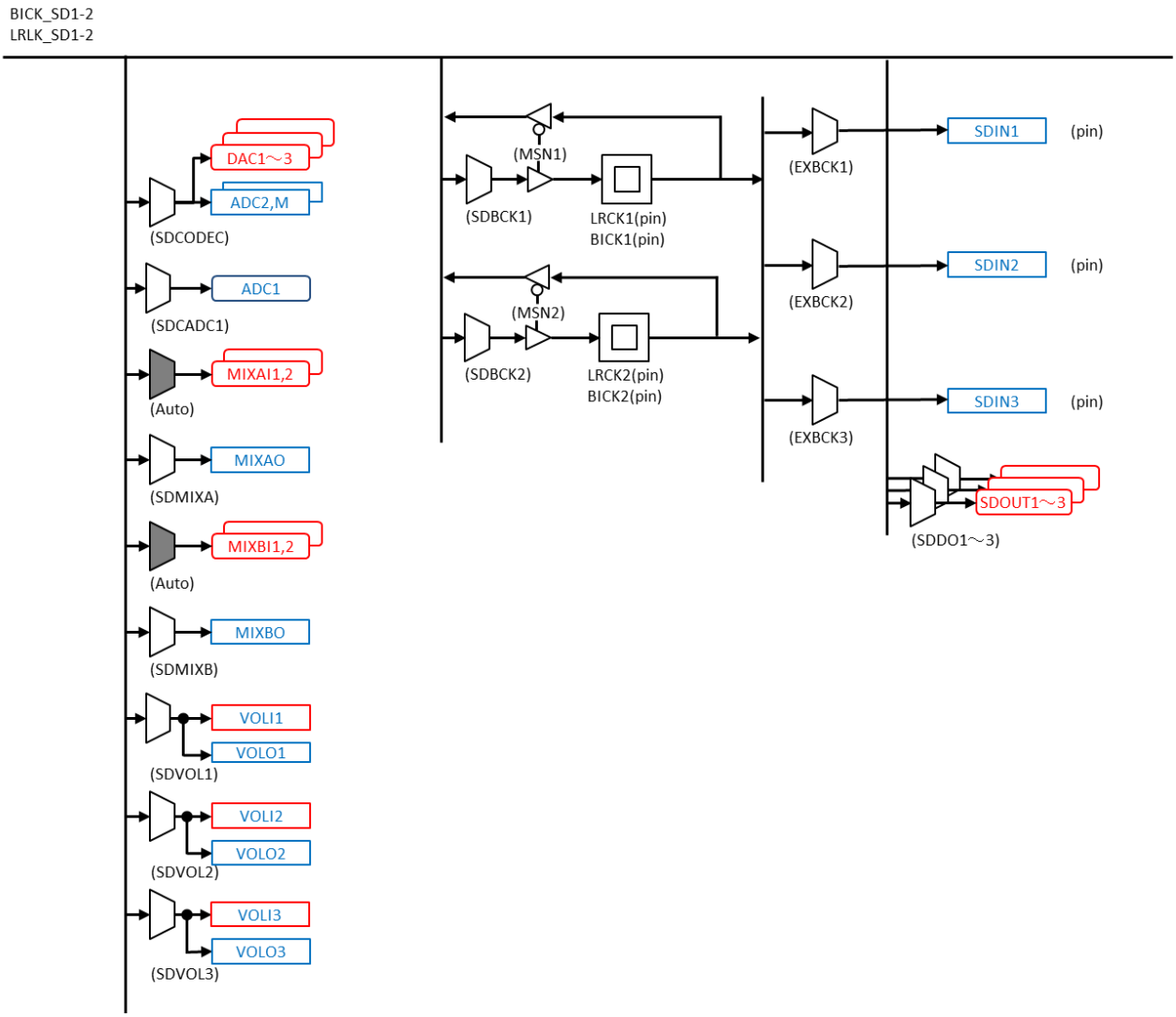


Figure 20. Clock Sync Domain Setting of Input/Output Port

2. Source Address, Source Selecting Registers

A source address is assigned to each input port source (Table 20). The output port source can be selected by setting a source address of input port to the registers. Data on the data bus can be selected freely by this source address. In TDM mode, arbitrary 2 channels audio data can be output from two selected SDOUTx pins (Table 21).

Source Address	Source Name	Source Contents	Input Port	Clock Sync Domain Setting Register (Table 19)
0x00	ALL0	0x0000 0000 fixed	ALL0	-
0x01	SDIN1A	SDIN1 Slot1, 2 Input	SDIN1	Note 44
0x02	SDIN1B	SDIN1 Slot3, 4 Input		
0x03	SDIN1C	SDIN1 Slot5, 6 Input		
0x04	SDIN1D	SDIN1 Slot7, 8 Input		
0x05	SDIN1E	SDIN1 Slot9, 10 Input		
0x06	SDIN1F	SDIN1 Slot11, 12 Input		
0x07	SDIN1G	SDIN1 Slot13, 14 Input		
0x08	SDIN1H	SDIN1 Slot15, 16 Input		
0x09	SDIN2	SDIN2 Input	SDIN2	Note 44
0x0A	SDIN3	SDIN3 Input	SDIN3	Note 44
0x10	VOLO1	VOL1 Output	VOLO1	SDVOL1[2:0]
0x11	VOLO2	VOL2 Output	VOLO2	SDVOL2[2:0]
0x12	VOLO3	VOL3 Output	VOLO3	SDVOL3[2:0]
0x15	ADC1	ADC1 Output	ADC1	SDADC1[2:0]
0x16	ADC2	ADC2 Output	CODEC	SDCODEC[2:0]
0x17	ADCM	ADCM Output		
0x18	Mixer A	Mixer A Output	Mixer A	SDMIXA[2:0]
0x19	Mixer B	Mixer B Output	Mixer B	SDMIXB[2:0]
Others	N/A	N/A	N/A	N/A

(N/A: Not Available)

Table 20. Clock Sync Domain Setting for Source Address and Input Port

Note 44. Clock Sync Domain of the SDINx pin is automatically selected by setting EXBCKx[2:0] bits, MSNx bit and SDBCKx[2:0] bits (Table 15, Table 16, Table 18).

Set a source address of input data by independent setting registers for each block if each block is obtaining data from the data bus.

If the output port sync domain setting is in auto mode, this register setting for source address is not necessary since an audio data port inherits the sync domain of the input data.

Source Select Registers	Contents	Output Port	Clock Sync Domain Setting Register (Table 19)
SELDO1A[5:0]	SDOUT1 Slot1, Slot2	SDOUT1	SDDO1[2:0]
SELDO1B[5:0]	SDOUT1 Slot3, Slot4		
SELDO1C[5:0]	SDOUT1 Slot5, Slot6		
SELDO1D[5:0]	SDOUT1 Slot7, Slot8		
SELDO1E[5:0]	SDOUT1 Slot9, Slot10		
SELDO1F[5:0]	SDOUT1 Slot11, Slot12		
SELDO1G[5:0]	SDOUT1 Slot13, Slot14		
SELDO1H[5:0]	SDOUT1 Slot15, Slot16		
SELDO2[5:0]	SDOUT2 Slot1, Slot2	SDOUT2	SDDO2[2:0]
SELDO3[5:0]	SDOUT3 Slot1, Slot2	SDOUT3	SDDO3[2:0]
SELDA1[5:0]	DAC1 Input	DAC1	SDCODEC[2:0]
SELDA2[5:0]	DAC2 Input	DAC2	
SELDA3[5:0]	DAC3 Input	DAC3	
SELVOL1[5:0]	VOL1 Input	VOLI1	(Auto)
SELVOL2[5:0]	VOL2 Input	VOLI2	
SELVOL3[5:0]	VOL3 Input	VOLI3	
SELMIXAI1[5:0]	MixerA Input1	MixerAI1	(Auto)
SELMIXAI2[5:0]	MixerA Input2	MixerAI2	
SELMIXBI1[5:0]	MixerB Input1	MixerBI1	
SELMIXBI2[5:0]	MixerB Input2	MixerBI1	

Table 21. Clock Sync Domain Settings for Source Select Registers and Output Port

3. Input/Output Serial Interface Format

3-1. Data Clocks

The AK4601 has two independent BICK/LRCK pins that are able to switch master and slave mode. MSNx bit selects Master/Slave mode of the BICKx pin and the LRCKx pin (Table 16). Clock format of LRCKx/BICKx pins can be selected by DCFx[2:0] bits. If a BICK/LRCK pins are master mode, desirable clock format is output according to DCFx[2:0] bits setting (Table 22). If a BICK/LRCK pins are slave mode, set DCFx[2:0] bits according to the input clock format.

Mode	DCFx[2]	DCFx[1]	DCFx[0]	Clock Format	
0	0	0	0	I^2S Mode	(default)
1	1	0	1	DSP Mode	
2	1	1	0	PCM Short Frame	
3	1	1	1	PCM Long Frame	

Table 22. AK4601 Data Clock Format

Clock edge relationship can be controlled by BCKPx bit.

BCKPx bit	BICKx Edge Referenced to LRCKx Start Edge	
0	Falling Edeg (FE)	(default)
1	Rising Edge (RE)	

Table 23. Clock Edge Relationship between BICKx and LRCKx

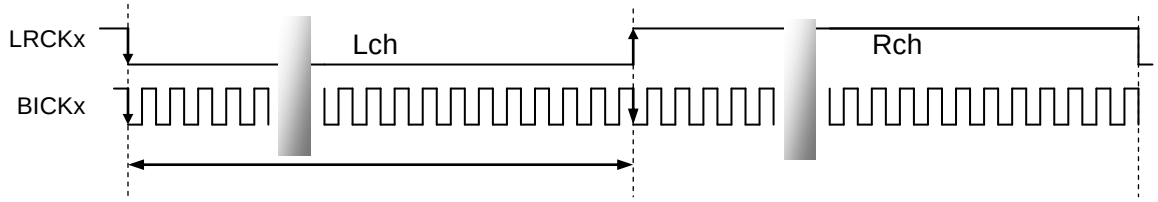


Figure 21. I^2S Mode

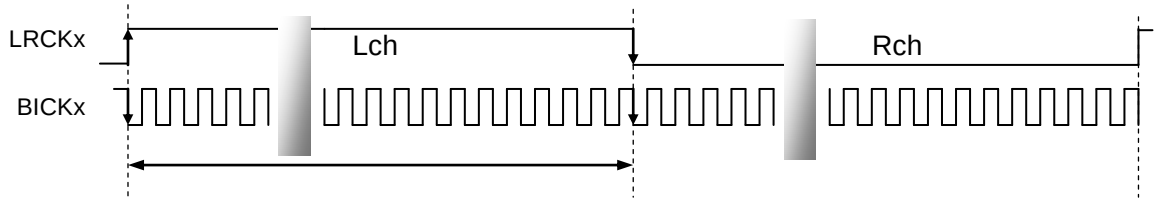


Figure 22. DSP Mode

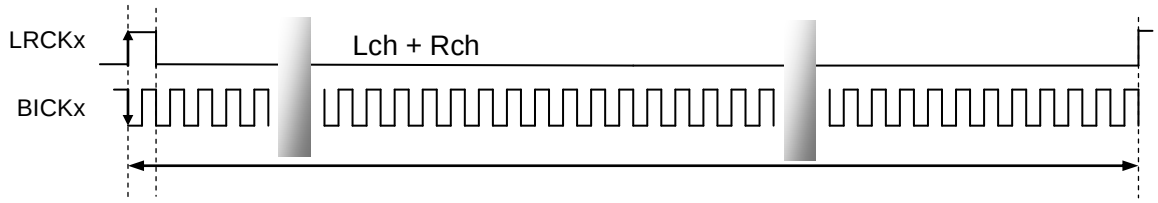


Figure 23. PCM Short Frame / PCM Long Frame (BCKPx bit = “0”)

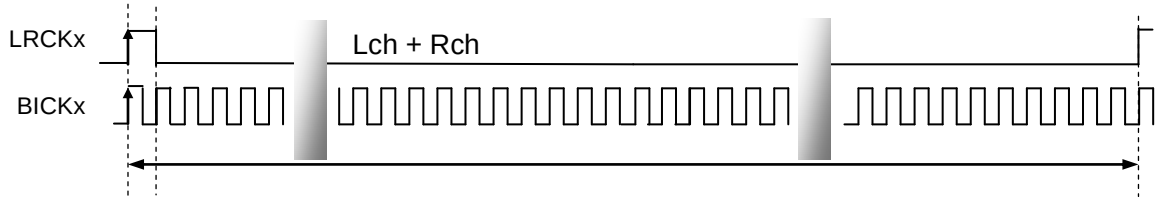


Figure 24. PCM Short Frame / PCM Long Frame (BCKPx bit = “1”)

3-2. Data Definitions

A serial bit stream that is sent or received by the AK4601 is a digital signal composed of slot, word and bit data.

Bit: It is a smallest component in a serial data stream. The bit duration is one serial clock cycle.

Word: It is a group of multiple bits that composes transmitting data between external devices and the AK4601. Figure 25 shows an example of a word consists of eight bits.

Slot: It is composed of a word and adequate additional bits for interfacing to an external device. In Figure 25, the audio data is an 8-bit valid data and a 12-bit slot needs additional four zeros to satisfy an interface protocol of the external device.
If the word length is shorter than the slot length, the data alignment of the word will be the beginning of the slot (MSB justified) or end of the slot (LSB justified). Figure 25 shows an example of MSB justified format. The slot length must be longer than the word length.

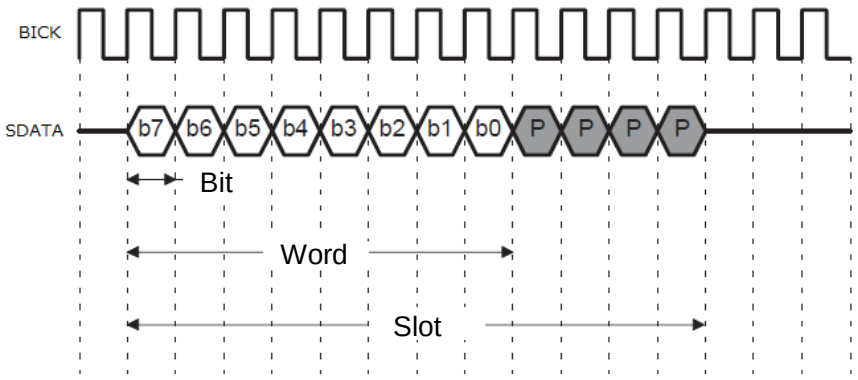


Figure 25. Bit and Word Slot Definition

5-3. Input/ Output Interface Format

The AK4601 has three digital input ports (SDIN1~SDIN3) and three digital output ports (SDOUT1~SDOUT3). The input data format is determined by a combination of DISLx[1:0], DIEDGENx, DILSBEx and DIDLx[1:0] bits settings (x=1~3). The output data format is determined by a of DOSLx[1:0], DOEDGENx, DOLSBEx and DODLx[1:0] bits settings (x=1~3).

DISLx[1:0] bits / DOSLx[1:0] bits (x=1~3) control input/output data slot length.

DISLx[1] bit DOSLx[1] bit	DISLx[0] bit DOSLx[0] bit	Slot Length	
0	0	24bit	(default)
0	1	20bit	
1	0	16bit	
1	1	32bit	

Table 24. Slot Length Setting of Input/Output Data

DIDLx[1:0] bits / DODLx[1:0] bits (x=1~3) control input/output audio data word length.

DIDLx[1] bit DODLx[1] bit	DIDLx[0] bit DODLx[0] bit	Word Length	
0	0	24bit	(default)
0	1	20bit	
1	0	16bit	
1	1	32bit	

Table 25. Word Length Setting of Input/Output Audio Data

DILSBEx bit/ DOLSBEx bit (x=1~3) selects the audio data format of a slot.

DILSBEx bit DOLSBEx bit	Slot Data Format	
0	MSB First	(default)
1	LSB First	

Table 26. Slot Data Format Setting

DIEDGENx bit / DOEDGENx bit (x=1~3) select data transmission start timing of the data after second channel

DIEDGENx bit DOEDGENx bit	Start Timing	
0	LRCK Edge Basis	(default)
1	Slot Length Basis	

Table 27. Data Transmission Start Timing of The Data After Second Channel

If the data transmitting timing is set to Slot length basis, the next channel's data is transmitted immediately without waiting a LRCK edge after transmitted one slot data (Figure 29 ~ Figure 32).
If the data transmitting timing is set to LRCK edge basis, the next channel's data will not be transmitted until a LRCK edge even finished transmitting one slot data (Figure 26 ~ Figure 28).

5-4. Stereo Mode

AK4601 supports stereo mode. BICK x pin should be set to arbitrary frequency more than word length x 2fs when DIEDGENx bit = "0". BICK x pin should be set to arbitrary frequency more than slot length x 2fs when DIEDGENx bit = "1". BICK clock is supported up to 24.576MHz.

The SDINx input pins of the AK4601 support stereo input mode. Two slots data input is available for each pin. A source address is assigned to each SDINx input pins when using stereo input mode. (Table 20). DISLx[1:0] bits control input data slot length of the SDINx pin. DIDLx[1:0] bits control the input data word length of the SDINx pin. The slot data format is set by DILSBEx bit.
In stereo mode, DIEDGENx bit must be set to "0" when the data transmission timing of second channel are LRCK edge basis. DISLx[1:0] bits setting are ignored when DIEDGENx bit = "0".

The SDOUTx output pins of the AK4601 support stereo output mode. Two slots data output is available for each pin. Each slot data can be assigned by setting SELDOxA-H[5:0] bits. DOSLx[1:0] bits control output data slot length of the SDOUTx pin. DODLx[1:0] bits control the output data word length of the SDOUTx pin. The slot data format is set by DOLSBEx bit.
In stereo mode, DOEDGENx bit must be set to "0" when the data transmission timing of second channel are LRCK edge basis. DOSLx[1:0] bits setting are ignored when DIEDGENx bit = "0".

Setting example of stereo mode is shown in Table 28.

Mode	Data Format	DCFx[2:0]	DILSBEx DOLSBEx	DIEDGENx DOEDGENx	DISLx[1:0] DOSLx[1:0]	DIDLx[1:0] DODLx[1:0]
0	I^2S Compatible	000	0	0	x	Word Length
1	MSB Justified	101	0	0	x	Word Length
2	LSB Justified	101	1	0	x	Word Length
3	PCM Short Frame	110	0	1	Slot Length	Word Length
4	PCM Long Frame	111	0	1	Slot Length	Word Length
5	Irregular I^2S	000	0	1	Slot Length	Word Length

Table 28. Input/Output Data Format Setting Example (x: Do Not Care)

5-4-1. Mode 0: I²S Compatible Format

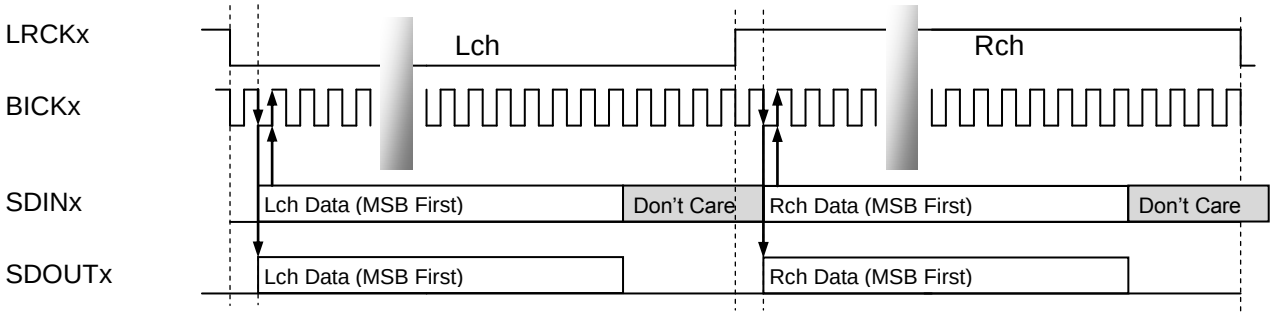


Figure 26. I²S Compatible Format

5-4-2. Mode 1: MSB Justified Format

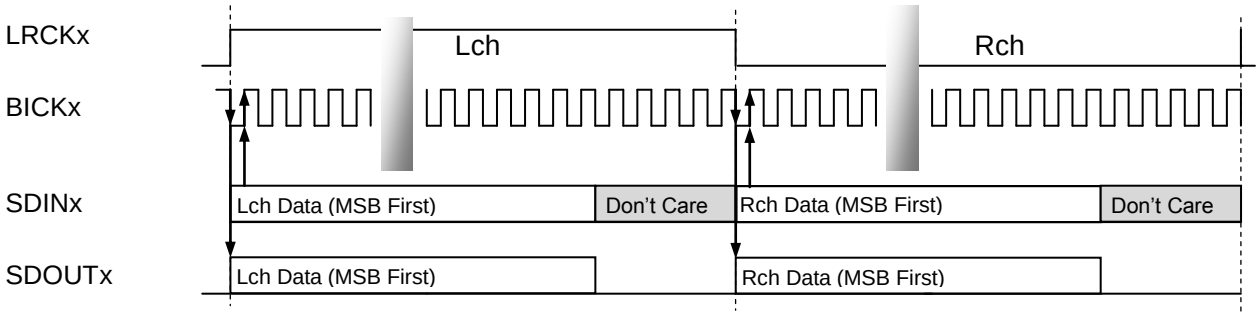


Figure 27. MSB Justified Format

5-4-3. Mode 2: LSB Justified

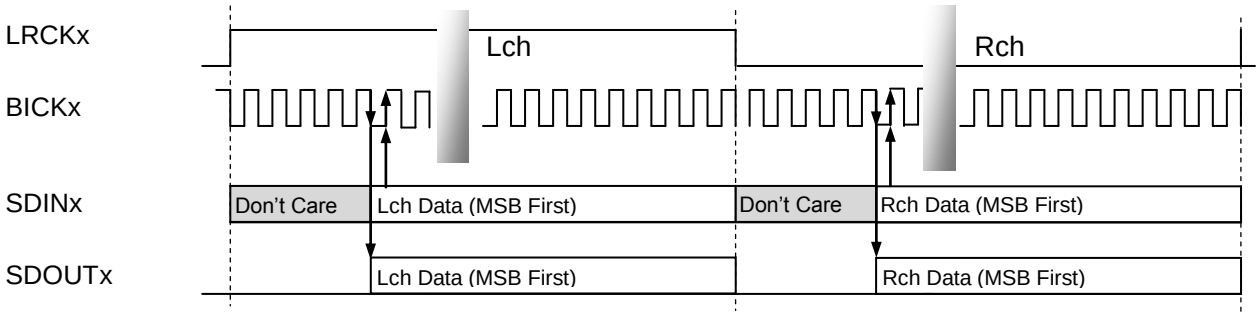


Figure 28. LSB Justified Format

5-4-4. Mode 3: PCM Short Frame Format

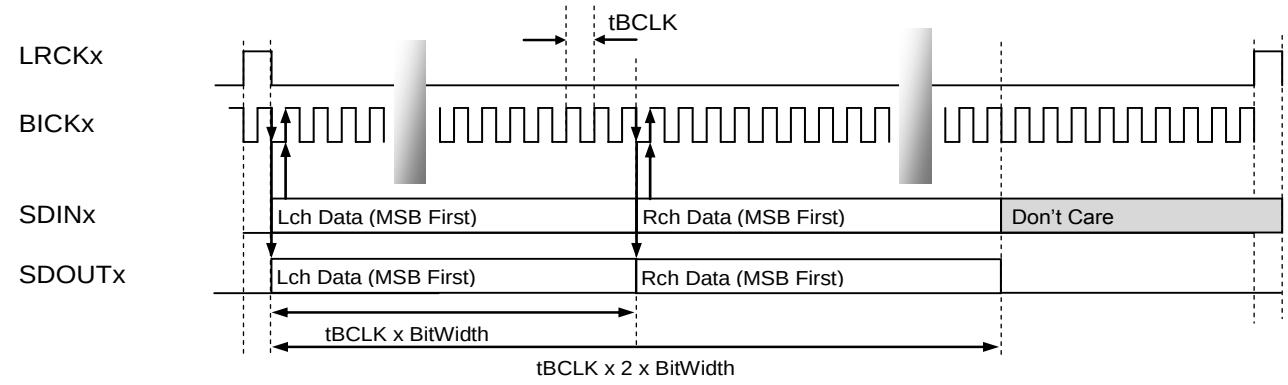


Figure 29. PCM Short Frame Format (BCKPx bit = "0")

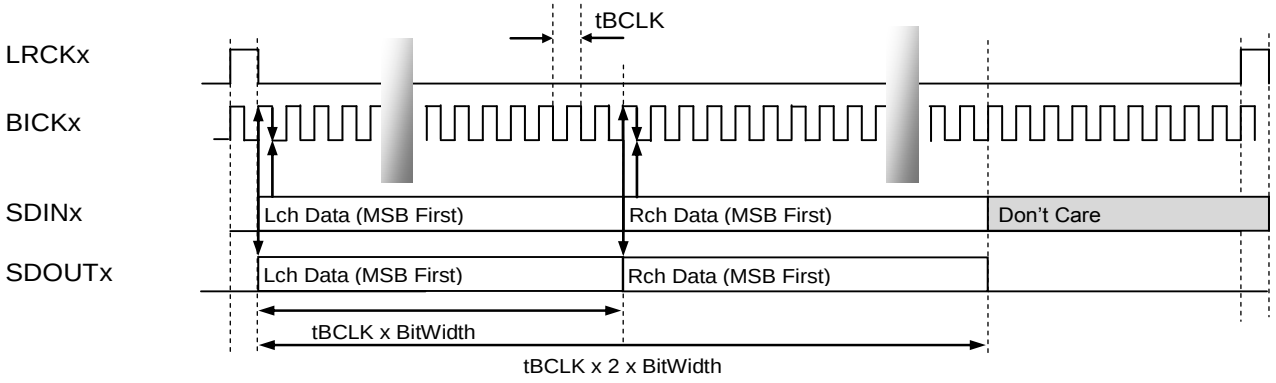


Figure 30. PCM Short Frame Format (BCKPx bit = "1")

5-4-5. Mode 4: PCM Long Frame Format

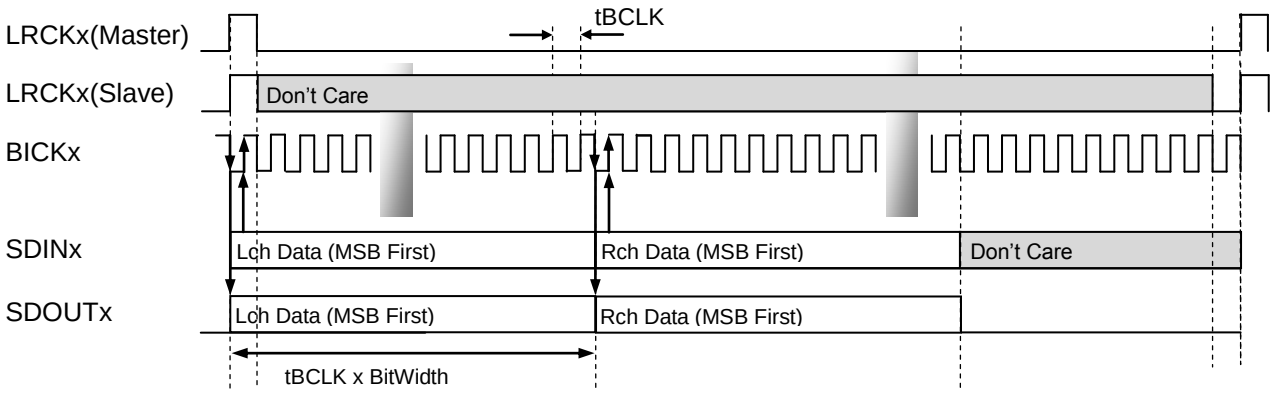


Figure 31. PCM Long Frame Format (BCKPx bit = "0")

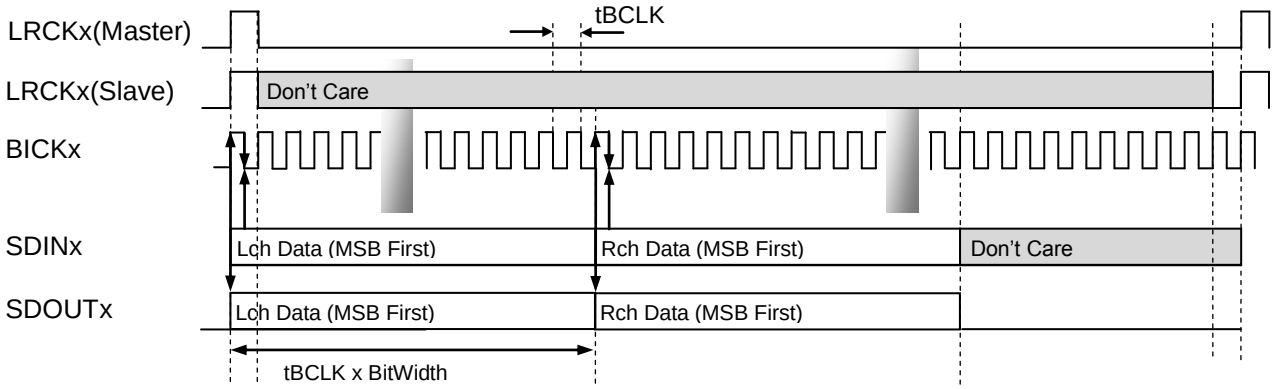


Figure 32. PCM Long Frame Format (BCKPx bit = "1")

5-4-6. Mode 5: Irregular I^{2}S Format

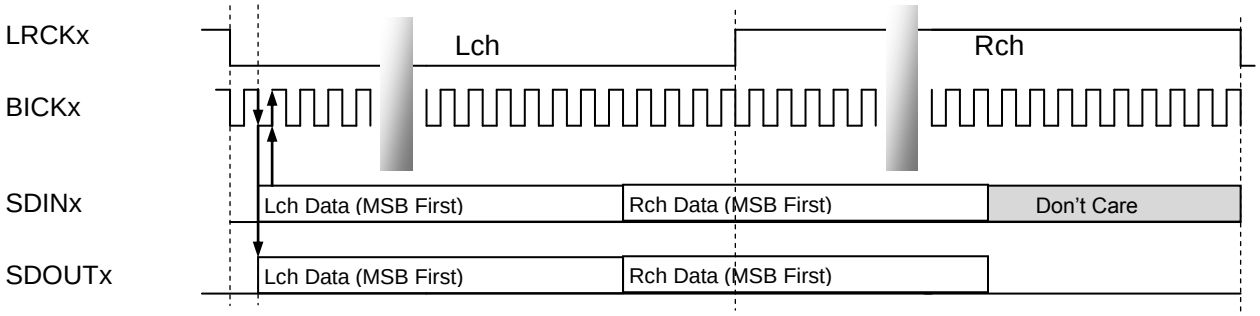


Figure 33. Irregular I^{2}S Format

5-5. TDM Mode

AK4601 supports TDM mode. BICK clock for data input/output should be set to 128fs, 192fs, 256fs or 512fs when using TDM mode. Up to 192kHz in 128fs mode (max. fs=128kHz in 192 mode, max. fs=96kHz in 256 mode, max. fs=48kHz in 512 mode) sampling frequency is supported.

The SDIN1 input pin of the AK4601 support TDM mode. Sixteen slots data input is available at a maximum. A source address is assigned to each 2 slot of SDIN1 input pin when using TDM mode. (Table 20). DISL1[1:0] bits control input data slot length of the SDIN1 pin. DIDL1 [1:0] bits control the input data word length of the SDIN1 pin. The slot data format is set by DILSBE1 bit.
In TDM mode, DIEDGEN1 bit must be set to “1” since the data transmission timing after second channel are slot length basis. Slot length, word length and slot data format of each input data slot should be the same setting.

The SDOUT1 output pins of the AK4601 support TDM mode. Sixteen slots data output is available for each pin at a maximum. Each slot data can be assigned independently by setting SELDO1A-H[5:0] bits in every two slots. DOSL1[1:0] bits control output data slot length of the SDOUT1 pin. DODL1[1:0] bits control the output data word length of the SDOUT1 pin. The slot data format is set by DOLSBE1 bit. In TDM mode, DOEDGEN1 bit must be set to “1” since the data transmission timing after second channel are slot length basis. Slot length, word length and slot data format of each input data slot should be the same setting.

Setting example of TDM mode is shown in Table 29.

Mode	Data Format	DCF1[2:0]	DILSBE1 DOLSBE1	DIEDGEN1 DOEDGEN1	DISL1 [1:0] DOSL1[1:0]	DIDL1 [1:0] DODL1[1:0]
0	I^2S Compatible	000	0	1	11 (32bit)	Word Length
1	MSB Justified	101	0	1	11 (32bit)	Word Length
2	LSB Justified	101	1	1	11 (32bit)	Word Length
3	PCM Short Frame	110	0	1	Slot Length	Word Length
4	PCM Long Frame	111	0	1	Slot Length	Word Length
5	Irregular I^2S	000	0	1	Slot Length	Word Length

Table 29. TDM Mode Setting Example

5-5-1. I²S Compatible Format

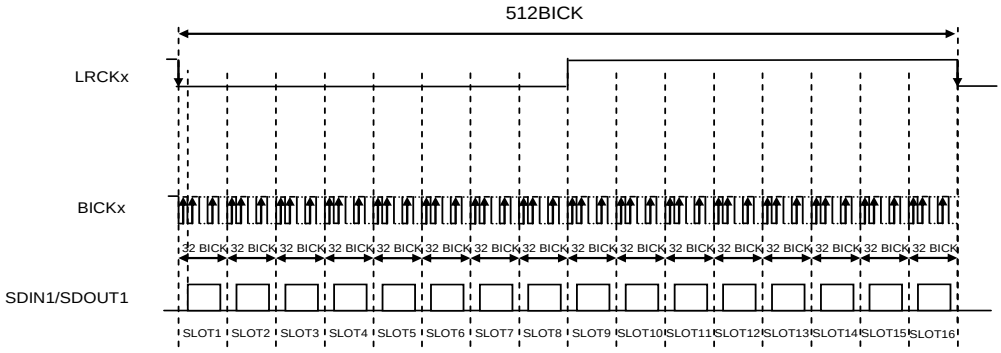


Figure 34. TDM Mode I^{2}S Compatible (BICK = 512fs)

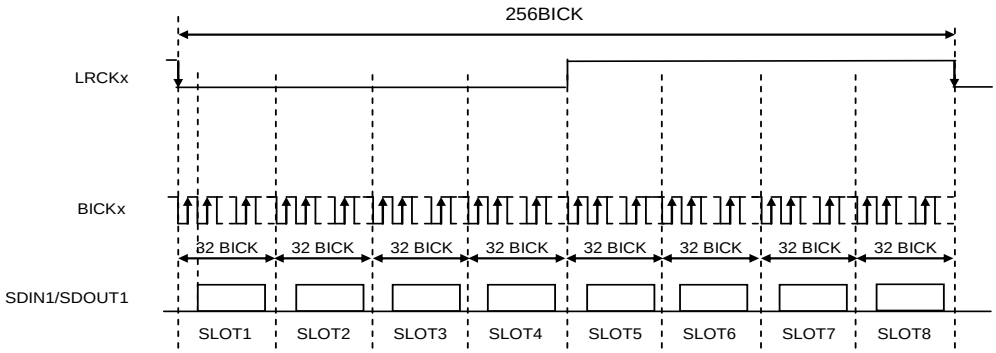


Figure 35. TDM Mode I^{2}S Compatible (BICK = 256fs)

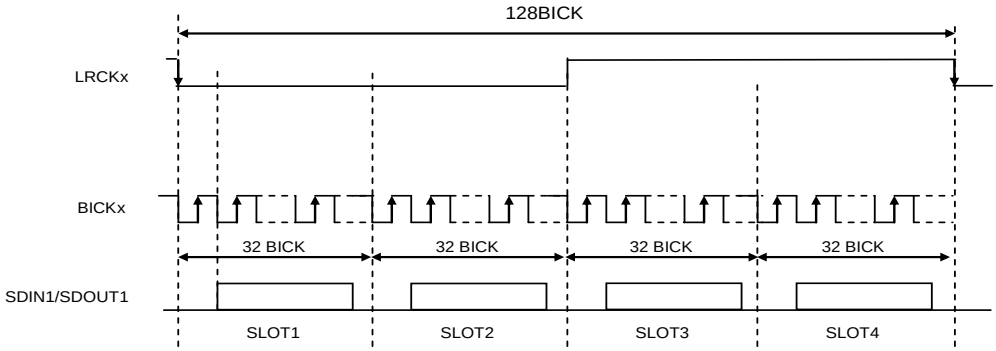


Figure 36. TDM Mode I^{2}S Compatible (BICK = 128fs)

5-5-2. MSB Justified Format

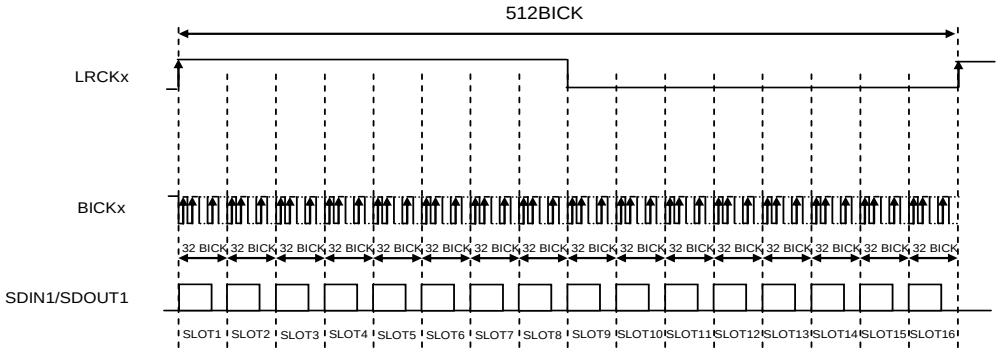


Figure 37. TDM Mode MSB Justified Format (BICK = 512fs)

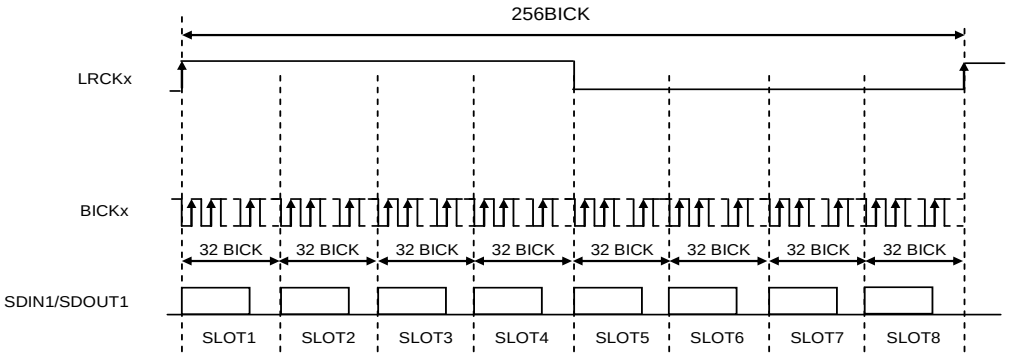


Figure 38. TDM Mode MSB Justified Format (BICK = 256fs)

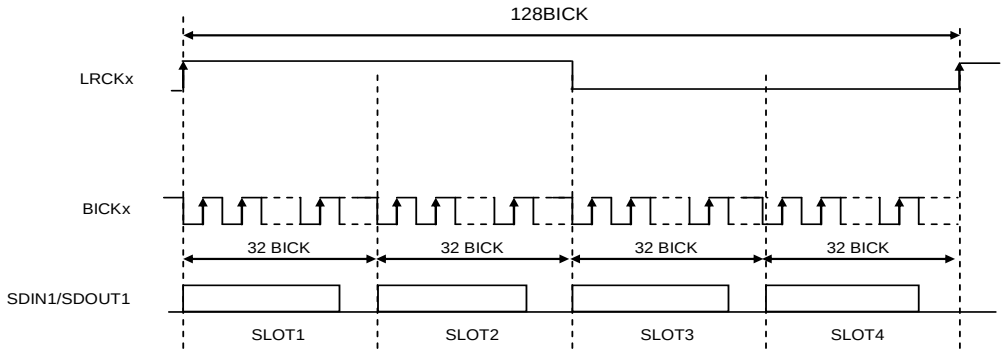


Figure 39. TDM Mode MSB Justified Format (BICK = 128fs)

5-5-3. LSB Justified Format

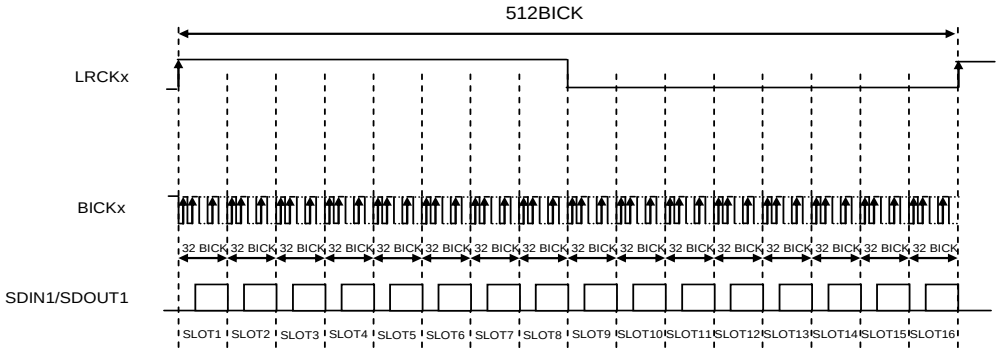


Figure 40. TDM Mode LSB Justified Format (BICK = 512fs)

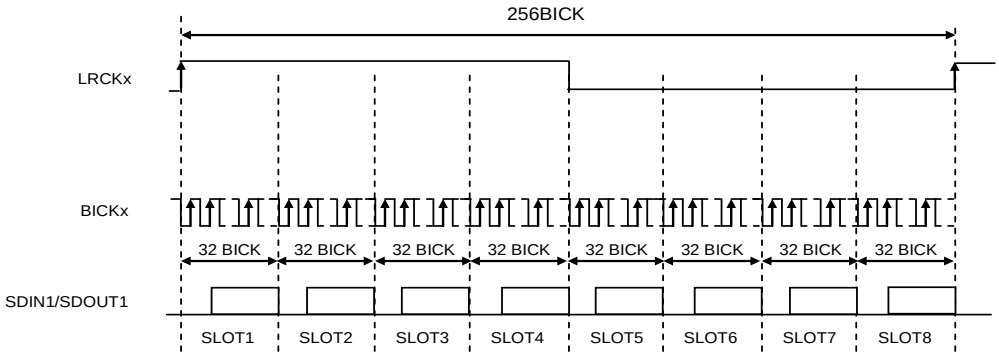


Figure 41. TDM Mode LSB Justified Format (BICK = 256fs)

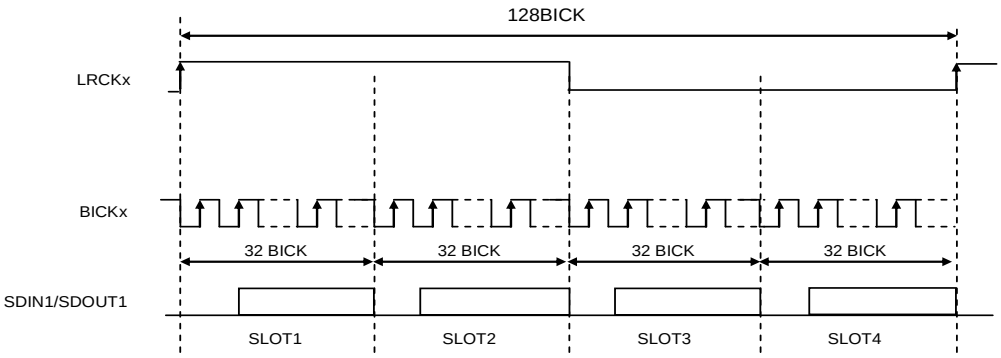


Figure 42. TDM Mode LSB Justified Format (BICK = 128fs)

5-5-4. PCM Short Frame Format

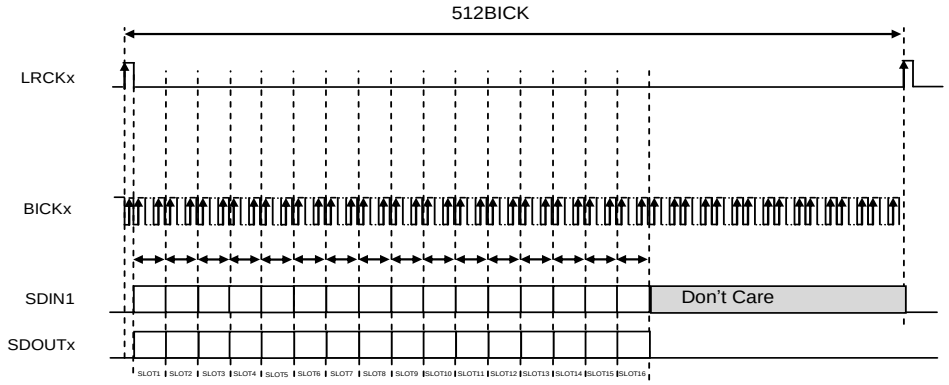


Figure 43. TDM mode PCM Short Frame (BICK = 512fs, BCKP bit = "0") (Note 45)

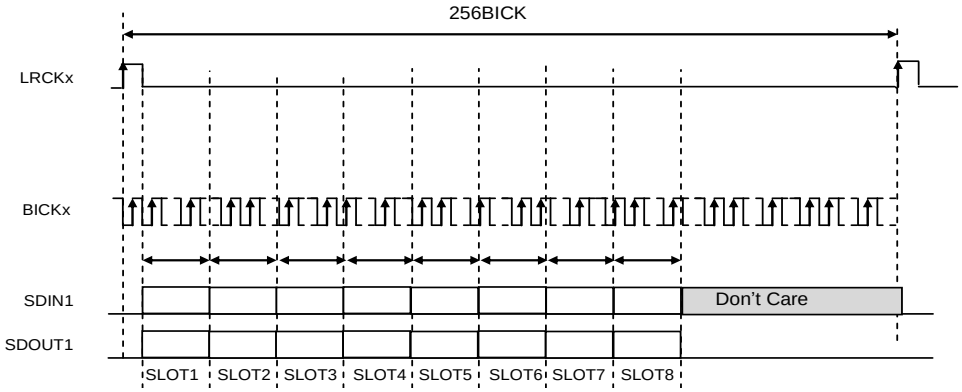


Figure 44. TDM mode PCM Short Frame (BICK = 256fs, BCKP bit = "0") (Note 45)

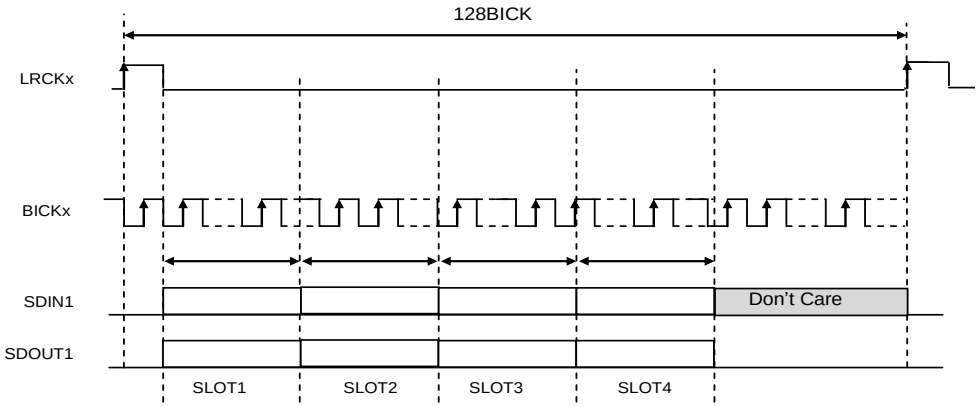


Figure 45. TDM mode PCM Short Frame (BICK = 128fs, BCKP bit = "0") (Note 45)

Note 45. When BCKPx bit = "1", a BICK rising edge "↑" corresponds to a LRCK rising edge "↑".

5-5-5. PCM Long Frame Format

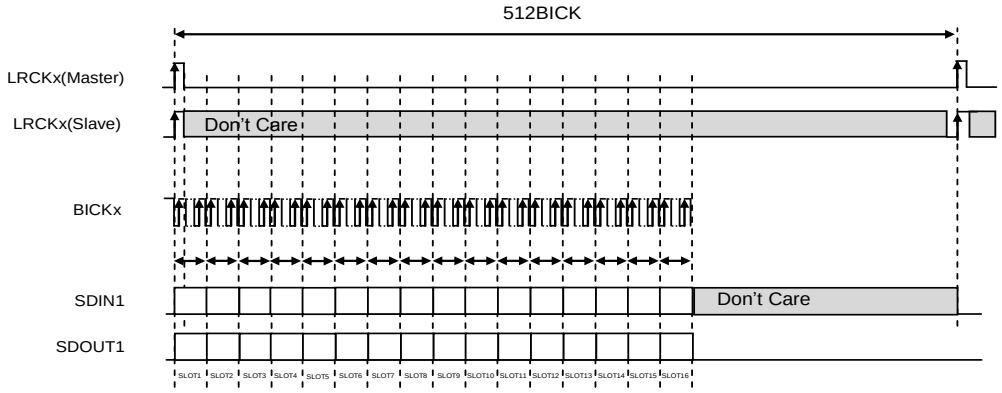


Figure 46. TDM mode PCM Long Frame (BICK = 512fs, BCKP bit = "0") (Note 46)

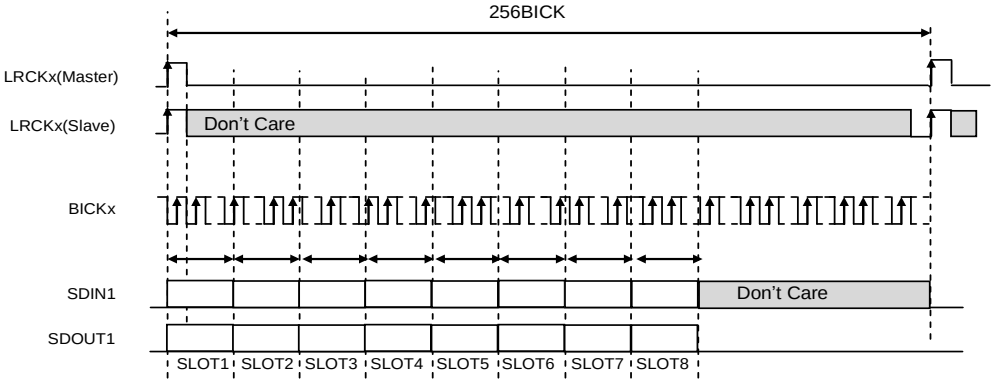


Figure 47. TDM mode PCM Long Frame (BICK = 256fs, BCKP bit = "0") (Note 46)

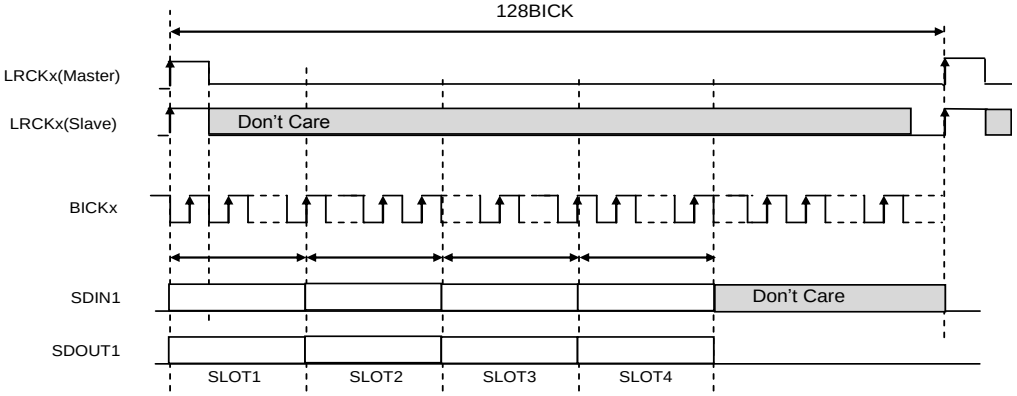


Figure 48. TDM mode PCM Long Frame (BICK = 128fs, BCKP bit = "0") (Note 46)

Note 46. When BCKPx bit = "1", a BICK rising edge "↑" corresponds to a LRCK rising edge "↑".

5-5-6. Irregular I²S Format

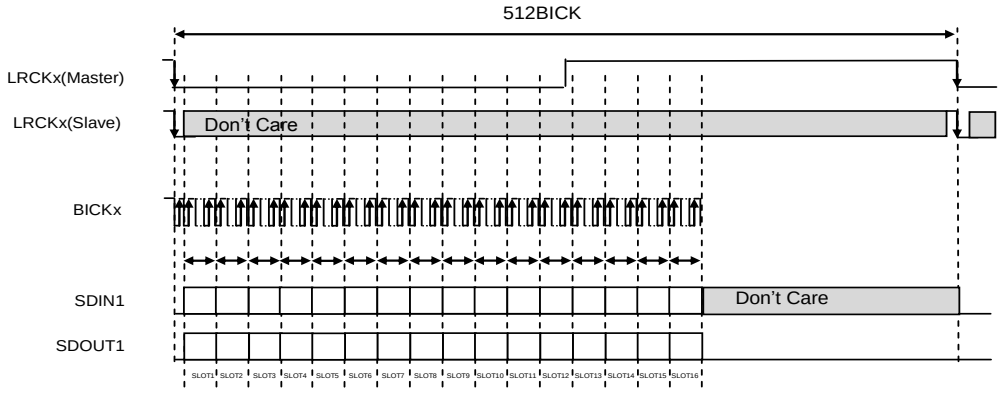


Figure 49. TDM Mode Irregular I²S Format (BICK = 512fs)

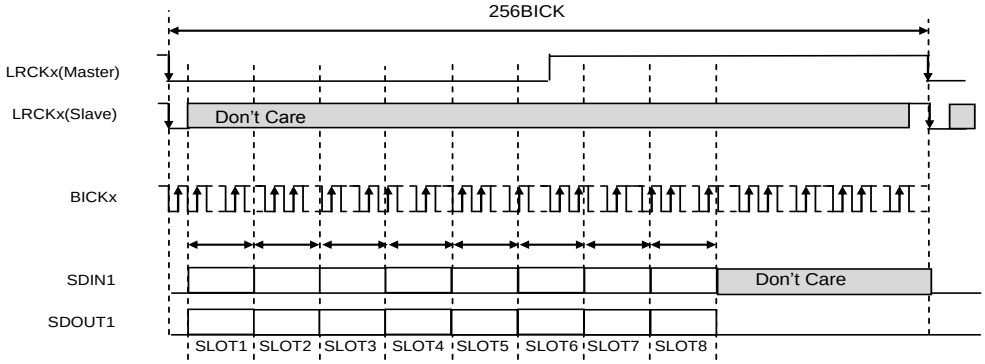


Figure 50. TDM Mode Irregular I²S Format (BICK = 256fs)

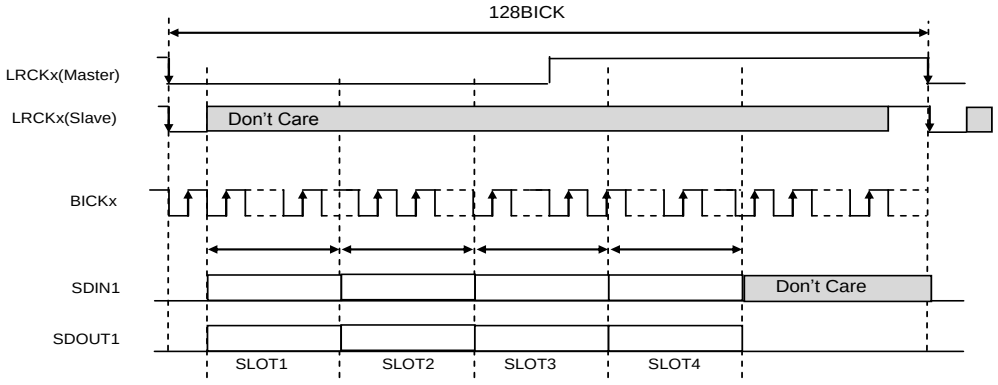


Figure 51. TDM Mode Irregular I²S Format (BICK = 128fs)

■ Power-up Sequence

1. Power-up Sequence

The AK4601 should be powered up when the PDN pin = “L”. Set the PDN pin to “H” to start the power supply circuits for REF (reference voltage source) generator and digital circuits after all power supplies are fed. By setting the PDN pin to “H”, control registers are initialized. Control register settings should be made with an interval of 1ms or more after the PDN pin = “H”.

The PLL starts operation by a clock reset release (CKRESETN bit = “0” → “1”) and generates the internal master clock after setting control registers. Therefore, necessary system clock must be input before a clock reset release.

The system clock must not be stopped except during clock reset and power-down mode (PDN pin = “L”).

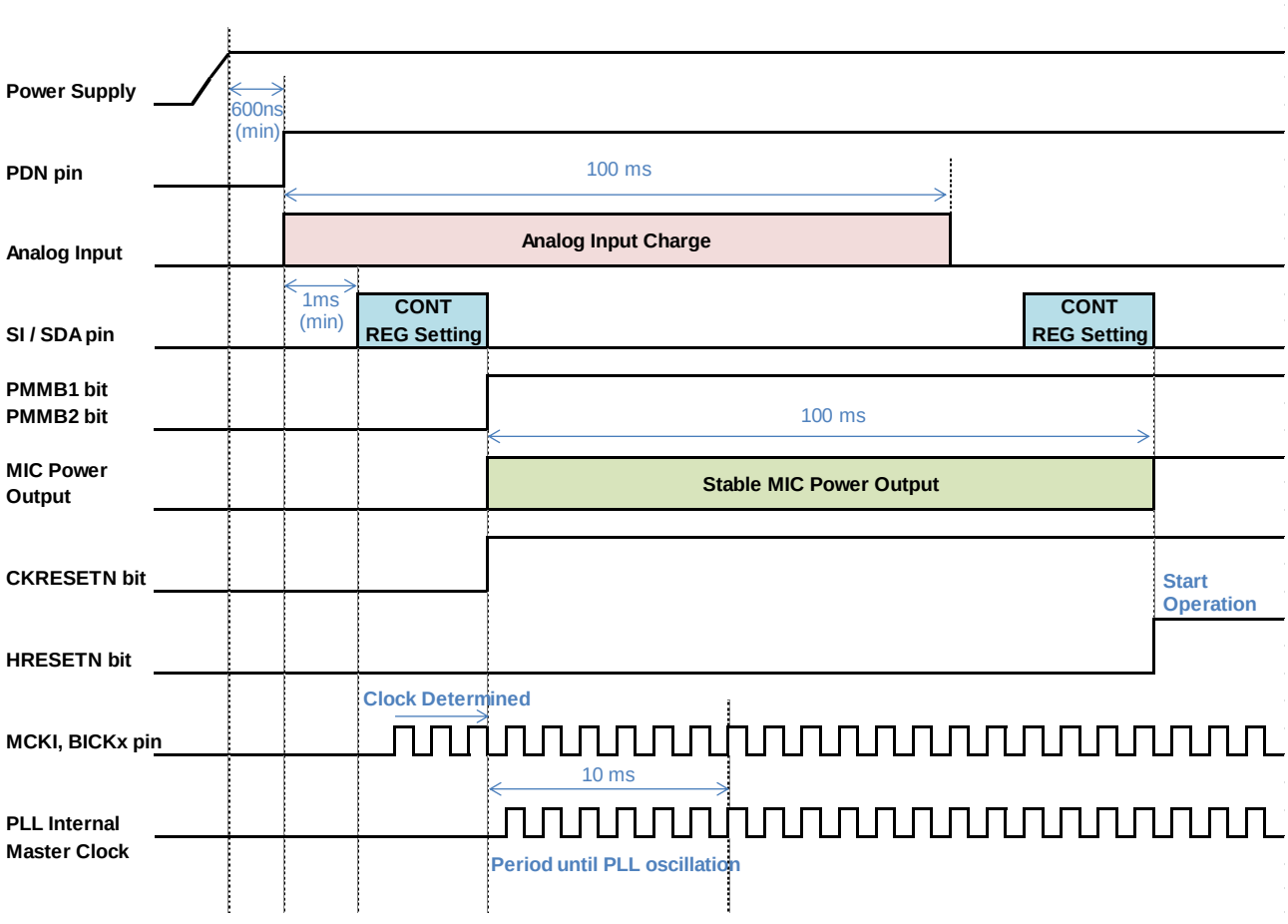


Figure 52. Power-up Sequence

Note 47. The analog input charge period depends on the capacitance of AC coupling capacitor. It will be 100 msec if the capacitance is 1 µF.

Note 48. The output period of a stable microphone power depends on the capacitance of decoupling capacitor at the MPREF pin. It will be 100 msec if the capacitance is 1 µF.

■ LDO (Internal Circuit Drive Regulator)

The AK4601 has a regulator for driving internal digital circuits (LDO). Connect a 2.2μF (±30%) capacitor between the AVDRV pin and the DVSS2 pin. The LDO starts operation by releasing power-down mode, and control register settings can be made 1ms after the power-down release (PDN pin="H").
The AK4601 has an overcurrent protection circuit to avoid abnormal heat of the device that is caused by a short of the AVDRV pin to VSS and etc., and an overvoltage protection circuit to protect from exceeded voltage when the voltage to the AVDRV pin gets too high. When these protection circuits perform, internal circuits are powered down. The internal circuit will not return to a normal operation until being reset by the PDN pin after removing the problems.

■ Power-down and Reset

1. AK4601 Power-down and Reset Statuses and Power Management

Power-down and power-down release of the AK4601 is controlled by the PDN pin. After power-down is released, the power management and reset of the AK4601 are controlled by registers such as CKRESETN bit (Clock Reset) and power management bits for each block.

There are two states for the AK4601 other than normal operation: Power-down and Clock Reset. The power-down state means the status that the PDN pin is "L". In this state, all blocks of the AK4601 stop the operation.
The clock reset state means the status that the PDN pin is "H" and CKRESETN bit is "0". In this state, the ADC, DAC, blocks are not in operation because the PLL circuit and internal clocks are stopped.

State	Setting	
	PDN pin	CKRESETN bit
Power-down	L	x
Clock Reset	H	0
Clock Reset Release	H	1

(Note 49)

Table 30. Reset State Definitions of the AK4601 (x: Don't Care)

Note 49. A stable clock should be supplied before releasing clock reset (CKRESETN bit = "1").

2. Power-down

The AK4601 can be powered down by bringing the PDN pin = "L". Output statuses of power-down mode are shown in Table 3.

3. Power-down Release

The REF generation circuit (reference voltage source) and a power supply circuit for internal digital circuit are powered-up by bringing the PDN pin to "H" from "L" after an interval of 600ns or more when AVDD, LVDD, TVDD are powered up. Control register settings should be made with an interval of 1ms or longer after setting the PDN pin = "H".

4. Clock Reset

When CKRESETN bit = “0” after power-down mode is released (PDN pin = “H”), the AK4601 is in clock reset state. All blocks except the power supply circuits for REF generation and digital circuits are in power-save mode. Even the internal PLL for master clock generation is powered down.

Control register settings should be made with an interval of 1ms (min) or more after releasing the power-down mode.

Necessary system clocks (Table 4, Table 5) should be input before the clock reset is released. The internal PLL starts operation and the master clock is generated when clock reset is released (CKRESETN bit = “1”) (Figure 52). The AK4601 will be in operation by releasing power-down mode of the blocks by setting each power-management bit.

System clocks must be changed during clock reset or in power-down mode (PDN pin = “L”). The PLL and the internal clocks are stopped by this clock reset and the clock change can be done safely. Change register settings and system clock frequencies during the clock reset. After system clock is stabilized, the PLL starts operation by setting CKRESETN bit to “1”.

Clock operated blocks (ADC and DAC) must be powered down before executing clock reset. These blocks can be powered down simultaneously by setting HRESETN bit to “0” from “1” (each PMAD and PMDA bits settings are not necessary). Set HRESETN bit to “1” from “0” with an interval of 10ms for stabilization of PLL after clock reset is released.

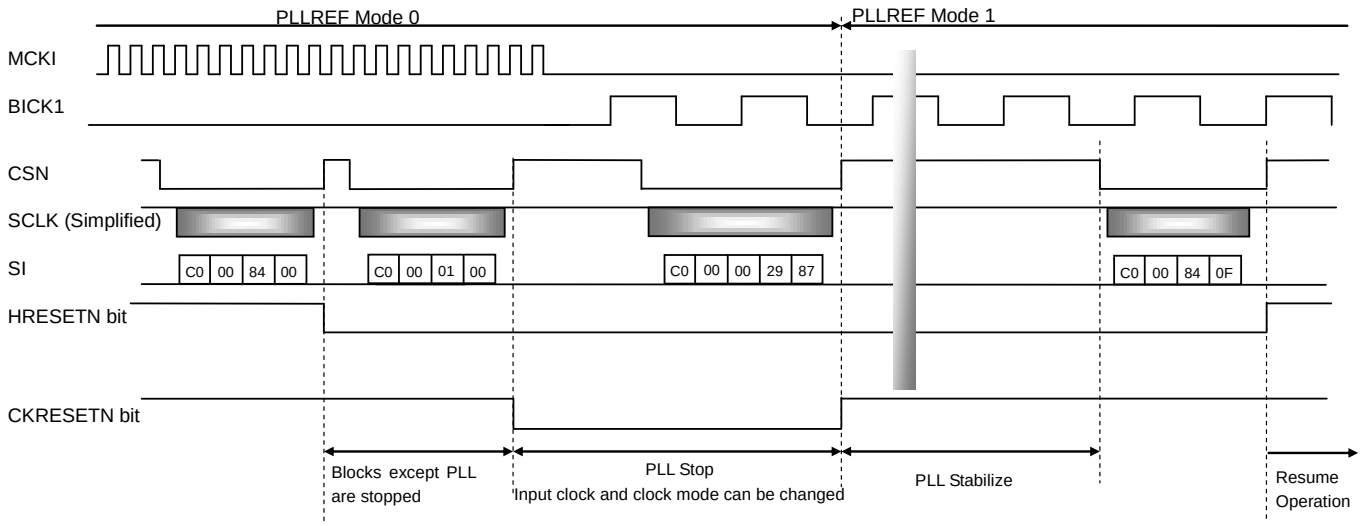


Figure 53. Clock Mode Switching Sequence

■ STO Bit Status

PLL lock signal can be read out from the STO bit when PLLLOCKE bit = “1”.

PLLLOCKE bit	STO bit	Note
0	No Error Detected: 1	(default)
1	No Error Detected: 1 PLLLOCK Error Detected: 0	

Table 31. STO Bit Status

■ µP Interface Setting and Pin Status

The AK4601 supports both SPI and I^2C interfaces. When using SPI interface, release the power-down state of the AK4601 while the CSN pin is “H”. After a power-down release, the AK4601 is set to I^2C interface mode. SPI interface mode become enabled by sending the dummy command mentioned below.

Input “0xDE → 0xADDA → 0x7A” to the SI/I2CFIL pin while the CSN pin is “L” for the dummy command. The data is in MSB first format.

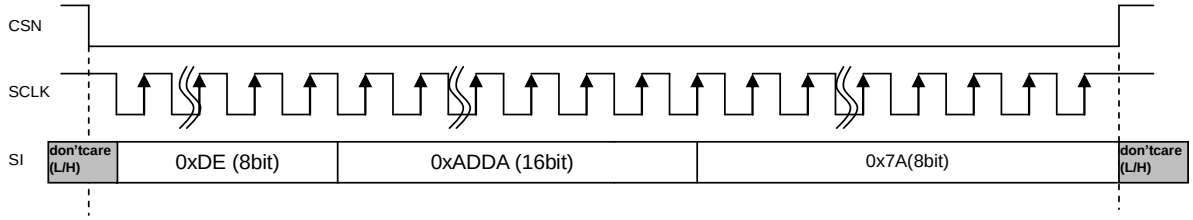


Figure 54. Dummy Command Write Sequence

Statuses of the SO/SDA, SCLK/SCL and SI/I2CFIL pins are changed depending on the CSN and PDN pins.

	CSN pin	PDN pin	SO/SDA pin	SCLK/SCL pin	SI/I2CFIL pin
SPI Interface	L	L	Hi-Z	Input	Input
	L	H	function	function	function
I^2C Interface	H	L	“Hi-Z”→ pull-up	Input	Input
	H	H	function	function	L (I^2C Fast Mode) H (I^2C Fast Mode Plus)

Table 32. µP Interface Setting

Note 50. The CSN pin and the SI/I2CFIL pin should be fixed to “L” or “H” when using I^2C interface mode.

■ SPI Interface

1. Register Write

(1) Control Register Write

Field	Write data
(1) COMMAND Code	0xC0
(2) ADDRESS	A15~A8
(3) ADDRESS	A7~A0
(4) DATA	D7~D0
	One byte of data may be written continuously for each address.

2. Register Read

(1) Control Register Read

Field	Write data	Readout data
(1) COMMAND Code	0x40	
(2) ADDRESS	A15~A8	
(3) ADDRESS	A7~A0	
(4) DATA		D7~D0
	One byte of data may be read continuously for each address.	

Write Operation

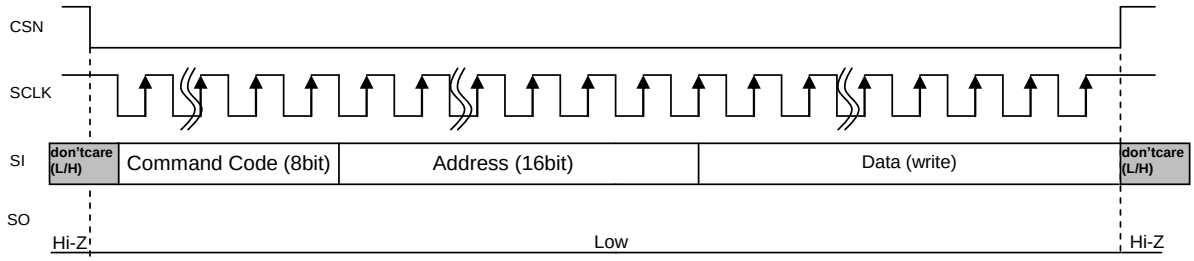


Figure 55. SPI Interface Timing (Write)

Read Operation

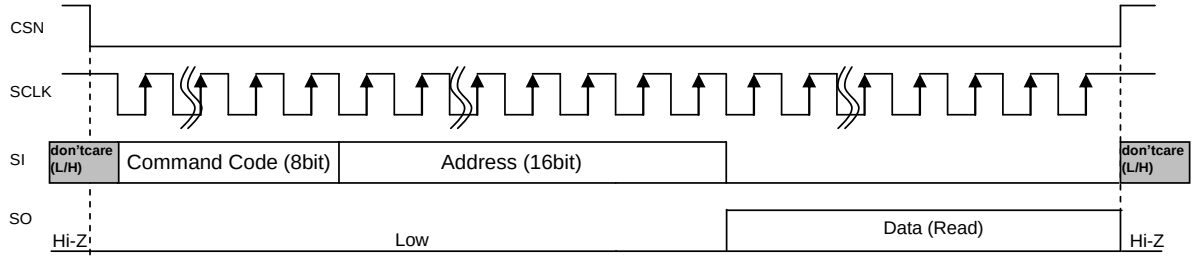


Figure 56. SPI Interface Timing (Read)

■ I²C Bus Interface (CSN = "H")

Access to the AK4601 registers and RAM can be controlled by an I²C bus. The AK4601 supports fast-mode I²C-bus (max: 400kHz) and fast-mode plus (max: 1MHz).

SI/I2CFIL pin	Bus Mode
L	Fast Mode
H	Fast Mode Plus

Table 33. I²C Bus Mode Setting

Note 51. The AK4601 does not support Hs mode (max: 3.4MHz).

1. Data Transfer

In order to access any IC devices on the I²C bus, input a start condition first, followed by one byte of Slave address which includes the Device Address. IC devices on the BUS compare this Device address with their own addresses and the IC device which has an identical address with the Device address generates an acknowledgement. An IC device with the identical address then executes either a read or a write operation. After the command execution, input a Stop condition.

1-1. Data Change

Change the data on the SDA line while the SCL line is "L". The SDA line condition must be stable and fixed while the clock is "H". Change the Data line condition between "H" and "L" only when the clock signal on the SCL line is "L". Change the SDA line condition while the SCL line is "H" only when the start condition or stop condition is input.

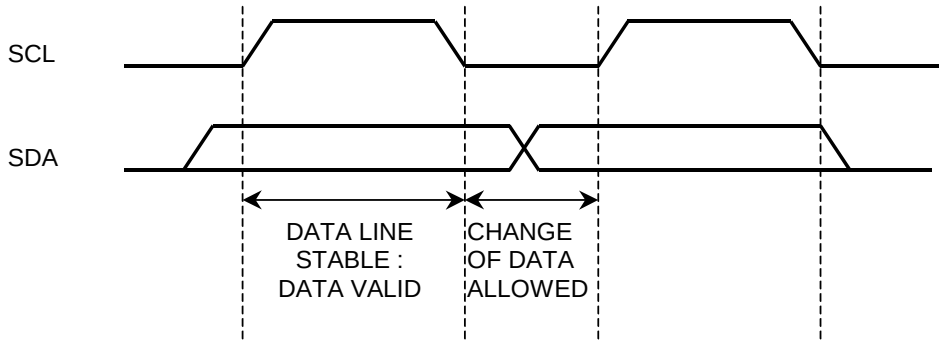


Figure 57. Data Change (I²C)

1-2. Start Condition and Stop Condition

A start condition is generated by the transition of "H" to "L" on the SDA line while the SCL line is "H". All instructions are initiated by a Start condition. A stop condition is generated by the transition of "L" to "H" on the SDA line while the SCL line is "H". All instructions end by a Stop condition.

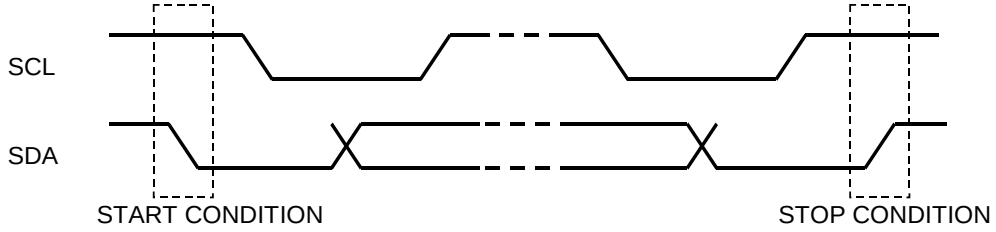


Figure 58. Start Condition and Stop Condition (I²C)

1-3. Repeated Start Condition

When a Start condition is received again instead of a Stop condition, the bus changes to a Repeated Start condition. A Repeated Start condition is functionally the same as a Start condition.

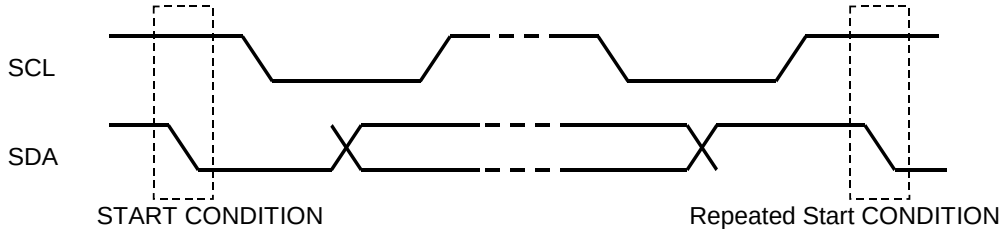


Figure 59. Repeated Start Condition (I^2C)

1-4. Acknowledge

The IC device that sends data releases the SDA line (“H”) after sending one byte of data. The IC device that receives data then sets the SDA line to “L” at the next clock. This operation is called “acknowledgement”, and it enables verification that the data transfer has been properly executed.

The AK4601 generates an acknowledgement upon receipt of a Start condition and a Slave address. For a write instruction, an acknowledgement is generated whenever receipt of each byte is completed. For a read instruction, succeeded by generation of an acknowledgement, the AK4601 releases the SDA line after outputting data at the designated address, and it monitors the SDA line condition. When the Master side generates an acknowledgement without sending a Stop condition, the AK4601 outputs data at the next address location. When no acknowledgement is generated, the AK4601 ends data output (not acknowledged).

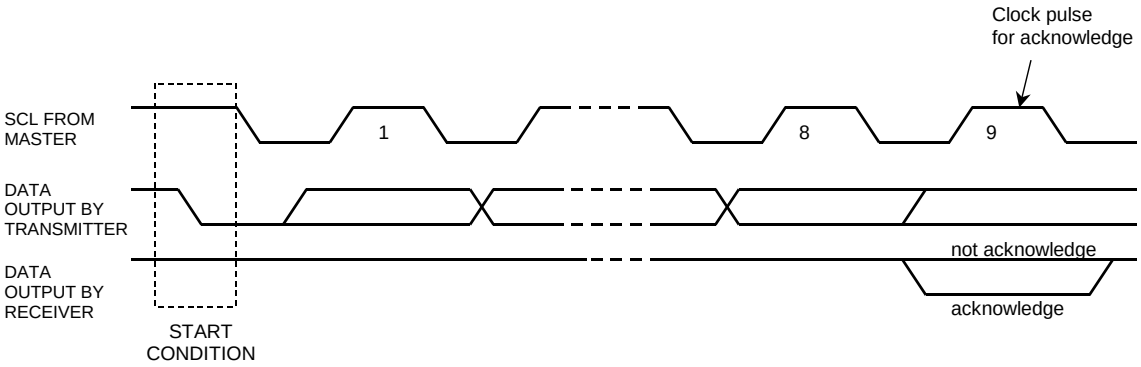


Figure 60. Generation of Acknowledgement

1-5. The First Byte

The First Byte, which includes the Slave-address, is input after the Start condition is set, and a target IC device that will be accessed on the bus is selected by the Slave-address.

The Slave-address is configured with the upper 7-bits and the data is “0010000”. When the Slave-address is inputted, an external device that has the identical device address generates an acknowledgement and instructions are then executed. The 8th bit of the First Byte (lowest bit) is allocated as the R/W Bit. When the R/W Bit is “1”, the read instruction is executed, and when it is “0”, the write instruction is executed.

Note 52. In this document, there is a case that describes a “Write Slave-address assignment” when both address bits match and a Slave-address at R/W Bit = “0” is received. There is a case that describes “Read Slave-address assignment” when both address bits matches and a Slave-address at R/W Bit = “1” is received.

0	0	1	0	0	0	0	R/W

Figure 61. First Byte Configuration (I^2C)

1-6. The Second and Succeeding Bytes

The data format of the second and succeeding bytes of the AK4601 Transfer / Receive Serial data (command code, address and data in microcontroller interface format) on the I^2C BUS are all configured with a multiple of 8-bits. When transferring or receiving those data on the I^2C BUS, they are divided into an 8-bit data stream segment and they are transferred / received with the MSB side data first with an acknowledgement in-between.

Example)
When transferring / receiving A1B2C3 (hex) 24-bit serial data in microprocessor interface format:

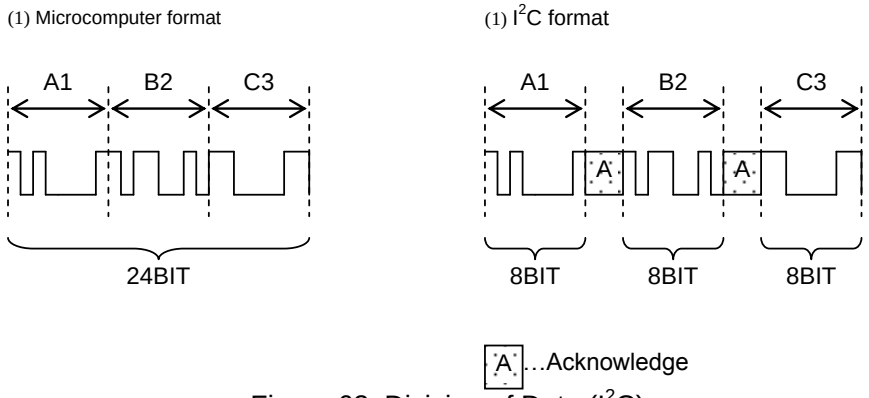


Figure 62. Division of Data (I^2C)

Note 53. In this document, there is a case that describes a write instruction command code which is received at the second byte as “Write Command”. There is a case that describes a read instruction command code which is received at the second byte as “Read Command”.

2. Write Sequence

In the AK4601, when a “Write-Slave-address assignment” is received at the first byte, the write command at the second byte, the address at the third and fourth bytes, and data at the fifth and succeeding bytes are received. The number of write data bytes is fixed by the received command code.

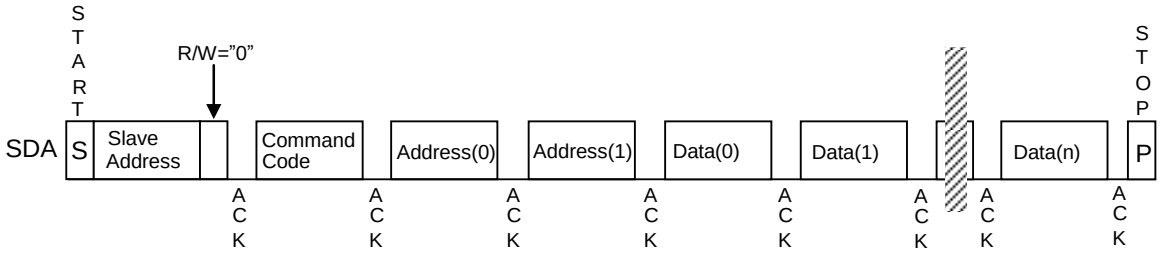


Figure 63. Write Sequence (I^2C)

3. Read Sequence

In the AK4601, when a “write- slave-address assignment” is received at the first byte, the read command at the second byte and the address at the third and fourth bytes are received. When the fourth byte is received and an acknowledgement is transferred, the read command waits for the next restart condition. When a “read slave-address assignment” is received at the first byte, data is transferred at the second and succeeding bytes. The number of readable data bytes is fixed by the received read command.

After reading the last byte, assure that a “not acknowledged” signal is received. If this “not acknowledged” signal is not received, the AK4601 continues to send data regardless whether data is present or not, and since it did not release the BUS, the stop condition cannot be properly received.

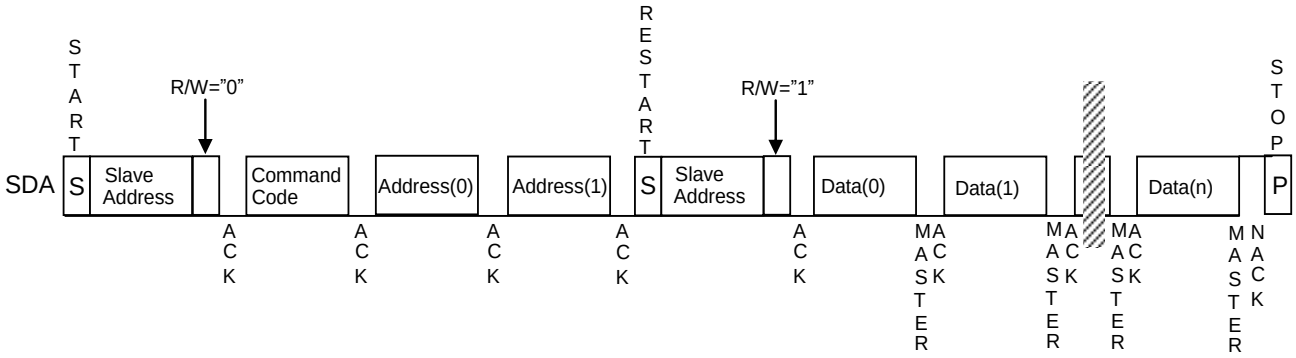


Figure 64. Read Sequence (I^2C)

4. Limitation in use of I^2C Interface

The I^2C interface does not support the following features.

(1) No operation in Hs Mode (max: 3.4MHz).
The AK4601 Supports Fast mode (max: 400kHz) and Fast plus mode (max: 1MHz).

Note 54. Do not turn off the power of the AK4601 whenever the power supplies of other devices of the same system are turned on. Pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage. (The diodes against TVDD exist in the SDA and SCL pins.)

■ Mixer

The AK4601 has two stereo input mixers that have level adjustment function for overflow protection after adding and data change function (Mixer A and Mixer B). Level adjustment is processed by shift operation. Since the level adjustment function is only for avoiding overflow by adding, it can only shift 1bit to the right.

Mixer A is controlled by SFTA1[1:0] bits, SFTA2[1:0] bits, SWPA1[1:0] bits and SWPA2[1:0] bits.
Mixer B is controlled by SFTB1[1:0] bits, SFTB2[1:0] bits, SWPB1[1:0] bits and SWPB2[1:0] bits.

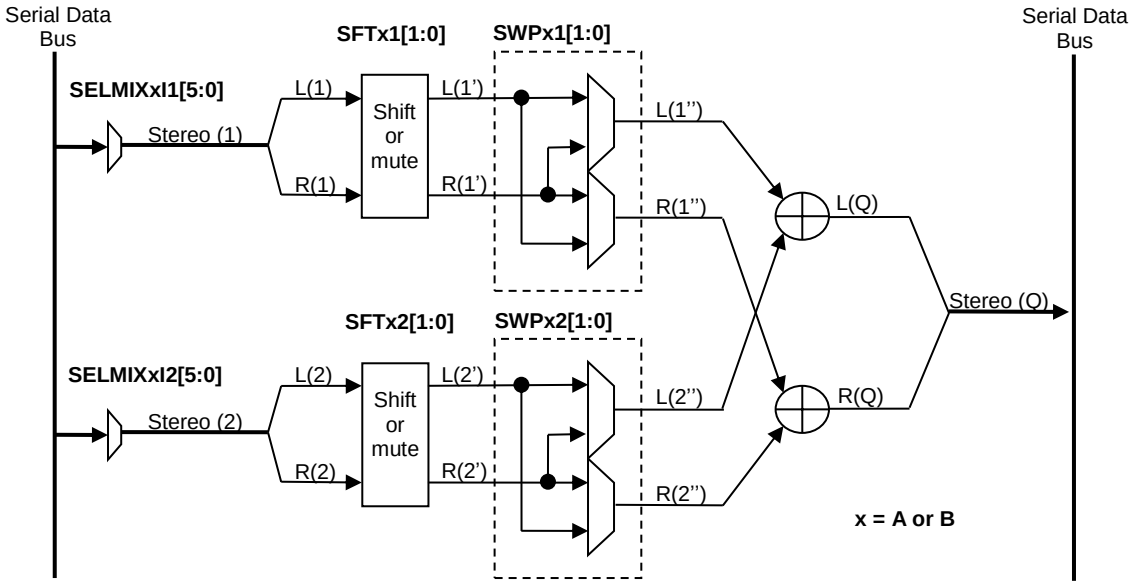


Figure 65. Block Diagram of the Mixer

Mode	SFTA1[1:0] / SFTA2[1:0] bits SFTB1[1:0] / SFTB2[1:0] bits	Shift Amount	L(y') (y=1 or 2)	R(y') (y=1 or 2)	Comment
0	00	No Shift	L(y)	R(y)	0dB
1	01	1 bit Right Shift	L(y) >> 1	R(y) >>1	About -6dB (x 1/2)
2	10	Mute	0	0	-∞dB
3	11				

Table 34. Level Adjustment of the Mixer

Mode	SWPA1[1:0] / SWPA2[1:0] bits SWPB1[1:0] / SWPB2[1:0] bits	L(y'') (y=1 or 2)	R(y'') (y=1 or 2)	Comment
0	00	L(y')	R(y')	Through
1	01	L(y')	L(y')	Lin → Lout, Rout
2	10	R(y')	R(y')	Rin → Lout, Rout
3	11	R(y')	L(y')	Swap Signal Lin → Rout Rin → Lout

Table 35. Data Change Function of the Mixer

■ Vol

The AK4601 has three digital volume circuits (+12~-115dB, 0.5dB steps) that have independent Lch and Rch.

VOL1 Lch VOL1L[7:0]	VOL1 Rch VOL1R[7:0]	VOL2 Lch VOL2L[7:0]	VOL2 Rch VOL2R[7:0]	VOL3 Lch VOL3L[7:0]	VOL3 Rch VOL3R[7:0]	Attenuation Level	
00h	00h	00h	00h	00h	00h	+12.0dB	
01h	01h	01h	01h	01h	01h	+11.5dB	
02h	02h	02h	02h	02h	02h	+11.0dB	
:	:	:	:	:	:	:	
17h	17h	17h	17h	17h	17h	+0.5dB	
18h	18h	18h	18h	18h	18h	0.0dB	(default)
19h	19h	19h	19h	19h	19h	-0.5dB	
:	:	:	:	:	:	:	
FDh	FDh	FDh	FDh	FDh	FDh	-114.5dB	
FEh	FEh	FEh	FEh	FEh	FEh	-115.0dB	
FFh	FFh	FFh	FFh	FFh	FFh	Mute (-∞)	

Table 36. Digital Volume Settings

ATSPVOL bit controls transition time between setting values of the volume.

MODE	ATSPVOL	ATT speed	
0	0	4/fs	(default)
1	1	16/fs	

Table 37. Volume Transition Time

When changing output levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. In Mode 0, it takes 1020/fs (21.3ms@fs=48kHz) from 18H(0dB) to FFH(MUTE). If the PDN pin goes to “L”, each channel of volume circuit is initialized to 18H.

ATSPVOL	00h ↔ FFh Transition Time				
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	1020/fs	21.3ms	23.1ms	127.5ms	(default)
1	4080/fs	85.0ms	92.5ms	510.0ms	

Table 38. Volume Transition Time between 00h and FFh

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	DB	code	dB
00h	12.0	20h	-4.0	40h	-20.0	60h	-36.0	80h	-52.0	A0h	-68.0	C0h	-84.0	E0h	-100.0
01h	11.5	21h	-4.5	41h	-20.5	61h	-36.5	81h	-52.5	A1h	-68.5	C1h	-84.5	E1h	-100.5
02h	11.0	22h	-5.0	42h	-21.0	62h	-37.0	82h	-53.0	A2h	-69.0	C2h	-85.0	E2h	-101.0
03h	10.5	23h	-5.5	43h	-21.5	63h	-37.5	83h	-53.5	A3h	-69.5	C3h	-85.5	E3h	-101.5
04h	10.0	24h	-.6.0	44h	-22.0	64h	-38.0	84h	-54.0	A4h	-70.0	C4h	-86.0	E4h	-102.0
05h	9.5	25h	-6.5	45h	-22.5	65h	-38.5	85h	-54.5	A5h	-70.5	C5h	-86.5	E5h	-102.5
06h	9.0	26h	-7.0	46h	-23.0	66h	-39.0	86h	-55.0	A6h	-71.0	C6h	-87.0	E6h	-103.0
07h	8.5	27h	-7.5	47h	-23.5	67h	-39.5	87h	-55.5	A7h	-71.5	C7h	-87.5	E7h	-103.5
08h	8.0	28h	-8.0	48h	-24.0	68h	-40.0	88h	-56.0	A8h	-72.0	C8h	-88.0	E8h	-104.0
09h	7.5	29h	-8.5	49h	-24.5	69h	-40.5	89h	-56.5	A9h	-72.5	C9h	-88.5	E9h	-104.5
0Ah	7.0	2Ah	-9.0	4Ah	-25.0	6Ah	-41.0	8Ah	-57.0	AAh	-73.0	CAh	-89.0	EAh	-105.0
0Bh	6.5	2Bh	-9.5	4Bh	-25.5	6Bh	-41.5	8Bh	-57.5	ABh	-73.5	CBh	-89.5	EBh	-105.5
0Ch	6.0	2Ch	-10.0	4Ch	-26.0	6Ch	-42.0	8Ch	-58.0	ACh	-74.0	CCh	-90.0	ECh	-106.0
0Dh	5.5	2Dh	-10.5	4Dh	-26.5	6Dh	-42.5	8Dh	-58.5	ADh	-74.5	CDh	-90.5	EDh	-106.5
0Eh	5.0	2Eh	-11.0	4Eh	-27.0	6Eh	-43.0	8Eh	-59.0	AEh	-75.0	CEh	-91.0	EEh	-107.0
0Fh	4.5	2Fh	-11.5	4Fh	-27.5	6Fh	-43.5	8Fh	-59.5	AFh	-75.5	CFh	-91.5	EFh	-107.5
10h	4.0	30h	-12.0	50h	-28.0	70h	-44.0	90h	-60.0	B0h	-76.0	D0h	-92.0	F0h	-108.0
11h	3.5	31h	-12.5	51h	-28.5	71h	-44.5	91h	-60.5	B1h	-76.5	D1h	-92.5	F1h	-108.5
12h	3.0	32h	-13.0	52h	-29.0	72h	-45.0	92h	-61.0	B2h	-77.0	D2h	-93.0	F2h	-109.0
13h	2.5	33h	-13.5	53h	-29.5	73h	-45.5	93h	-61.5	B3h	-77.5	D3h	-93.5	F3h	-109.5
14h	2.0	34h	-14.0	54h	-30.0	74h	-46.0	94h	-62.0	B4h	-78.0	D4h	-94.0	F4h	-110.0
15h	1.5	35h	-14.5	55h	-30.5	75h	-46.5	95h	-62.5	B5h	-78.5	D5h	-94.5	F5h	-110.5
16h	1.0	36h	-15.0	56h	-31.0	76h	-47.0	96h	-63.0	B6h	-79.0	D6h	-95.0	F6h	-111.0
17h	0.5	37h	-15.5	57h	-31.5	77h	-47.5	97h	-63.5	B7h	-79.5	D7h	-95.5	F7h	-111.5
18h	0.0	38h	-16.0	58h	-32.0	78h	-48.0	98h	-64.0	B8h	-80.0	D8h	-96.0	F8h	-112.0
19h	-0.5	39h	-16.5	59h	-32.5	79h	-48.5	99h	-64.5	B9h	-80.5	D9h	-96.5	F9h	-112.5
1Ah	-1.0	3Ah	-17.0	5Ah	-33.0	7Ah	-49.0	9Ah	-65.0	BAh	-81.0	DAh	-97.0	FAh	-113.0
1Bh	-1.5	3Bh	-17.5	5Bh	-33.5	7Bh	-49.5	9Bh	-65.5	BBh	-81.5	DBh	-97.5	FBh	-113.5
1Ch	-2.0	3Ch	-18.0	5Ch	-34.0	7Ch	-50.0	9Ch	-66.0	BCh	-82.0	DCh	-98.0	FCh	-114.0
1Dh	-2.5	3Dh	-18.5	5Dh	-34.5	7Dh	-50.5	9Dh	-66.5	BDh	-82.5	DDh	-98.5	FDh	-114.5
1Eh	-3.0	3Eh	-19.0	5Eh	-35.0	7Eh	-51.0	9Eh	-67.0	BEh	-83.0	DEh	-99.0	FEh	-115.0
1Fh	-3.5	3Fh	-19.5	5Fh	-35.5	7Fh	-51.5	9Fh	-67.5	BFh	-83.5	DFh	-99.5	FFh	Mute

Table 39. Digital Volume Level Setting of the VOL Circuit

■ Analog Input Blcok

1. Microphone Input Gain

The AK4601 has gain amplifiers for microphone input. The gain of L and R channels can be independently selected by MGNL[3:0] and MGNR[3:0] bits (Table 40). The input impedance is typ. 20kΩ@ADC1VL/R bit = “0” and typ. 25kΩ@ADC1VL/R bit = “1”. This gain amplifier executes zero crossing detection when changing the gain by setting MICLZCE bit = “1” / MICRZCE bit = “1”. Zero crossing detection is executed independently for L and R channels. Zero crossing timeout period is 16ms@fs=48kHz. When MICLZCE bit = “0”/ MICRZCE bit = “0”, the volume is changed immediately by register settings.

When writing to MGNL/R[3:0] bits continuously, take an interval of zero crossing timeout period or more. If the MGNL/R[3:0] bits are changed before zero crossing, the volume of Lch and Rch may differ. When the volume level that is same as the present volume is set, the zero crossing counter is not reset and time outs according to the previous writing timing. Therefore, in this case, writing to MGNL/R [3:0] bits continuously is possible with a shorter interval of the zero crossing timeout period.

1-1. Microphone Input Selector

Mode	MGNL[3] MGNR[3]	MGNL[2] MGNR[2]	MGNL[1] MGNR[1]	MGNL[0] MGNR[0]	Input Gain	
0	0	0	0	0	0dB	(default)
1	0	0	0	1	2dB	
2	0	0	1	0	4dB	
3	0	0	1	1	6dB	
4	0	1	0	0	8dB	
5	0	1	0	1	10dB	
6	0	1	1	0	12dB	
7	0	1	1	1	14dB	
8	1	0	0	0	16dB	
9	1	0	0	1	18dB	
A	1	0	1	0	21dB	
B	1	0	1	1	24dB	
C	1	1	0	0	27dB	
D	1	1	0	1	30dB	
E	1	1	1	0	33dB	
F	1	1	1	1	36dB	

Table 40. Microphone Input Gain

1-2. Zero Crossing Timeout

The microphone gain is changed independently on the timing of zero crossing detection or zero crossing timeout.

	PLL_MCLK	Zero Crossing Timeout Period
48kHz base	122.880MHz	16.0ms
44.1kHz base	112.986MHz	17.4ms

Table 41. Zero Crossing Timeout Period

1-3. Start-up Time of MIC Input Pin

The AK4601 starts to charge a DC cut capacitor when the PDN pin is set to “H” from “L”. Since the input impedance is 25kΩ, the time constant will be 25ms if the DC cut capacitor is 1μF. A wait time of about 100ms should be taken before power up the ADC to charge the DC cut capacitor sufficiently. A click noise may occur just after the ADC is powered up if this wait time is not enough.

2. Microphone Input Selector

The AK4601 has microphone input selectors. Each microphone amplifier input is selectable between single-ended input and differential input by AD1LSEL bit or AD1RSEL bit.

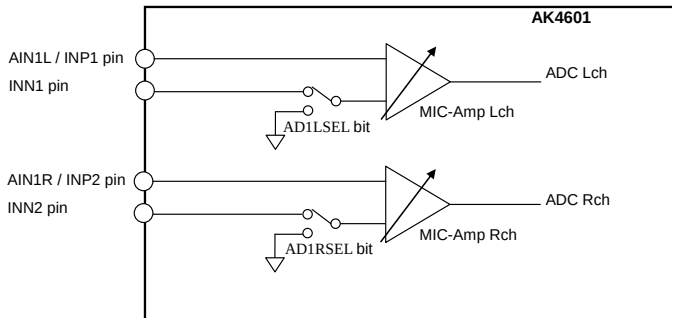


Figure 66. Microphone Input Selector

AD1LSEL bit	ADC Lch
0	INP1/INN1 (default)
1	AIN1L

AD1RSEL bit	ADC Rch
0	INP2/INN2 (default)
1	AIN1R

Table 42. Microphone Input Selector

3. Microphone Bias Output

The AK4601 has two lines of microphone bias outputs. The power supply of microphones are supplied from the MPWR1 pin and the MPWR2 pin by setting PMMB1 bit = “1” and PMMB2 bit = “1”, respectively. The output voltage is 2.5V (AVDD=3.3V) and the load resistance is min. 2kΩ.

PMMB1 bit	MPWR1 pin
0	Hi-Z (default)
1	Output

PMMB2bit	MPWR2 pin
0	Hi-Z (default)
1	Output

Table 43. Microphone Bias Output

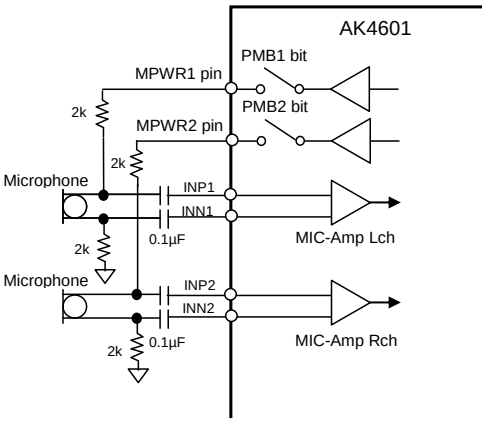


Figure 67. MIC Block Circuit (Differential Input)

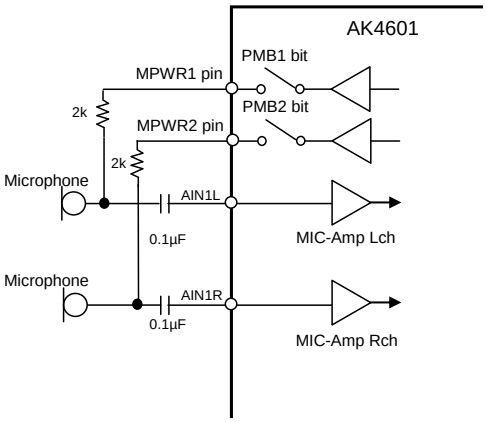


Figure 68. MIC Block Circuit (Single-end Input)

■ ADC Block (ADC1, ADC2, ADCM)

1. ADC Block High Pass Filter

The AK4601 has a digital high pass filter (HPF) for DC offset cancelling of each ADC. The cut-off frequency of the HPF is about 0.93Hz (fs=48kHz), depending on operation frequency.

fs	48kHz	44.1kHz	8kHz
Cut-off Frequency	0.93Hz	0.86Hz	0.16Hz

Table 44. HPF Cut-off Frequency

2. ADC Digital Volume

The AK4601 has independent digital volume controls for Lch and Rch (256 levels, 0.5dB steps) of each ADC.

ADC1 VOLAD1L[7:0]	ADC1 VOLAD1R[7:0]	ADC2 VOLAD2L[7:0]	ADC2 VOLAD2R[7:0]	ADCM VOLADM[7:0]	Attenuation Level	
00h	00h	00h	00h	00h	+24.0dB	
01h	01h	01h	01h	01h	+23.5dB	
02h	02h	02h	02h	02h	+23.0dB	
:	:	:	:	:	:	
2Fh	2Fh	2Fh	2Fh	2Fh	+0.5dB	
30h	30h	30h	30h	30h	0.0dB	(default)
31h	31h	31h	31h	31h	-0.5dB	
:	:	:	:	:	:	
FDh	FDh	FDh	FDh	FDh	-102.5dB	
FEh	FEh	FEh	FEh	FEh	-103.0dB	
FFh	FFh	FFh	FFh	FFh	Mute (-∞)	

Table 45. ADC Digital Volume Control Setting

The transition time between set values is selected by ATSPAD bit.

Mode	ATSPAD bit	ATT speed	
0	0	4/fs	(default)
1	1	16/fs	

Table 46. ADC Volume Level Transition Time

When changing output levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. In Mode 0, it takes 1020/fs (21.3ms@fs=48kHz) from 00H(0dB) to FFH(MUTE). If the PDN pin goes to “L”, each channel of the ADC is initialized to 30H.

ATSPAD bit	00h ↔ FFh Transition Time				
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	1020/fs	21.3ms	23.1ms	127.5ms	(default)
1	4080/fs	85.0ms	92.5ms	510.0ms	

Table 47. ADC Volume Transition Time between 00h and FFh

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	dB
00h	24.0	20h	8.0	40h	-8.0	60h	-24.0	80h	-40.0	A0h	-56.0	C0h	-72.0	E0h	-88.0
01h	23.5	21h	7.5	41h	-8.5	61h	-24.5	81h	-40.5	A1h	-56.5	C1h	-72.5	E1h	-88.5
02h	23.0	22h	7.0	42h	-9.0	62h	-25.0	82h	-41.0	A2h	-57.0	C2h	-73.0	E2h	-89.0
03h	22.5	23h	6.5	43h	-9.5	63h	-25.5	83h	-41.5	A3h	-57.5	C3h	-73.5	E3h	-89.5
04h	22.0	24h	6.0	44h	-10.0	64h	-26.0	84h	-42.0	A4h	-58.0	C4h	-74.0	E4h	-90.0
05h	21.5	25h	5.5	45h	-10.5	65h	-26.5	85h	-42.5	A5h	-58.5	C5h	-74.5	E5h	-90.5
06h	21.0	26h	5.0	46h	-11.0	66h	-27.0	86h	-43.0	A6h	-59.0	C6h	-75.0	E6h	-91.0
07h	20.5	27h	4.5	47h	-11.5	67h	-27.5	87h	-43.5	A7h	-59.5	C7h	-75.5	E7h	-91.5
08h	20.0	28h	4.0	48h	-12.0	68h	-28.0	88h	-44.0	A8h	-60.0	C8h	-76.0	E8h	-92.0
09h	19.5	29h	3.5	49h	-12.5	69h	-28.5	89h	-44.5	A9h	-60.5	C9h	-76.5	E9h	-92.5
0Ah	19.0	2Ah	3.0	4Ah	-13.0	6Ah	-29.0	8Ah	-45.0	AAh	-61.0	CAh	-77.0	EAh	-93.0
0Bh	18.5	2Bh	2.5	4Bh	-13.5	6Bh	-29.5	8Bh	-45.5	ABh	-61.5	CBh	-77.5	EBh	-93.5
0Ch	18.0	2Ch	2.0	4Ch	-14.0	6Ch	-30.0	8Ch	-46.0	ACh	-62.0	CCh	-78.0	ECh	-94.0
0Dh	17.5	2Dh	1.5	4Dh	-14.5	6Dh	-30.5	8Dh	-46.5	ADh	-62.5	CDh	-78.5	EDh	-94.5
0Eh	17.0	2Eh	1.0	4Eh	-15.0	6Eh	-31.0	8Eh	-47.0	AEh	-63.0	CEh	-79.0	EEh	-95.0
0Fh	16.5	2Fh	0.5	4Fh	-15.5	6Fh	-31.5	8Fh	-47.5	AFh	-63.5	CFh	-79.5	EFh	-95.5
10h	16.0	30h	0.0	50h	-16.0	70h	-32.0	90h	-48.0	B0h	-64.0	D0h	-80.0	F0h	-96.0
11h	15.5	31h	-0.5	51h	-16.5	71h	-32.5	91h	-48.5	B1h	-64.5	D1h	-80.5	F1h	-96.5
12h	15.0	32h	-1.0	52h	-17.0	72h	-33.0	92h	-49.0	B2h	-65.0	D2h	-81.0	F2h	-97.0
13h	14.5	33h	-1.5	53h	-17.5	73h	-33.5	93h	-49.5	B3h	-65.5	D3h	-81.5	F3h	-97.5
14h	14.0	34h	-2.0	54h	-18.0	74h	-34.0	94h	-50.0	B4h	-66.0	D4h	-82.0	F4h	-98.0
15h	13.5	35h	-2.5	55h	-18.5	75h	-34.5	95h	-50.5	B5h	-66.5	D5h	-82.5	F5h	-98.5
16h	13.0	36h	-3.0	56h	-19.0	76h	-35.0	96h	-51.0	B6h	-67.0	D6h	-83.0	F6h	-99.0
17h	12.5	37h	-3.5	57h	-19.5	77h	-35.5	97h	-51.5	B7h	-67.5	D7h	-83.5	F7h	-99.5
18h	12.0	38h	-4.0	58h	-20.0	78h	-36.0	98h	-52.0	B8h	-68.0	D8h	-84.0	F8h	-100.0
19h	11.5	39h	-4.5	59h	-20.5	79h	-36.5	99h	-52.5	B9h	-68.5	D9h	-84.5	F9h	-100.5
1Ah	11.0	3Ah	-5.0	5Ah	-21.0	7Ah	-37.0	9Ah	-53.0	BAh	-69.0	DAh	-85.0	FAh	-101.0
1Bh	10.5	3Bh	-5.5	5Bh	-21.5	7Bh	-37.5	9Bh	-53.5	BBh	-69.5	DBh	-85.5	FBh	-101.5
1Ch	10.0	3Ch	-.6.0	5Ch	-22.0	7Ch	-38.0	9Ch	-54.0	BCh	-70.0	DCh	-86.0	FCh	-102.0
1Dh	9.5	3Dh	-6.5	5Dh	-22.5	7Dh	-38.5	9Dh	-54.5	BDh	-70.5	DDh	-86.5	FDh	-102.5
1Eh	9.0	3Eh	-7.0	5Eh	-23.0	7Eh	-39.0	9Eh	-55.0	BEh	-71.0	DEh	-87.0	FEh	-103.0
1Fh	8.5	3Fh	-7.5	5Fh	-23.5	7Fh	-39.5	9Fh	-55.5	BFh	-71.5	DFh	-87.5	FFh	Mute

Table 48. ADC Digital Volume Level Setting

3. ADC Soft Mute

The ADC block has a digital soft mute circuit. The soft mute operation is performed at digital domain. The output signal is attenuated to -∞ in "ATT setting level x ATT transition time" from the current ADC digital volume setting level by setting AD1MUTE bit, AD2MUTE bit or ADMMUTE bit to "1". When the AD1MUTE bit, AD2MUTE bit or ADMMUTE bit returns to "0", the mute is cancelled and the output attenuation level gradually changes to ATT setting level in "ATT setting level x ATT transition time". If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and the volume level returns to original volume setting level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

The attenuation level transition takes 828/fs from 0dB to -∞ and from -∞ to 0dB. Soft mute function is available when each ADC is in operation. The attenuation value is initialized by setting the PDN pin = "L".

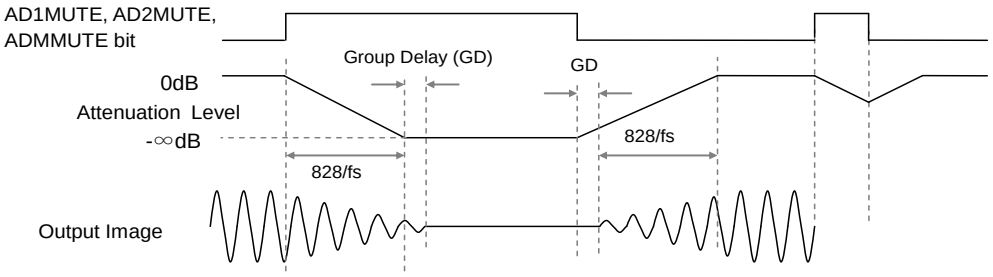


Figure 69. ADC Soft Mute

4. ADC Input Selector

ADC2 of the AK4601 has an input selector for 1 stereo differential input or 2 stereo single-ended inputs, and 1 stereo semi-differential input. Differential or single-ended input can be selected for the ADCM. These inputs are selected by AD2SEL[1:0] bits and ADMSEL bit. In the case that these registers are changed during operation, mute output signal to reduce switching noise as needed.

Mode	AD2SEL[1:0] bits	Selected Pins	
0	00	AIN2LP, AIN2LN, AIN2RP, AIN2RN	(default)
1	01	AIN3L, AIN3R	
2	10	AIN4L, AIN4R	
3	11	AIN5L, AIN5R, GNDIN5	

Table 49. ADC2 Input Select

Mode	ADMSEL bit	Selected Pins	
0	0	Differential (AINMP, AINMN)	(default)
1	1	Single-ended (AINM)	

Table 50. ADCM Input Select

4-1. Input Selector Switching Sequence

The input selector should be changed after enabling soft mute function to reduce the switching noise of the input selector.

ADC2 Input selector switching sequence:
1) Enable Soft Mute Function before Changing Channel
2) Change Channel
3) Disable Soft Mute Function

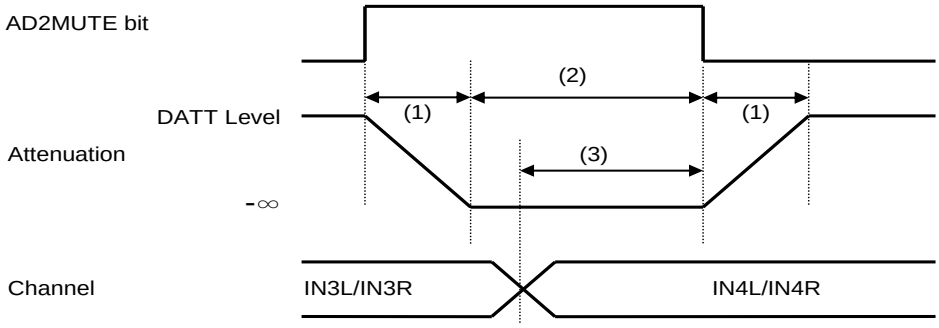


Figure 70. ADC2 Input Channel Switching Sequence Example

The period of (1) varies according to the setting value of the DATT level. Transition time of attenuation level from 0dB to -∞ is shown below.

ATSPAD	(1) Period (max)				
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	828/fs	17.25ms	18.78ms	103.5ms	(default)
1	828/fs x 4	69ms	75.10ms	414ms	

The input channel should be changed during the period (2). An interval around 200ms is needed before releasing the soft mute after changing the channel (period (3)).

5. ADC Digital Filter Select

The AK4601 has four kinds of digital filters in ADC block. ADSD and ADSL bits select a digital filter.

Mode	ADSD bit	ADSL bit	Digital Filter	
0	0	0	Sharp Roll-Off Filter	(default)
1	0	1	Slow Roll-Off Filter	
2	1	0	Short Delay Sharp Roll-Off Filter	
3	1	1	Short Delay Slow Roll-Off Filter	

Table 51. ADC Digital Filter Select

6. ADC Full Scale Voltage

Single-ended input amplitude (differential input amplitude) of ADC1 L/Rch, ADC2 L/Rch and ADCM can be switched between 2.3Vpp (±2.3Vpp) and 2.83Vpp (±2.83Vpp) by ADC1VL/R bit, ADC2VL/R bit and ADCMV bit, respectively (Table 52).

Mode	ADC1VL, ADC1VR, ADC2VL, ADC2VR, ADCMV	Full Scale		
		Single-end	Differential	
0	0	2.3Vpp	±2.3Vpp	(default)
1	1	2.83Vpp	±2.83Vpp	

Table 52. ADC Input Voltage

■ DAC Block (DAC1, DAC2 and DAC3)

1. DAC Digital Volume

The AK4601 has channel-independent digital volume controls in DAC block. (256 levels, 0.5 steps)

DAC1 Lch VOLDA1L[7:0]	DAC1 Rch VOLDA1R[7:0]	DAC2 Lch VOLDA2L[7:0]	DAC2 Rch VOLDA2R[7:0]	DAC3 Lch VOLDA3L[7:0]	DAC3 Rch VOLDA3R[7:0]	Attenuation Level	
00h	00h	00h	00h	00h	00h	+12.0dB	
01h	01h	01h	01h	01h	01h	+11.5dB	
02h	02h	02h	02h	02h	02h	+11.0dB	
:	:	:	:	:	:	:	
17h	17h	17h	17h	17h	17h	+0.5dB	
18h	18h	18h	18h	18h	18h	0.0dB	(default)
19h	19h	19h	19h	19h	19h	-0.5dB	
:	:	:	:	:	:	:	
FDh	FDh	FDh	FDh	FDh	FDh	-114.5dB	
FEh	FEh	FEh	FEh	FEh	FEh	-115.0dB	
FFh	FFh	FFh	FFh	FFh	FFh	Mute (-∞)	

Table 53. DAC Digital Volume Setting

Transition time between set values can be selected by ATSPDA bit.

MODE	ATSPDA	ATT speed	
0	0	4/fs	(default)
1	1	16/fs	

Table 54. DAC Volume Transition Time Setting

When changing output levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. In Mode 0, it takes 1020/fs (21.3ms@fs=48kHz) from 00H(0dB) to FFH(MUTE). If the PDN pin goes to “L”, each channel of the DAC is initialized to 18H.

ATSPDA	00h ↔ FFh Transition Time				
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	1020/fs	21.3ms	23.1ms	127.5ms	(default)
1	4080/fs	85.0ms	92.5ms	510.0ms	

Table 55. DAC Volume Transition Time between 00h and FFh

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	DB	code	dB
00h	12.0	20h	-4.0	40h	-20.0	60h	-36.0	80h	-52.0	A0h	-68.0	C0h	-84.0	E0h	-100.0
01h	11.5	21h	-4.5	41h	-20.5	61h	-36.5	81h	-52.5	A1h	-68.5	C1h	-84.5	E1h	-100.5
02h	11.0	22h	-5.0	42h	-21.0	62h	-37.0	82h	-53.0	A2h	-69.0	C2h	-85.0	E2h	-101.0
03h	10.5	23h	-5.5	43h	-21.5	63h	-37.5	83h	-53.5	A3h	-69.5	C3h	-85.5	E3h	-101.5
04h	10.0	24h	-.6.0	44h	-22.0	64h	-38.0	84h	-54.0	A4h	-70.0	C4h	-86.0	E4h	-102.0
05h	9.5	25h	-6.5	45h	-22.5	65h	-38.5	85h	-54.5	A5h	-70.5	C5h	-86.5	E5h	-102.5
06h	9.0	26h	-7.0	46h	-23.0	66h	-39.0	86h	-55.0	A6h	-71.0	C6h	-87.0	E6h	-103.0
07h	8.5	27h	-7.5	47h	-23.5	67h	-39.5	87h	-55.5	A7h	-71.5	C7h	-87.5	E7h	-103.5
08h	8.0	28h	-8.0	48h	-24.0	68h	-40.0	88h	-56.0	A8h	-72.0	C8h	-88.0	E8h	-104.0
09h	7.5	29h	-8.5	49h	-24.5	69h	-40.5	89h	-56.5	A9h	-72.5	C9h	-88.5	E9h	-104.5
0Ah	7.0	2Ah	-9.0	4Ah	-25.0	6Ah	-41.0	8Ah	-57.0	AAh	-73.0	CAh	-89.0	EAh	-105.0
0Bh	6.5	2Bh	-9.5	4Bh	-25.5	6Bh	-41.5	8Bh	-57.5	ABh	-73.5	CBh	-89.5	EBh	-105.5
0Ch	6.0	2Ch	-10.0	4Ch	-26.0	6Ch	-42.0	8Ch	-58.0	ACh	-74.0	CCh	-90.0	ECh	-106.0
0Dh	5.5	2Dh	-10.5	4Dh	-26.5	6Dh	-42.5	8Dh	-58.5	ADh	-74.5	CDh	-90.5	EDh	-106.5
0Eh	5.0	2Eh	-11.0	4Eh	-27.0	6Eh	-43.0	8Eh	-59.0	AEh	-75.0	CEh	-91.0	EEh	-107.0
0Fh	4.5	2Fh	-11.5	4Fh	-27.5	6Fh	-43.5	8Fh	-59.5	AFh	-75.5	CFh	-91.5	EFh	-107.5
10h	4.0	30h	-12.0	50h	-28.0	70h	-44.0	90h	-60.0	B0h	-76.0	D0h	-92.0	F0h	-108.0
11h	3.5	31h	-12.5	51h	-28.5	71h	-44.5	91h	-60.5	B1h	-76.5	D1h	-92.5	F1h	-108.5
12h	3.0	32h	-13.0	52h	-29.0	72h	-45.0	92h	-61.0	B2h	-77.0	D2h	-93.0	F2h	-109.0
13h	2.5	33h	-13.5	53h	-29.5	73h	-45.5	93h	-61.5	B3h	-77.5	D3h	-93.5	F3h	-109.5
14h	2.0	34h	-14.0	54h	-30.0	74h	-46.0	94h	-62.0	B4h	-78.0	D4h	-94.0	F4h	-110.0
15h	1.5	35h	-14.5	55h	-30.5	75h	-46.5	95h	-62.5	B5h	-78.5	D5h	-94.5	F5h	-110.5
16h	1.0	36h	-15.0	56h	-31.0	76h	-47.0	96h	-63.0	B6h	-79.0	D6h	-95.0	F6h	-111.0
17h	0.5	37h	-15.5	57h	-31.5	77h	-47.5	97h	-63.5	B7h	-79.5	D7h	-95.5	F7h	-111.5
18h	0.0	38h	-16.0	58h	-32.0	78h	-48.0	98h	-64.0	B8h	-80.0	D8h	-96.0	F8h	-112.0
19h	-0.5	39h	-16.5	59h	-32.5	79h	-48.5	99h	-64.5	B9h	-80.5	D9h	-96.5	F9h	-112.5
1Ah	-1.0	3Ah	-17.0	5Ah	-33.0	7Ah	-49.0	9Ah	-65.0	BAh	-81.0	DAh	-97.0	FAh	-113.0
1Bh	-1.5	3Bh	-17.5	5Bh	-33.5	7Bh	-49.5	9Bh	-65.5	BBh	-81.5	DBh	-97.5	FBh	-113.5
1Ch	-2.0	3Ch	-18.0	5Ch	-34.0	7Ch	-50.0	9Ch	-66.0	BCh	-82.0	DCh	-98.0	FCh	-114.0
1Dh	-2.5	3Dh	-18.5	5Dh	-34.5	7Dh	-50.5	9Dh	-66.5	BDh	-82.5	DDh	-98.5	FDh	-114.5
1Eh	-3.0	3Eh	-19.0	5Eh	-35.0	7Eh	-51.0	9Eh	-67.0	BEh	-83.0	DEh	-99.0	FEh	-115.0
1Fh	-3.5	3Fh	-19.5	5Fh	-35.5	7Fh	-51.5	9Fh	-67.5	BFh	-83.5	DFh	-99.5	FFh	Mute

Table 56. DAC Digital Volume Level Setting

2. DAC Soft Mute

The DAC block has a digital soft mute circuit. The soft mute operation is performed at digital domain. The output signal is attenuated to -∞ in “ATT setting level x ATT transition time” from the current DAC digital volume setting level by setting DA1MUTE bit, DA2MUTE bit or DA3MUTE bit to “1”. When the DA1MUTE bit, DA2MUTE bit or DA3MUTE bit returns to “0”, the mute is cancelled and the output attenuation level gradually changes to ATT setting level in “ATT setting level x ATT transition time”. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and the volume level returns to original volume setting level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

The attenuation level transition takes 924/fs from 0dB to -∞ and from -∞ to 0dB. Soft mute function is available when each DAC is in operation. The attenuation value is initialized by setting the PDN pin = “L”.

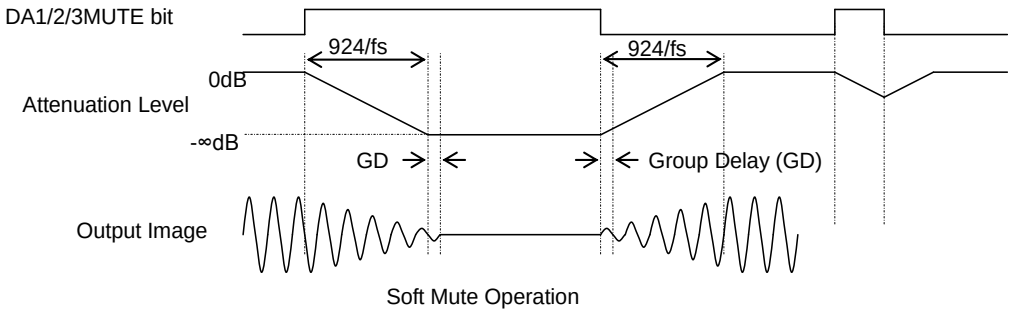


Figure 71. DAC Sof Mute Operation

The analog output pin will be in a mode that outputs VCOM voltage by changing HRESETN pin to “0” from “1” while PMDA bit = “1” when changing system clock during DAC operation. This mode can prevent a click noise when the DAC resumes operation after changing the system clock (Figure 72, CASE1). The analog output will be Hi-z state when changing HRESETN to “0” from “1” while PMDA bit = “0”. A click noise may occur when resuming the DAC operation after the system clock is changed (Figure 72, CASE2).

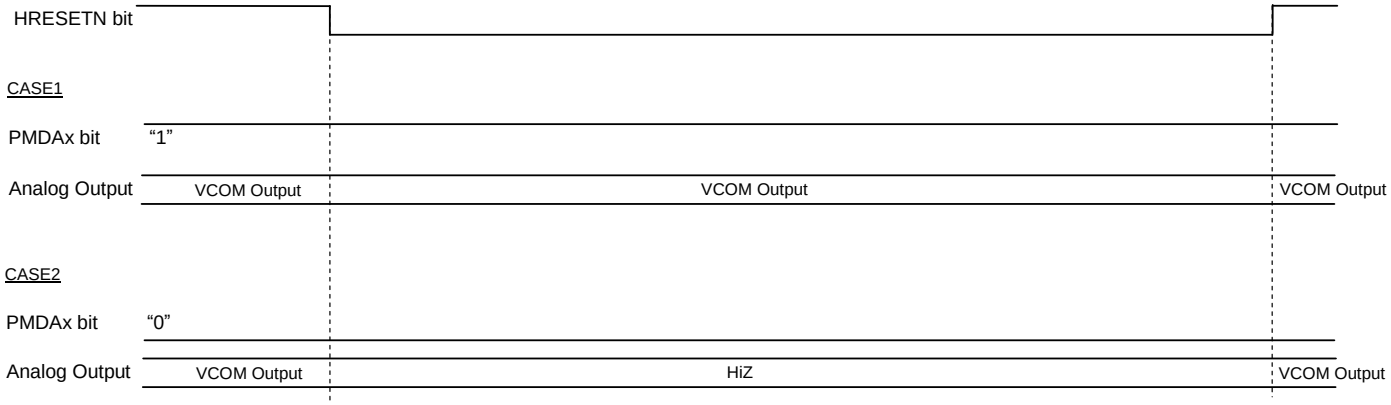


Figure 72. Analog Output in HUB Reset

3. DAC Digital Filter Select

The AK4601 has four kinds of digital filters in DAC block. DASD and DASL bits select a digital filter.

Mode	DASD bit	DASL bit	Digital Filter	
0	0	0	Sharp Roll-Off Filter	
1	0	1	Slow Roll-Off Filter	
2	1	0	Short Delay Sharp Roll-Off Filter	(default)
3	1	1	Short Delay Slow Roll-Off Filter	

Table 57. DAC Digital Filter Select

4. De-emphasis Filter Control

The AK4601 has a digital de-emphasis filter (tc=50/15μs) which corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz) by IIR filter. It is enabled or disabled with the DEMx[1:0] bits (x=1~3) (Table 58).

DEMx[1] bit	DEMx[0] bit	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 58. De-emphasis Filter Control

The de-emphasis filer only corresponds to the frequencies shown in Table 58. DEMx[1:0] bits must be set to the default setting “01” when the AK4601 is operated with other sampling frequencies.

• In the case that the AK4601 is operated with a sampling frequency other than shown in Table 58. The frequency characteristics of the de-emphasis filter will track the sampling frequency of the actual operation.

(e.g. The cut-off frequency exists around 1kHz in 48kHz mode, around 2kHz in 96kHz mode and around 0.5kHz in 24kHz mode.)

■ Register Map

Control registers can be initialized by a power-down release (PDN pin = “L” → “H”).
Do not write to registers in the address after 008CH and write "0" into 0 bits and write "1" into 1 bit.

Normal Registers

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0000	System Clock Setting 1	REFSEL[2:0]			REFMODE[4:0]					00
0001	System Clock Setting 2	CKRESETN	0	0	FSMODE[4:0]					00
0002	Mic Bias Power Management	PSW1N	PSW2N	0	0	0	0	PMMB1	PMMB2	00
0003	Sync Domain 1 Setting 1	MSN1	CKS1[2:0]			BDV1[8]	SDV1[2:0]			00
0004	Sync Domain 1 Setting 2	BDV1[7:0]								00
0005	Sync Domain 2 Setting 1	MSN2	CKS2[2:0]			BDV2[8]	SDV2[2:0]			00
0006	Sync Domain 2 Setting 2	BDV2[7:0]								00
0007	Reserved	0								00
0008	Reserved	0								00
0009	Reserved	0								00
000A	Reserved	0								00
000B	Reserved	0								00
000C	Reserved	0								00
000D	Reserved	0								00
000E	Reserved	0								00
000F	CLKO Output Setting	0	0	0	0	CLKOE	CLKOSEL[2:0]			00
0010	Pin Setting	0	0	0	0	0	0	0	MSELN	00
0011	Sync Domain Select 1	0	SDBCK1[2:0]			0	SDBCK2[2:0]			00
0012	Reserved	0								00
0013	Sync Domain Select 3	0	0	0	0	0	EXBCK1[2:0]			00
0014	Sync Domain Select 4	0	EXBCK2[2:0]			0	EXBCK3[2:0]			00
0015	Reserved	0								00
0016	Sync Domain Select 6	0	SDDO1[2:0]			0	SDDO2[2:0]			00
0017	Sync Domain Select 7	0	SDDO3[2:0]			0	0	0	0	00
0018	Sync Domain Select 8	0	0	0	0	0	SDVOL1[2:0]			00
0019	Sync Domain Select 9	0	SDVOL2[2:0]			0	SDVOL3[2:0]			00
001A	Reserved	0								00
001B	Reserved	0								00
001C	Reserved	0								00
001D	Reserved	0								00
001E	Reserved	0								00
001F	Sync Domain Select 15	0	SDMIXA[2:0]			0	SDMIXB[2:0]			00
0020	Sync Domain Select 16	0	SDADC1[2:0]			0	SDCODEC[2:0]			00
0021	SDOUT1 TDM SLOT1-2 Data Select	0	0	SELDO1A[5:0]						00
0022	SDOUT1 TDM SLOT3-4 Data Select	0	0	SELDO1B[5:0]						00
0023	SDOUT1 TDM SLOT5-6 Data Select	0	0	SELDO1C[5:0]						00
0024	SDOUT1 TDM SLOT7-8 Data Select	0	0	SELDO1D[5:0]						00
0025	SDOUT1 TDM SLOT9-10 Data Select	0	0	SELDO1E[5:0]						00
0026	SDOUT1 TDM SLOT11-12 Data Select	0	0	SELDO1F[5:0]						00
0027	SDOUT1 TDM SLOT13-14 Data Select	0	0	SELDO1G[5:0]						00
0028	SDOUT1 TDM SLOT15-16 Data Select	0	0	SELDO1H[5:0]						00
0029	SDOUT2 Output Data Select	0	0	SELDO2[5:0]						00
002A	SDOUT3 Output Data Select	0	0	SELDO3[5:0]						00
002B	Reserved	0								00
002C	Reserved	0								00
002D	Reserved	0								00
002E	Reserved	0								00
002F	Reserved	0								00
0030	Reserved	0								00
0031	Reserved	0								00

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0032	Reserved	0								00
0033	Reserved	0								00
0034	Reserved	0								00
0035	DAC1 Input Data Select	0	0	SELDA1[5:0]						00
0036	DAC2 Input Data Select	0	0	SELDA2[5:0]						00
0037	DAC3 Input Data Select	0	0	SELDA3[5:0]						00
0038	VOL1 Input Data Select	0	0	SELVOL1[5:0]						00
0039	VOL2 Input Data Select	0	0	SELVOL2[5:0]						00
003A	VOL3 Input Data Select	0	0	SELVOL3[5:0]						00
003B	Reserved	0								00
003C	Reserved	0								00
003D	Reserved	0								00
003E	Reserved	0								00
003F	Reserved	0								00
0040	Reserved	0								00
0041	Reserved	0								00
0042	Reserved	0								00
0043	Reserved	0								00
0044	Reserved	0								00
0045	Mixer A Ch1 Input Data Select	0	0	SELMIXAI1[5:0]						00
0046	Mixer A Ch2 Input Data Select	0	0	SELMIXAI2[5:0]						00
0047	Mixer B Ch1 Input Data Select	0	0	SELMIXBI1[5:0]						00
0048	Mixer B Ch2 Input Data Select	0	0	SELMIXBI2[5:0]						00
0049	Reserved	0								00
004A	Reserved	0								00
004B	Reserved	0								00
004C	Clock Format Setting 1	BCKP1	DCF1[2:0]			BCKP2	DCF2[2:0]			00
004D	Reserved	0								00
004E	Reserved	0								00
004F	Reserved	0								00
0050	SDIN1 Digital Input Format	DIEDGEN1	0	DISL1[1:0]		DILSBE1	0	DIDL1[1:0]		00
0051	SDIN2 Digital Input Format	DIEDGEN2	0	DISL2[1:0]		DILSBE2	0	DIDL2[1:0]		00
0052	SDIN3 Digital Input Format	DIEDGEN3	0	DISL3[1:0]		DILSBE3	0	DIDL3[1:0]		00
0053	Reserved	0								00
0054	Reserved	0								00
0055	SDOUT1 Digital Output Format	DOEDGEN1	0	DOSL1[1:0]		DOLSBE1	0	DODL1[1:0]		00
0056	SDOUT2 Digital Output Format	DOEDGEN2	0	DOSL2[1:0]		DOLSBE2	0	DODL2[1:0]		00
0057	SDOUT3 Digital Output Format	DOEDGEN3	0	DOSL3[1:0]		DOLSBE3	0	DODL3[1:0]		00
0058	Reserved	0								00
0059	Reserved	0								00
005A	SDOUT Phase Setting	0	0	0	0	0	SDOPH3	SDOPH2	SDOPH1	00
005B	Reserved	0								00
005C	Reserved	0								00
005D	Reserved	0								00
005E	Output Port Enable Setting	0	0	SDOUT1E	SDOUT2E	SDOUT3E	0	0	0	00
005F	Reserved	0								00
0060	Mixer A Setting	SFTA2[1:0]		SFTA1[1:0]		SWPA2[1:0]		SWPA1[1:0]		00
0061	Mixer B Setting	SFTB2[1:0]		SFTB1[1:0]		SWPB2[1:0]		SWPB1[1:0]		00
0062	MIC AMP Gain	MGNL[3:0]				MGNR[3:0]				00
0063	Analog Input Gain Control	ADC1VL	ADC1VR	ADC2VL	ADC2VR	ADCMV	0	MICLZCE	MICRZCE	00
0064	ADC1 Lch Digital Volume	VOLAD1L[7:0]								30
0065	ADC1 Rch Digital Volume	VOLAD1R[7:0]								30
0066	ADC2 Lch Digital Volume	VOLAD2L[7:0]								30
0067	ADC2 Rch Digital Volume	VOLAD2R[7:0]								30
0068	ADCM Digital Volume	VOLADM[7:0]								30
0069	Reserved	0								00
006A	Reserved	0								00

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
006B	Analog Input Select Setting	ADSD	ADSL	0	ADMSEL	AD1LSEL	AD1RSEL	AD2SEL[1:0]		00
006C	ADC Mute & HPF Control	ATSPAD	AD1MUTE	AD2MUTE	ADMMUTE	0	AD1HPFN	AD2HPFN	ADMHPFN	00
006D	DAC1 Lch Digital Volume	VOLDA1L[7:0]								18
006E	DAC1 Rch Digital Volume	VOLDA1R[7:0]								18
006F	DAC2 Lch Digital Volume	VOLDA2L[7:0]								18
0070	DAC2 Rch Digital Volume	VOLDA2R[7:0]								18
0071	DAC3 Lch Digital Volume	VOLDA3L[7:0]								18
0072	DAC3 Rch Digital Volume	VOLDA3R[7:0]								18
0073	DAC Mute & Filter Setting	ATSPDA	DA1MUTE	DA2MUTE	DA3MUTE	0	DSMN	DASD	DASL	02
0074	DAC DEM Setting	0	0	DEM3[1:0]		DEM2[1:0]		DEM1[1:0]		15
0075	VOL1 Lch Digital Volume	VOL1L[7:0]								18
0076	VOL1 Rch Digital Volume	VOL1R[7:0]								18
0077	VOL2 Lch Digital Volume	VOL2L[7:0]								18
0078	VOL2 Rch Digital Volume	VOL2R[7:0]								18
0079	VOL3 Lch Digital Volume	VOL3L[7:0]								18
007A	VOL3 Rch Digital Volume	VOL3R[7:0]								18
007B	Reserved	0	0	0	1	1	0	0	0	18
007C	Reserved	0	0	0	1	1	0	0	0	18
007D	Reserved	0	0	0	1	1	0	0	0	18
007E	Reserved	0	0	0	1	1	0	0	0	18
007F	VOL Setting	ATSPVOL	0	0	0	0	0	0	0	00
0080	Reserved	0								00
0081	Reserved	0								00
0082	Reserved	0								00
0083	STO Flag Setting 1	0	PLLLOCKE	0	0	0	0	0	0	00
0084	Reserved	0								00
0085	Reserved	0								00
0086	Reserved	0	0	0	0	0	1	0	0	04
0087	Reserved	0	0	0	0	0	0	1	0	02
0088	Reserved	0								00
0089	Reserved	0								00
008A	Power Management 1	0	0	PMAD1	PMAD2	PMADM	PMDA1	PMDA2	PMDA3	00
008B	Reserved	0								00
008C	Reset Control	0	0	1	CRESETN	0	0	0	HRESETN	20

Read Only Registers

Read these registers after Clock reset is released (when PLL is stabilized).

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0100	Reserved	0								00
0101	Reserved	0								00
0102	Status Read Out	0	STO	0	0	0	0	0	0	40

■ Register Definitions

Normal Registers

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0000	System Clock Setting 1	REFSEL[2:0]			REFMODE[4:0]				
R/W		R/W			R/W				
Default		000			00H				

REFSEL[3:0]: PLL Reference Clock Input Pin Setting (Table 4)
Default: “000” (MCKI)

REFMODE[4:0]: PLL Reference Clock Frequency Setting (Table 5)
Default: 00H (256kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0001	System Clock Setting 2	CKRESETN	0		FSMODE[4:0]				
R/W		R/W	R/W	R/W	R/W				
Default		0	0	0	00H				

CKRESETN: Clock Reset
0: Clock Reset (default)
1: Clock Reset Release

FSMODE[4:0]: Operation Sampling Frequency Mode Setting for each Block (Table 12)
Default: 00H (8kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0002	Mic Bias Power Management	PSW1N	PSW2N	0				PMMB1	PMMB2
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PSW1N: Pull-down Setting for BICK1pin / LRCK1 pin (Table 2)
0: Pulled Down (46kΩ) (default)
1: Release

PSW2N: Pull-down Setting for BICK2 pin/ LRCK2 pin (Table 2)
0: Pulled Down (46kΩ) (default)
1: Release

PMMB1: Power Management Setting for MIC Bias Output 1
0: Power Save Mode (default)
1: Normal Operation

PMMB2: Power Management Setting for MIC Bias Output 2
0: Power Save Mode (default)
1: Normal Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0003	Sync Domain 1 Setting 1	MSN1	CKS1[2:0]			BDV1[8]	SDV1[2:0]		
0004	Sync Domain 1 Setting 2	BDV1[7:0]							
R/W		R/W	R/W			R/W	R/W		
Default		0	000			0	000		

MSN1: Slave/Master Mode Setting for BICK1 pin/LRCK1 pin (Table 16)
- 0: Slave Mode (default)
- 1: Master Mode

CKS1[2:0]: MBICK1 Divider Reference Clock Setting of Clock Sync Domain 1 (Table 8)
Default: “000” (TieLow)

BDV1[8:0]: MBICK1 Divider Setting (Table 9)
Default: 000H (Divided by 1)

SDV1[2:0]: MLRCK1 Divider Setting (Table 10)
Default: “000” (Divided by 64)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0005	Sync Domain 2 Setting 1	MSN2	CKS2[2:0]			BDV2[8]	SDV2[2:0]		
0006	Sync Domain 2 Setting 2	BDV2[7:0]							
R/W		R/W	R/W			R/W	R/W		
Default		0	000			0	000		

MSN2: Slave/Master Mode Setting for BICK2 pin/LRCK2 pin (Table 16)
- 0: Slave Mode (default)
- 1: Master Mode

CKS2[2:0]: MBICK2 Divider Reference Clock Setting of Clock Sync Domain 2 (Table 8)
Default: “000” (TieLow)

BDV2[8:0]: MBICK2 Divider Setting (Table 9)
Default: 000H (Divided by 1)

SDV2[2:0]: MLRCK2 Divider Setting (Table 10)
Default: “000” (Divided by 64)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000F	CLKO Output Setting	0				CLKOE	CLKOSEL[2:0]		
R/W		R/W	R/W	R/W	R/W	R/W	R/W		
Default		0	0	0	0	0	000		

CLKOE: CLKO pin Output Enable
- 0: CLKO pin = “L” (default)
- 1: CLKO Output Enable

CLKOSEL[2:0]: CLKO pin Output Clock Frequency Setting (Table 13)
Default: “000” (12.288MHz / 11.2896MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0010	Pin Setting	0							MSELN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MSELN: BICK2/SDIN3 pin and LRCK2/SDOUT3 pin setting
0: BICK2 pin, LRCK2 pin (default)
1: SDIN3 pin, SDOUT3 pin

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0011	Sync Domain Select 1	0	SDBCK1[2:0]			0	SDBCK2[2:0]		
0013	Sync Domain Select 3	0					EXBCK1[2:0]		
0014	Sync Domain Select 4	0	EXBCK2[2:0]			0	EXBCK3[2:0]		
0016	Sync Domain Select 6	0	SDDO1[2:0]			0	SDDO2[2:0]		
0017	Sync Domain Select 7	0	SDDO3[2:0]			0			
0018	Sync Domain Select 8	0					SDVOL1[2:0]		
0019	Sync Domain Select 9	0	SDVOL2[2:0]			0	SDVOL3[2:0]		
001F	Sync Domain Select 15	0	SDMIXA[2:0]			0	SDMIXB[2:0]		
0020	Sync Domain Select 16	0	SDADC1[2:0]			0	SDCODEC[2:0]		
R/W		R/W	R/W			R/W	R/W		
Default		0	000			0	000		

SDxxxx[2:0]: Clock Sync Domain Setting for Input/Output Port (Table 20, Table 21)
Default: “000” (Not Assigned)

EXBCKx[2:0]: SDINx pin Symchronizing Clock Select (Table 15)
Default: “000” (Not Assigned)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0021	SDOUT1 TDM SLOT1-2 Data Select	0		SELDO1A[5:0]					
0022	SDOUT1 TDM SLOT3-4 Data Select	0		SELDO1B[5:0]					
0023	SDOUT1 TDM SLOT5-6 Data Select	0		SELDO1C[5:0]					
0024	SDOUT1 TDM SLOT7-8 Data Select	0		SELDO1D[5:0]					
0025	SDOUT1 TDM SLOT9-10 Data Select	0		SELDO1E[5:0]					
0026	SDOUT1 TDM SLOT11-12 Data Select	0		SELDO1F[5:0]					
0027	SDOUT1 TDM SLOT13-14 Data Select	0		SELDO1G[5:0]					
0028	SDOUT1 TDM SLOT15-16 Data Select	0		SELDO1H[5:0]					
0029	SDOUT2 Output Data Select	0		SELDO2[5:0]					
002A	SDOUT3 Output Data Select	0		SELDO3[5:0]					
0035	DAC1 Input Data Select	0		SELDA1[5:0]					
0036	DAC2 Input Data Select	0		SELDA2[5:0]					
0037	DAC3 Input Data Select	0		SELDA3[5:0]					
0038	VOL1 Input Data Select	0		SELVOL1[5:0]					
0039	VOL2 Input Data Select	0		SELVOL2[5:0]					
003A	VOL3 Input Data Select	0		SELVOL3[5:0]					
0045	Mixer A Ch1 Input Data Select	0		SELMIXAI1[5:0]					
0046	Mixer A Ch2 Input Data Select	0		SELMIXAI2[5:0]					
0047	Mixer B Ch1 Input Data Select	0		SELMIXBI1[5:0]					
0048	Mixer B Ch2 Input Data Select	0		SELMIXBI2[5:0]					
R/W		R/W	R/W	R/W					
Default		0	0	00H					

SELxxx[5:0]: Data Source Select of Output Port (Table 21)
Default: 00H (ALL0)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004C	Clock Format Setting 1	BCKP1	DCF1[2:0]			BCKP2	DCF2[2:0]		
R/W		R/W	R/W			R/W	R/W		
Default		0	000			0	000		

BCKP1: Relationship of LRCK1 and BICK1 Edges (Table 23)
- 0: LRCK1 starts on a BICK1 falling edge (default)
- 1: LRCK1 starts on a BICK1 rising edge

DCF1[2:0]: LRCK1/BICK1 Clock Format Setting (Table 22)
Default: "000" (I^2S Mode)

BCKP2: Relationship of LRCK2 and BICK2 Edges (Table 23)
- 0: LRCK2 starts on a BICK2 falling edge (default)
- 1: LRCK2 starts on a BICK2 rising edge

DCF2[2:0]: LRCK2/BICK2 Clock Format Setting (Table 22)
Default: "000" (I^2S Mode)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0050	SDIN1 Digital Input Format	DIEDGEN1	0	DISL1[1:0]		DILSBE1	0	DIDL1[1:0]	
R/W		R/W	R/W	R/W		R/W	R/W	R/W	
Default		0	0	00		0	0	00	

DIEDGEN1: Start Timing Setting of Data Transferring for Second and Succeeding Channels of SDIN1
- 0: LRCK Edge Basis (default)
- 1: Slot Length Basis

DISL1[1:0]: SDIN1 Data Slot Length Setting (Table 24)
Default: "00" (24bit)

DILSBE1: MSB/LSB Setting of Audio Data in Data Slot of SDIN1
- 0: MSB (default)
- 1: LSB

DIDL1[1:0]: Audio Data Word Length Setting of SDIN1 (Table 25)
Default: "00" (24bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0051	SDIN2 Digital Input Format	DIEDGEN2	0	DISL2[1:0]		DILSBE2	0	DIDL2[1:0]	
R/W		R/W	R/W	R/W		R/W	R/W	R/W	
Default		0	0	00		0	0	00	

DIEDGEN2: Start Timing Setting of Data Transferring for Second and Succeeding Channels of SDIN2
- 0: LRCK Edge Basis (default)
- 1: Slot Length Basis

DISL2[1:0]: SDIN2 Data Slot Length Setting (Table 24)
Default: "00" (24bit)

DILSBE2: MSB/LSB Setting of Audio Data in Data Slot of SDIN2
- 0: MSB (default)
- 1: LSB

DIDL2[1:0]: Audio Data Word Length Setting of SDIN2 (Table 25)
Default: "00" (24bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0052	SDIN3 Digital Input Format	DIEDGEN3	0	DISL3[1:0]		DILSBE3	0	DIDL3[1:0]	
R/W		R/W	R/W	R/W		R/W	R/W	R/W	
Default		0	0	00		0	0	00	

DIEDGEN3: Start Timing Setting of Data Transferring for Second and Succeeding Channels of SDIN3
- 0: LRCK Edge Basis (default)
- 1: Slot Length Basis

DISL3[1:0]: SDIN3 Data Slot Length Setting (Table 24)
Default: “00” (24bit)

DILSBE3: MSB/LSB Setting of Audio Data in Data Slot of SDIN3
- 0: MSB (default)
- 1: LSB

DIDL3[1:0]: Audio Data Word Length Setting of SDIN3 (Table 25)
Default: “00” (24bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0055	SDOUT1 Digital Output Format	DOEDGEN1	0	DOSL1[1:0]		DOLSBE1	0	DODL1[1:0]	
R/W		R/W	R/W	R/W		R/W	R/W	R/W	
Default		0	0	00		0	0	00	

DOEDGEN1: Start Timing Setting of Data Transferring for Second and Succeeding Channels of SDOUT1
- 0: LRCK Edge Basis (default)
- 1: Slot Length Basis

DOSL1[1:0]: SDOUT1 Data Slot Length Setting (Table 24)
Default: “00” (24bit)

DOLSBE1: MSB/LSB Setting of Audio Data in Data Slot of SDOUT1
- 0: MSB (default)
- 1: LSB

DODL1[1:0]: Audio Data Word Length Setting of SDOUT1 (Table 25)
Default: “00” (24bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0056	SDOUT2 Digital Output Format	DOEDGEN2	0	DOSL2[1:0]		DOLSBE2	0	DODL2[1:0]	
R/W		R/W	R/W	R/W		R/W	R/W	R/W	
Default		0	0	00		0	0	00	

DOEDGEN2: Start Timing Setting of Data Transferring for Second and Succeeding Channels of SDOUT2
- 0: LRCK Edge Basis (default)
- 1: Slot Length Basis

DOSL2[1:0]: SDOUT2 Data Slot Length Setting (Table 24)
Default: “00” (24bit)

DOLSBE2: MSB/LSB Setting of Audio Data in Data Slot of SDOUT2
- 0: MSB (default)
- 1: LSB

DODL2[1:0]: Audio Data Word Length Setting of SDOUT2 (Table 25)
Default: “00” (24bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0057	SDOUT3 Digital Output Format	DOEDGEN3	0	DOSL3[1:0]		DOLSBE3	0	DODL3[1:0]	
R/W		R/W	R/W	R/W		R/W	R/W	R/W	
Default		0	0	00		0	0	00	

DOEDGEN3: Start Timing Setting of Data Transferring for Second and Succeeding Channels of SDOUT3
0: LRCK Edge Basis (default)
1: Slot Length Basis

DOSL3[1:0]: SDOUT3 Data Slot Length Setting (Table 24)
Default: “00” (24bit)

DOLSBE3: MSB/LSB Setting of Audio Data in Data Slot of SDOUT3
0: MSB (default)
1: LSB

DODL3[1:0]: Audio Data Word Length Setting of SDOUT3 (Table 25)
Default: “00” (24bit)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
005A	SDOUT Phase Setting	0					SDOPH3	SDOPH2	SDOPH1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SDOPH3: High speed mode setting for SDOUT3 in slave mode (Note 41)
0: Normal Mode (default)
1: High speed mode

SDOPH2: High speed mode setting for SDOUT2 in slave mode (Note 41)
0: Normal Mode (default)
1: High speed mode

SDOPH1: High speed mode setting for SDOUT1 in slave mode (Note 41)
0: Normal Mode (default)
1: High speed mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
005E	Output Port Enable Setting	0		SDOUT1E	SDOUT2E	SDOUT3E	0		
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SDOUT1E: SDOUT1 Output Enable
0: SDOUT1 pin = “L” (default)
1: SDOUT1 Output Enable

SDOUT2E: SDOUT2 Output Enable
0: SDOUT2 pin = “L” (default)
1: SDOUT2 Output Enable

SDOUT3E: SDOUT3 Output Enable
0: SDOUT3 pin = “L” (default)
1: SDOUT3 Output Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0060	Mixer A Setting	SFTA2[1:0]		SFTA1[1:0]		SWPA2[1:0]		SWPA1[1:0]	
	R/W	R/W		R/W		R/W		R/W	
	Default	00		00		00		00	

SFTA2[1:0]: Level Adjustment Function Setting for Input2 of Mixer A (Table 34)
Default: “00” (Not Shifted)

SFTA1[1:0]: Level Adjustment Function Setting for Input1 of Mixer A (Table 34)
Default: “00” (Not Shifted)

SWPA2[1:0]: Data Change Setting for Input 2 of Mixer A (Table 35)
Default: “00” (Through)

SWPA1[1:0]: Data Change Setting for Input 1 of Mixer A (Table 35)
Default: “00” (Through)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0061	Mixer B Setting	SFTB2[1:0]		SFTB1[1:0]		SWPB2[1:0]		SWPB1[1:0]	
	R/W	R/W		R/W		R/W		R/W	
	Default	00		00		00		00	

SFTB2[1:0]: Level Adjustment Function Setting for Input2 of Mixer B (Table 34)
Default: “00” (Not Shifted)

SFTB1[1:0]: Level Adjustment Function Setting for Input1 of Mixer B (Table 34)
Default: “00” (Not Shifted)

SWPB2[1:0]: Data Change Setting for Input 2 of Mixer B (Table 35)
Default: “00” (Through)

SWPB1[1:0]: Data Change Setting for Input 1 of Mixer B (Table 35)
Default: “00” (Through)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0062	MIC AMP Gain	MGNL[3:0]				MGNR[3:0]			
	R/W	R/W				R/W			
	Default	0000				0000			

MGNL[3:0]: MIC Input Lch Gain Setting (Table 40)
Default: 0H (0dB)

MGNR[3:0]: MIC Input Rch Gain Setting (Table 40)
Default: 0H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0063	Analog Input Gain Control	ADC1VL	ADC1VR	ADC2VL	ADC2VR	ADCMV	0	MICLZCE	MICRZCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ADC1VL: Lch Input Voltage Setting of ADC1 (Table 52)
Default: "0"(2.3Vpp(±2.3Vpp))

ADC1VR: Rch Input Voltage Setting of ADC1 (Table 52)
Default: "0"(2.3Vpp(±2.3Vpp))

ADC2VL: Lch Input Voltage Setting of ADC2 (Table 52)
Default: "0"(2.3Vpp(±2.3Vpp))

ADC2VR: Rch Input Voltage Setting of ADC2 (Table 52)
Default: "0"(2.3Vpp(±2.3Vpp))

ADCMV: Input Voltage Setting of ADCM (Table 52)
Default: "0"(2.3Vpp(±2.3Vpp))

MICLZCE: MIC Gain Zero Crossing Enable for Lch
0: Lch Zero Crossing Detection is OFF (default)
1: Lch Zero Crossing Detection is ON

MICRZCE: MIC Gain Zero Crossing Enable for Rch
0: Rch Zero Crossing Detection is OFF (default)
1: Rch Zero Crossing Detection is ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0064	ADC1 Lch Digital Volume	VOLAD1L[7:0]							
0065	ADC1 Rch Digital Volume	VOLAD1R[7:0]							
0066	ADC2 Lch Digital Volume	VOLAD2L[7:0]							
0067	ADC2 Rch Digital Volume	VOLAD2R[7:0]							
0068	ADCM Digital Volume	VOLADM[7:0]							
R/W		R/W							
Default		30H							

VOLAD1L[7:0]: Lch Digital Volume Setting of ADC1 (Table 45)
Default: 30H (0dB)

VOLAD1R[7:0]: Rch Digital Volume Setting of ADC1 (Table 45)
Default: 30H (0dB)

VOLAD2L[7:0]: Lch Digital Volume Setting of ADC2 (Table 45)
Default: 30H (0dB)

VOLAD2R[7:0]: Rch Digital Volume Setting of ADC2 (Table 45)
Default: 30H (0dB)

VOLADM[7:0]: Digital Volume Setting of ADCM (Table 45)
Default: 30H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
006B	Analog Input Select Setting	ADSD	ADSL	0	ADMSEL	AD1LSEL	AD1RSEL	AD2SEL[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Default		0	0	0	0	0	0	00	

ADSD, ADSL: ADC Digital Filter Select (Table 51)
- 00: Sharp Roll-Off Filter (default)
- 01: Slow Roll-Off Filter
- 10: Short Delay Sharp Roll-Off Filter
- 11: Short Delay Slow Roll-Off Filter

ADMSEL: ADCM Input Pin Select (Table 50)
- 0: AINMP, AINMN (default)
- 1: AINMP

AD1LSEL: ADC1 Lch Input Pin Select (Table 42)
- 0: INP1/INN1 (default)
- 1: AIN1L

AD1RSEL: ADC1 Rch Input Pin Select (Table 42)
- 0: INP2/INN2 (default)
- 1: AIN1R

AD2SEL[1:0]: ADC2 Input Pin Select (Table 49)
Default: “00” (AIN2LP, AIN2LN, AIN2RP, AIN2RN)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
006C	ADC Mute & HPF Control	ATSPAD	AD1MUTE	AD2MUTE	ADMMUTE	0	AD1HPFN	AD2HPFN	ADMHPFN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATSPAD: ADC Digital Volume Transition Time Setting (Table 46)
- 0: 4/fs (default)
- 1: 16/fs

AD1MUTE: ADC1 Soft Mute Enable
- 0: Soft Mute Disable (default)
- 1: Soft Mute Enable

AD2MUTE: ADC2 Soft Mute Enable
- 0: Soft Mute Disable (default)
- 1: Soft Mute Enable

ADMMUTE: ADCM Soft Mute Enable
- 0: Soft Mute Disable (default)
- 1: Soft Mute Enable

AD1HPFN: ADC1 HPF Enable for DC Offset Cancelling
- 0: HPF Enable (default)
- 1: HPF Disable

AD2HPFN: ADC2 HPF Enable for DC Offset Cancelling
- 0: HPF Enable (default)
- 1: HPF Disable

ADMHPFN: ADCM HPF Enable for DC Offset Cancelling
- 0: HPF Enable (default)
- 1: HPF Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
006D	DAC1 Lch Digital Volume	VOLDA1L[7:0]							
006E	DAC1 Rch Digital Volume	VOLDA1R[7:0]							
006F	DAC2 Lch Digital Volume	VOLDA2L[7:0]							
0070	DAC2 Rch Digital Volume	VOLDA2R[7:0]							
0071	DAC3 Lch Digital Volume	VOLDA3L[7:0]							
0072	DAC3 Rch Digital Volume	VOLDA3R[7:0]							
R/W		R/W							
Default		18H							

VOLDA1L[7:0]: Lch Digital Volume Setting of DAC1 (Table 53)
Default: 18H (0dB)

VOLDA1R[7:0]: Rch Digital Volume Setting of DAC1 (Table 53)
Default: 18H (0dB)

VOLDA2L[7:0]: Lch Digital Volume Setting of DAC2 (Table 53)
Default: 18H (0dB)

VOLDA2R[7:0]: Rch Digital Volume Setting of DAC2 (Table 53)
Default: 18H (0dB)

VOLDA3L[7:0]: Lch Digital Volume Setting of DAC3 (Table 53)
Default: 18H (0dB)

VOLDA3R[7:0]: Rch Digital Volume Setting of DAC3 (Table 53)
Default: 18H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0073	DAC Mute & Filter Setting	ATSPDA	DA1MUTE	DA2MUTE	DA3MUTE	0	DSMN	DASD	DASL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

ATSPDA: DAC Digital Volume Transition Time Setting (Table 54)
0: 4/fs (default)
1: 16/fs

DA1MUTE: DAC1 Soft Mute Enable
0: Soft Mute Disable (default)
1: Soft Mute Enable

DA2MUTE: DAC2 Soft Mute Enable
0: Soft Mute Disable (default)
1: Soft Mute Enable

DA3MUTE: DAC3 Soft Mute Enable
0: Soft Mute Disable (default)
1: Soft Mute Enable

DSMN: Sampling Clock Setting for Delta Sigma Module of DAC
0: 12.288MHz / 11.2896MHz Fixed (default)
1: fs Based

DASD, DASL: DAC Digital Filter Select (Table 57)
00: Sharp Roll-Off Filter
01: Slow Roll-Off Filter
10: Short Delay Sharp Roll-Off Filter (default)
11: Short Delay Slow Roll-Off Filter

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0074	DAC DEM Setting	0		DEM3[1:0]		DEM2[1:0]		DEM1[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	1	0	1

DEM1[1:0]: De-emphasis Filter Setting of DAC1 (Table 58)
- 00: 44.1kHz
- 01: OFF (default)
- 10: 48kHz
- 11: 32kHz

DEM2[1:0]: De-emphasis Filter Setting of DAC2 (Table 58)
- 00: 44.1kHz
- 01: OFF (default)
- 10: 48kHz
- 11: 32kHz

DEM3[1:0]: De-emphasis Filter Setting of DAC3 (Table 58)
- 00: 44.1kHz
- 01: OFF (default)
- 10: 48kHz
- 11: 32kHz

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0075	VOL1 Lch Digital Volume	VOL1L[7:0]							
0076	VOL1 Rch Digital Volume	VOL1R[7:0]							
0077	VOL2 Lch Digital Volume	VOL2L[7:0]							
0078	VOL2 Rch Digital Volume	VOL2R[7:0]							
0079	VOL3 Lch Digital Volume	VOL3L[7:0]							
007A	VOL3 Rch Digital Volume	VOL3R[7:0]							
R/W		R/W							
Default		18H							

VOL1L[7:0]: Lch Digital Volume Setting of VOL1 (Table 36)
Default: 18H (0dB)

VOL1R[7:0]: Rch Digital Volume Setting of VOL1 (Table 36)
Default: 18H (0dB)

VOL2L[7:0]: Lch Digital Volume Setting of VOL2 (Table 36)
Default: 18H (0dB)

VOL2R[7:0]: Rch Digital Volume Setting of VOL2 (Table 36)
Default: 18H (0dB)

VOL3L[7:0]: Lch Digital Volume Setting of VOL3 (Table 36)
Default: 18H (0dB)

VOL3R[7:0]: Rch Digital Volume Setting of VOL3 (Table 36)
Default: 18H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
007F	VOL Setting	ATSPVOL	0						
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATSPVOL: Digital Volume Transition Speed Setting of VOL (Table 37)
0: 4/fs (default)
1: 16/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0083	STO Flag Setting 1	0	PLLLOCKE	0					
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PLLLOCKE: STO bit Setting of PLL Lock Signal
0: Do Not Output to STO bit (default)
1: Output to STO bit

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
008A	Power Management 1	0		PMAD1	PMAD2	PMADM	PMDA1	PMDA2	PMDA3
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMAD1: ADC1 Power Management Setting
- 0: Power Save Mode (default)
- 1: Normal Operation

PMAD2: ADC2 Power Management Setting
- 0: Power Save Mode (default)
- 1: Normal Operation

PMADM: ADCM Power Management Setting
- 0: Power Save Mode (default)
- 1: Normal Operation

PMDAx(x=1~3): DAC1~3 Power Management Setting
- 0: Power Save Mode (default)
- 1: Normal Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
008C	Reset Control	0	0	1	CRESETN	0			HRESETN
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	1	0	0	0	0	0

CRESETN: ADC1 and CODEC Reset
- 0: ADC1 and CODEC Reset (default)
- 1: Reset Release

CODEC means ADC2, ADC, DAC1, DAC2 and DAC3.

HRESETN: HUB Reset
- 0: HUB Reset (default)
  All ADC1/2, ADCM, DAC1/2/3 and Serial Signal Bus are Reset
- 1: HUB Reset Release

Read Only Registers

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0102	Status Read Out	0	STO	0					
	Default	0	1	0	0	0	0	0	0

STO: STO bit Status Read
- 0: Error State
- 1: Normal Operation (default)

13. Recommended External Circuits

■ Connection Diagram

1. I²C Interface

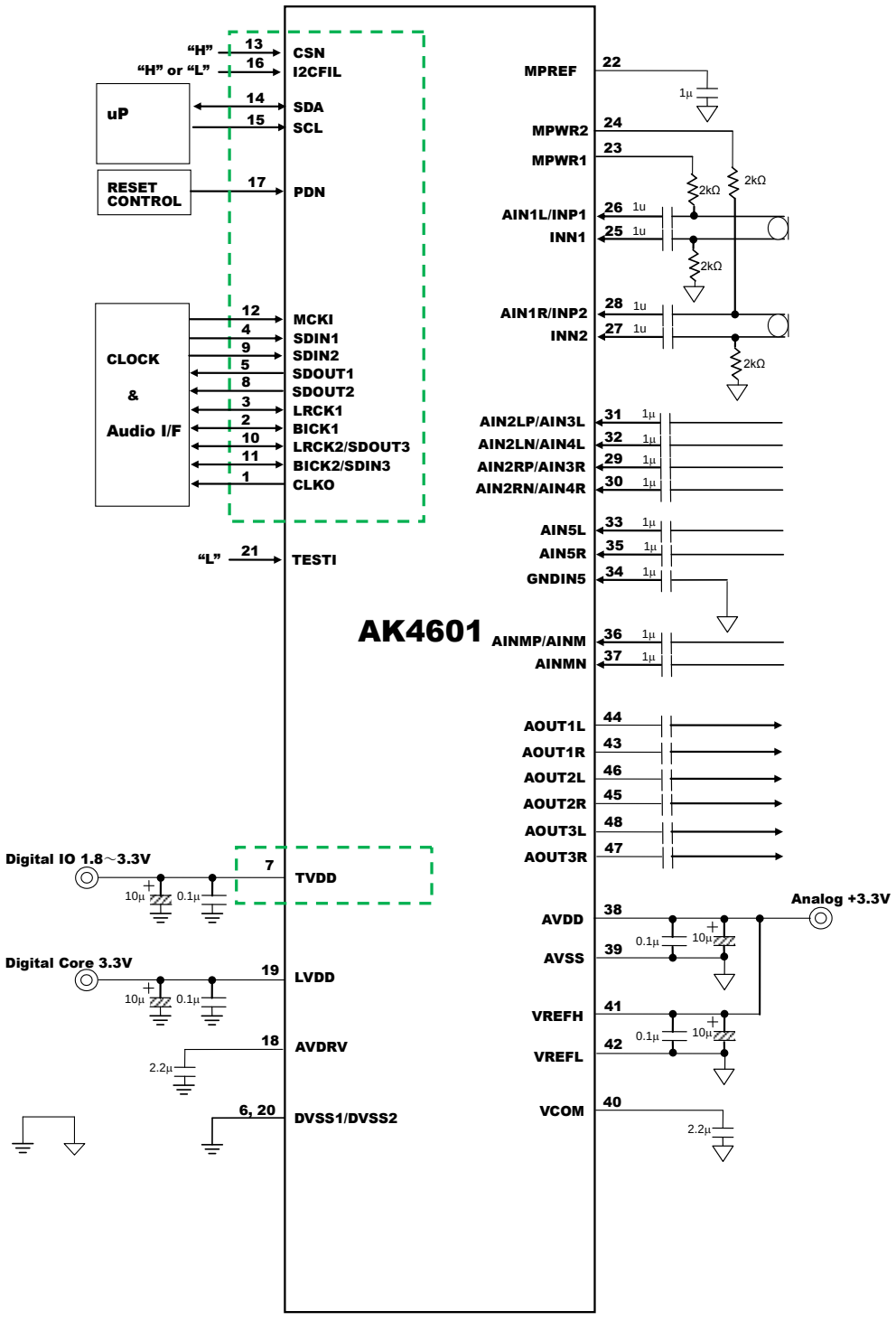


Figure 73. I²C Interface Connection Example

2. SPI Interface

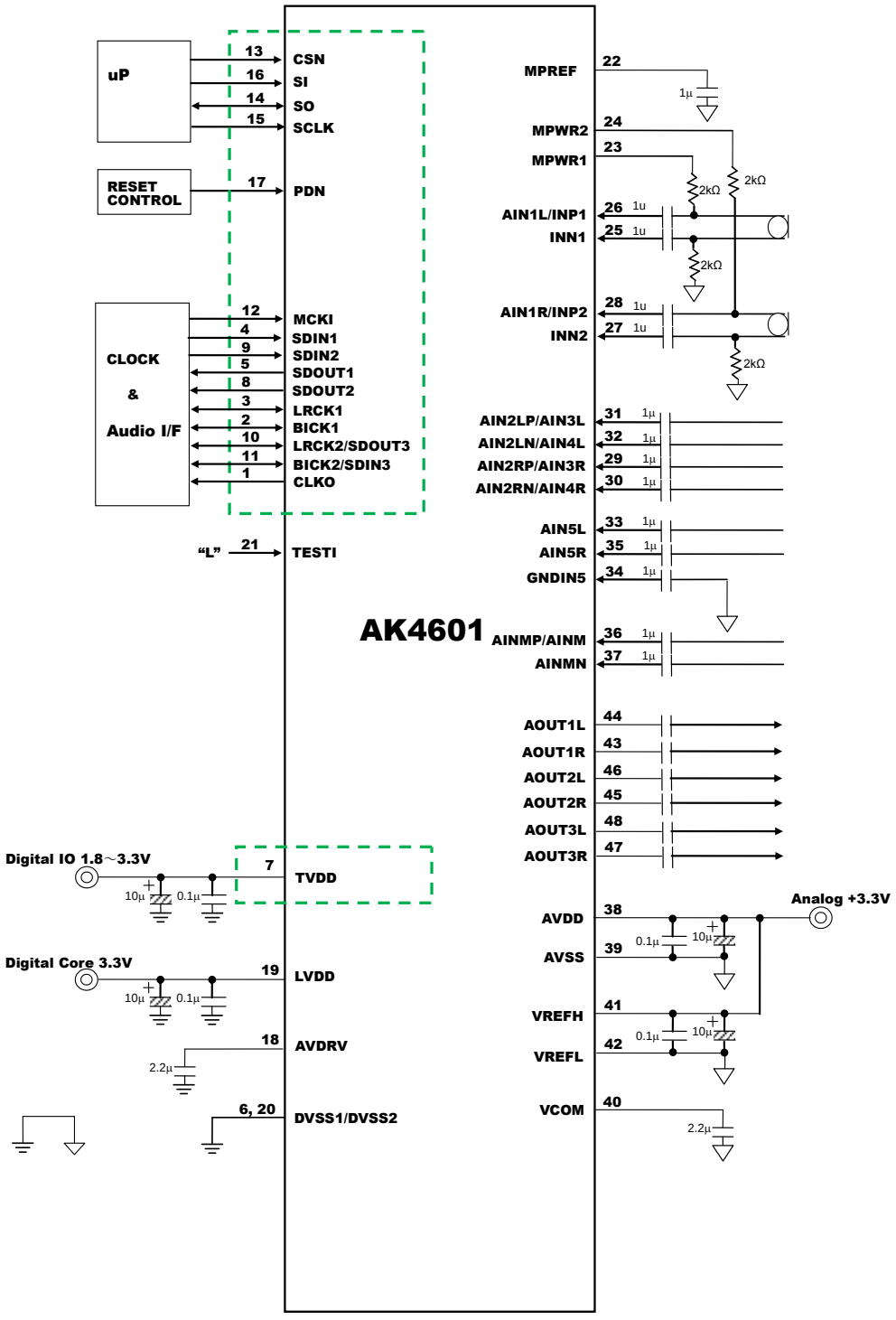


Figure 74. SPI Interface Connection Example

■ Peripheral Circuit

1. Ground

AVSS, DVSS1 and DVSS2 should be connected to the same ground. Decoupling capacitors, particularly capacitors of small capacity, should be placed at positions as close as possible to the AK4601.

2. Reference Voltage

The AVDD voltage controls analog signal range. VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2µF capacitor should be connected between the VCOM pin and AVSS.

Do not connect the VCOM pin to any external devices. Digital signal lines, especially clock signal line should be kept away as far as possible from this pin in order to avoid unwanted coupling into the AK4601.

3. Analog Input

The analog input signal is input to the analog modulator of the AK4601. When AVDD = 3.3V and AVSS = 0.0V, the input voltage range at differential input pin is ±2.30Vpp or ±2.83Vpp (Typ.) and 2.30Vpp or 2.83Vpp (Typ.) at single-ended input pin. The output code format is 2's complements. The internal HPF removes the DC offset.

After power-down is released, the internal operating point level AVDD/2 occurs on analog input pins of the AK4601. Concerning the internal operating point formation circuit, each input pin has impedance of 25kΩ (typ). The pins that are connected to AC coupling capacitors require start-up time (time constant).

The AK4601 samples the analog inputs at 6.144MHz when fs=48kHz. Digital filters remove noise around from 30kHz to 6.114MHz. The AK4601 includes an anti-aliasing filter (RC filter). This filter attenuates noises around 6.114MHz ~ 6.144MHz, which are not removed by the digital filters. Therefore no external low-pass filter is needed in front of the ADC since most of audio signals do not have a large noise around 6.114MHz. However, an external low-pass filter should be connected before the ADC for the signal which has large out-of-band noise such as D/A converted signals.

The analog power supply to the AK4601 is +3.3V typical. Voltage of AVDD + 0.3V or larger, voltage of AVSS - 0.3V or smaller, and current of 10mA or larger must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. Accordingly, if the external analog circuit voltage is ±15V, the analog input pins must be protected from signals which are equal or larger than absolute maximum ratings.

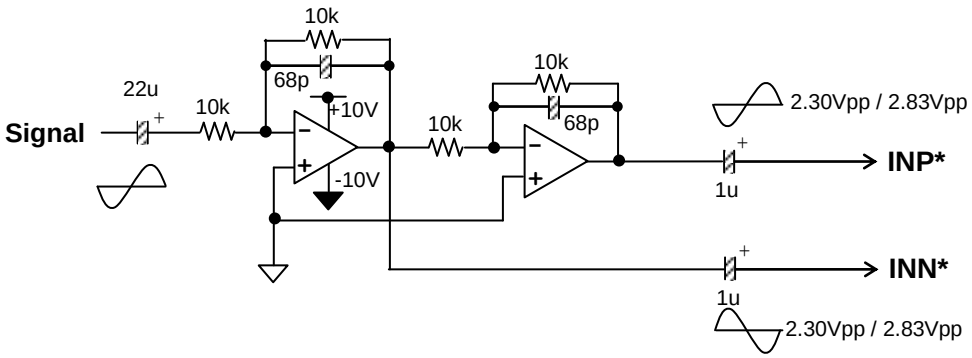


Figure 75. Input Buffer Circuit Example at fs=48kHz (Differential Input)

4. Analog Output

The analog output is single-ended and the output signal range is typically 0.86 x AVDD Vpp centered on VCOM. The digital input data format is two's compliment. Positive full-scale output corresponds to 7FFFFFFFH (@32bit) input code, Negative full scale is 80000000H (@32bit) and VCOM voltage ideally is 00000000H (@32bit). The Out-of-Band noise (shaping noise) generated by the internal delta-sigma modulator is attenuated by an integrated switched capacitor filter (SCF) and a continuous time filter (CTF).

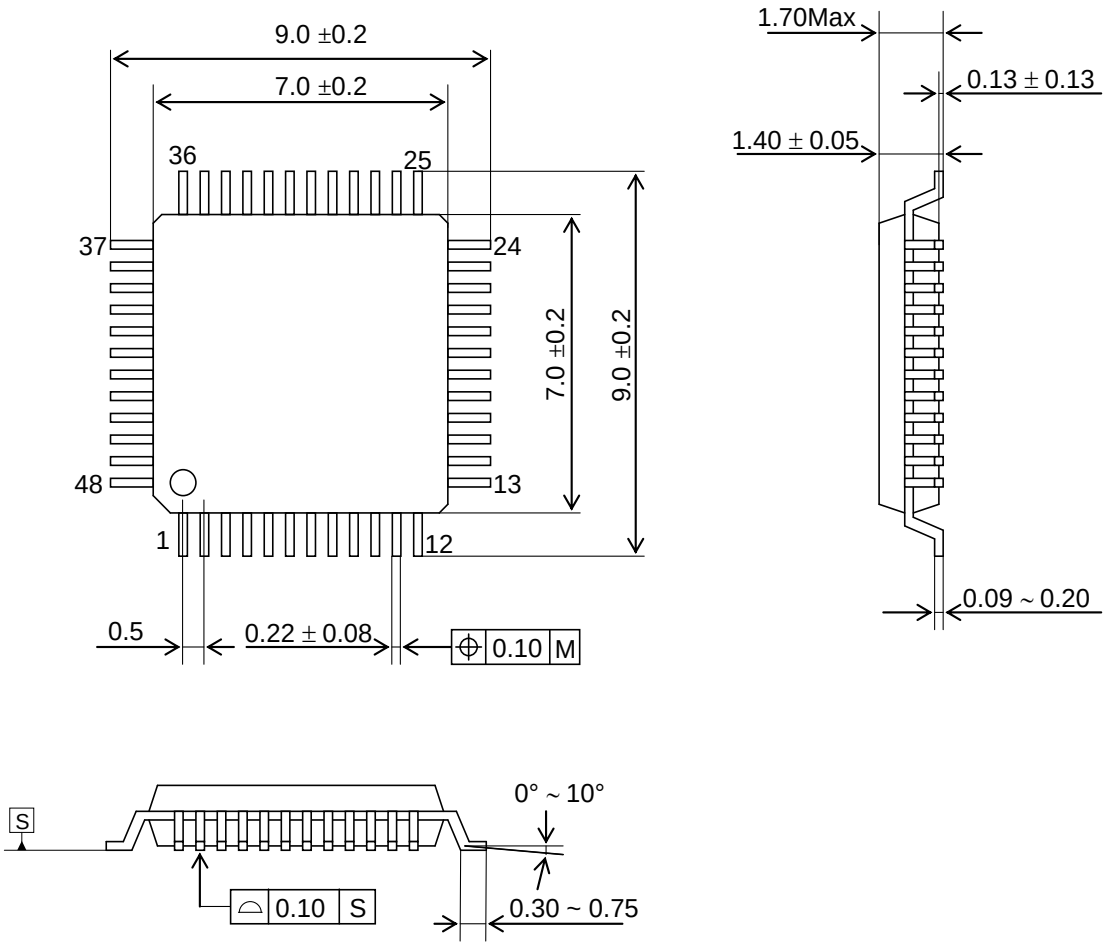
5. Connection to Digital Circuit

To minimize the noise from digital circuits, the digital output of the AK4601 must be connected to CMOS or low voltage logic ICs such as 74HC and 74AC for CMOS and 74LV, 74LV-A, 74ALVC and 74AVC for low voltage logic ICs.

14. Package

■ Outline Dimensions

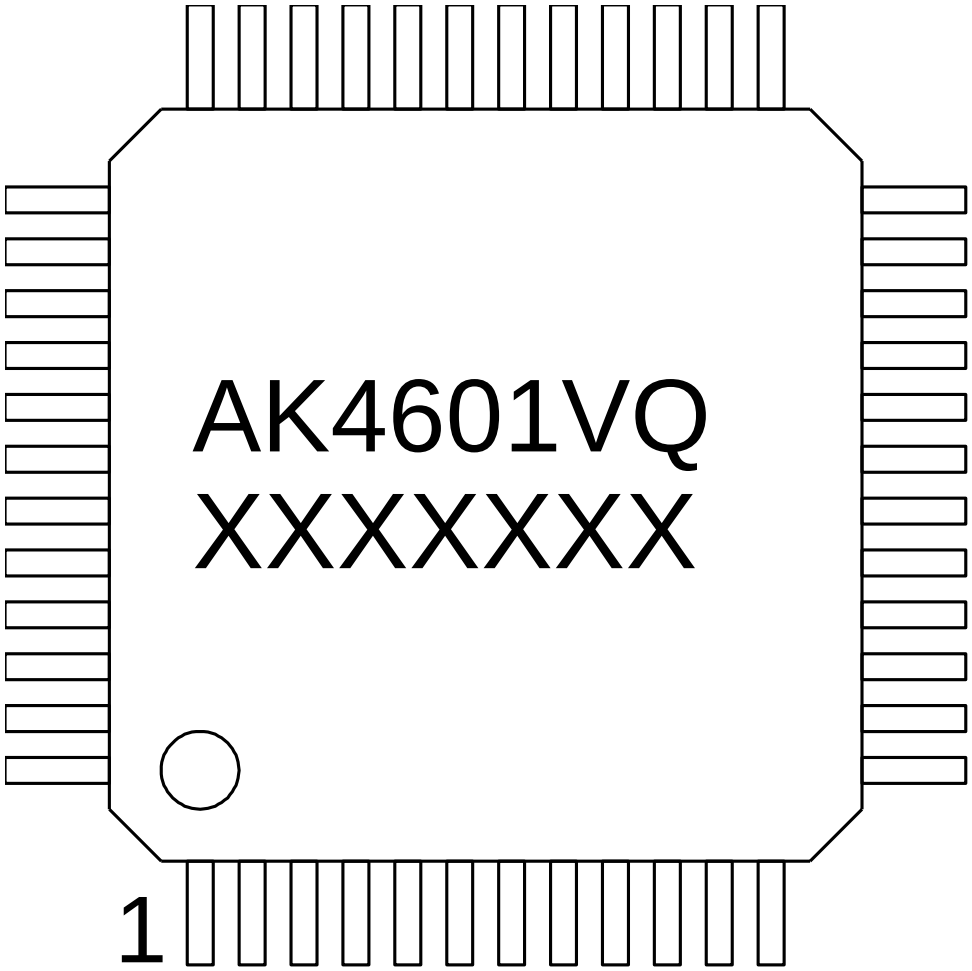
48-pin LQFP(Unit: mm)



■ Material and Lead Finish

Package: Epoxy
Lead frame: Copper
Terminal surface treatment: Soldering (Pb free) plate

■ **Marking**



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4601VQ
4) Asahi Kasei Logo

15. Ordering Guide

■ **Ordering Guide**

AK4601	-40 ~ +85°C	48-pin LQFP (0.5mm pitch)
AKD4601	Evaluation Board for the AK4601	

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
16/03/23	00	First Edition		
16/12/08	01	Error Correction	5	Figure of PDN pin I/O pin → Input pin
			102	ATSPVOL: Digital Volume Transition Speed Setting of VOL (Table 37) 0: 1/fs (default) → 4/fs (default) 1: 4/fs → 16/fs

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