SNx5LVDS3xxxx High-Speed Differential Line Receivers

1 Features

- Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard
- Operate With a Single 3.3-V Supply
- Designed for Signaling Rates of up to 150 Mbps (See)
- Differential Input Thresholds ±100 mV Max
- Typical Propagation Delay Time of 2.1 ns
- Power Dissipation 60 mW Typical Per Receiver at Maximum Data Rate
- Bus-Terminal ESD Protection Exceeds 8 kV
- Low-Voltage TTL (LVTTL) Logic Output Levels
- Pin Compatible With AM26LS32, MC3486, and μA9637
- Open-Circuit Fail-Safe
- Cold Sparing for Space and High-Reliability Applications Requiring Redundancy

2 Applications

- Wireless Infrastructure
- Telecom Infrastructure
- Printer

3 Description

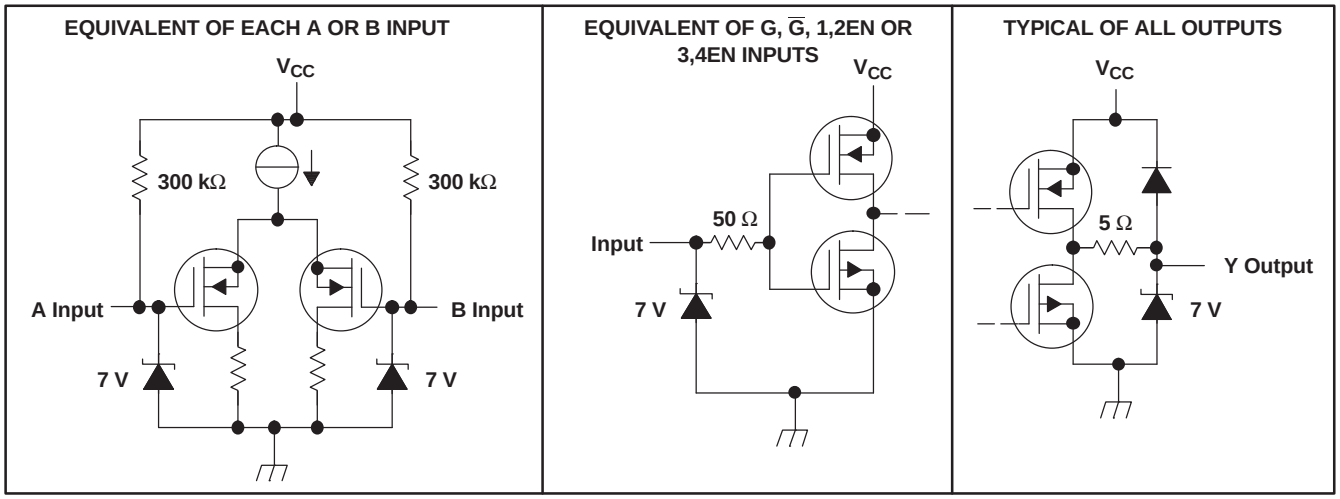
The SN55LVDS32, SN65LVDS32, SN65LVDS3486, and SN65LVDS9637 devices are differential line receivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the differential receivers provides a valid logical output state with a ±100-mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN55LVDS32	LCCC (20)	8.89 mm × 8.89 mm
	CDIP (16)	19.56 mm × 6.92 mm
	CFP (16)	10.30 mm × 6.73 mm
SN65LVDS32	SOIC (16)	9.90 mm × 3.91 mm
	SOP (16)	10.30 mm × 5.30 mm
	TSSOP (16)	5.50 mm × 4.40 mm
SN65LVDS3486	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.50 mm × 4.40 mm
SN65LVDS9637	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Equivalent Input and Output Schematic Diagrams



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4 Revision History

Changes from Revision Q (July 2007) to Revision R **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Description (Continued)

The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer depends on the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS32, SN65LVDS3486, and SN65LVDS9637 devices are characterized for operation from –40°C to 85°C. The SN55LVDS32 device is characterized for operation from –55°C to 125°C.

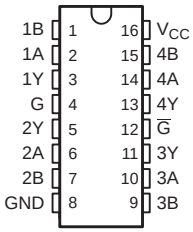
6 Device Options

Maximum Recommended Operating Speeds

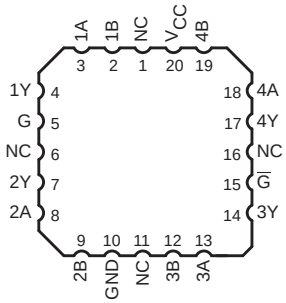
PART NUMBER	ALL Rx ACTIVE
SN65LVDS32	100 Mbps
SN65LVDS3486	100 Mbps
SN65LVDS9637	150 Mbps

7 Pin Configuration and Functions

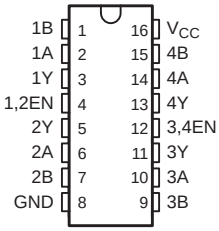
SN55LVDS32 . . . J OR W
SN65LVDS32 . . . D OR PW
(Marked as **LVDS32** or **65LVDS32**)
(TOP VIEW)



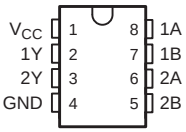
SN55LVDS32FK
(TOP VIEW)



SN65LVDS3486D (Marked as **LVDS3486**)
(TOP VIEW)



SN65LVDS9637D (Marked as **DK637** or **LVDS37**)
SN65LVDS9637DGN (Marked as **L37**)
SN65LVDS9637DGK (Marked as **AXF**)
(TOP VIEW)



Pin Functions: SNx5LVDS32xx

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	16	–	Supply voltage
GND	8	–	Ground
1A	2	I	Differential (LVDS) non-inverting input
1B	1	I	Differential (LVDS) inverting input
1Y	3	O	LVTTL output signal
2A	6	I	Differential (LVDS) non-inverting input
2B	7	I	Differential (LVDS) inverting input
2Y	5	O	LVTTL output signal
3A	10	I	Differential (LVDS) non-inverting input
3B	9	I	Differential (LVDS) inverting input
3Y	11	O	LVTTL output signal
4A	14	I	Differential (LVDS) non-inverting input
4B	15	I	Differential (LVDS) inverting input
4Y	13	O	LVTTL output signal
G	4	I	Enable (HI = ENABLE)
G/	12	I	Enable (LO = ENABLE)

Pin Functions: SN55LVDS32FK

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	20	–	Supply voltage
GND	10	–	Ground
1A	3	I	Differential (LVDS) non-inverting input
1B	2	I	Differential (LVDS) inverting input
1Y	4	O	LVTTL output signal
2A	8	I	Differential (LVDS) non-inverting input
2B	9	I	Differential (LVDS) inverting input
2Y	7	O	LVTTL output signal
3A	13	I	Differential (LVDS) non-inverting input
3B	12	I	Differential (LVDS) inverting input
3Y	14	O	LVTTL output signal
4A	18	I	Differential (LVDS) non-inverting input
4B	19	I	Differential (LVDS) inverting input
4Y	17	O	LVTTL output signal
G	5	I	Enable (HI = ENABLE)
G/	15	I	Enable (LO = ENABLE)
NC	1, 6, 11, 16	–	No connection

Pin Functions: SN65LVDS3486D

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	16	–	Supply voltage
GND	8	–	Ground
1A	2	I	Differential (LVDS) non-inverting input
1B	1	I	Differential (LVDS) inverting input
1Y	3	O	LVTTL output signal
2A	6	I	Differential (LVDS) non-inverting input
2B	7	I	Differential (LVDS) inverting input
2Y	5	O	LVTTL output signal
3A	10	I	Differential (LVDS) non-inverting input
3B	9	I	Differential (LVDS) inverting input
3Y	11	O	LVTTL output signal
4A	14	I	Differential (LVDS) non-inverting input
4B	15	I	Differential (LVDS) inverting input
4Y	13	O	LVTTL output signal
1,2EN	4	I	Enable for channels 1 and 2
3,4EN	12	I	Enable for channels 3 and 4

Pin Functions: SN65LVDS9637Dxx

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	1	–	Supply voltage
GND	4	–	Ground
1A	8	I	Differential (LVDS) non-inverting input
1B	7	I	Differential (LVDS) inverting input
1Y	2	O	LVTTL output signal
2A	6	I	Differential (LVDS) non-inverting input
2B	5	I	Differential (LVDS) inverting input
2Y	3	O	LVTTL output signal

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.5	4	V
V_I	Input voltage range	Enables and output	–0.5	V_{CC} + 0.5	V
		A or B	–0.5	4	V
	Continuous total power dissipation		See *Thermal Information*		
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, bus pins(1)	±8000	V
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	G, $\overline{G}$, 1, 2EN, or 3, 4EN	2			
V_{IL}	Low-level input voltage	G, $\overline{G}$, 1, 2EN, or 3, 4EN			0.8	
$\lvert V_{ID}\rvert$	Magnitude of differential input voltage		0.1		0.6	
V_{IC}	Common-mode input voltage (see Figure 1)		$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 - \frac{\lvert V_{ID}\rvert}{2}$	
					$V_{CC} - 0.8$	
T_A	Operating free-air temperature	SN65 prefix	–40		85	°C
		SN55 prefix	–55		125	

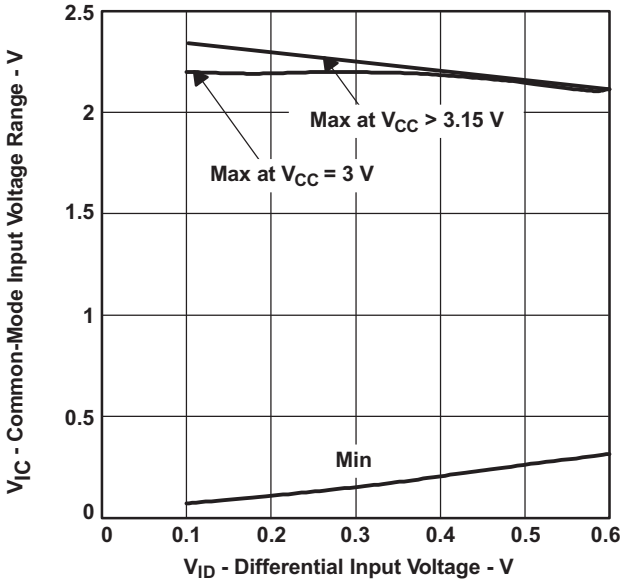


Figure 1. V_{IC} vs V_{ID} and V_{CC}

8.4 Thermal Information

THERMAL METRIC[1]		SN55LVDS32			SN65LVDS32, SN65LVDS3486			SN65LVDS9637		UNIT
		FK	J	W	D	NS	PW	D	DGK	
		20 PINS	16 PINS		16 PINS			8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance				76.4	88.7	111.5		177.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance				38.0	46.8	46.4		65.6	
$R_{\theta JB}$	Junction-to-board thermal resistance				33.7	49.1	56.6		97.3	
Ψ_{JT}	Junction-to-top characterization parameter				7.6	12.5	5.5		8.9	
Ψ_{JB}	Junction-to-board characterization parameter				33.5	48.8	56.1		95.8	
	Derating Factor Above T_A = 25°C	11.0	11.0	8.0	7.6	–	6.2	5.8	3.4	mW/°C
Power Rating	$T_A \le 25°C$	1375	1375	1000	950	–	774	725	425	mW
	$T_A \le 70°C$	880	880	640	608	–	496	464	272	
	$T_A \le 85°C$	715	715	520	494	–	402	377	221	
	$T_A \le 125°C$	275	275	200	–	–	–	–	–	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics: SN55LVDS32

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 7, Table 1, and (2)			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold(3)	See Figure 7, Table 1, and (2)	–100			mV
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_{CC}	Supply current	Enabled, No load		10	18	mA
		Disabled		0.25	0.5	
I_I	Input current (A or B input)	V_I = 0	–2	–10	–20	µA
		V_I = 2.4 V	–1.2	–3		
$I_{I(OFF)}$	Power-off input current (A or B input)	V_{CC} = 0, V_I = 2.4 V		6	20	µA
I_{IH}	High-level input current (EN, G, or $\overline{G}$ input)	V_{IH} = 2 V			10	µA
I_{IL}	Low-level input current (EN, G, or $\overline{G}$ input)	V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current	V_O = 0 or V_{CC}			±12	µA

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
(2) $|V_{ITH}|$ = 200 mV for operation at –55°C
(3) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.

8.6 Electrical Characteristics: SN65LVDSxxxx

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN65LVDS32 SN65LVDS3486 SN65LVDS9637			UNIT
				MIN	TYP(1)	MAX	
V_{IT+}	Positive-going differential input voltage threshold		See Figure 7 and Table 1			100	mV
$V_{IT–}$	Negative-going differential input voltage threshold(2)		See Figure 7 and Table 1	–100			mV
V_{OH}	High-level output voltage		I_{OH} = –8 mA	2.4			V
			I_{OH} = –4 mA	2.8			
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.4	V
I_{CC}	Supply current	SN65LVDS32, SN65LVDS3486	Enabled, No load		10	18	mA
			Disabled		0.25	0.5	
		SN65LVDS9637	No load		5.5	10	
I_I	Input current (A or B inputs)		V_I = 0	–2	–10	–20	µA
			V_I = 2.4 V	–1.2	–3		
$I_{I(OFF)}$	Power-off input current (A or B input)		V_{CC} = 0, V_I = 3.6 V		6	20	µA
I_{IH}	High-level input current (EN, G, or $\overline{G}$ input)		V_{IH} = 2 V			10	µA
I_{IL}	Low-level input current (EN, G, or $\overline{G}$ input)		V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current		V_O = 0 or V_{CC}			±10	µA

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.

8.7 Switching Characteristics: SN55LVDS32

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 8	1.3	2.3	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.4	2.2	6.1	ns
$t_{sk(o)}$	Channel-to-channel output skew(1)			0.1		ns
t_r	Output signal rise time, 20% to 80%			0.6		ns
t_f	Output signal fall time, 80% to 20%			0.7		ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 9		6.5	12	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			5.5	12	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			8	14	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			3	12	ns

(1) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

8.8 Switching Characteristics: SN65LVDSxxxx

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LVDS32 SN65LVDS3486 SN65LVDS9637			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 8	1.5	2.1	3	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.5	2.1	3	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			0	0.4	ns
$t_{sk(o)}$	Channel-to-channel output skew(1)			0.1	0.3	ns
$t_{sk(pp)}$	Part-to-part skew(2)				1	ns
t_r	Output signal rise time, 20% to 80%			0.6		ns
t_f	Output signal fall time, 80% to 20%			0.7		ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 9		6.5	12	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			5.5	12	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			8	12	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			3	12	ns

(1) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

8.9 Typical Characteristics

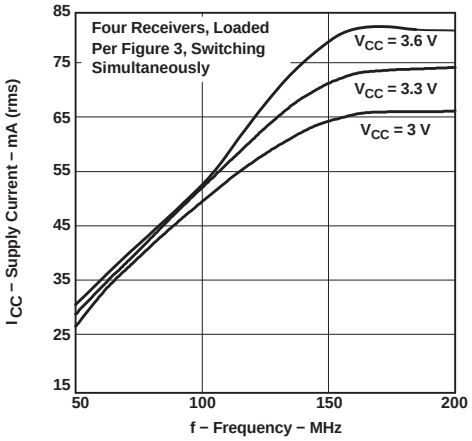


Figure 2. SN55LVDS32, SN65LVDS32 Supply Current vs Frequency

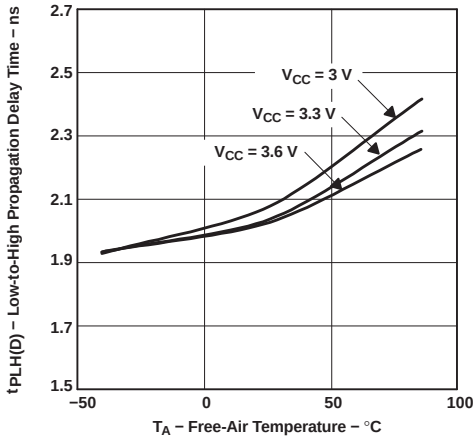


Figure 3. Low-to-High Propagation Delay Time vs Free-Air Temperature

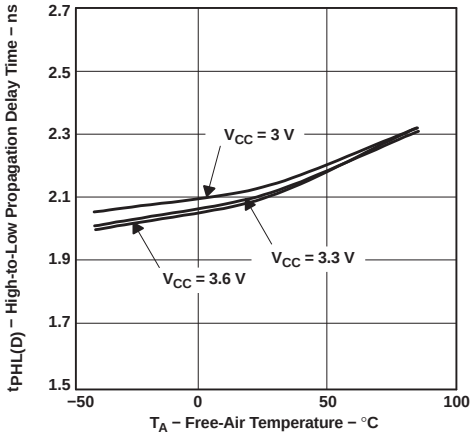


Figure 4. High-to-Low Propagation Delay Time vs Free-Air Temperature

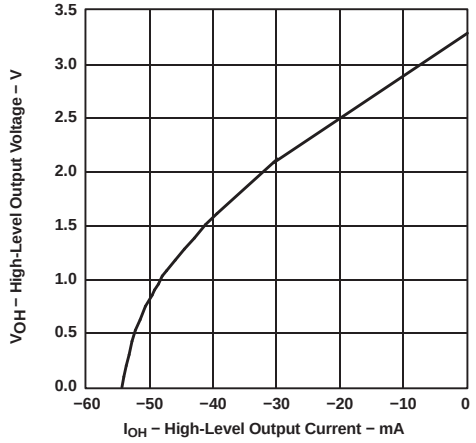


Figure 5. High-Level Output Voltage vs High-Level Output Current

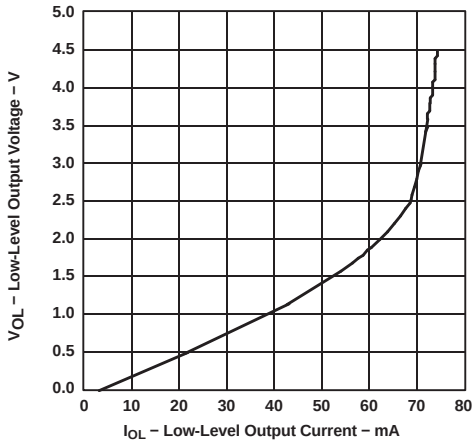


Figure 6. High-Level Output Voltage vs Low-Level Output Current

9 Parameter Measurement Information

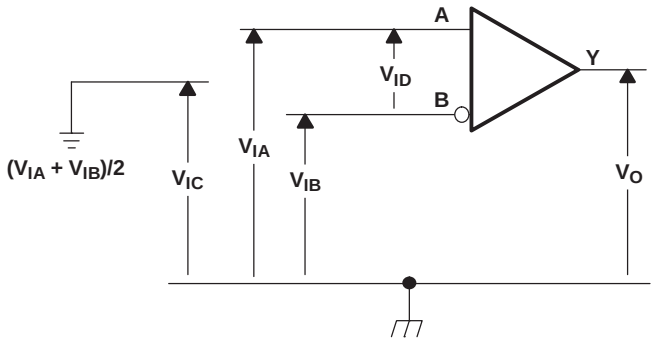
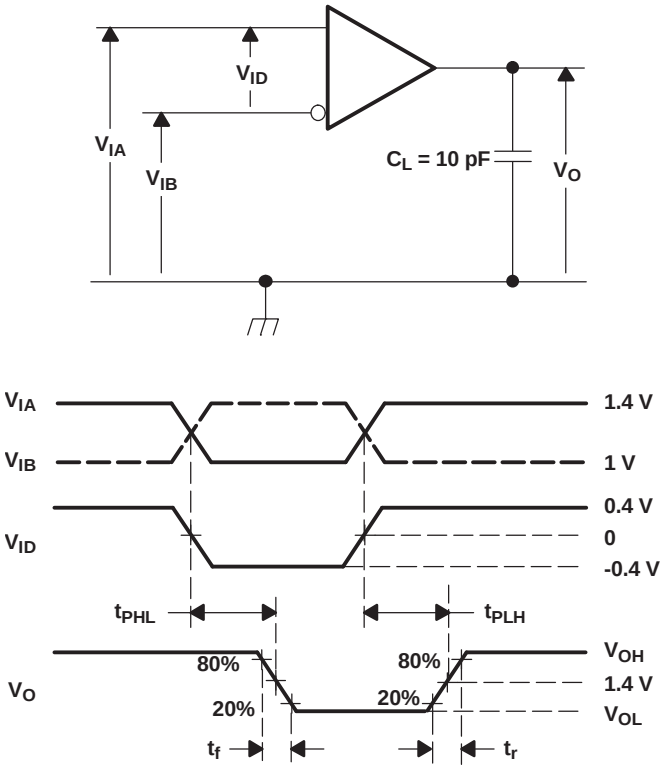


Figure 7. Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

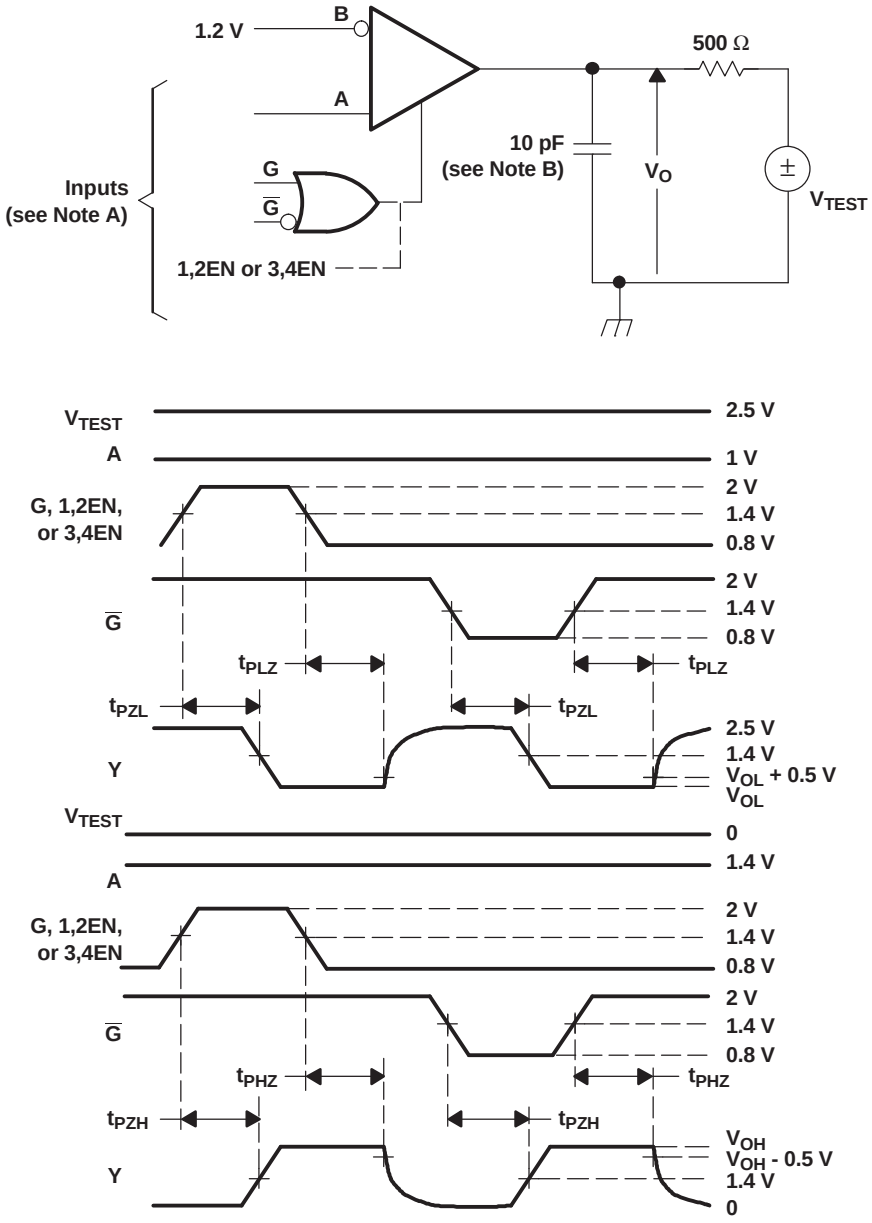
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA} (V)	V_{IB} (V)	V_{ID} (mV)	V_{IC} (V)
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the device under test.

Figure 8. Timing Test Circuit and Waveforms



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the device under test.

Figure 9. Enable or Disable Time Test Circuit and Waveforms

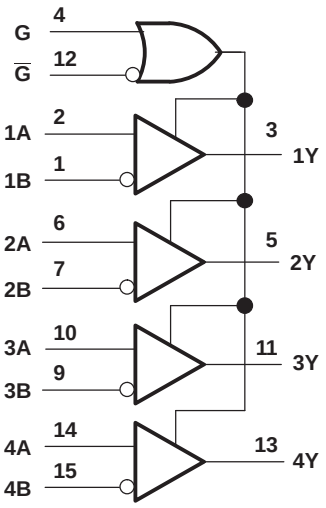
10 Detailed Description

10.1 Overview

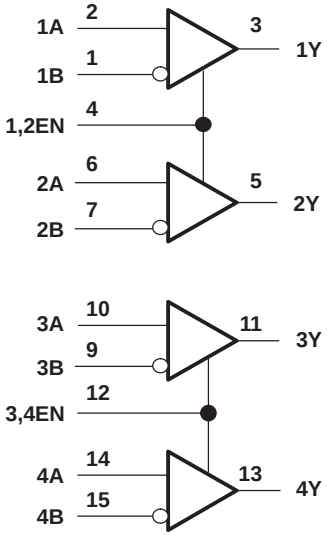
The SNx5LVDSxx devices are LVDS line receivers. They operate from a single supply that is nominally 3.3 V, but can be as low as 3.0 V and as high as 3.6 V. The input signals to the SNx5LVDSxx device are differential LVDS signals. The output of the device is an LVTTL digital signal. This LVDS receiver requires a ±100-mV input signal to determine the correct state of the received signal. Compliant LVDS receivers can accept input signals with a common-mode range between 0.05 V and 2.35 V. As the common-mode output voltage of an LVDS driver is 1.2 V, the SNx5LVDSxx correctly determines the line state when operated with a 1-V ground shift between driver and receiver.

10.2 Functional Block Diagram

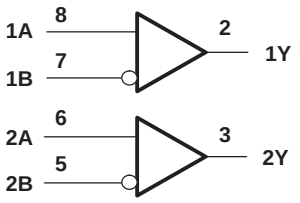
'LVDS32 logic diagram (positive logic)



SN65LVDS3486D logic diagram (positive logic)



SN65LVDS9637D logic diagram (positive logic)



10.3 Feature Description

10.3.1 Receiver Output States

When the receiver differential input signal is greater than 100 mV, the receiver output is high; and when the differential input voltage is below –100 mV, the receiver output is low. When the input voltage is between these thresholds (for example, between –100 mV and 100 mV), the receiver output is indeterminate. It may be high or low. A special case occurs when the input to the receiver is open-circuited, which is covered in *Receiver Open-Circuit Fail-Safe*. When the receiver is disabled, the receiver outputs will be high-impedance.

10.3.2 Receiver Open-Circuit Fail-Safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. However, the SNx5LVDSxx receiver is different in how it handles the open-input circuit situation.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal to V_{CC} through a 300-kΩ resistor as shown in Figure 10. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level regardless of the differential input voltage.

Feature Description (continued)

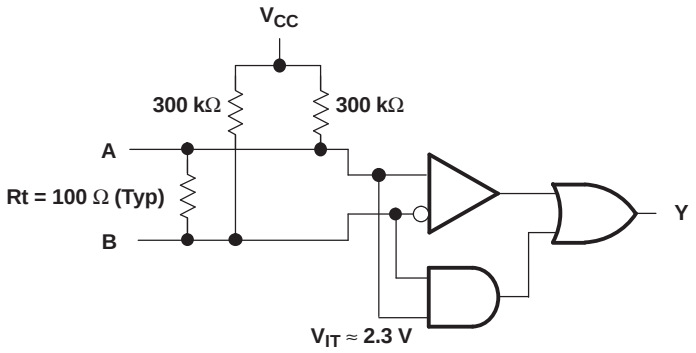


Figure 10. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt does not affect the fail-safe function as long as it is connected as shown in Figure 10. Other termination circuits may allow a dc-current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

10.3.3 Common-Mode Range vs Supply Voltage

The SNx5LVDSxx receivers operate over an input common-mode range of ½ × V_{ID} V to 2.4 – ½ × V_{ID} V. If the input signal is anywhere within this range and has a differential magnitude greater than or equal to 100 mV, the receivers correctly output the LVDS bus state.

10.3.4 General Purpose Comparator

While the SNx5LVDSxx receivers are LVDS standard-compliant receivers, their utility and applications extend to a wider range of signals. As long as the input signals are within the required differential and common-mode voltage ranges mentioned above, the receiver output will be a faithful representation of the input signal.

10.3.5 Receiver Equivalent Schematics

The receiver equivalent input and output schematic diagrams are shown in Figure 11. The receiver input is a high-impedance differential pair. 7-V Zener diodes are included on each input to provide ESD protection. The receiver output structure shown is a CMOS inverter with an additional Zener diode, again for ESD protection.

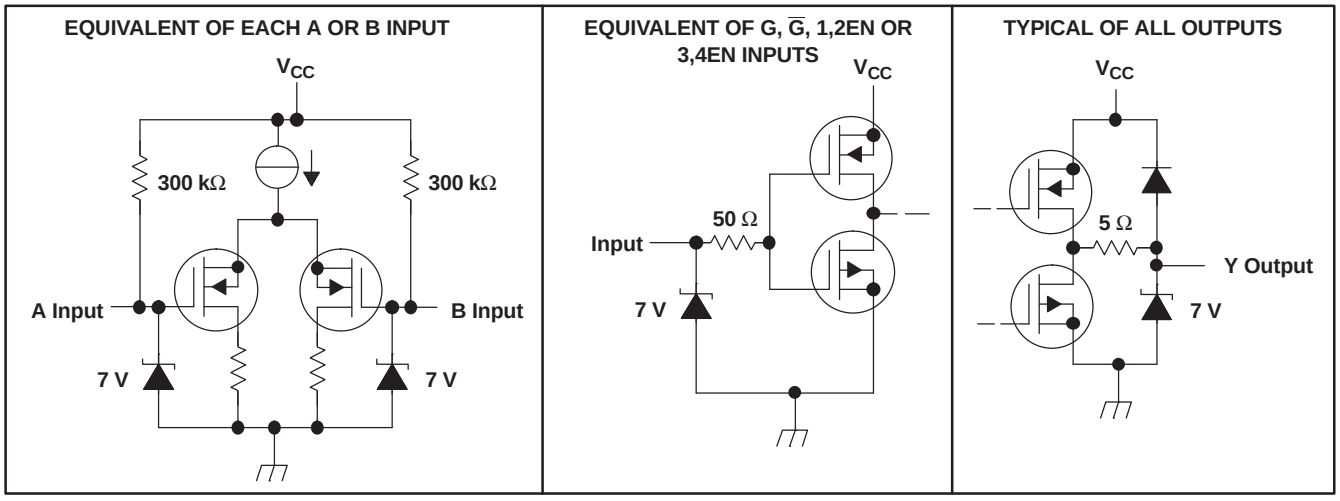
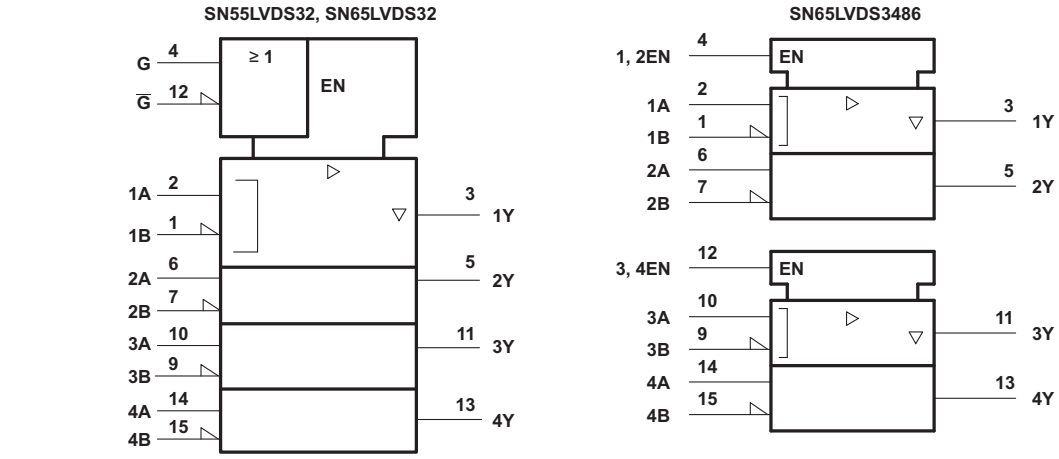


Figure 11. Equivalent Input and Output Schematic Diagrams

10.4 Device Functional Modes

SN55LVDS32, SN65LVDS32 (1)				SN65LVDS3486 (1)		
DIFFERENTIAL INPUT A, B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y	DIFFERENTIAL INPUT A, B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 100$ mV	H X	X L	H H	$V_{ID} \geq 100$ mV	H	H
–100 mV < V_{ID} < 100 mV	H X	X L	? ?	–100 mV < V_{ID} < 100 mV	H	?
$V_{ID} \leq$ –100 mV	H X	X L	L L	$V_{ID} \leq$ –100 mV	H	L
X	L	H	Z	X	L	Z
Open	H X	X L	H H	Open	H	H

(1) H = high level, L = low level, X = irrelevant, Z = high-impedance (off), ? = indeterminate



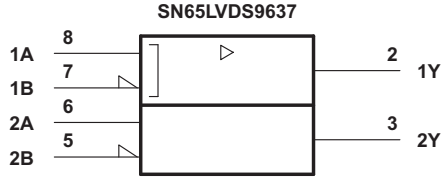
This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 12. SN55LVDS32, SN65LVDS32, and SN65LVDS3486 Logic Symbols

Table 2. Function Table SN65LVDS9637 (1)

DIFFERENTIAL INPUT A, B	OUTPUT Y
$V_{ID} \geq 100$ mV	H
–100 mV < V_{ID} < 100 mV	?
$V_{ID} \leq$ –100 mV	L
Open	H

(1) H = high level, L = low level, ? = indeterminate



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 13. SN65LVDS9637 Logic Symbol

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The SNx5LVDSxx devices are LVDS receivers. These devices are generally used as building blocks for high-speed, point-to-point, data transmission where ground differences are less than 1 V. LVDS drivers and receivers provide high-speed signaling rates that are often implemented with ECL class devices without the ECL power and dual-supply requirements.

11.2 Typical Application

11.2.1 Point-to-Point Communications

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 14.

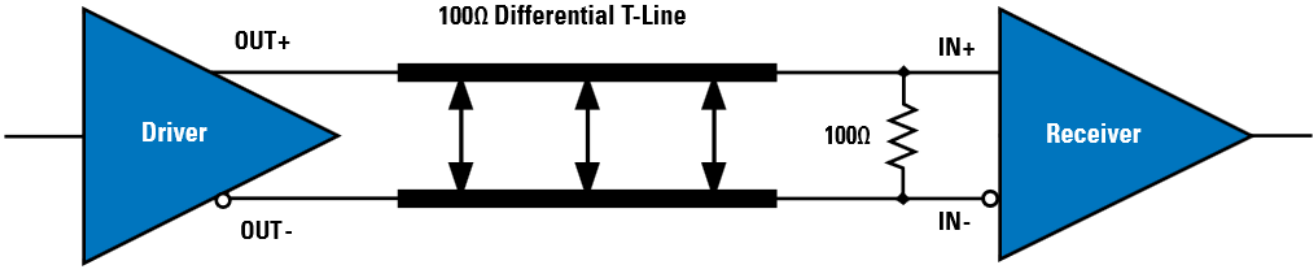


Figure 14. Point-to-Point Topology

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 14 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

11.2.1.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6 V
Driver Input Voltage	0.8 to 3.3 V
Driver Signaling Rate	DC to 100 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6 V
Receiver Input Voltage	0 to 24 V
Receiver Signaling Rate	DC to 100 Mbps
Ground shift between driver and receiver	±1 V

11.2.1.2 Detailed Design Procedure

11.2.1.2.1 Equipment

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS7404 Real Time Scope
- Agilent ParBERT E4832A

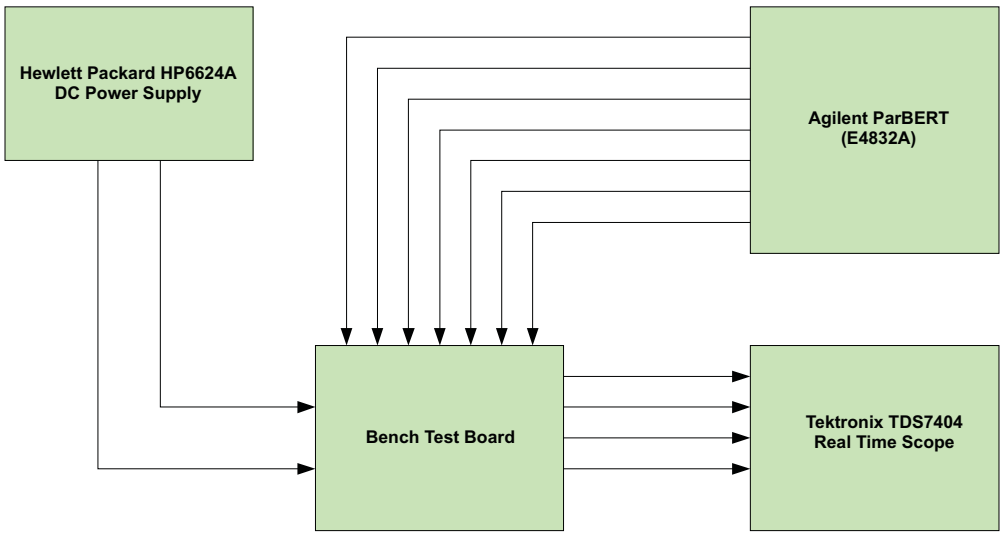


Figure 15. Equipment Setup

11.2.1.2.2 Driver Supply Voltage

An LVDS driver is operated from a single supply. The device can support operation with a supply as low as 3 V and as high as 3.6 V. The differential output voltage is nominally 340 mV over the complete output range. The minimum output voltage stays within the specified LVDS limits (247 mV to 454 mV) for a 3.3-V supply.

11.2.1.2.3 Driver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very-low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 µF to 1000 µF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one should resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson, equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV; however, this figure varies depending on the noise budget available in your design. (1)

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

$$C_{LVDS} = \left(\frac{1A}{0.2V} \right) \times 200\ ps = 0.001\ \mu F \quad (2)$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.001 µF). You should place the smallest value of capacitance as close as possible to the chip.

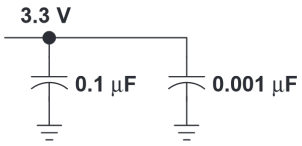


Figure 16. Recommended LVDS Bypass Capacitor Layout

11.2.1.2.4 Driver Output Voltage

A standard-compliant LVDS driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 340 mV. This 340 mV is the absolute value of the differential swing (V_{OD} = $|V^+ – V^–|$). The peak-to-peak differential voltage is twice this value, or 680 mV.

11.2.1.2.5 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces. The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with a variation of no more than 10% (90 Ω to 132 Ω).

11.2.1.2.6 PCB Transmission Lines

As per SNLA187, Figure 17 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 17 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

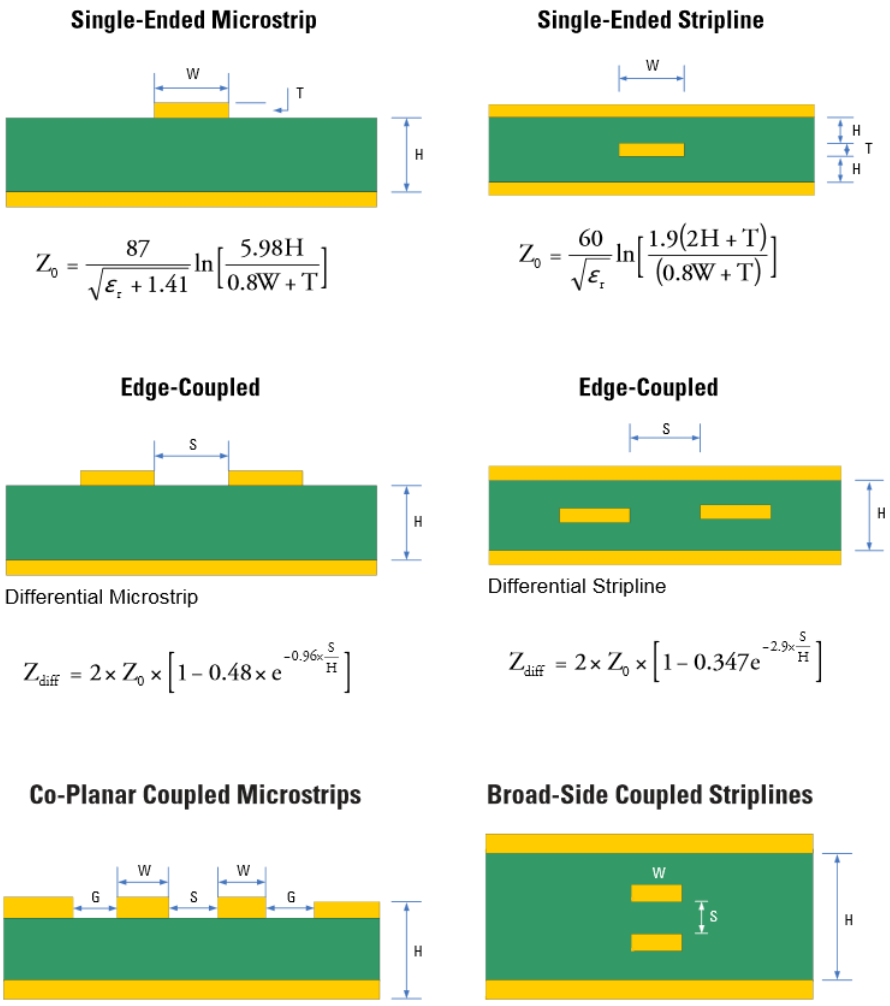


Figure 17. Controlled-Impedance Transmission Lines

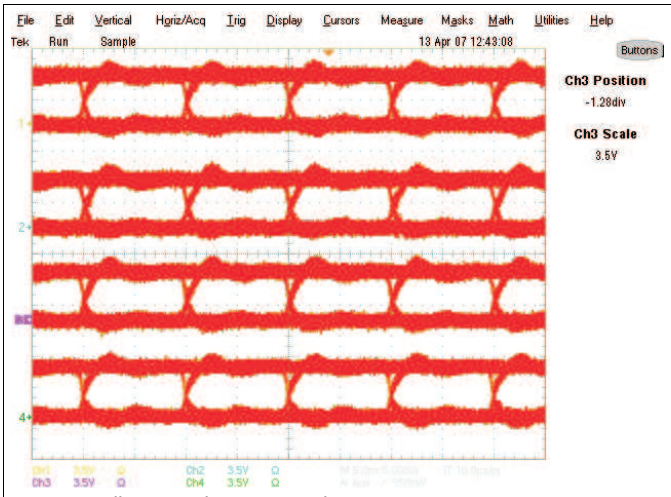
11.2.1.2.7 Termination Resistor

An LVDS communication channel employs a current source driving a transmission line which is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure incident wave switching (which is necessary to operate the channel at the highest signaling rate), the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be between 90 and 110 Ω.

The line termination resistance should be located as close as possible to the receiver, thereby minimizing the stub length from the resistor to the receiver. The limiting case would be to incorporate the termination resistor into the receiver, which is exactly what is offered with a device like the SN65LVDT386.

While we talk in this section about point-to-point communications, a word of caution is useful when a multidrop topology is used. In such topologies, line termination resistors are to be located only at the end(s) of the transmission line. In such an environment, LVDS receivers could be used for loads branching off the main bus with an LVDT receiver used only at the bus end.

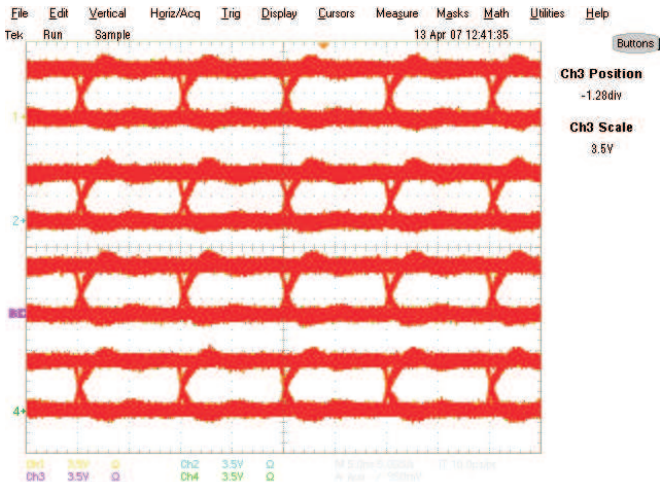
11.2.1.3 Application Curves



All Rx running at 100 Mbps;
Channel 1: 1Y
Channel 2: 2Y
Channel 3: 3Y
Channel 4: 4Y

T = 25°C
V_{CC} = 3.6 V
PRBS = 2^{23} – 1

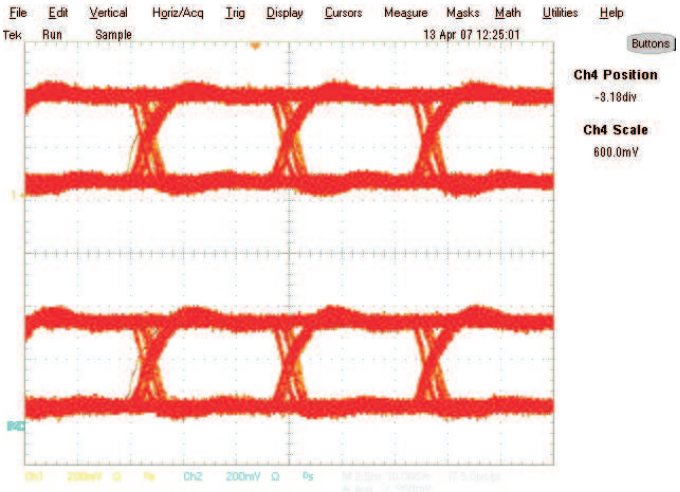
Figure 18. Typical Eye Patterns SN65LVDS32



All Rx running at 100 Mbps;
Channel 1: 1Y
Channel 2: 2Y
Channel 3: 3Y
Channel 4: 4Y

T = 25°C
V_{CC} = 3.6 V
PRBS = 2^{23} – 1

Figure 19. Typical Eye Patterns SN65LVDS3486



All Rx running at 150 Mbps;
Channel 1: 1Y
Channel 2: 2Y

T = 25°C
V_{CC} = 3.6 V
PRBS = 2^{23} – 1

Figure 20. Typical Eye Patterns SN65LVDS9637

12 Power Supply Recommendations

The LVDS driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 2.4 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than |±1 V|. Board-level and local device-level bypass capacitance should be used and are covered in *Driver Bypass Capacitance*.

13 Layout

13.1 Layout Guidelines

13.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 21.

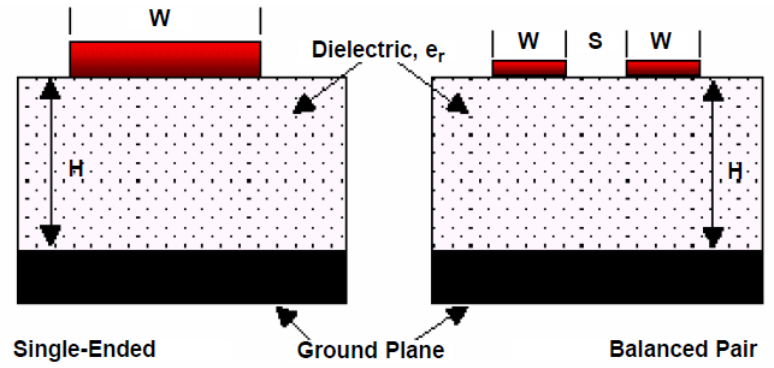


Figure 21. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 2, 3, and 4 provide formulas for Z_O and t_{PD} for differential and single-ended traces. (1) (2) (3)

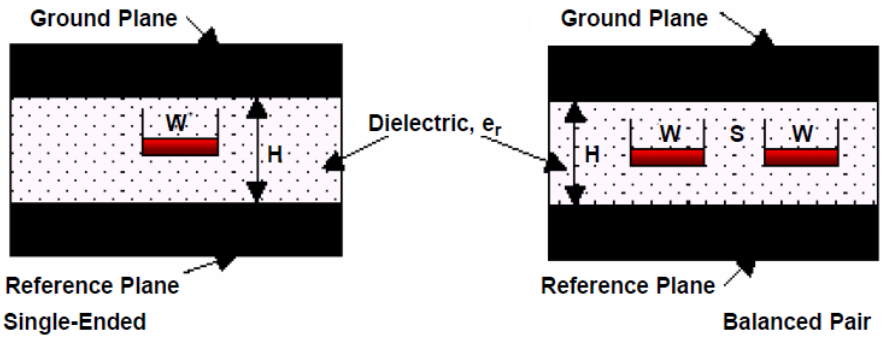


Figure 22. Stripline Topology

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Layout Guidelines (continued)

13.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz.
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

13.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you should decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 23.

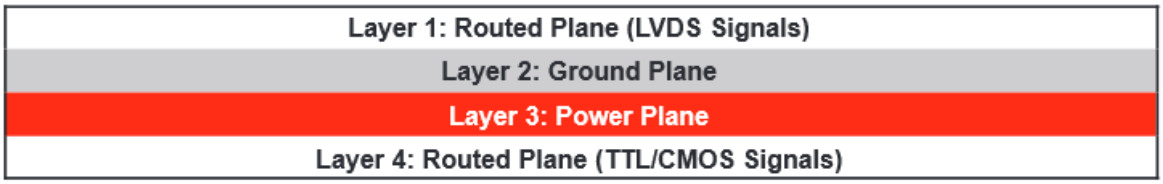


Figure 23. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 24.

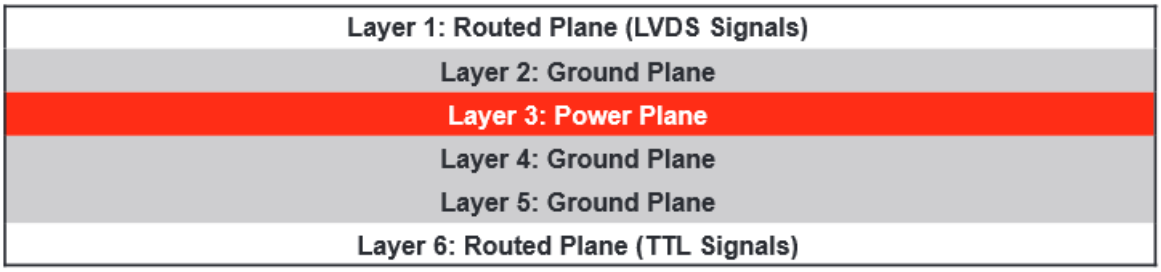


Figure 24. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

Layout Guidelines (continued)

13.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces should be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

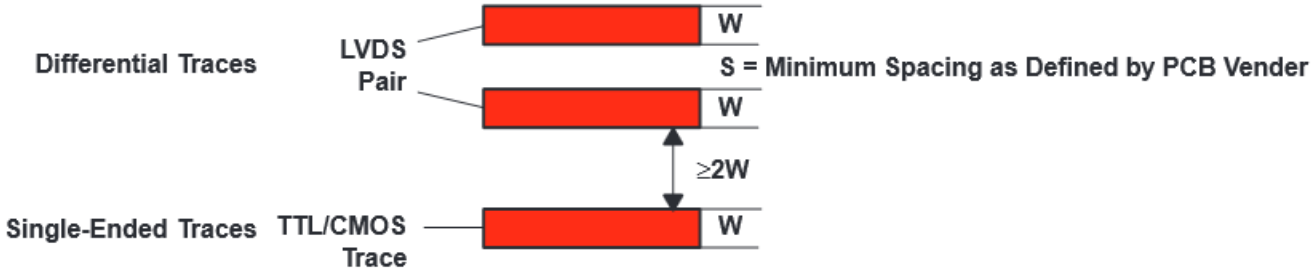


Figure 25. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

13.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

13.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 26.

Layout Example (continued)

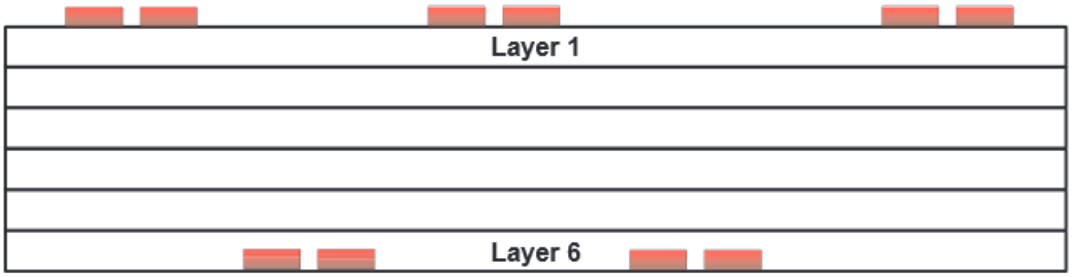


Figure 26. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 27. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

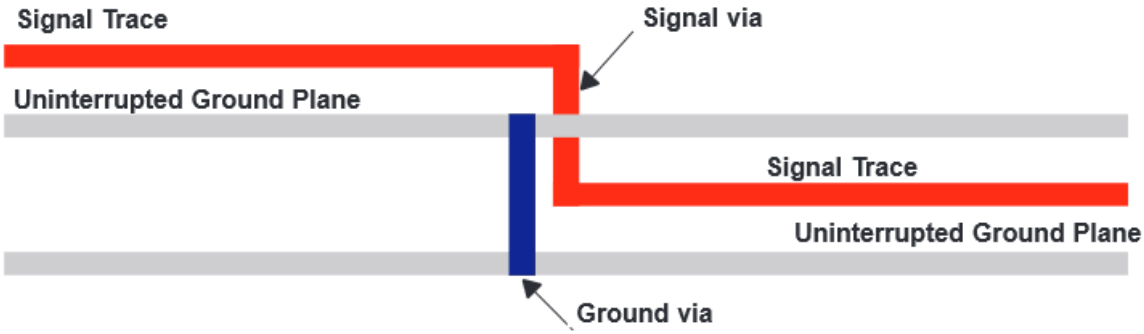


Figure 27. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

14 Device and Documentation Support

14.1 Device Support

14.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

14.1.2 Other LVDS Products

For other products and application notes in the LVDS and LVDM product families visit our Web site at http://www.ti.com/sc/datatran.

14.2 Documentation Support

14.2.1 Related Information

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

14.3 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN55LVDS32	Click here	Click here	Click here	Click here	Click here
SN65LVDS32	Click here	Click here	Click here	Click here	Click here
SN65LVDS3486	Click here	Click here	Click here	Click here	Click here
SN65LVDS9637	Click here	Click here	Click here	Click here	Click here

14.4 Trademarks

Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

14.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9762201Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762201Q2A SNJ55LVDS32FK
5962-9762201QEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762201QEA SNJ55LVDS32J
5962-9762201QFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762201QFA SNJ55LVDS32W
SN55LVDS32W	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55LVDS32W
SN65LVDS32D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32DG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32DRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32DRG4.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32NS.B	Active	Production	SOP (NS) | 16	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32NSR.B	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS32PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32
SN65LVDS3486D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486
SN65LVDS3486D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486
SN65LVDS3486DG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486
SN65LVDS3486DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486
SN65LVDS3486DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS3486DRG4.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486
SN65LVDS9637D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637
SN65LVDS9637D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637
SN65LVDS9637DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF
SN65LVDS9637DGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF
SN65LVDS9637DGKG4	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF
SN65LVDS9637DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF
SN65LVDS9637DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF
SN65LVDS9637DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF
SN65LVDS9637DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37
SN65LVDS9637DGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37
SN65LVDS9637DGNG4	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37
SN65LVDS9637DGNG4.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37
SN65LVDS9637DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37
SN65LVDS9637DGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37
SN65LVDS9637DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637
SN65LVDS9637DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637
SN65LVDS9637DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637
SN65LVDS9637DRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637
SNJ55LVDS32FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762201Q2A SNJ55 LVDS32FK
SNJ55LVDS32J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762201QE A SNJ55LVDS32J
SNJ55LVDS32W	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762201QF A SNJ55LVDS32W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55LVDS32 :

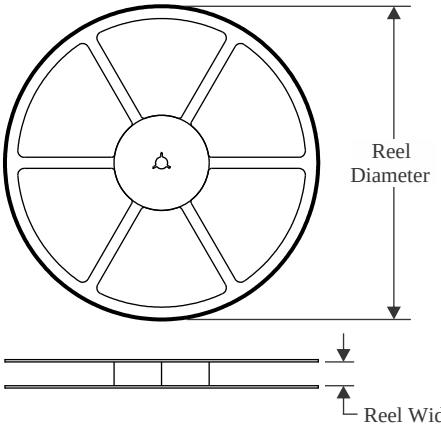
- Catalog : SN75LVDS32
- Space : SN55LVDS32-SP

NOTE: Qualified Version Definitions:

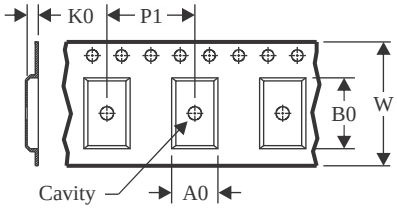
- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

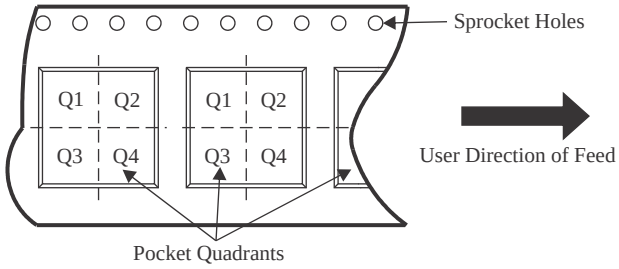


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

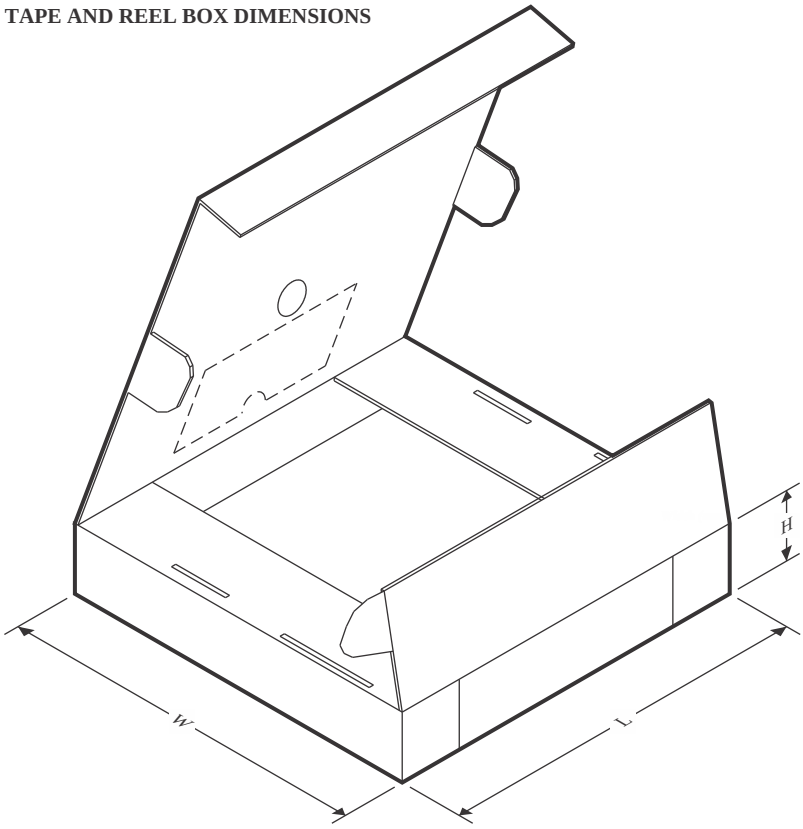
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS32DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS32DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS32NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65LVDS32PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS3486DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS9637DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS9637DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS9637DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDS9637DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

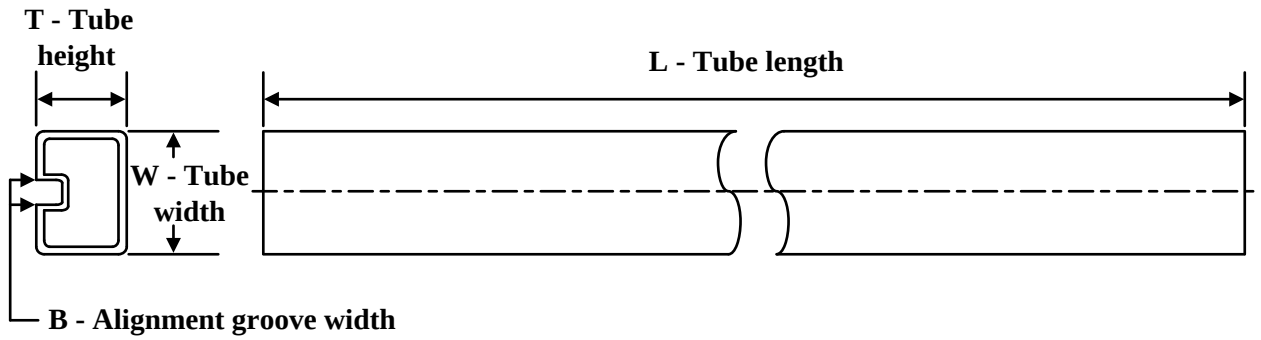
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS32DR	SOIC	D	16	2500	340.5	336.1	32.0
SN65LVDS32DRG4	SOIC	D	16	2500	340.5	336.1	32.0
SN65LVDS32NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN65LVDS32PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDS3486DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS9637DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDS9637DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
SN65LVDS9637DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65LVDS9637DRG4	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

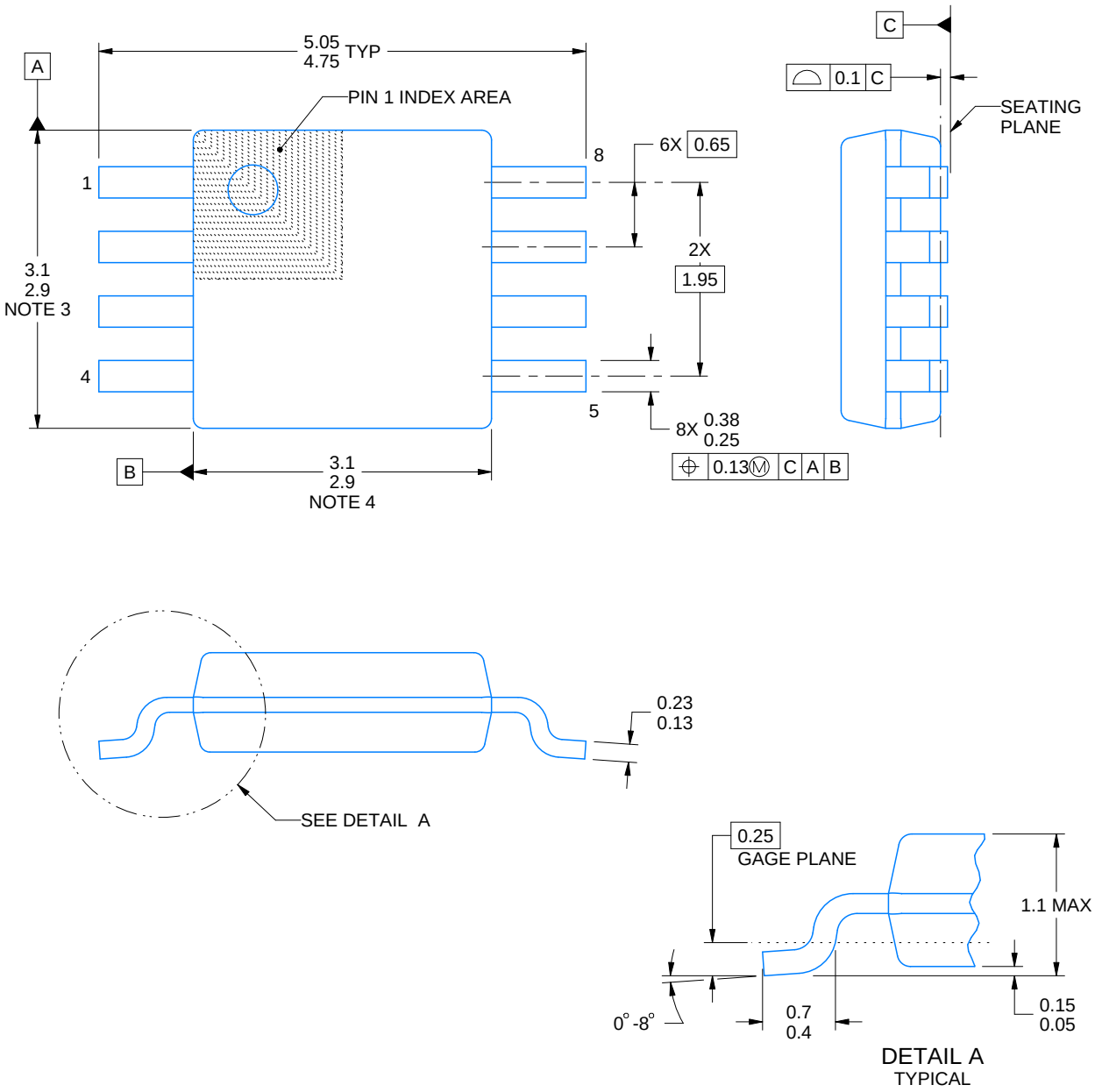
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9762201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9762201QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN55LVDS32W	W	CFP	16	25	506.98	26.16	6220	NA
SN65LVDS32D	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS32D.B	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS32DG4	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS32NS.B	NS	SOP	16	50	530	10.5	4000	4.1
SN65LVDS32PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS32PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS3486D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS3486D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS3486DG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS9637D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDS9637D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDS9637D.B	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDS9637D.B	D	SOIC	8	75	507	8	3940	4.32
SNJ55LVDS32FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55LVDS32W	W	CFP	16	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

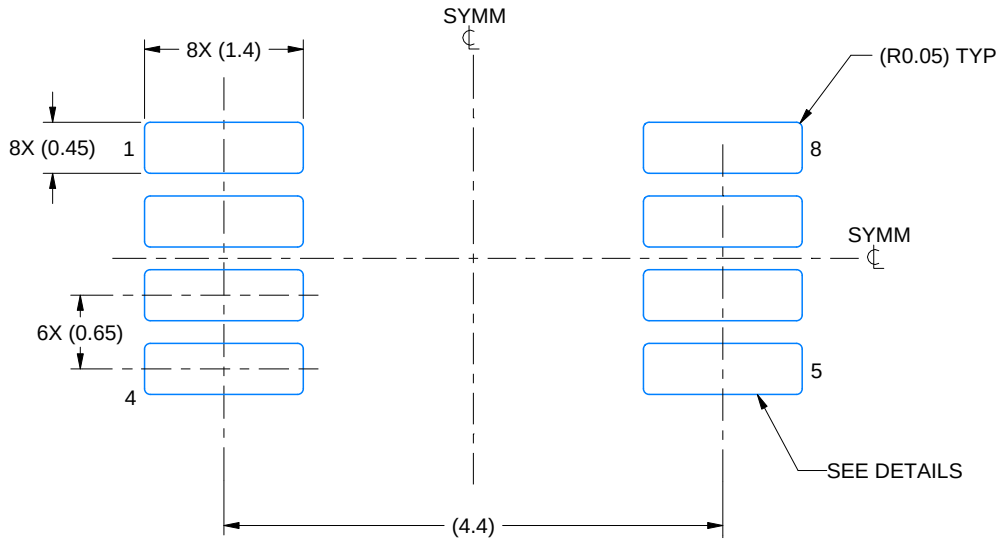
SMALL OUTLINE PACKAGE



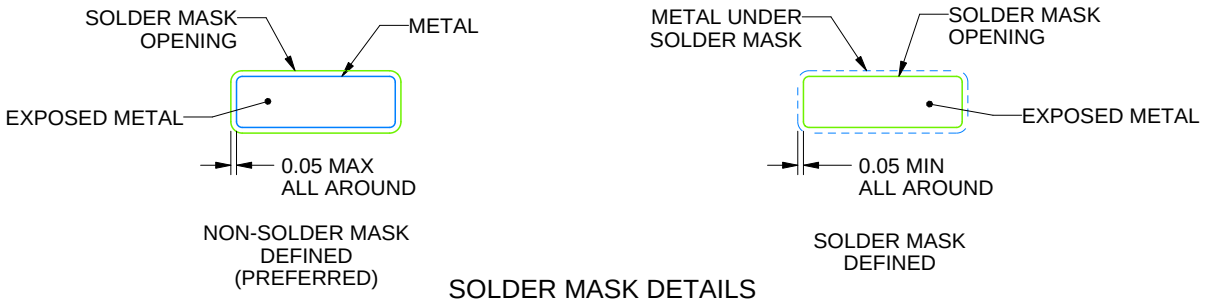
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

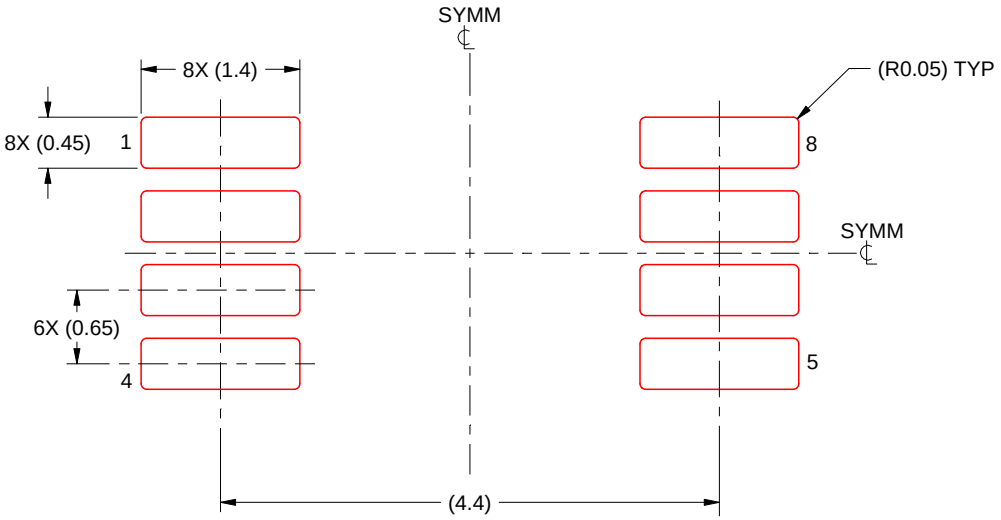


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

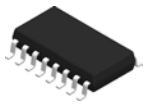


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

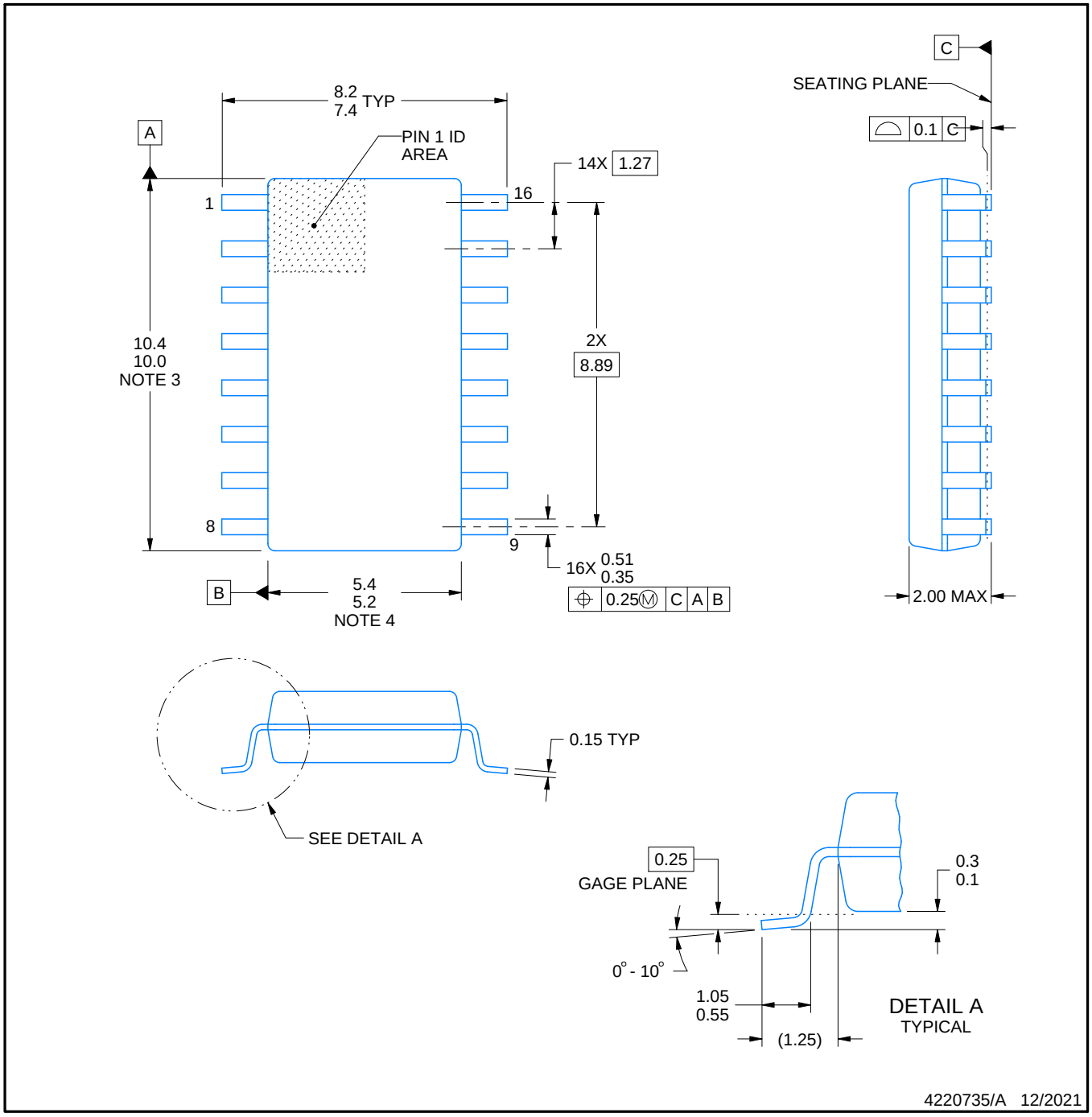


PACKAGE OUTLINE

NS0016A

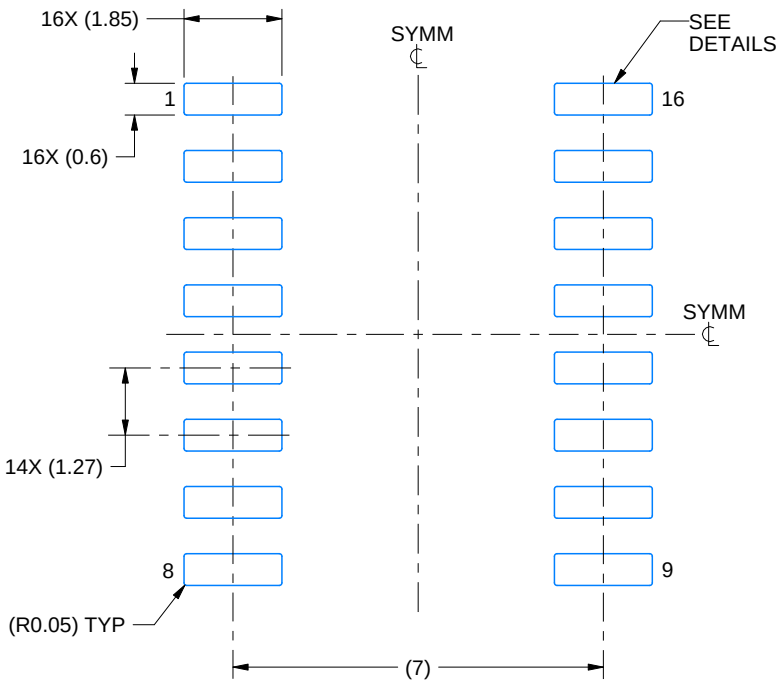
SOP - 2.00 mm max height

SOP

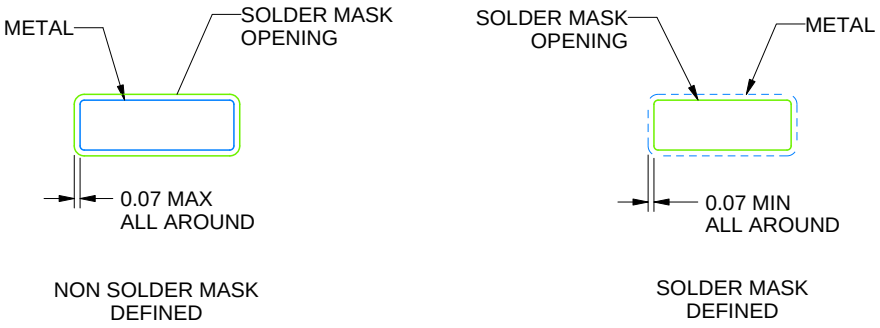


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

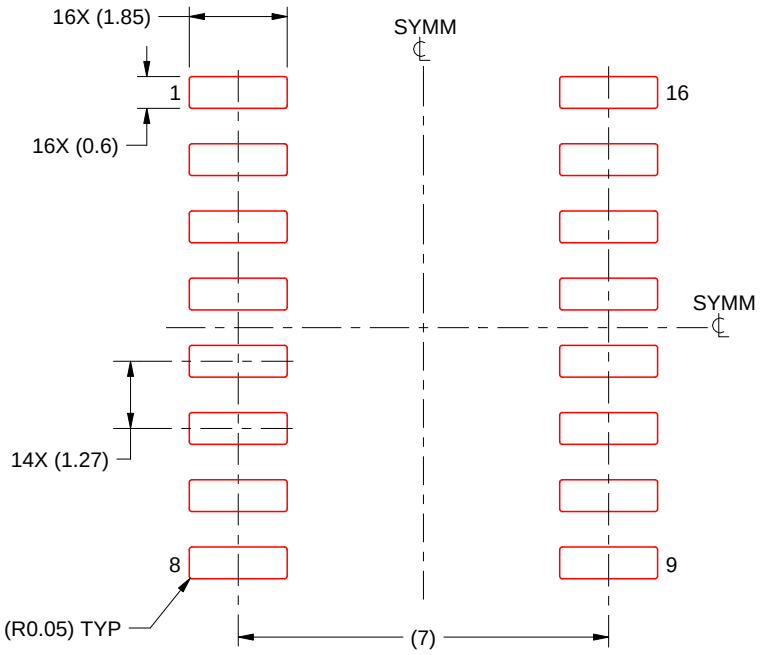
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



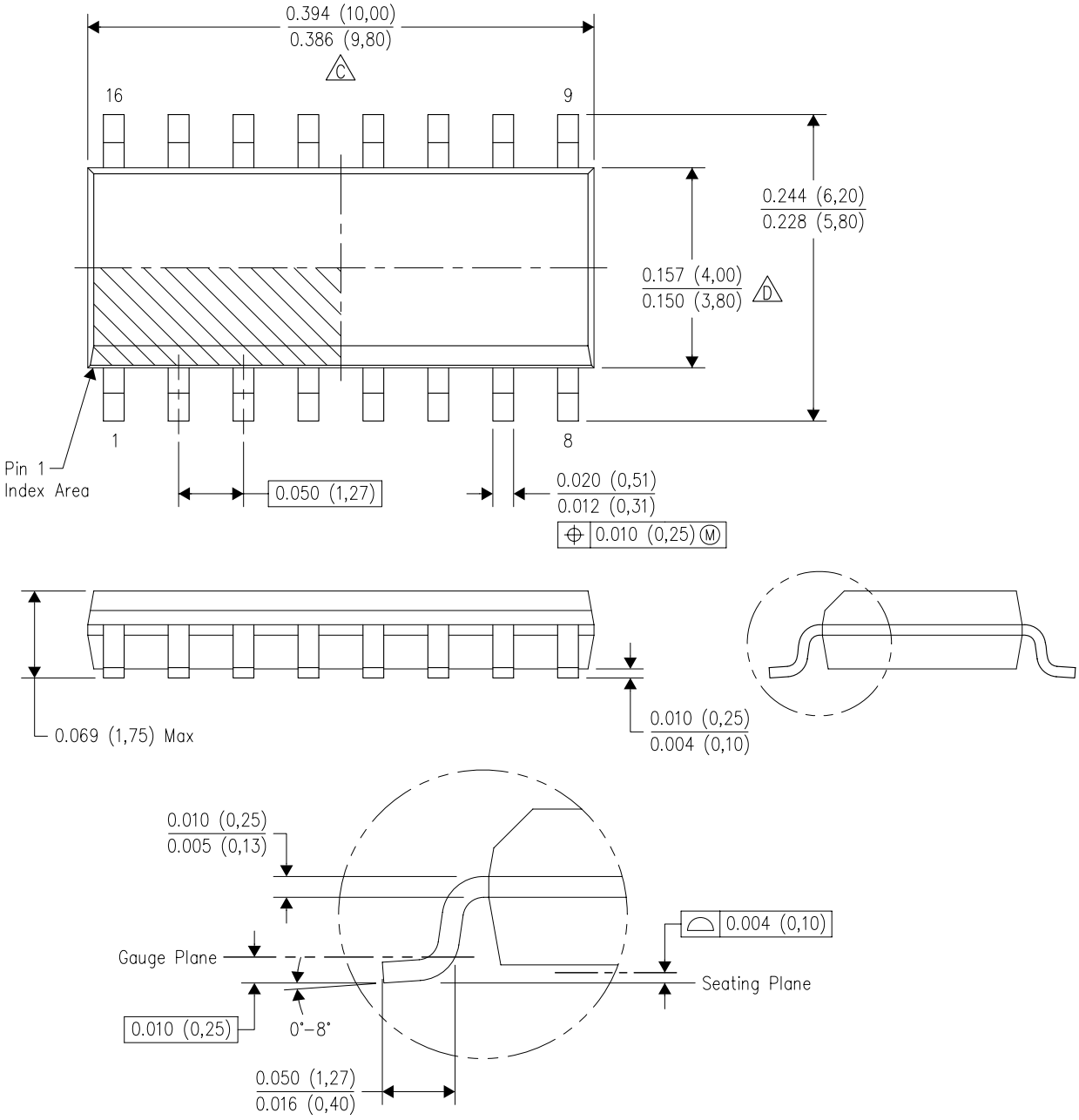
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



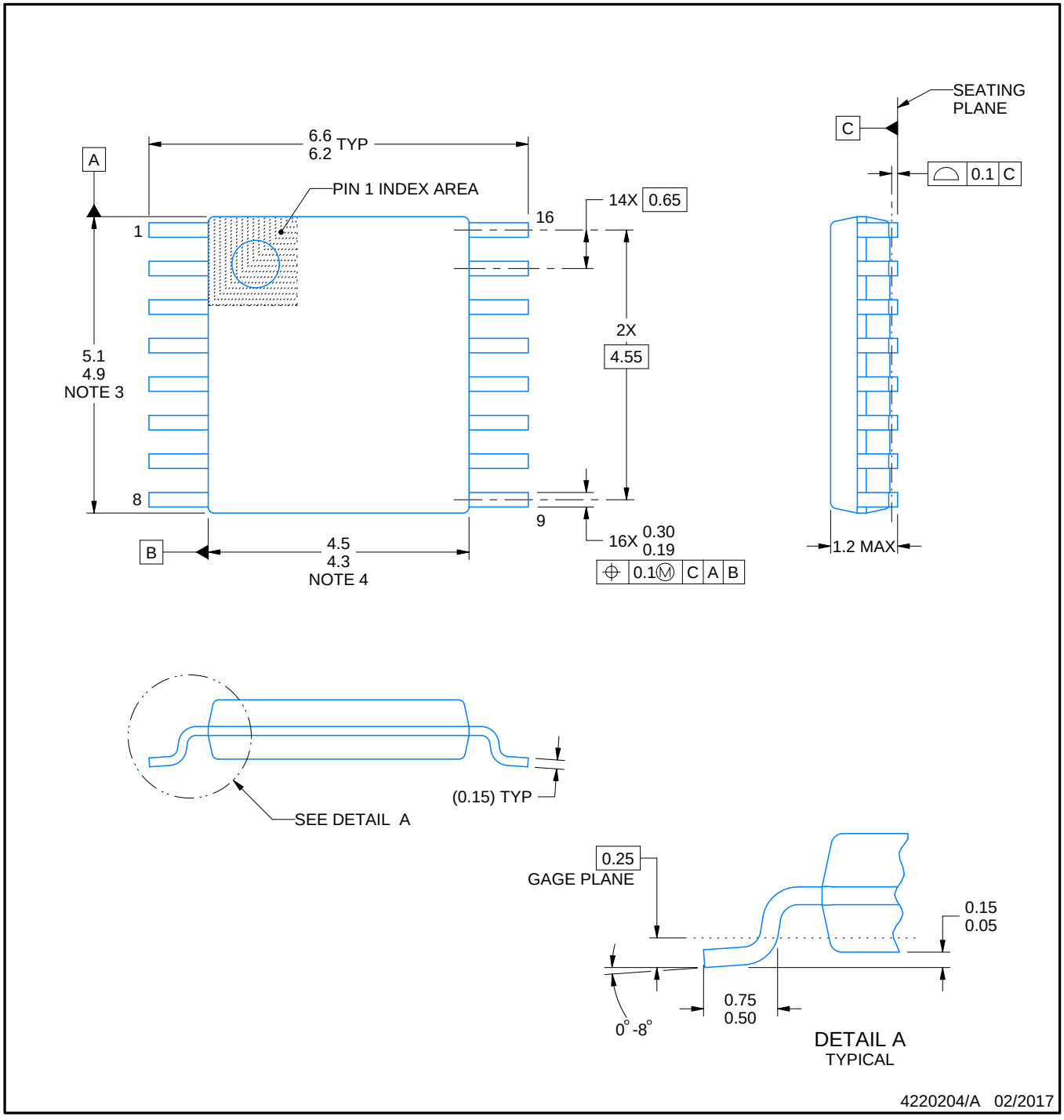
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

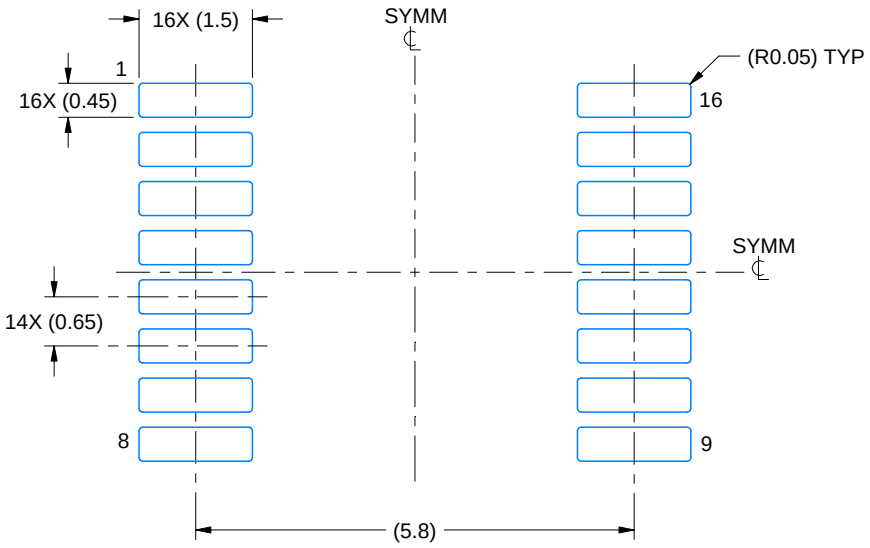
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

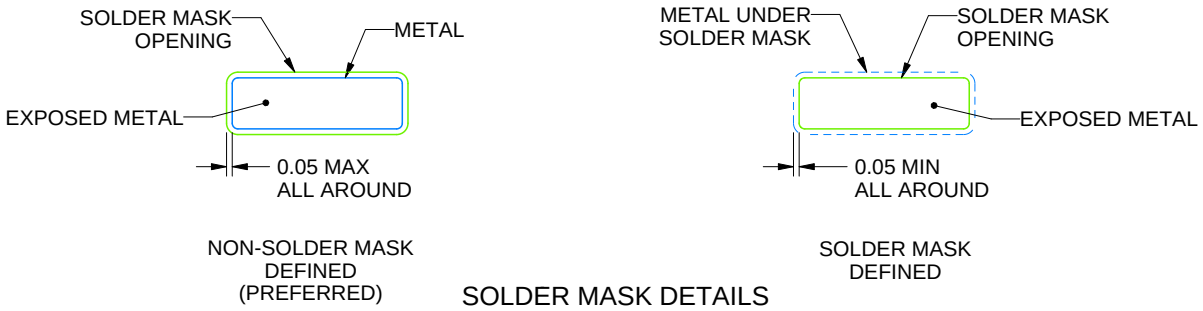


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

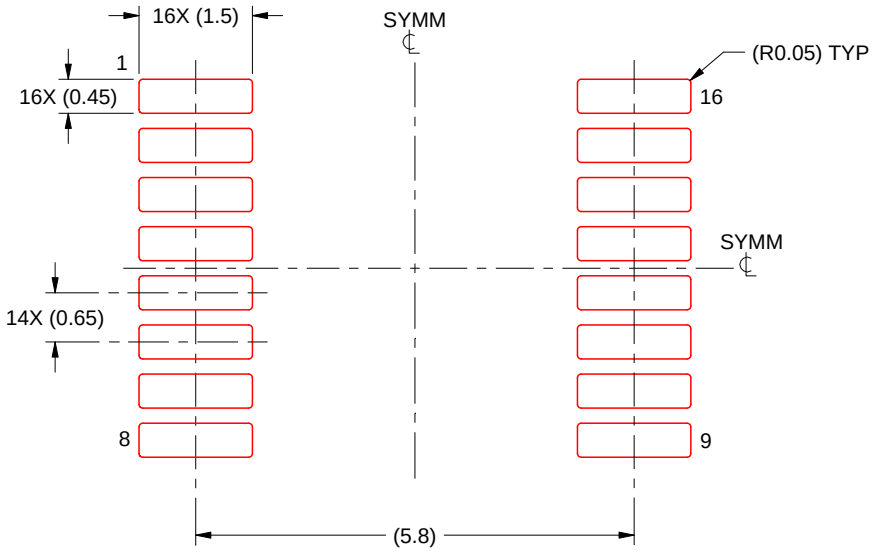


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

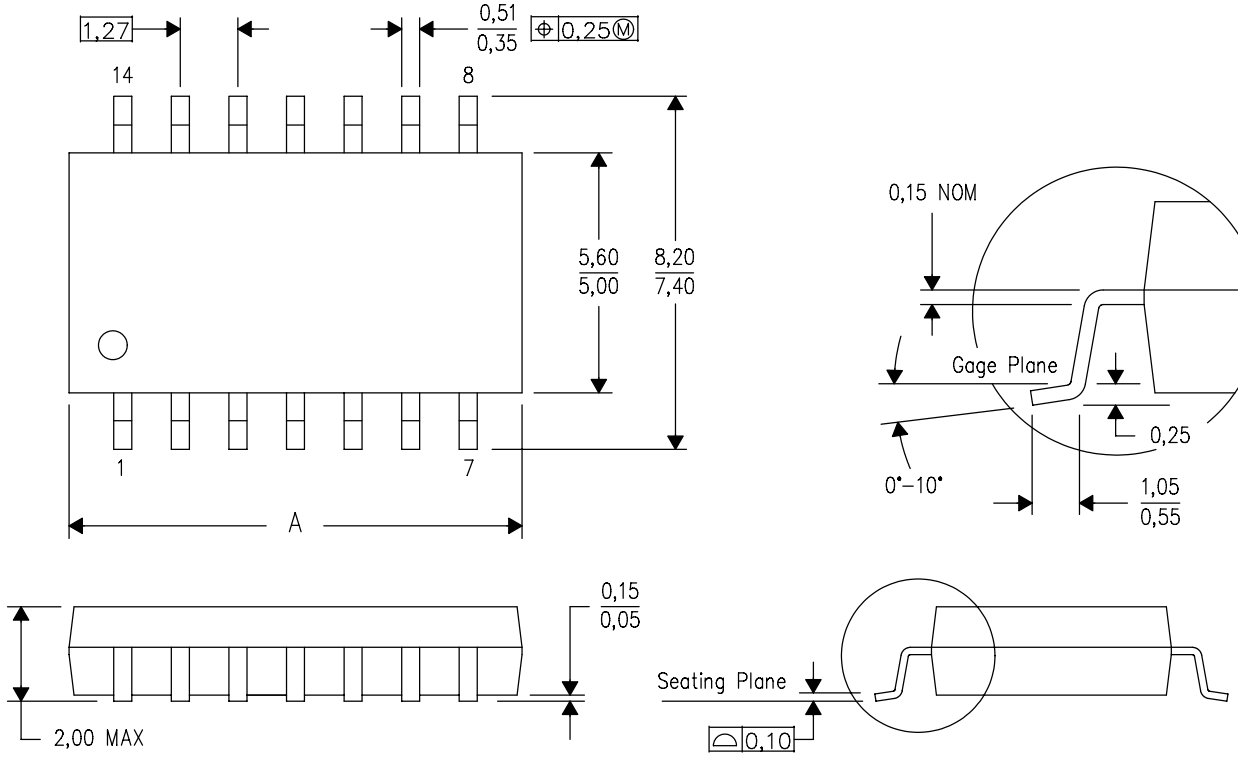
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

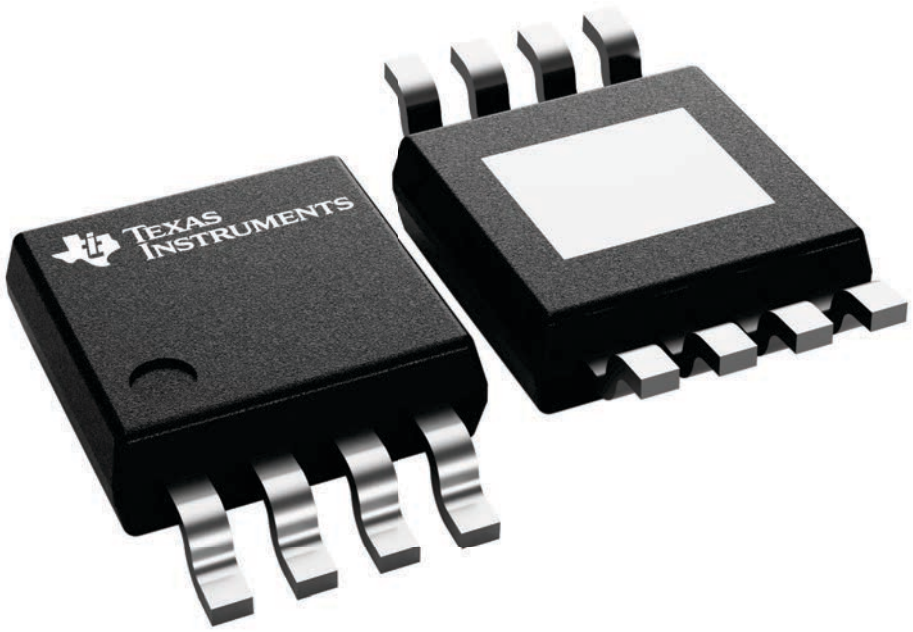
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

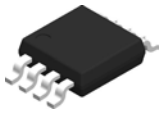
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

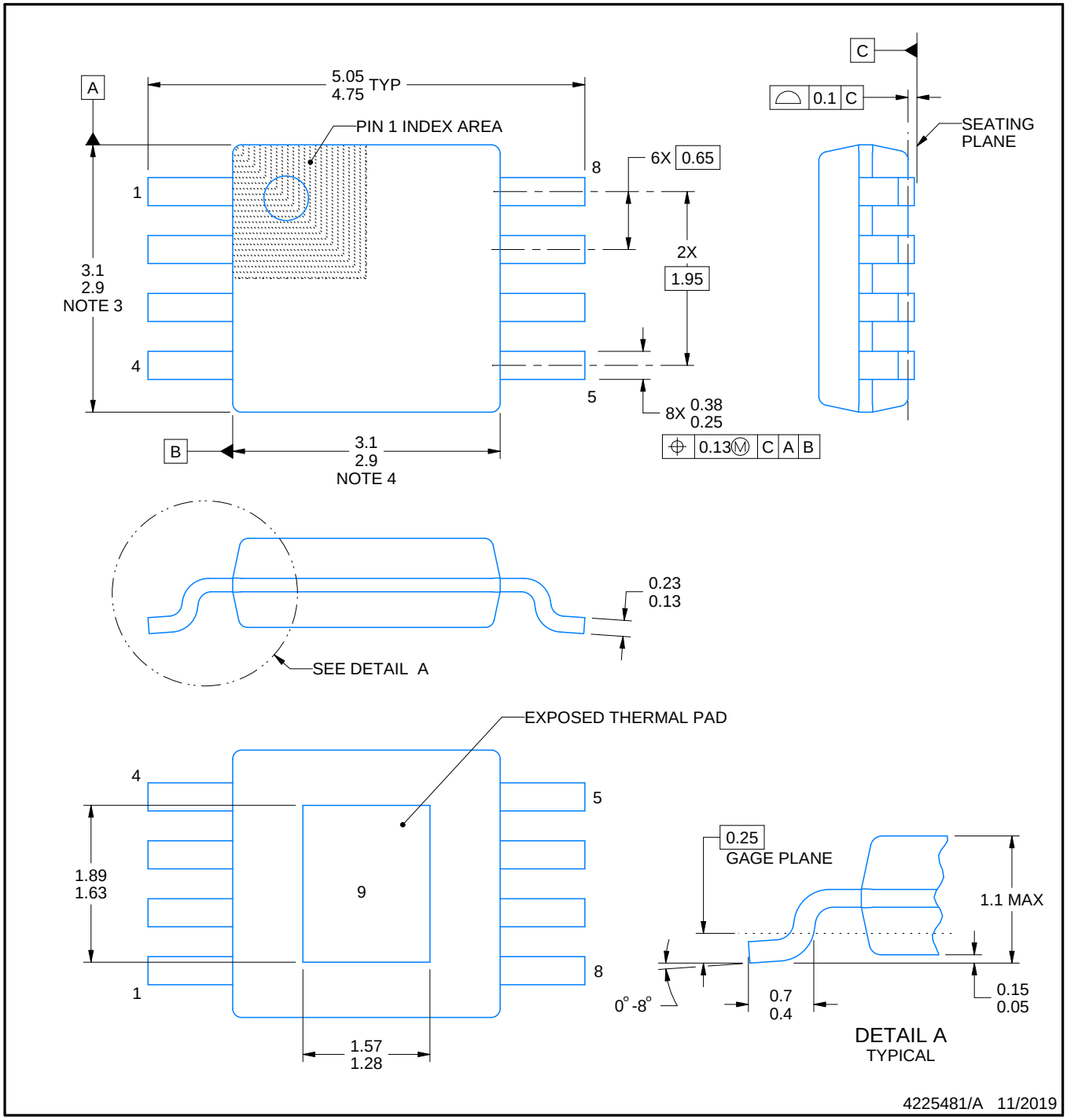
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

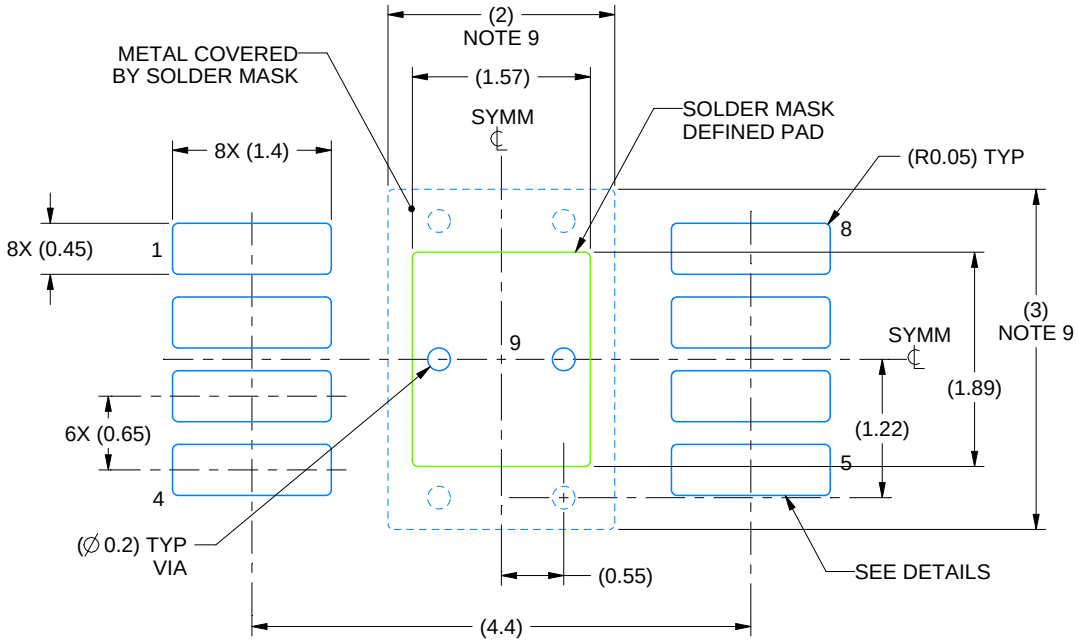
SMALL OUTLINE PACKAGE



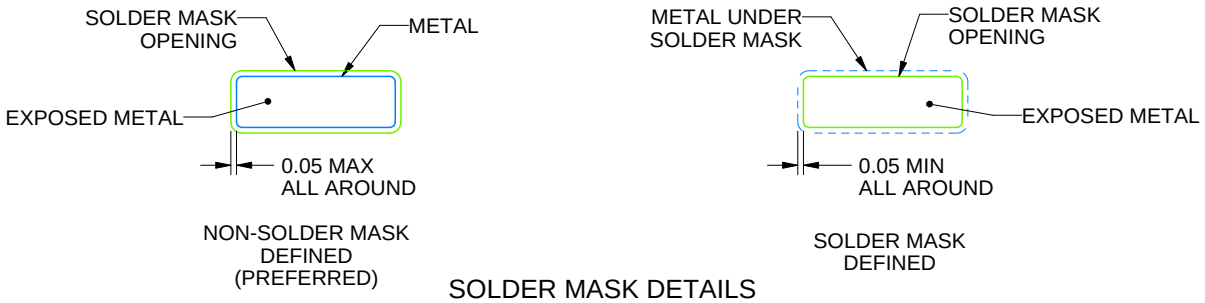
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

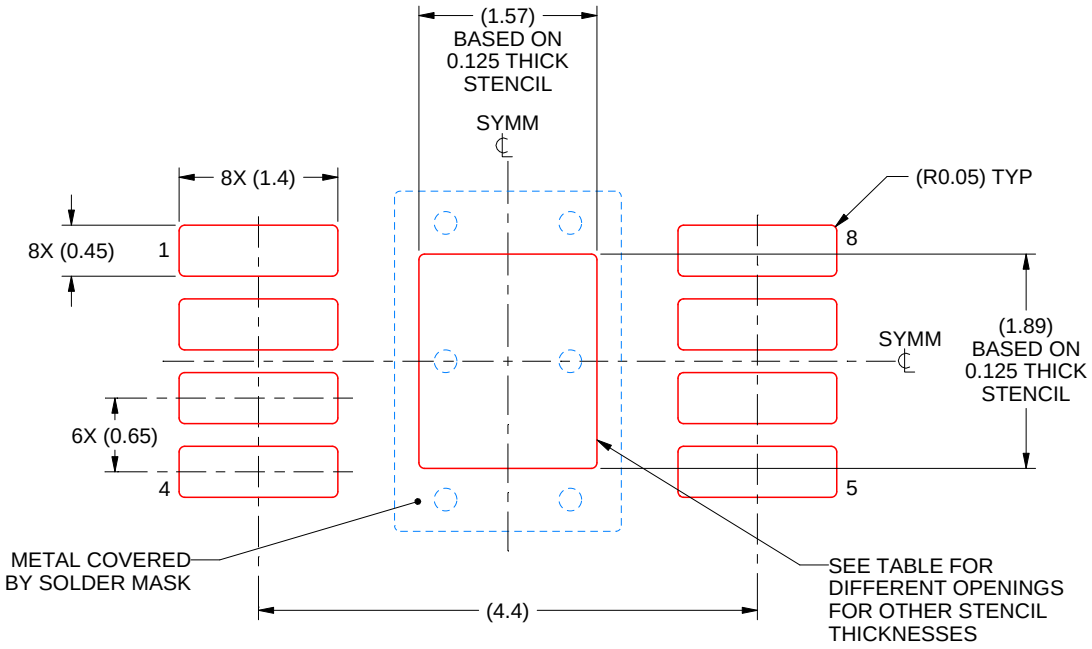


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

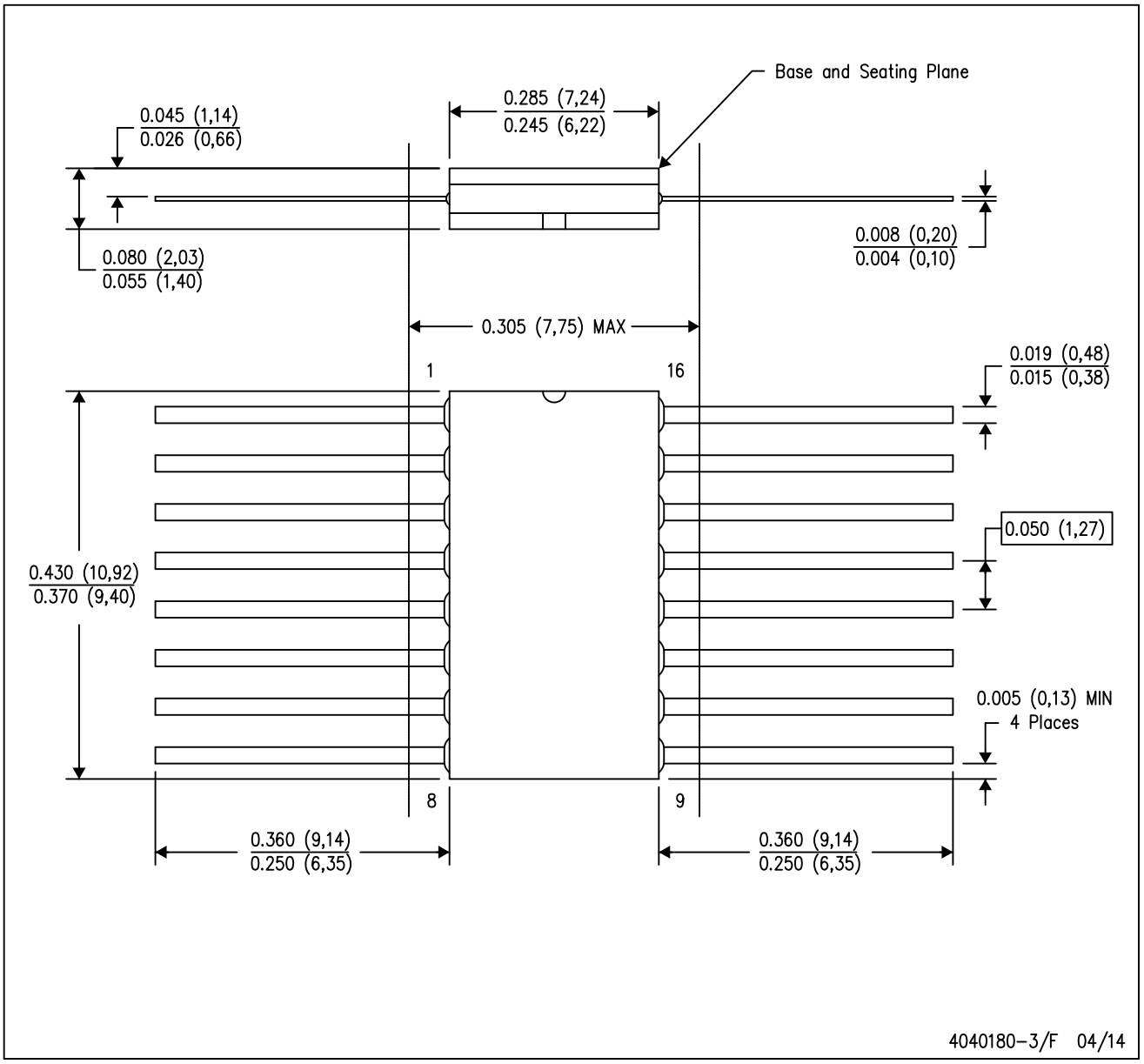
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

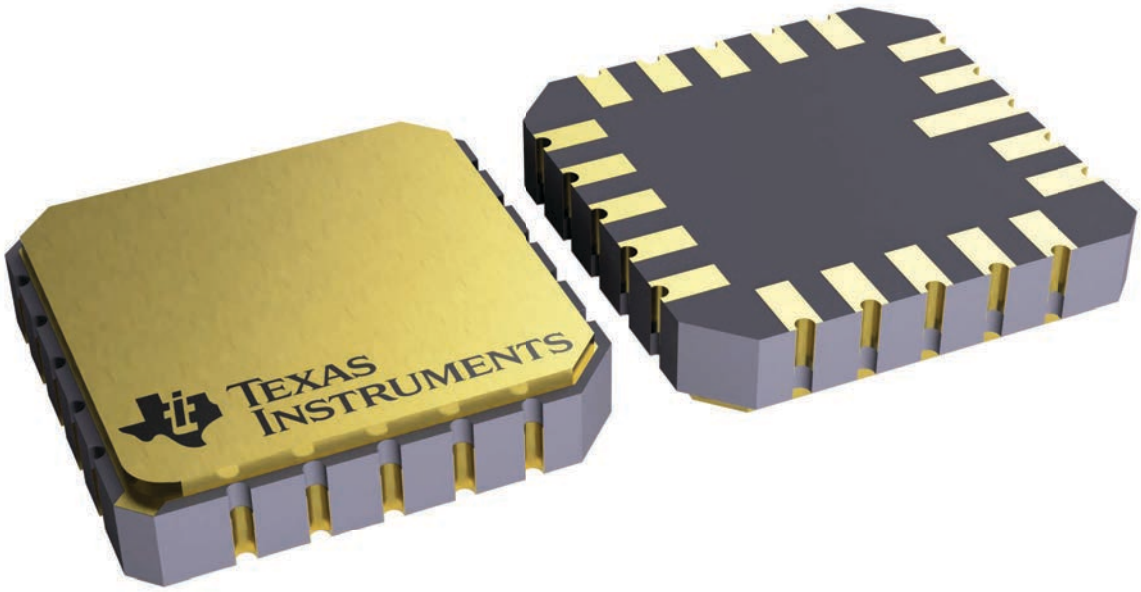
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

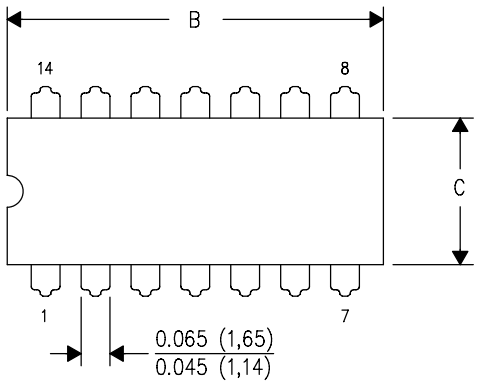


4229370VA\

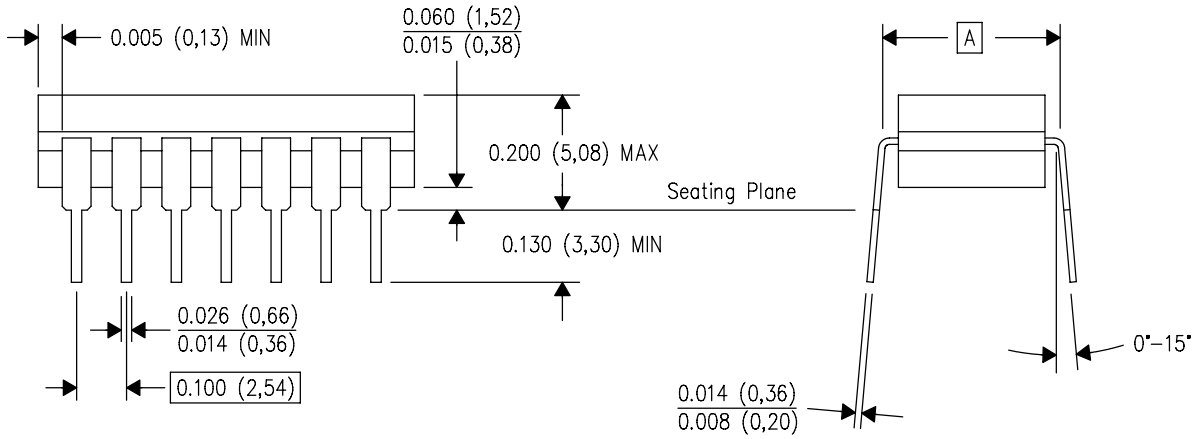
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE

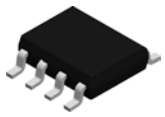


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

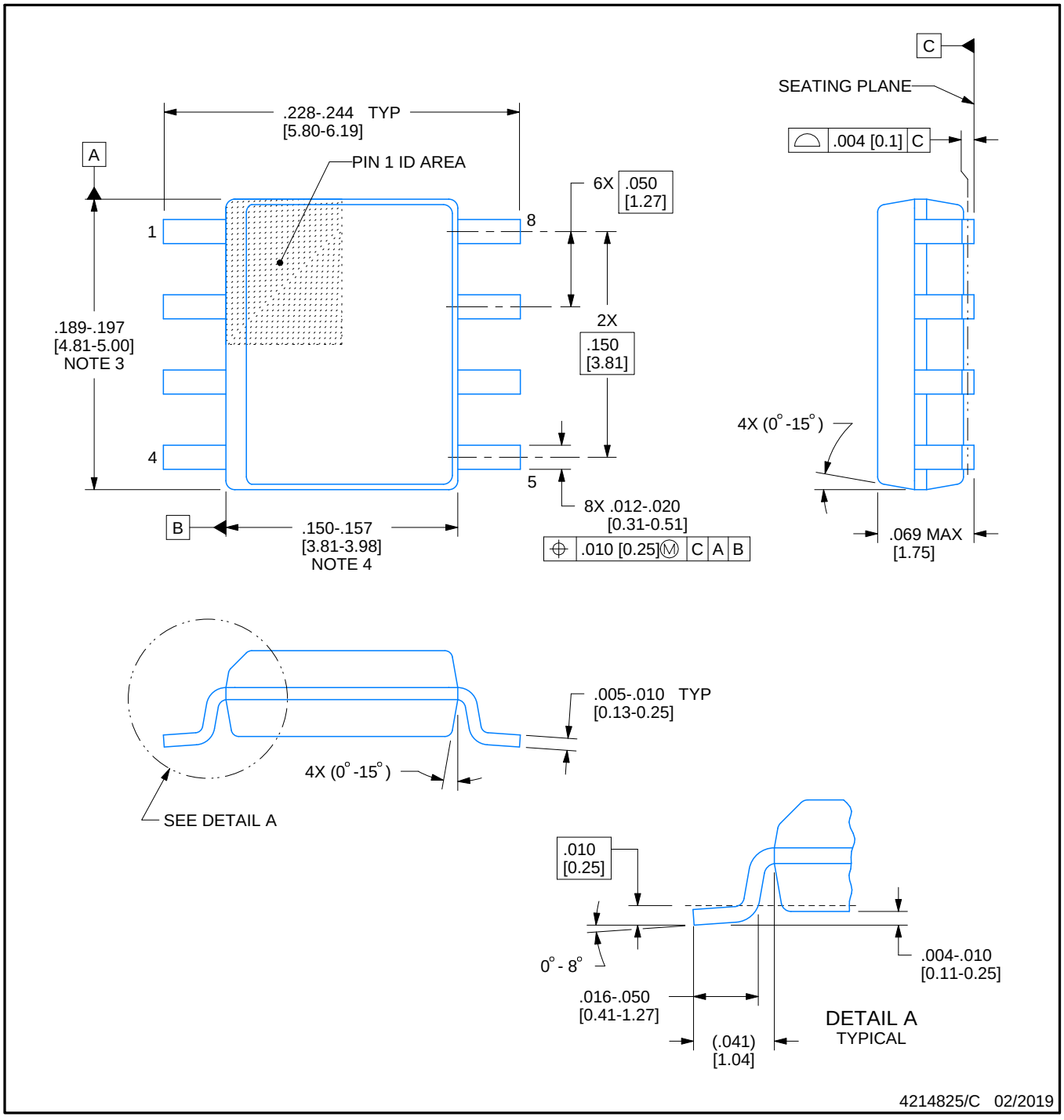


PACKAGE OUTLINE

D0008A

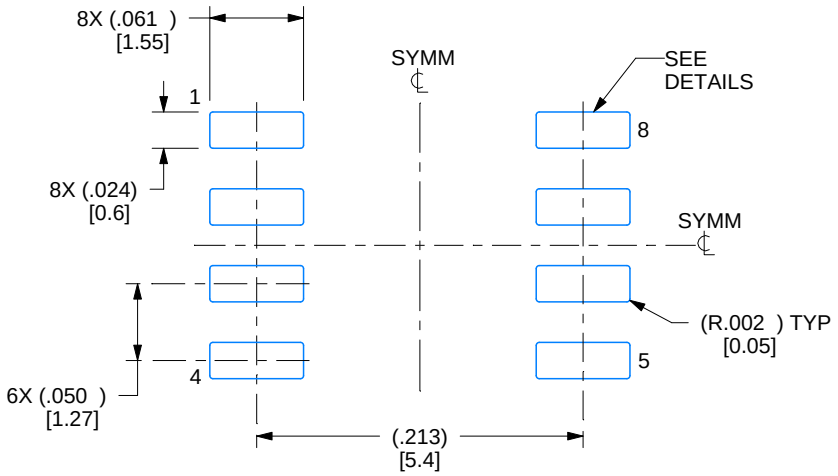
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

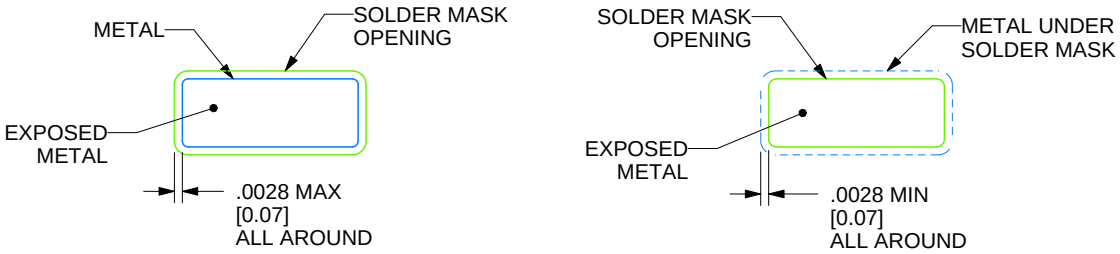


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

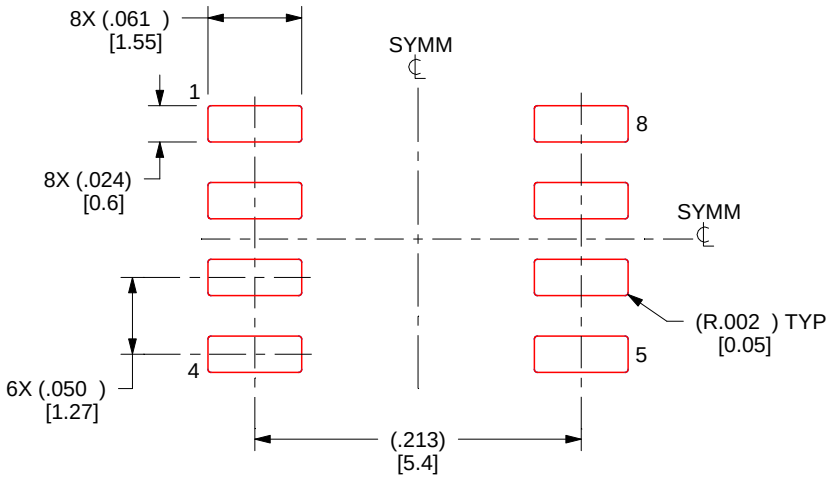
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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