

SN65C116xE Dual Differential Drivers and Receivers With $\pm 15\text{kV}$ ESD Protection

1 Features

- Meet or exceed standards TIA/EIA-422-B and ITU recommendation V.11
- Operate from single 5V power supply
- ESD Protection for RS-422 bus pins
 - $\pm 15\text{kV}$ Human-body model (HBM)
 - $\pm 8\text{kV}$ IEC 61000-4-2, Contact discharge
 - $\pm 8\text{kV}$ IEC 61000-4-2, Air-gap discharge
- Low supply-current requirements: 9mA maximum
- Low pulse skew
- Receiver input impedance: 17k Ω (Typical)
- Receiver input sensitivity: $\pm 200\text{mV}$
- Receiver common-mode input voltage range of –7V to +7V
- Glitch-free power-up and power-down protection
- Receiver 3-state outputs active-low enable (SN65C1167E only)

2 Applications

- AC and servo [motor drives](#)
- [Factory automation and control](#)
- [Wireless infrastructure](#)

3 Description

The SN65C1167E and SN65C1168E consist of dual drivers and dual receivers with $\pm 15\text{kV}$ ESD (Human Body Model [HBM]) and $\pm 8\text{-kV}$ ESD (IEC61000-4-2 Air-Gap Discharge and Contact Discharge) for RS-422 bus pins. The devices meet the requirements of TIA/EIA-422-B and ITU recommendation V.11.

The SN65C1167E combines dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control.

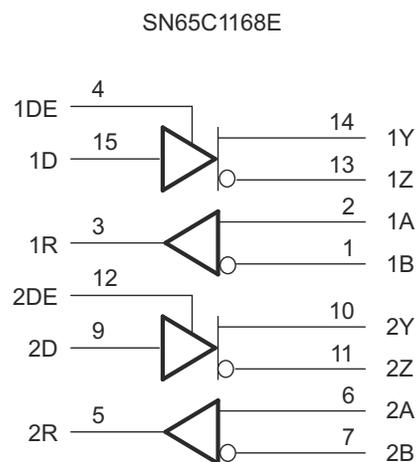
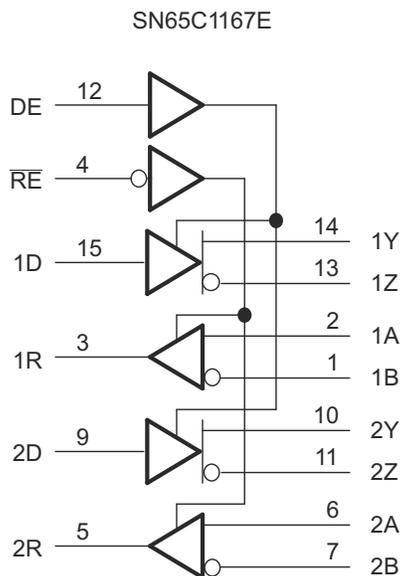
SN65C1168E drivers have individual active-high enables.

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ |
|-------------|------------------------|-----------------------------|
| SN65C116xE | SO (16) | 10.3mm × 5.3mm |
| | TSSOP (16) | 5mm × 4.4mm |
| | VQFN (16) | 4mm × 3.5mm |

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Copyright © 2017, Texas Instruments Incorporated

Block Diagram



Table of Contents

| | | | |
|---|----|--|----|
| 1 Features | 1 | 7.3 Feature Description..... | 11 |
| 2 Applications | 1 | 7.4 Device Functional Modes..... | 12 |
| 3 Description | 1 | 8 Application and Implementation | 13 |
| 4 Pin Configuration and Functions | 3 | 8.1 Application Information..... | 13 |
| 5 Specifications | 5 | 8.2 Typical Application..... | 14 |
| 5.1 Absolute Maximum Ratings..... | 5 | 8.3 Power Supply Recommendations..... | 14 |
| 5.2 Driver Output and Receiver Input ESD Ratings..... | 5 | 9 Device and Documentation Support | 15 |
| 5.3 Recommended Operating Conditions..... | 6 | 9.1 Device Support..... | 15 |
| 5.4 Thermal Information..... | 6 | 9.2 Receiving Notification of Documentation Updates.... | 15 |
| 5.5 Driver Section Electrical Characteristics..... | 7 | 9.3 Support Resources..... | 15 |
| 5.6 Receiver Section Electrical Characteristics..... | 7 | 9.4 Trademarks..... | 15 |
| 5.7 Driver Section Switching Characteristics..... | 8 | 9.5 Electrostatic Discharge Caution..... | 15 |
| 5.8 Receiver Section Switching Characteristics..... | 8 | 9.6 Glossary..... | 15 |
| 6 Parameter Measurement Information | 9 | 10 Revision History | 15 |
| 7 Detailed Description | 11 | 11 Mechanical, Packaging, and Orderable Information | 15 |
| 7.1 Overview..... | 11 | | |
| 7.2 Functional Block Diagram..... | 11 | | |

4 Pin Configuration and Functions

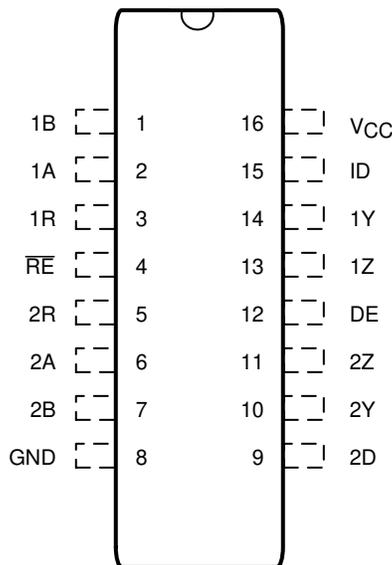


Figure 4-1. NS or PW Package 16 Pin (NS or TSSOP) Top View

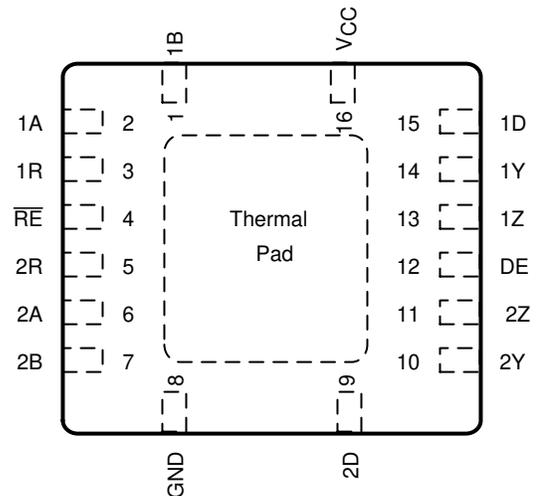


Figure 4-2. RGY Package 16 Pin (VQFN) Top View

Table 4-1. Pin Functions, SN65C1167E

| NAME | PIN | | | I/O | DESCRIPTION |
|-----------------|-----|-------|------|-----|---|
| | SO | TSSOP | VQFN | | |
| 1A | 2 | 2 | 2 | I | RS422 differential input (noninverting) to receiver 1 |
| 2A | 6 | 6 | 6 | I | RS422 differential input (noninverting) to receiver 2 |
| 1B | 1 | 1 | 1 | I | RS422 differential input (inverting) to receiver 1 |
| 2B | 7 | 7 | 7 | I | RS422 differential input (inverting) to receiver 2 |
| 1D | 15 | 15 | 15 | I | Logic data input to RS422 driver 1 |
| 2D | 9 | 9 | 9 | I | Logic data input to RS422 driver 2 |
| DE | 12 | 12 | 12 | I | Driver enable (active high) |
| GND | 8 | 8 | 8 | — | Device ground pin |
| 1R | 3 | 3 | 3 | O | Logic data output of RS422 receiver 1 |
| 2R | 5 | 5 | 5 | O | Logic data output of RS422 receiver 2 |
| RE | 4 | 4 | 4 | I | Receiver enable pin (active low) |
| V _{CC} | 16 | 16 | 16 | — | Power supply |
| 1Y | 14 | 14 | 14 | O | RS-422 differential (noninverting) driver output 1 |
| 2Y | 10 | 10 | 10 | O | RS-422 differential (noninverting) driver output 2 |
| 1Z | 13 | 13 | 13 | O | RS-422 differential (inverting) driver output 1 |
| 2Z | 11 | 11 | 11 | O | RS-422 differential (inverting) driver output 2 |

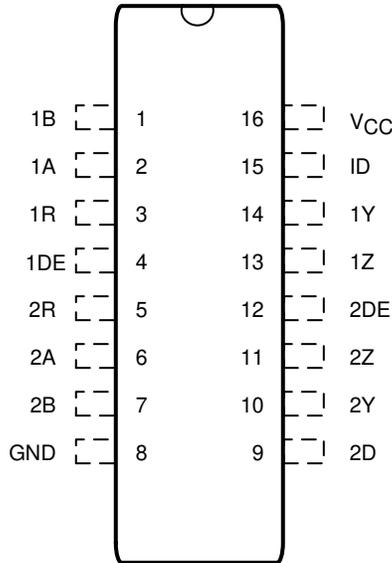


Figure 4-3. NS or PW Package 16 Pin (NS or TSSOP) Top View

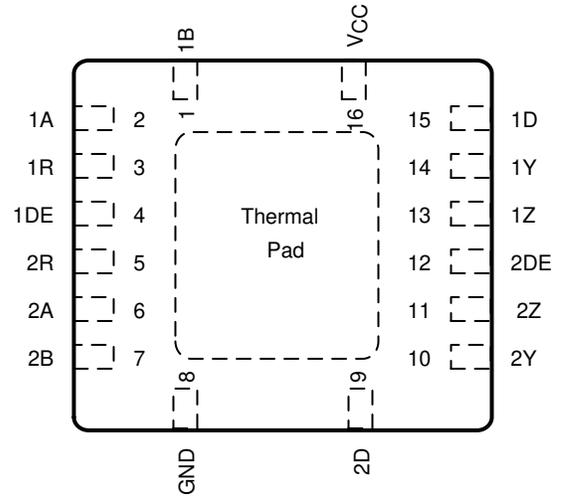


Figure 4-4. RGY Package 16 Pin (VQFN) Top View

Table 4-2. Pin Functions, SN65C1168E

| NAME | PIN | | | I/O | DESCRIPTION |
|-----------------|-----|-------|------|-----|---|
| | SO | TSSOP | VQFN | | |
| 1A | 2 | 2 | 2 | I | RS422 differential input (noninverting) to receiver 1 |
| 2A | 6 | 6 | 6 | I | RS422 differential input (noninverting) to receiver 2 |
| 1B | 1 | 1 | 1 | I | RS422 differential input (inverting) to receiver 1 |
| 2B | 7 | 7 | 7 | I | RS422 differential input (inverting) to receiver 2 |
| 1D | 15 | 15 | 15 | I | Logic data input to RS422 driver 1 |
| 2D | 9 | 9 | 9 | I | Logic data input to RS422 driver 2 |
| 1DE | 4 | 4 | 4 | I | Driver 1 enable (active high) |
| 2DE | 12 | 12 | 12 | I | Driver 2 enable (active high) |
| GND | 8 | 8 | 8 | — | Device ground |
| 1R | 3 | 3 | 3 | O | Logic data output of RS422 receiver 1 |
| 2R | 5 | 5 | 5 | O | Logic data output of RS422 receiver 2 |
| V _{CC} | 16 | 16 | 16 | — | Power supply |
| 1Y | 14 | 14 | 14 | O | RS-422 differential (noninverting) driver output 1 |
| 2Y | 10 | 10 | 10 | O | RS-422 differential (noninverting) driver output 2 |
| 1Z | 13 | 13 | 13 | O | RS-422 differential (noninverting) driver output 1 |
| 2Z | 11 | 11 | 11 | O | RS-422 differential (noninverting) driver output 2 |

5 Specifications

5.1 Absolute Maximum Ratings

over recommended operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------|---|----------------------------|------|-----------------------|---|
| V _{CC} | Supply voltage ⁽²⁾ | -0.5 | 7 | V | |
| V _I | Input voltage | Driver, DE, RE | -0.5 | 7 | V |
| | | A or B, Receiver | -14 | 14 | |
| V _{ID} | Differential input voltage ⁽³⁾ | -14 | 14 | V | |
| V _O | Output voltage | Driver | -0.5 | 7 | V |
| | | Receiver | -0.5 | V _{CC} + 0.5 | |
| I _{IK} | Input clamp current | Driver, V _I < 0 | -20 | mA | |
| I _{OK} | Output clamp current | Driver, V _O < 0 | -20 | mA | |
| | | Receiver | ±20 | | |
| I _O | Output current | Driver | ±150 | mA | |
| | | Receiver | ±25 | | |
| I _{CC} | Supply current | | 200 | mA | |
| | | GND current | -200 | | |
| T _J | Operating virtual junction temperature | | 150 | °C | |
| T _A | Operating free-air temperature | -40 | 85 | °C | |
| T _{stg} | Storage temperature | -65 | 150 | °C | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential input voltage are with respect to the network GND.
- (3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.

5.2 Driver Output and Receiver Input ESD Ratings

| | | VALUE | UNIT | |
|--------------------|-------------------------|--|--------|---|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±15000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 | |
| | | IEC 61000-4-2, air-gap discharge | ±8000 | |
| | | IEC 61000-4-2, contact discharge | ±8000 | |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|-----------------|--|----------|-----|-----------------|------|
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V _{IC} | Common-mode input voltage ⁽¹⁾ | | | ±7 | V |
| V _{ID} | Differential input voltage | | | ±7 | V |
| V _I | Input voltage | 0 | | 5.5 | V |
| V _O | Output voltage | 0 | | V _{CC} | V |
| V _{IH} | High-level input voltage | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{OH} | High-level output current | Receiver | | -6 | mA |
| | | Driver | | -20 | |
| I _{OL} | Low-level output current | Receiver | | 6 | mA |
| | | Driver | | 20 | |
| T _A | Operating free-air temperature | -40 | | 85 | °C |

(1) Refer to TIA/EIA-422-B for exact conditions.

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN65C116xE | | | UNIT | |
|-------------------------------|--|------------|------------|------|------|
| | SO (NS) | PW (TSSOP) | RGY (VQFN) | | |
| | 16 PINS | 16 PINS | 16 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 88.5 | 107.5 | 48.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 46.2 | 38.4 | 46.4 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 50.7 | 53.7 | 24.6 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 13.5 | 3.2 | 2.3 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 50.3 | 53.1 | 24.5 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | n/a | 8.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Driver Section Electrical Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---------------------|--|--|---|-----|--------------------|------|------|
| V _{IK} | Input clamp voltage | I _I = -18mA | | | | -1.5 | V |
| V _{OH} | High-level output voltage | V _{IH} = 2V, | V _{IL} = 0.8V, I _{OH} = -20mA | 2.4 | 3.5 | | V |
| V _{OL} | Low-level output voltage | V _{IH} = 2V, | V _{IL} = 0.8V, I _{OL} = 20mA | | 0.2 | 0.4 | V |
| V _{OD1} | Differential output voltage 1 | I _O = 0mA | | 2 | | 6 | V |
| V _{OD2} | Differential output voltage 2 | R _L = 100Ω, | See Figure 6-1 ⁽²⁾ | 2 | 3.7 | | V |
| Δ V _{OD} | Change in magnitude of differential output voltage | R _L = 100Ω, | See Figure 6-1 ⁽²⁾ | | | ±0.4 | V |
| V _{OC} | Common-mode output voltage | R _L = 100Ω, | See Figure 6-1 ⁽²⁾ | | | ±3 | V |
| Δ V _{OCl} | Change in magnitude of common-mode output voltage | R _L = 100Ω, | See Figure 6-1 ⁽²⁾ | | | ±0.4 | V |
| I _{O(OFF)} | Output current with power off | V _{CC} = 0V | V _O = 6V | | | 100 | μA |
| | | | V _O = -0.25V | | | 100 | |
| I _{OZ} | High-impedance-state output current | V _O = 2.5V | | | | 20 | μA |
| | | V _O = 5V | | | | -20 | |
| I _{IH} | High-level input current | V _I = V _{CC} or V _{IH} | | | | 1 | μA |
| I _{IL} | Low-level input current | V _I = GND or V _{IL} | | | | -1 | μA |
| I _{OS} | Short-circuit output current | V _O = V _{CC} or GND ⁽³⁾ | | -30 | | -150 | mA |
| I _{CC} | Supply current (total package) | No load, Enabled | V _I = V _{CC} or GND | | 4 | 6 | mA |
| | | | V _I = 2.4 or 0.5V ⁽⁴⁾ | | 5 | 9 | |
| C _i | Input capacitance | | | | 6 | | pF |

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) Refer to TIA/EIA-422-B for exact conditions.

(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

(4) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

5.6 Receiver Section Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|--|---|---|-----------------------|--------------------|------|------|
| V _{IT+} | Positive-going input threshold voltage, differential input | | | | | 0.2 | V |
| V _{IT-} | Negative-going input threshold voltage, differential input | | | -0.2 ⁽²⁾ | | | V |
| V _{hys} | Input hysteresis (V _{IT+} - V _{IT-}) | | | | 60 | | mV |
| V _{IK} | Input clamp voltage, RE | SN65C1167E | I _I = -18mA | | | -1.5 | V |
| V _{OH} | High-level output voltage | V _{ID} = 200mV, I _{OH} = -6mA | | 3.8 | 4.2 | | V |
| V _{OL} | Low-level output voltage | V _{ID} = -200mV, I _{OL} = 6mA | | | 0.1 | 0.3 | V |
| I _{OZ} | High-impedance state output current | SN65C1167E | V _O = V _{CC} or GND | | ±0.5 | ±5 | μA |
| I _I | Line input current | | Other input at 0V | V _I = 10V | | 1.5 | mA |
| | | | | V _I = -10V | | -2.5 | |
| I _I | Enable input current, RE | SN65C1167E | V _I = V _{CC} or GND | | | ±1 | μA |
| r _i | Input resistance | V _{IC} = -7V to 7V, Other input at 0V | | 4 | 17 | | kΩ |
| I _{CC} | Supply current (total package) | No load, Enabled | V _I = V _{CC} or GND | | 4 | 6 | mA |
| | | | V _{IH} = 2.4V or 0.5V ⁽³⁾ | | 5 | 9 | |

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) Refer to TIA/EIA-422-B for exact conditions.

5.7 Driver Section Switching Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------|---|--|-----------------------------|-----|--------------------|-----|------|
| t _{PHL} | Propagation delay time, high- to low-level output | R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See Figure 6-2 | R3 = 500Ω, S1 is open, | | 8 | 16 | ns |
| t _{PLH} | Propagation delay time, low- to high-level output | | | | 8 | 16 | ns |
| t _{sk(p)} | Pulse skew | | | | 1.5 | 4 | ns |
| t _r | Rise time | R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See Figure 6-3 | R3 = 500Ω, S1 is open, | | 5 | 8 | ns |
| t _f | Fall time | | | | 5 | 8 | ns |
| t _{PZH} | Output-enable time to high level | R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See Figure 6-4 | R3 = 500Ω, S1 is closed, | | 10 | 19 | ns |
| t _{PZL} | Output-enable time to low level | | | | 10 | 19 | ns |
| t _{PHZ} | Output-disable time from high level | R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See Figure 6-4 | R3 = 500Ω, S1 is closed, | | 7 | 16 | ns |
| t _{PLZ} | Output-disable time from low level | | | | 7 | 16 | ns |
| f _{SW} | Maximum switching frequency | R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See Figure 6-3 | R3 = 500Ω, S1 is open, | 20 | | | MHz |

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

5.8 Receiver Section Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽²⁾

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|------------------|---|----------------------|--|----------------|--------------------|-----|------|----|
| t _{PLH} | Propagation delay time, low- to high-level output | See Figure 6-5 | | 9 | 15 | 27 | ns | |
| t _{PHL} | Propagation delay time, high- to low-level output | See Figure 6-5 | | 9 | 15 | 27 | ns | |
| t _{TLH} | Transition time, low- to high-level output | V _{IC} = V, | See Figure 6-5 | | 4 | 9 | ns | |
| t _{THL} | Transition time, high- to low-level output | | | | 4 | 9 | ns | |
| t _{PZH} | Output-enable time to high level | SN65C1167E | R _L = 1kΩ, C _L = 50pF | See Figure 6-6 | | 7 | 22 | ns |
| t _{PZL} | Output-enable time to low level | | | | | 7 | 22 | ns |
| t _{PHZ} | Output-disable time from high level | | | | | 12 | 22 | ns |
| t _{PLZ} | Output-disable time from low level | | | | | 12 | 22 | ns |

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) Measured per input while the other inputs are at V_{CC} or GND

6 Parameter Measurement Information

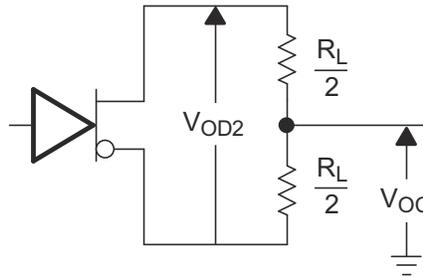
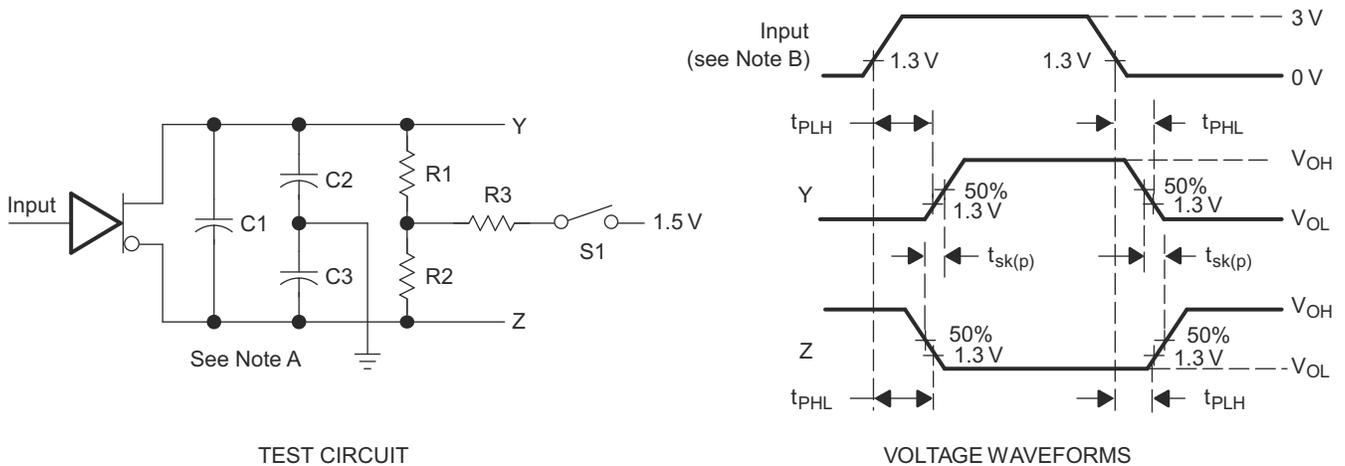
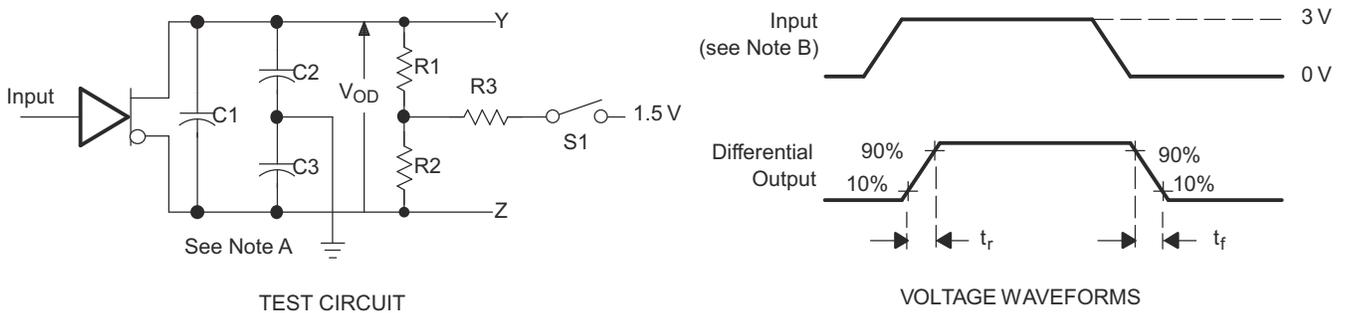


Figure 6-1. Driver Test Circuit, V_{OD} and V_{OC}



- A. C1, C2, and C3 include probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

Figure 6-2. Driver Test Circuit and Voltage Waveforms

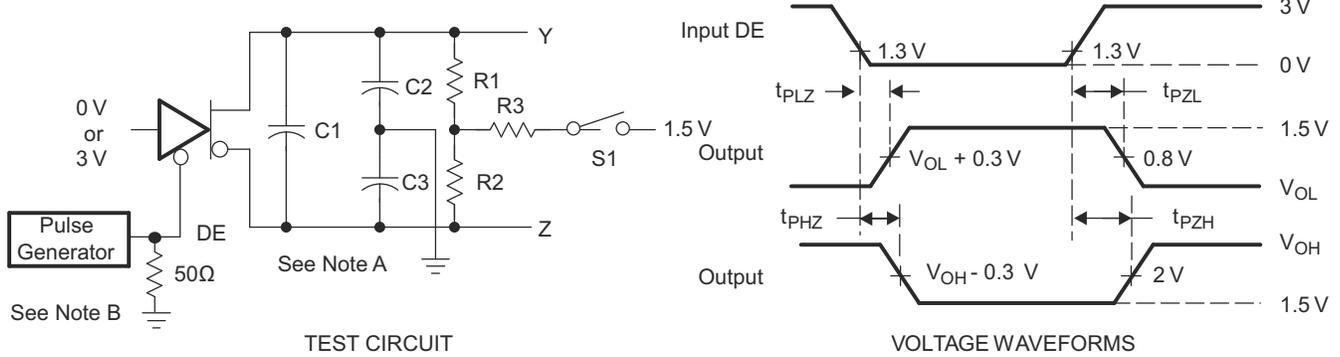


- A. C1, C2, and C3 include probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

Figure 6-3. Driver Test Circuit and Voltage Waveforms

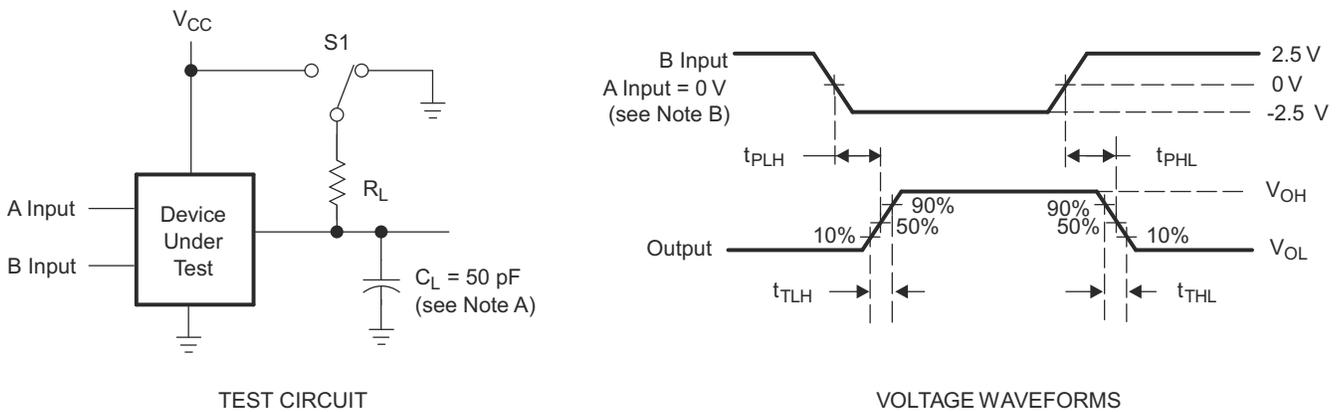
SN65C1167E, SN65C1168E

SLLS740C – MARCH 2007 – REVISED FEBRUARY 2024



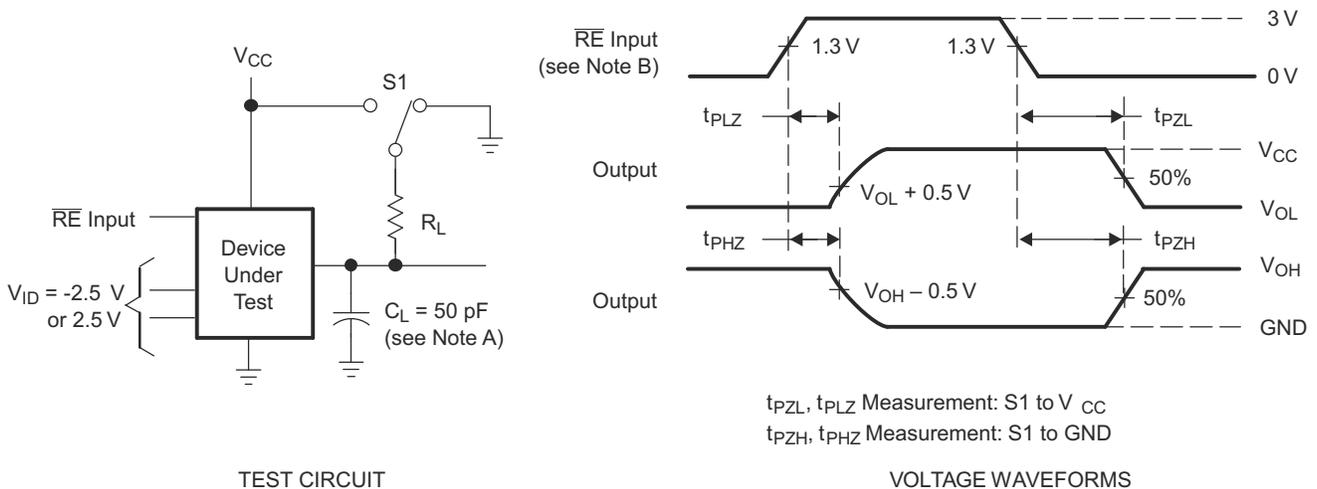
- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6\text{ns}$.

Figure 6-4. Driver Test Circuit and Voltage Waveforms



- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6\text{ns}$.

Figure 6-5. Receiver Test Circuit and Voltage Waveforms



- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6\text{ns}$.

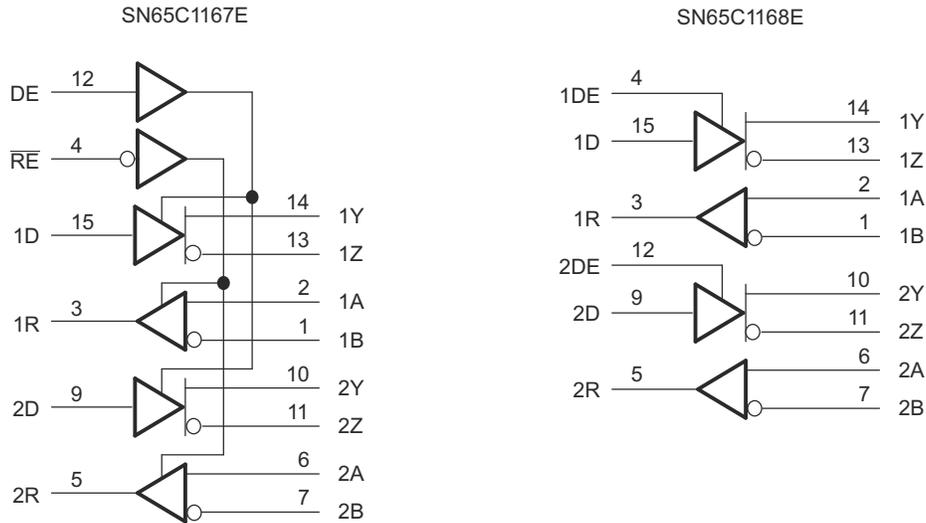
Figure 6-6. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN65C1167E and SN65C1168E consist of dual drivers and dual receivers powered from a single 5V supply. These devices meet the requirements of TIA/EIA-422-B and ITU recommendation V.11.

7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Active High Driver Output Enables

Both drivers of SN65C1167E can be configured with the single DE logic input. Both drivers are set at high-impedance when disabled.

SN65C1168E drivers can be configured individually by 1DE and 2DE logic inputs. Both drivers are set at high-impedance when disabled.

7.3.2 Active Low Receiver Enables

Both SN65C1167E receivers can be configured with the single \overline{RE} logic input. Receiver logic outputs are set at high-impedance when disabled.

7.4 Device Functional Modes

Table 7-1 and Table 7-2 list the functional modes of SN65C1167E and SN65C1168E.

Table 7-1. Each Driver

| INPUT D | ENABLE DE | OUTPUTS | |
|------------|--------------|---------|---|
| | | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

Table 7-2. SN65C1167E, Each Receiver⁽¹⁾

| DIFFERENTIAL INPUTS A–B | ENABLE \overline{RE} | OUTPUT R |
|---|---------------------------|-------------|
| $V_{ID} \geq 0.2\text{ V}$ | L | H |
| $-0.2\text{ V} < V_{ID} < 0.2\text{ V}$ | L | ? |
| $V_{ID} \leq -0.2\text{ V}$ | L | L |
| X | H | Z |
| Open | L | H |

(1) H = High level, L = Low level, ? = Indeterminate, X = Irrelevant, Z = High impedance (off)

Table 7-3. SN65C1168E, Each Receiver⁽¹⁾

| DIFFERENTIAL INPUTS A–B | OUTPUT R |
|---|-------------|
| $V_{ID} \geq 0.2\text{ V}$ | H |
| $-0.2\text{ V} < V_{ID} < 0.2\text{ V}$ | ? |
| $V_{ID} \leq -0.2\text{ V}$ | L |
| Open | H |

(1) H = High level, L = Low level, ? = Indeterminate

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Figure 8-1 shows a typical RS-422 application. One transmitter is able to broadcast to multiple receiving nodes connected together over a shared differential bus. Twisted-pair cabling with a controlled differential impedance is used, and a termination resistance is placed at the farthest receive end of the cable in order to match the transmission line impedance and minimize signal reflections.

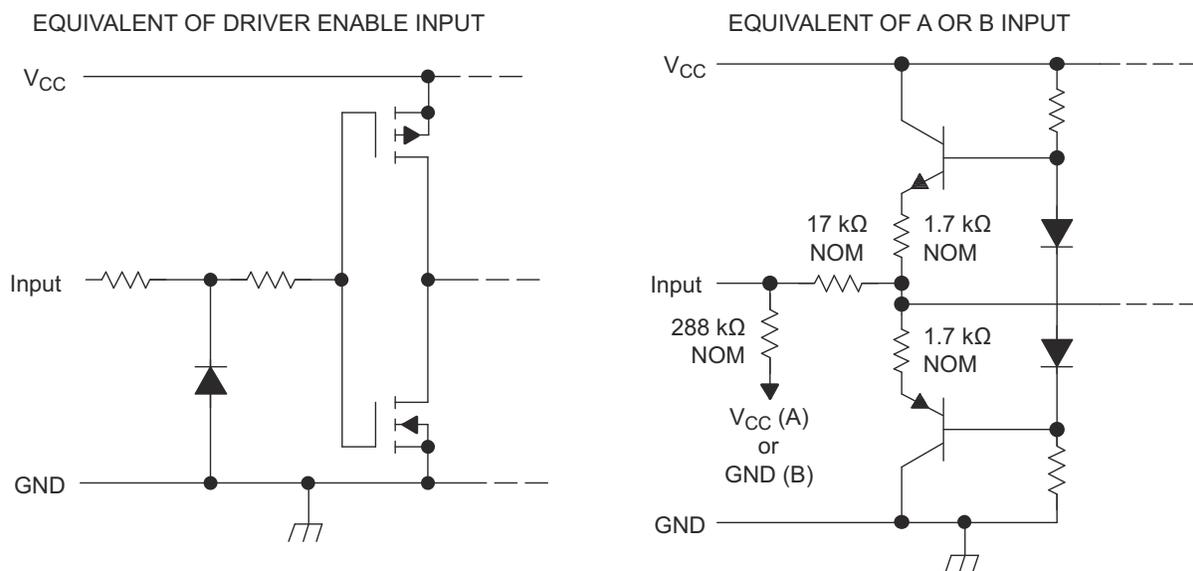


Figure 8-1. Schematic of Inputs

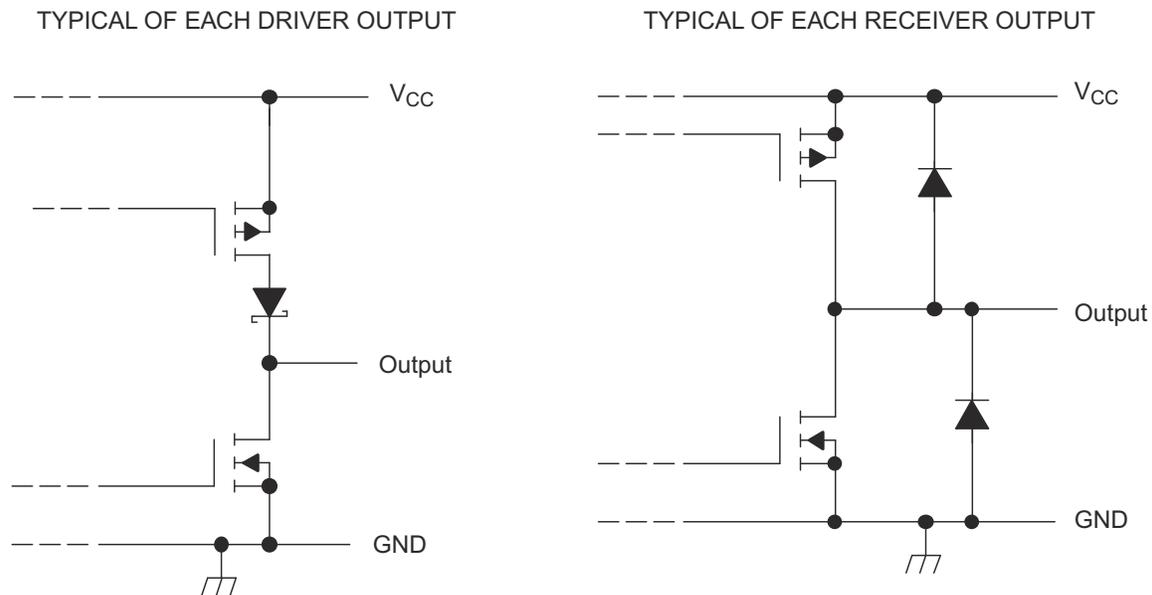


Figure 8-2. Schematic of Outputs

8.2 Typical Application

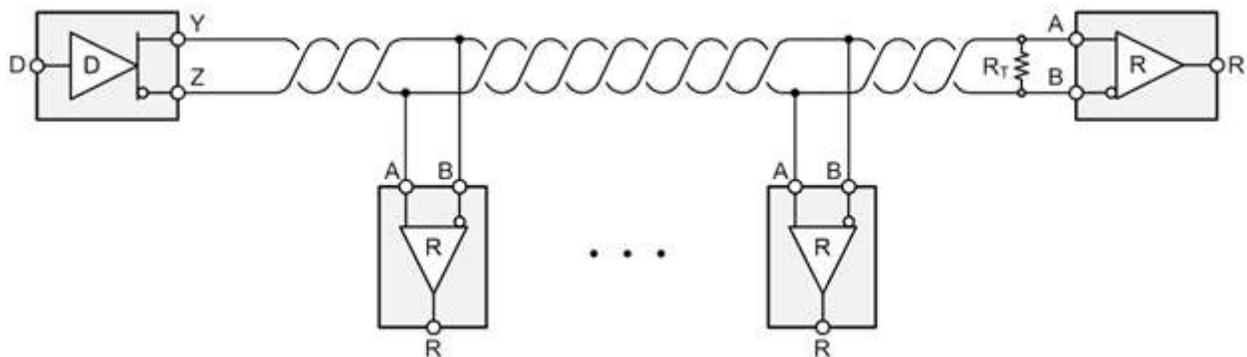


Figure 8-3. Typical RS-422 Application

8.2.1 Design Requirements

A typical RS-422 implementation using SN65C116xE requires the following:

- 5V power source.
- Connector that ensures the correct polarity for port pins.
- Cabling that supports the desired operating rate and transmission distance.

8.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure ± 200 mV on the A-B port when the driver circuit is disabled.

8.3 Power Supply Recommendations

Use a 5V power supply for V_{CC} place $0.1\mu\text{F}$ bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high impedance power supplies.

9 Device and Documentation Support

9.1 Device Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (May 2017) to Revision C (February 2024) | Page |
|--|-------------|
| • Changed the Device Information table to the Package Information table..... | 1 |
| • Deleted the thermal packaging information from the <i>Absolute Maximum Ratings</i> | 5 |
| • Changed the <i>Thermal Information</i> table..... | 6 |

| Changes from Revision A (April 2007) to Revision B (May 2017) | Page |
|--|-------------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes, Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1 |
| • Changed the Rise Time Max value From: 10 ns To: 8 ns in the <i>Driver Section Switching Characteristics</i> table. | 8 |
| • Changed the Fall Time Max value From: 10 ns To: 8 ns in the <i>Driver Section Switching Characteristics</i> table. | 8 |
| • Added Maximum switching frequency to the <i>Driver Section Switching Characteristics</i> table..... | 8 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN65C1167ENS | Obsolete | Production | SOP (NS) 16 | - | - | Call TI | Call TI | -40 to 85 | 65C1167E |
| SN65C1167ENSR | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C1167E |
| SN65C1167ENSR.A | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C1167E |
| SN65C1167ENSRG4 | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C1167E |
| SN65C1167ENSRG4.A | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C1167E |
| SN65C1167EPW | Obsolete | Production | TSSOP (PW) 16 | - | - | Call TI | Call TI | -40 to 85 | CB1167E |
| SN65C1167EPWR | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1167E |
| SN65C1167EPWR.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1167E |
| SN65C1167EPWRG4 | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1167E |
| SN65C1167EPWRG4.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1167E |
| SN65C1167ERGYR | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1167 |
| SN65C1167ERGYR.A | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1167 |
| SN65C1167ERGYRG4 | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1167 |
| SN65C1167ERGYRG4.A | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1167 |
| SN65C1168ENS | Obsolete | Production | SOP (NS) 16 | - | - | Call TI | Call TI | -40 to 85 | 65C1168E |
| SN65C1168ENSR | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C1168E |
| SN65C1168ENSR.A | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C1168E |
| SN65C1168EPW | Obsolete | Production | TSSOP (PW) 16 | - | - | Call TI | Call TI | -40 to 85 | CB1168E |
| SN65C1168EPWR | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1168E |
| SN65C1168EPWR.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1168E |
| SN65C1168EPWRG4 | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1168E |
| SN65C1168ERGYR | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CB1168 |
| SN65C1168ERGYR.A | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CB1168 |
| SN65C1168ERGYRG4 | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1168 |
| SN65C1168ERGYRG4.A | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB1168 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

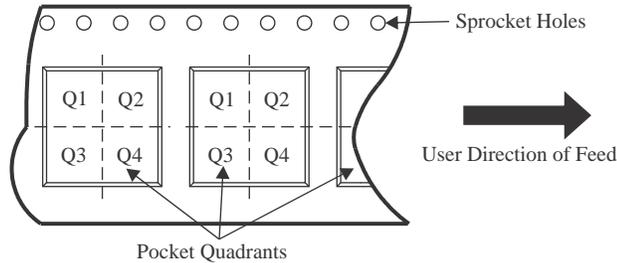
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65C1167ENSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C1167ENSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C1167ENSRG4 | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C1167ENSRG4 | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C1167EPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN65C1167EPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN65C1167EPWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN65C1167EPWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN65C1167ERGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| SN65C1167ERGYRG4 | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| SN65C1168ENSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C1168ENSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C1168EPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN65C1168EPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN65C1168ERGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| SN65C1168ERGYRG4 | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65C1167ENSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN65C1167ENSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN65C1167ENSRG4 | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN65C1167ENSRG4 | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN65C1167EPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN65C1167EPWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN65C1167EPWRG4 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN65C1167EPWRG4 | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN65C1167ERGYR | VQFN | RGY | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| SN65C1167ERGYRG4 | VQFN | RGY | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| SN65C1168ENSR | SOP | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN65C1168ENSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN65C1168EPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN65C1168EPWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN65C1168ERGYR | VQFN | RGY | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| SN65C1168ERGYRG4 | VQFN | RGY | 16 | 3000 | 360.0 | 360.0 | 36.0 |

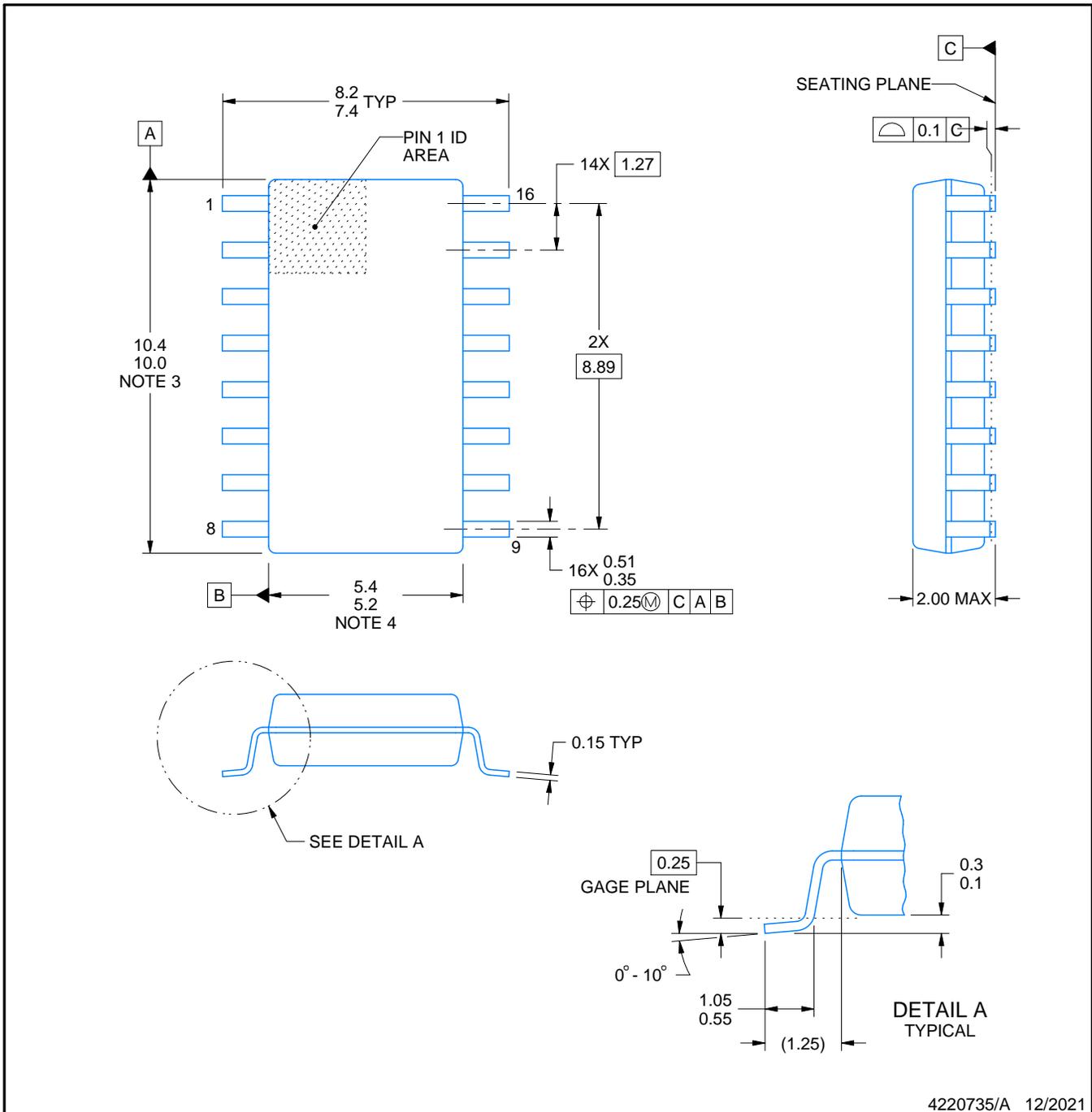


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

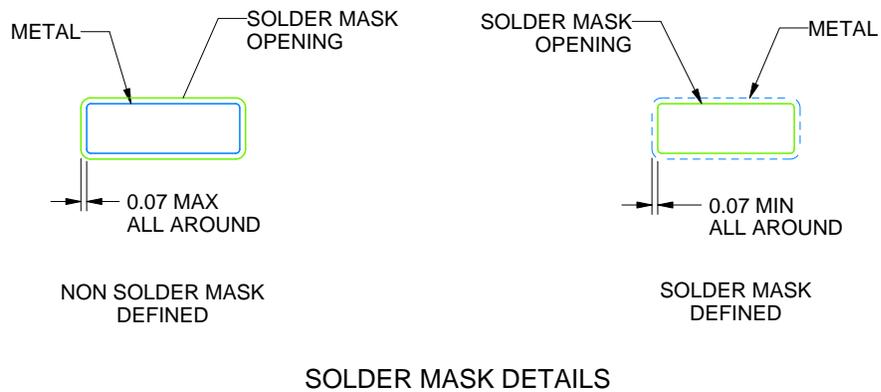
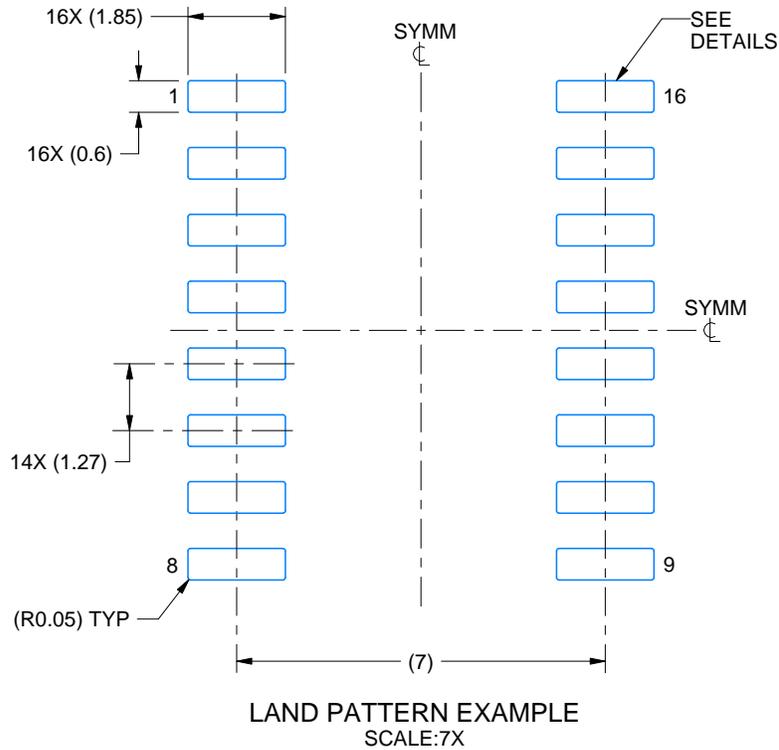
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

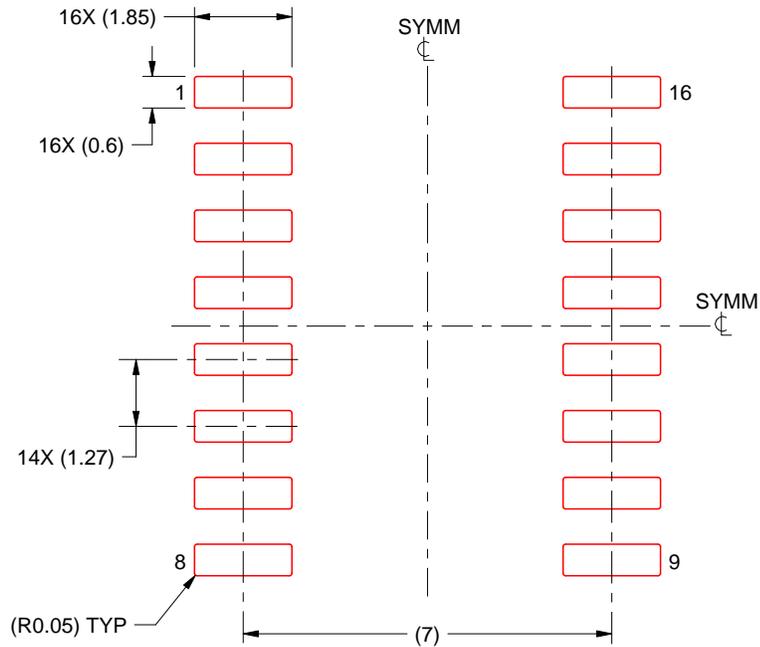
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP

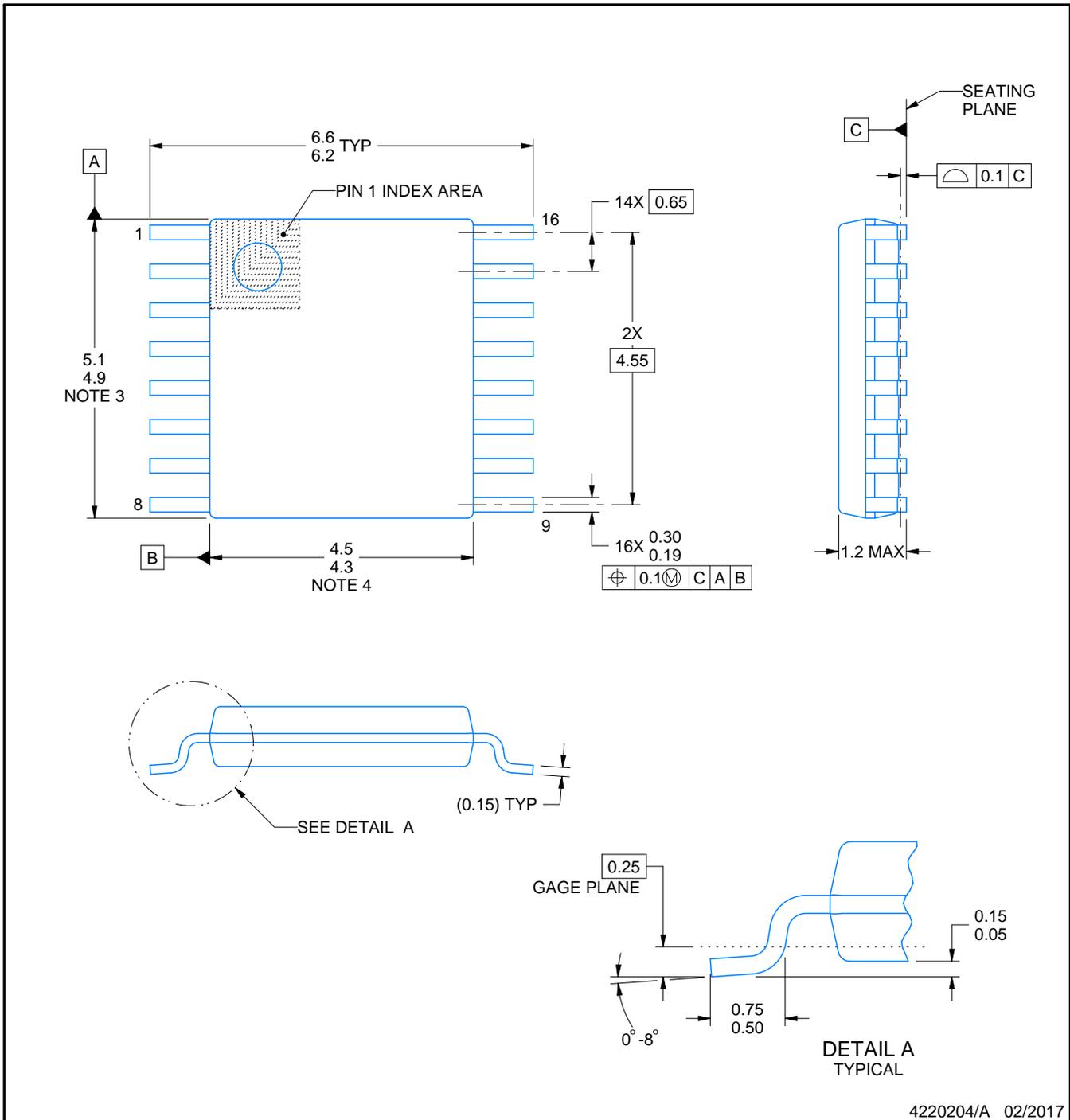


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220204/A 02/2017

NOTES:

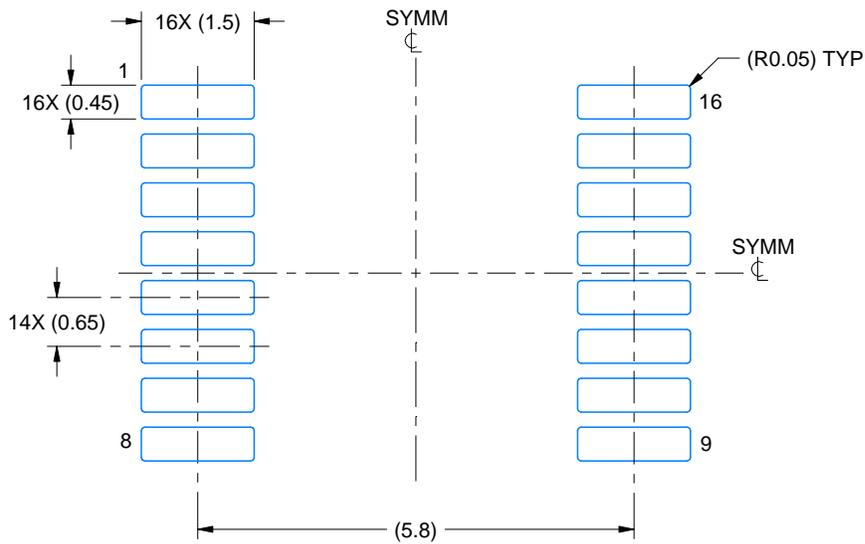
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

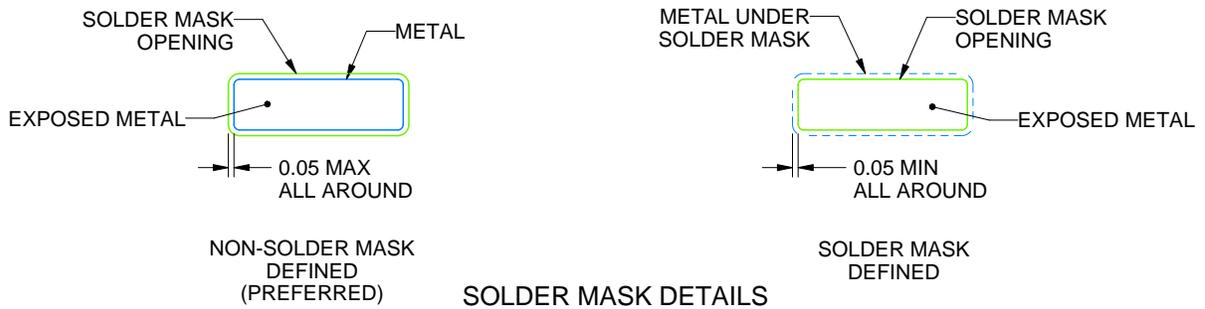
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

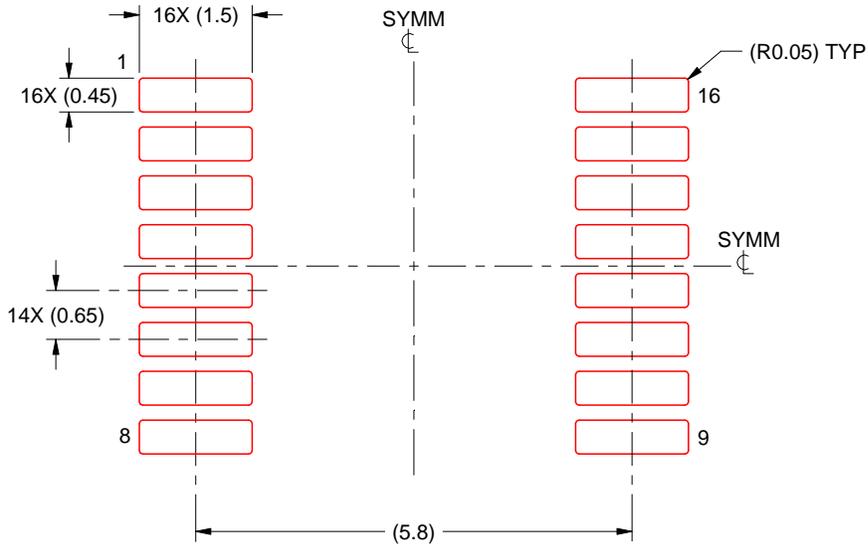
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

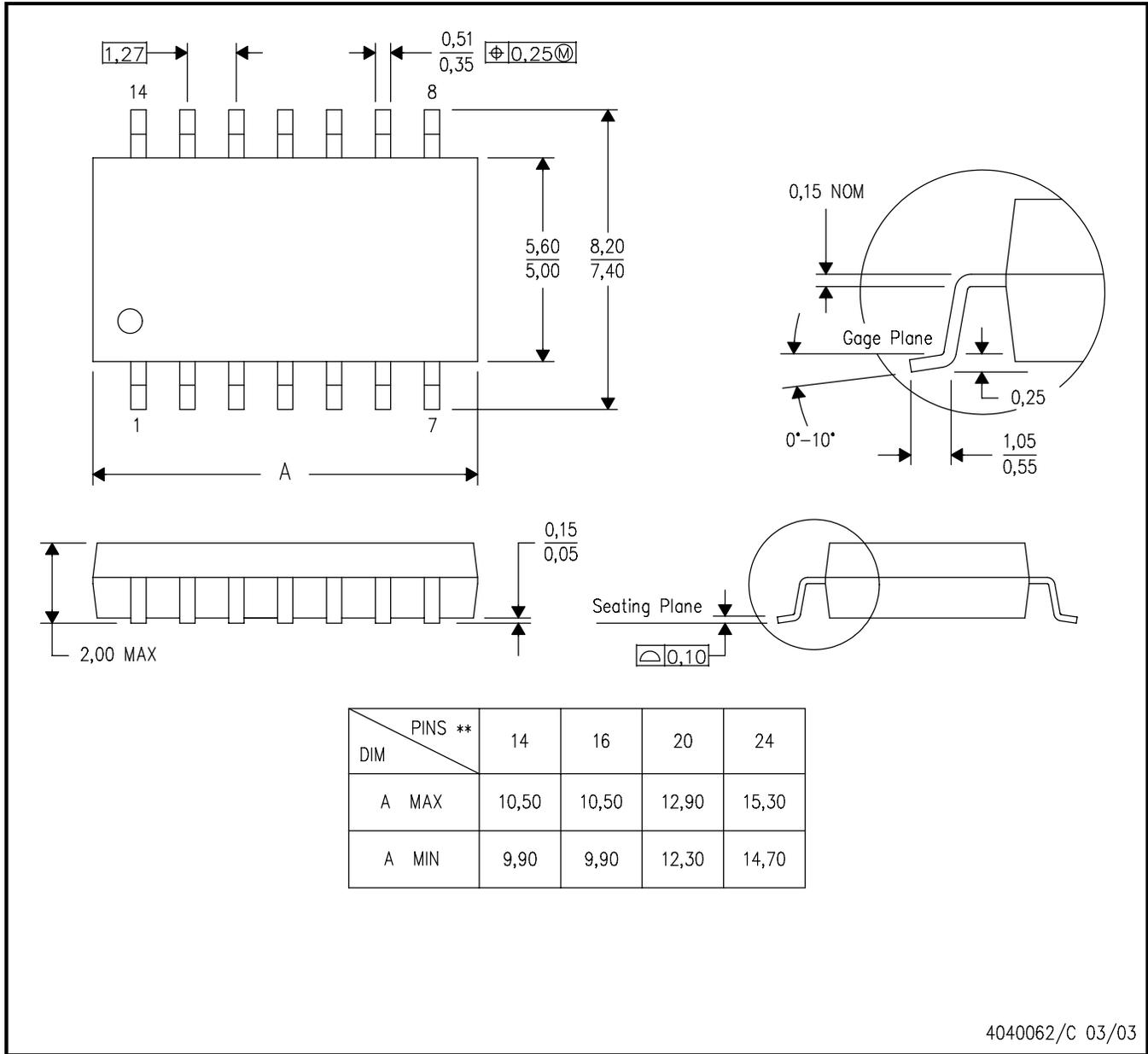
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

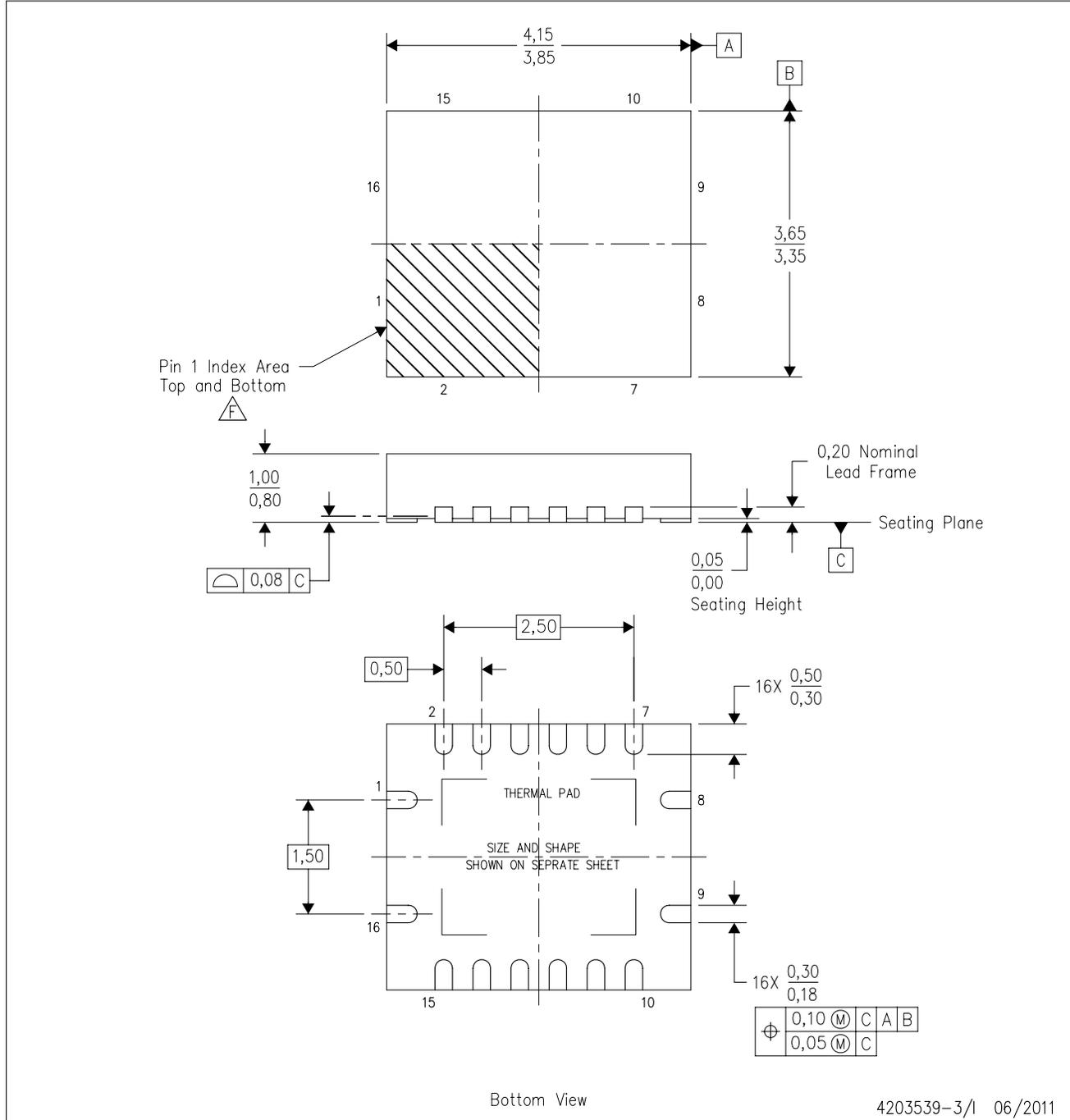
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

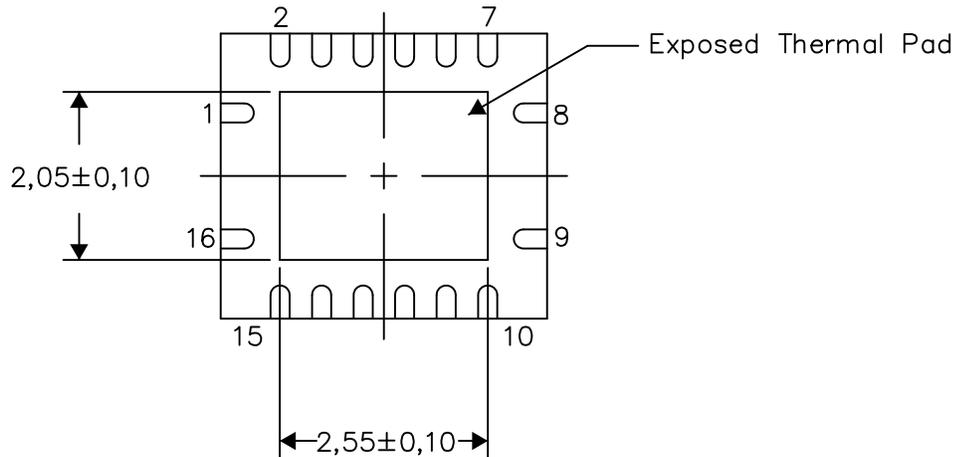
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

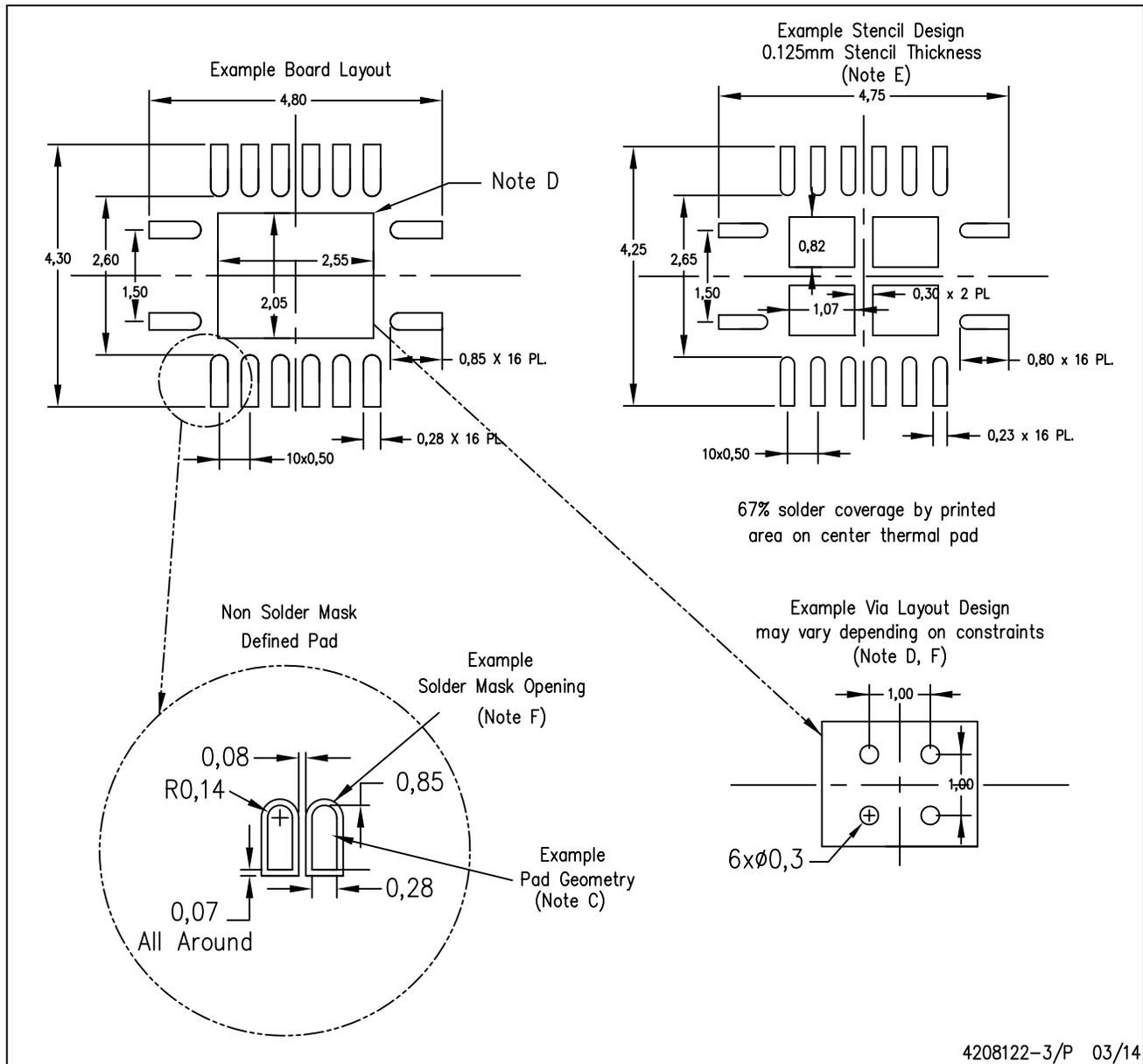
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated