2-SERIES, 3-SERIES, AND 4-SERIES CELL LITHIUM-ION OR LITHIUM-POLYMER BATTERY PROTECTION AFE

Check for Samples: bq29330

FEATURES

- **2-Series, 3-Series, or 4-Series Cell Protection Control**
- **Can Directly Interface with the bq803x-Based Gas Gauge Family**
- **Watchdog and POR for the Host**
- **Provides Individual Cell Voltages and Battery Voltage to Battery Management Host**
- **Capable of Operation With 5-mΩ Sense Resistor Integrated Cell Balancing Drive**
- **I²C Compatible User Interface Allows Access to Battery Information**
- **Programmable Threshold and Delay for Overload Short Circuit in Discharge and Short Circuit in Charge**
- **NMOS FET Drive for Charge and Discharge FETs**
- **Host Control can Initiate Sleep and Ship Power Modes**
- **Integrated 2.5-V, 16-mA LDO**
- **Integrated 3.3-V, 25-mA LDO**
- **Supply Voltage Range from 4.5 V to 28 V**
- **Low Supply Current of 100 µA Typical**

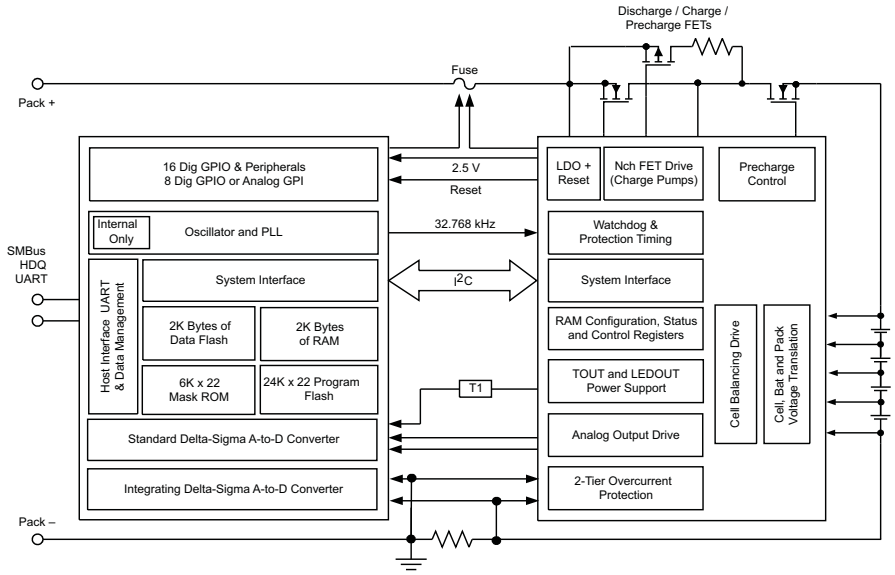
APPLICATIONS

- **Notebook Computers**
- **Medical and Test Equipment**
- **Instrumentation and Measurement Systems**

DESCRIPTION

The bq29330 is a 2-series, 3-series, and 4-series cell lithium-ion battery pack full-protection analog front end (AFE) IC that incorporates a 2.5-V, 16-mA and 3.3-V, 25-mA low dropout regulator (LDO). The bq29330 also integrates an I²C-compatible interface to extract battery parameters such as battery voltage, individual cell voltages, and control output status. Other parameters such as current protection thresholds and delays can also be programmed into the bq29330 to increase the flexibility of the battery management system.

SYSTEM DIAGRAM



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The bq29330 provides safety protection for overload, short circuit in charge, and short circuit in discharge conditions and can also provide cell overvoltage, battery overvoltage and battery undervoltage protection with the battery management host. In overload, short circuit in charge and short circuit in discharge conditions, the bq29330 turns off the FET drive autonomously, depending on the internal configuration setting. The communications interface allows the host to observe and control the status of the bq29330, enable cell balancing, enter different power modes, set current protection levels, and set the blanking delay times.

Cell balancing of each cell can be performed via a cell bypass path integrated into the bq29330, which can be enabled via the internal control register accessible via the I^2C-compatible interface. The maximum bypass current is set via an external series resistor and internal FET on resistance (typ. 400 Ω).

ORDERING INFORMATION(1)

T_A	PACKAGE	
	TSSOP(DBT)(2)	QFN(RSM)(2)
–40°C to 110°C	bq29330DBT	bq29330RSM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The bq29330 can be ordered in tape and reel by adding the suffix R to the orderable part number, i.e., bq29330DBTR.

THERMAL INFORMATION

THERMAL METRIC(1)		bq29330		UNITS
		TSSOP (DBT)	QFN (RSM)	
		30 PINS	32 PINS	
$\theta_{JA, High K}$	Junction-to-ambient thermal resistance	81.4	37.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	16.2	30.6	
θ_{JB}	Junction-to-board thermal resistance	34.1	7.7	
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	
ψ_{JB}	Junction-to-board characterization parameter	33.6	7.5	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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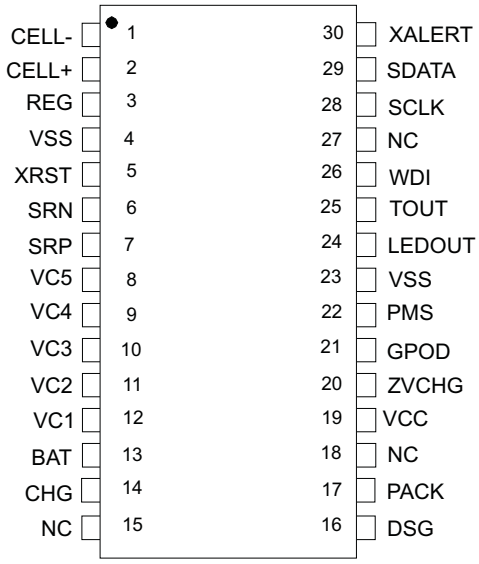
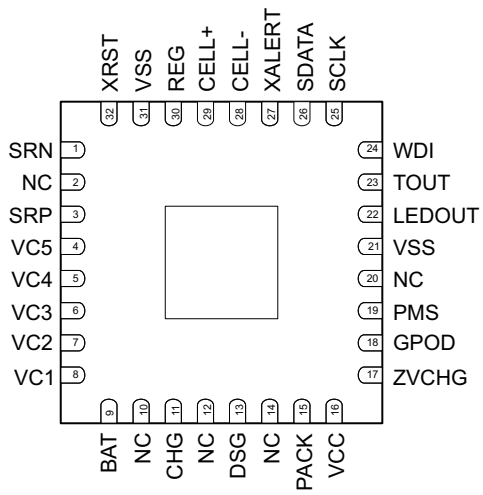
PACKAGE OPTION PIN DIAGRAMS

TSSOP PACKAGE
(TOP VIEW)



RSM PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN			DESCRIPTION
NAME	DBT NO.	RSM NO.	
CELL–	1	28	Output of scaled value of the measured cell voltage.
CELL+	2	29	Output of scaled value of the measured cell voltage.
REG	3	30	Integrated 2.5-V regulator output
VSS	4, 23	31,21	Power supply ground
XRST	5	32	Active-low output
SRN	6	1	Current sense terminal
SRP	7	3	Current sense positive terminal when charging relative to SRN; current sense negative terminal when discharging relative to SRN
VC5	8	4	Sense voltage input terminal for most negative cell; balance current input for least positive cell.
VC4	9	5	Sense voltage input terminal for least positive cell, balance current input for least positive cell, and return balance current for third most positive cell.
VC3	10	6	Sense voltage input terminal for third most positive cell, balance current input for third most positive cell, and return balance current for second most positive cell.
VC2	11	7	Sense voltage input terminal for second most positive cell, balance current input for second most positive cell, and return balance current for most positive cell.
VC1	12	8	Sense voltage input terminal for most positive cell, balance current input for most positive cell, and battery stack measurement input
BAT	13	9	Device power supply input
CHG	14	11	Charge pump, charge N-CH FET gate drive
DSG	16	13	Charge pump output, discharge N-CH FET gate drive
PACK	17	15	PACK positive terminal and alternative power source
VCC	19	16	Power supply voltage
ZVCHG	20	17	Connect the precharge P-CH FET drive here
GPOD	21	18	NCH FET open-drain output
PMS	22	19	Determines CHG output state on POR
LEDOUT	24	22	3.3-V output for LED display power supply
TOUT	25	23	Provides thermistor bias current

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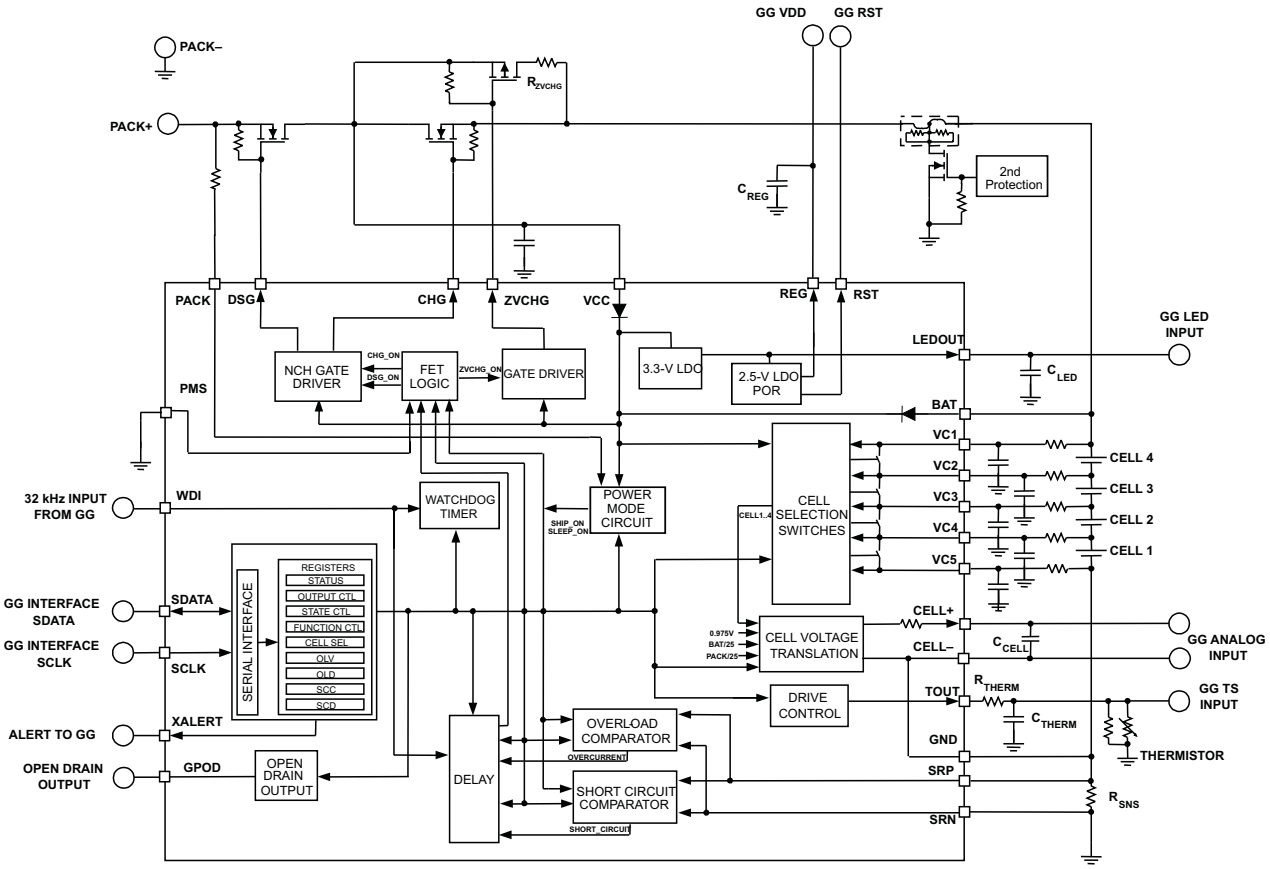
PIN FUNCTIONS (continued)

PIN			DESCRIPTION
NAME	DBT NO.	RSM NO.	
WDI	26	24	Digital input that provides the timing clock for the OC and SC delays and also acts as the watchdog clock.
SCLK	28	25	Open-drain serial interface clock with internal 10-kΩ pullup to V_{REG}
SDATA	29	26	Open-drain bidirectional serial interface data with internal 10-kΩ pullup to V_{REG}
XALERT	30	27	Open-drain output used to indicate status register changes. With internal 100-kΩ pullup to V_{REG}
NC	15,18,27	2, 10, 12, 14, 20	Not electrically connected to the IC

FUNCTIONAL BLOCK DIAGRAM



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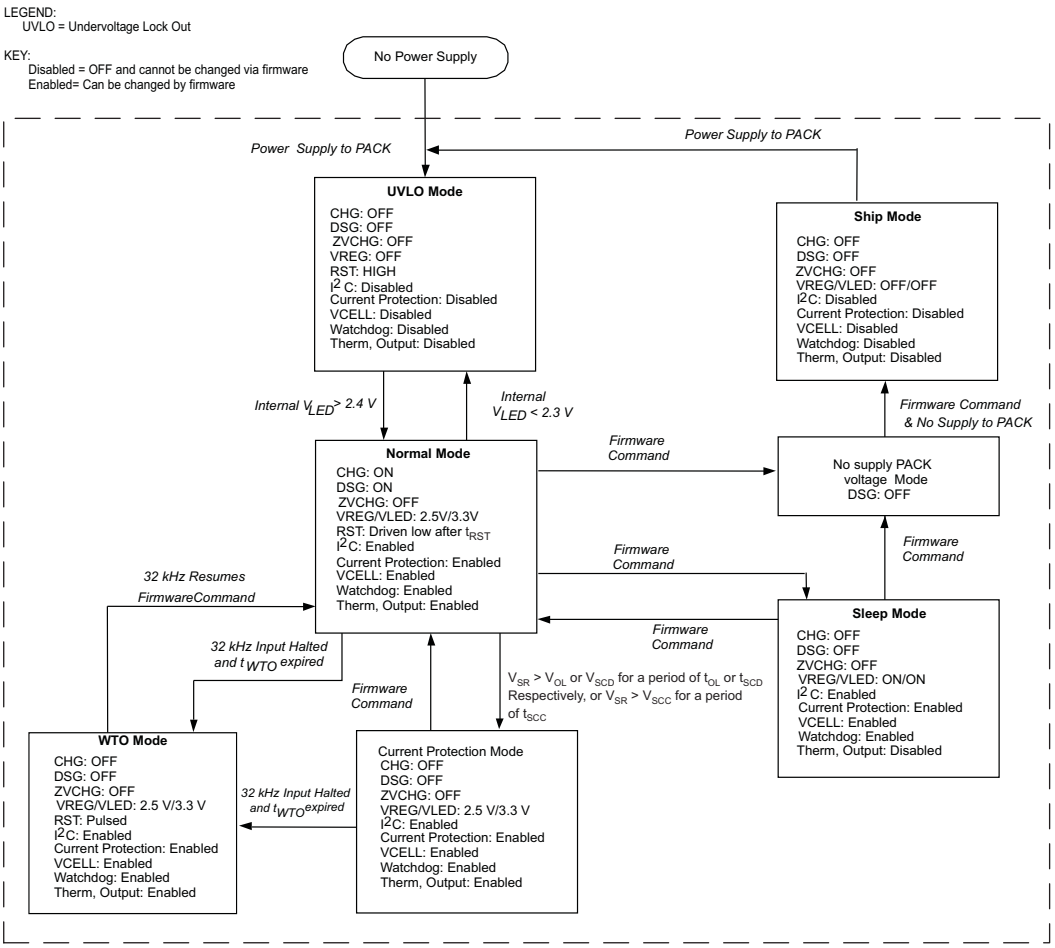
SAFETY STATE DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		bq29330	UNIT
Supply voltage range	(VCC, BAT)	–0.3 to 34	V
Input voltage range	(VC1, VC2, VC3, VC4, PACK, PMS)	–0.3 to 34	
	(VC5)	–0.3 to 1.0	
	(SRP, SRN)	–1.0 to 1.0	
	(VC1 to VC2, VC2 to VC3, VC3 to VC4, VC4 to VC5)	–0.3 to 8.5	
	(WDI, SCLK, SDATA)	–0.3 to 8.5	
Output voltage range	(DSG,CHG)	–0.3 to BAT	
	(ZVCHG)	–0.3 to 34	
	(GPOD)	–0.3 to 34	
	(TOUT, SDATA, CELL, XALERT, XRST, LEDOUT)	–0.3 to 7	
	(CELL+)	–0.3 to 7	
Current for cell balancing		10	mA
Storage temperature range, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground of this device except VCn–VC(n+1), where n=1, 2, 3, 4 cell voltage.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
	Supply voltage (VCC, BAT)		4.5		25	V
$V_{I(STARTUP)}$	Start up voltage (VCC, BAT)		5.5			V
V_I	Input voltage range	VC1, VC2, VC3, VC4	0		VDD	V
		VC5	0		0.5	
		SRP, SRN	–0.5		0.5	
		VCn – VC(n+1), (n=1, 2, 3, 4)	0		5.0	
		PACK, PMS			25	
V_{IH}	Logic level input voltage	SCLK, SDATA, WDI	0.8×REG		REG	V
V_{IL}			0		0.2×REG	
V_O	Output voltage	GPOD			25	V
V_O	Output voltage range	XALERT, SDATA, XRST			REG	V
		CELL+, CELL–		0.975		
	External 2.5-V REG capacitor	C_{REG}	1.0			µF
	External LEDOUT capacitor	C_{LED}	2.2			µF
	Extend CELL output capacitor	C_{CELL}		0.1		µF
	IOL	GPOD			1	mA
	RPACK			1		kΩ
	Input frequency	WDI		32.768		kHz
	WDI high time		2			µs
T_A	Operating temperature		–25		85	°C
	Functional temperature		–40		110	°C

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ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT, T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V (unless otherwise noted)							
I_{CC1}	Supply Current 1	No load at REG, LEDOUT, TOUT, XALERT, SCLK, SDATA, ZVCHG= off, WDI = 32 kHz VMEN = on, VC5 = VC4 = VC3 = VC2 = VC1 = 0 V select VC5 = VC4 = 0 V	T_A = 25°C		140	190	µA
			T_A = –40°C to 110°C			220	µA
I_{CC2}	Supply Current 2	No load at REG, LEDOUT TOUT, XALERT, SCLK, SDATA. ZVCHG = off, WDI = 32 kHz, VMEN = off	T_A = –40°C to 110°C		105	185	µA
$I_{(SLEEP)}$	Sleep current	CHG, DSG and ZVCHG = off, REG = on, VMEN = off, WDI no clock, SLEEP = 1	T_A = –40°C to 110°C		30	50	µA
$I_{(SHUTDOWN)}$	Shutdown mode	CHG, DSG and ZVCHG = off, REG = off, VMEN = off, WDI no clock, VPACK = 0 V, VC1 = VC2 = VC3 = VC4 = 3.5 V	T_A = –40°C to 110°C		0.1	1	µA
2.5 V LDO, T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V, $I_{OUT\ 33}$ = 0 mA (unless otherwise noted)							
$V_{(REG)}$	Regulator output voltage	4.5 V < VCC or BAT ≤ 25 V, I_{OUT25} ≤ 16 mA	T_A = –40°C to 110°C	2.41	2.5	2.59	V
$\Delta V_{(EGTEMP)}$	Regulator output change with temperature	VCC or BAT = 14 V, I_{OUT25} = 2 mA	T_A = –40°C to 110°C		±0.2%		
$\Delta V_{(REGLINE)}$	Line regulation	5.4 V ≤ VCC or BAT ≤ 25 V, I_{OUT25} = 2 mA	T_A = 25°C		3	10	mV
$\Delta V_{(REGLOAD)}$	Load regulation	VCC or BAT = 14 V, 0.2 mA ≤ I_{OUT25} ≤ 2 mA	T_A = 25°C		7	15	mV
		VCC or BAT = 14 V, 0.2 mA ≤ I_{OUT25} ≤ 16 mA	T_A = 25°C		15	50	mV
$I_{(REGMAX)}$	Current limit	VCC or BAT = 14 V, REG = 2 V	T_A = 25°C	16		75	mA
		VCC or BAT = 14 V, REG = 0 V	T_A = 25°C	5		45	
3.3 V LED, T_A = 25°C, CREG = 1.0 µF , C_L = 2.2 µF, VCC or BAT = 14 V, I_{OUT25} = 0 mA (unless otherwise noted)							
$V_{O(LED)}$	Regulator output voltage	4.5 V < VCC or BAT ≤ 25 V, I_{OUT33} ≤ 10 mA	T_A = –40°C to 110°C	3	3.3	3.6	V
		6.5 V < VCC or BAT ≤ 25 V, I_{OUT33} ≤ 25 mA		3	3.3	3.6	
$\Delta V_{(LEDEMP)}$	Regulator output change with temperature	VCC or BAT = 14 V, I_{OUT33} = 2 mA	T_A = –40°C to 110°C		±0.2%		
$\Delta V_{(LEDLINE)}$	Line regulation	5.4 V ≤ VCC or BAT ≤ 25 V, I_{OUT33} = 2 mA	T_A = 25°C		3	10	mV
$\Delta V_{(LEDLOAD)}$	Load regulation	VCC or BAT = 14 V, 0.2 mA ≤ I_{OUT33} ≤ 2 mA	T_A = 25°C		7	15	mV
		VCC or BAT = 14 V, 0.2 mA ≤ I_{OUT33} ≤ 25 mA			40	100	
$I_{(LEDMAX)}$	Current limit	VCC or BAT = 14 V, REG = 3 V	T_A = 25°C	25		125	mA
		VCC or BAT = 14 V, REG = 0 V		12		50	
THERMISTOR DRIVE, T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V (unless otherwise noted)							
VTOUT		I_{TOUT} = 0 mA		2.4		2.6	V
$R_{DS(ON)}$	TOUT Pass-element series resistance	I_{TOUT} = –1 mA at TOUT pin, $R_{DS(ON)}$ = [V_{REG} – V_{OUT} (TOUT)] / 1 mA	T_A = –40°C to 110°C		50	100	Ω
SHUTDOWN WAKE, T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V (unless otherwise noted)							
$V_{STARTUP}$	PACK Exit shutdown threshold	VCC or BAT = 14 V, PACK = 1.4 V				1	µA
POR, T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V (unless otherwise noted)							
V_{POR}	VREGTH–			–3%	1.8	3%	V
	Hysteresis (V_{regth+} – $V_{regth–}$)			50	150	250	mV

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ELECTRICAL CHARACTERISTICS (Continued)

CELL VOLTAGE MONITOR, T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V (unless otherwise noted)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(CELLOUT)}$	CELL output	$V_{Cn} – V_{Cn+1}$ = 0 V, 8 V ≤ VDD ≤ 25 V	0.950	0.975	1	V
		$V_{Cn} – V_{Cn+1}$ = 4.5 V, 8 V ≤ VDD ≤ 25 V	0.275	0.3	0.325	
REF		Mode (1), 8 V ≤ VDD ≤ 25 V	–1%	0.975	1%	V
PACK		Mode [Register Address = 0x03, b1(PACK) = 1, b0(VMEN) = 1]	–2%	PACK/18	2%	V
BAT		Mode [Register Address = 0X03, b6(BAT) = 1, b0 (VMEN) = 1]	–2%	BAT/18	2%	V
CMRR	Common mode rejection	CELL max to CELL min	40			dB
$V_{(CELLSLEW)}$	CELL output rise	Min to Max 10% to 90%	9			ms
K	CELL scale factor	K = {CELL output (VC5 = 0 V, VC4 = 4.5 V) –CELL output (VC5 = VC4 = 0 V)} / 4.5	0.147	0.150	0.153	
		K = {CELL output (VC2 = 13.5 V, VC1 = 18 V) –CELL output (VC2 = VC1 = 13.5 V)} / 4.5	0.147	0.150	0.153	
$I_{(VCELLOUT)}$	Drive current	$V_{Cn–}$ V_{Cn+1} = 0 V , Vcell = 0 V, T_A = –40° to 110°	12	18		µA
V_{ICR}	CELL output offset error	CELL output (VC2 = 18 V, VC1 = 18 V) –CELL output (VC2 = VC1 = 0 V)		–1		mV
$R_{(BAL)}$	Cell balance internal resistance	$R_{DS(ON)}$ for internal FET switch at V_{DS} = 2 V	–50%	400	50%	Ω

(1) Register Address = 0x04, b2(CAL0) = b3(CAL1) = 1, Register Address = 0x03, b0(VMEN) = 1

CURRENT PROTECTION DETECTION, T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V (unless otherwise noted)							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(OLT)}$	OL detection threshold voltage range, typical(1)	RSNS = 0	RSNS is set in FUNCTION_CTL register	–50		–205	mV
		RSNS = 1		–25		–102.5	
$ΔV_{(OLT)}$	OL detection threshold voltage program step	RSNS = 0			–5		mV
		RSNS = 1			–2.5		
$V_{(SCCT)}$	SCC detection threshold voltage range, typical (2)	RSNS = 0		100		475	mV
		RSNS = 1		50		237.5	
$ΔV_{(SCCT)}$	SCC detection threshold voltage program step	RSNS = 0			25		mV
		RSNS = 1			12.5		
$V_{(SCDT)}$	SCD detection threshold voltage range, typical(3)	RSNS = 0		–100		–475	mV
		RSNS = 1		–50		–237.5	
$ΔV_{(SCDT)}$	SCD detection threshold voltage program step	RSNS = 0			–25		mV
		RSNS = 1			–12.5		
$V_{OL(acr)}$	OL detection threshold voltage accuracy(1)	V_{OL} = –25 mV (typ)		–15	–25	–35	mV
		V_{OL} = –100 mV (typ) (RSNS = 0,1)		–90	–100	–110	
		V_{OL} = –205 mV (typ)		–185	–205	–225	
$V_{(SCC\_acr)}$	SCC detection threshold voltage accuracy(2)	V_{SCC} = 50 mV (typ)		30	50	70	mV
		V_{SCC} = 200 mV (typ) (RSNS = 0,1)		180	200	220	
		V_{SCC} = 475 mV (typ)		428	475	523	
$V_{(SCD\_acr)}$	SCD detection threshold voltage accuracy(3)	V_{SCD} = –50 mV (typ)		–30	–50	–70	mV
		V_{SCD} = –200 mV (typ) (RSNS = 0,1)		–180	–200	–220	
		V_{SCD} = –475 mV (typ)		–426	–475	–523	

(1) See OLV register for setting detection threshold
(2) See SCC register for setting detection threshold
(3) See SCD register for setting detection threshold

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ELECTRICAL CHARACTERISTICS (Continued)

FET DRIVE CIRCUIT, T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V (unless otherwise noted)							
PARAMETER		**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNIT**
$V_{O(FETON)}$	Output voltage, charge, and discharge FETs on	$V_{O(FETOND)} = V_{(DSG)} – Vpack$ VGS connect 10 MΩ	T_A = 25°C	7.5	12	15.5	V
			T_A = –40°C to 110°C	8	12	16	
		$V_{O(FETONC)} = V_{(CHG)} – V_{BAT}$ VGS connect 10 MΩ	T_A = 25°C	7.5	12	15.5	V
			T_A = –40°C to 110°C	8	12	16	
$V_{(ZCHG)}$	ZVCHG clamp voltage	BAT = 4.5 V		3.3	3.5	3.7	V
$V_{O(FETOFF)}$	Output voltage, charge, and discharge FETs off	VFETOND = VDSG – Vpack				0.2	V
		VFETONC = VCHG – VBAT				0.2	
t_r	Rise time	C_L = 4700 pF	$V_{(CHG)}$: Vpack ≥ Vpack + 4 V		400	1000	µs
			$V_{(DSG)}$: VBAT ≥ VBAT + 4 V		400	1000	
t_f	Fall time	C_L = 4700 pF	$V_{(CHG)}$: Vpack + VCHG (FETON) ≥ pack + 1 V		40	200	µs
			$V_{(DSG)}$: VC1 + VDSG (FETON) ≥ VC1 + 1 V		40	200	
LOGIC, T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V (unless otherwise noted)							
$R_{(PUP)}$	Internal pullup resistance	XALERT	T_A = –40°C to 110°C	60	100	200	kΩ
		SDATA, SCLK		6	10	20	
		XRST		1	3	6	
V_{OL}	Low Logic level output voltage	XALERT	T_A = –40°C to 110°C			0.2	V
		SDATA, I_{OUT} = 200 µA				0.4	
		GPOD, I_{OUT} = 50 µA				0.6	
		VCC or BAT = 7 V, VREG = 1.5 V, XRST, I_{OUT} = 200 µA				0.4	
V_{IH}	SCLK (hysteresis input)	Hysteresis			450		mV

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, CREG = 1 µF, C_L = 2.2 µF, VCC or BAT = 14 V (unless otherwise noted)

PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
t_{WDTINT}	WDT start up detect time		250	500	1000	ms
t_{WDWT}	WDT detect time		50	100	150	µs
t_{RST}	XRST Active high time		100	250	560	µs

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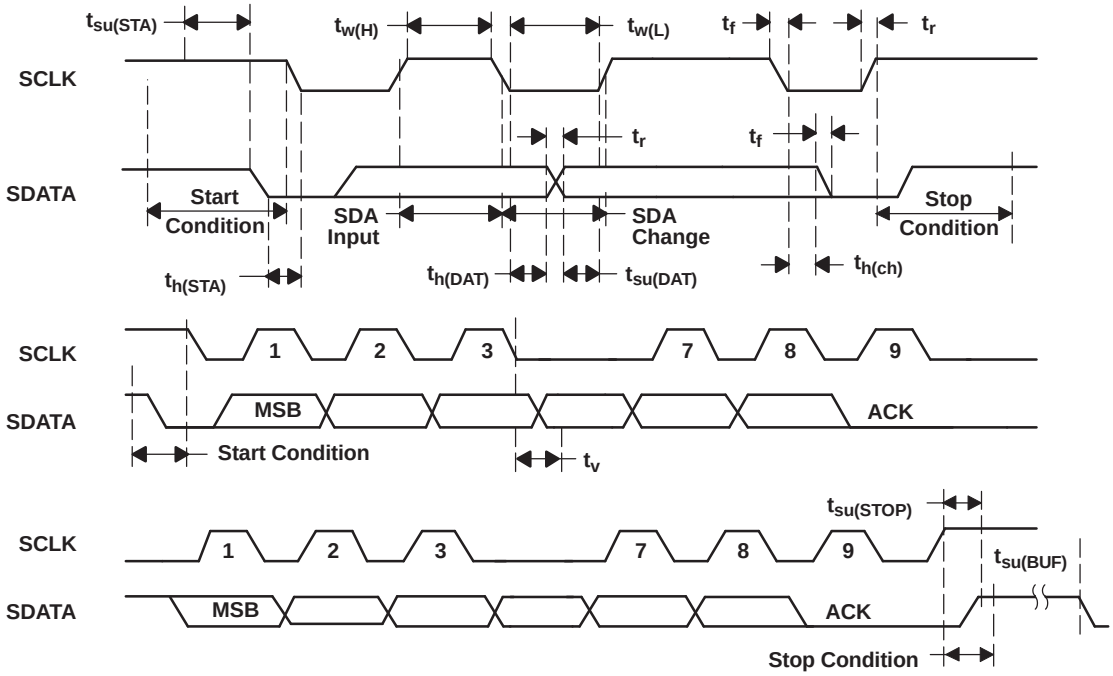
AC TIMING REQUIREMENTS (I²C compatible serial interface)

T_A = 25°C, CREG = 1 µF, VCC or BAT = 14 V (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_r	SCLK, SDATA rise time		1000	ns
t_f	SCLK, SDATA fall time		300	ns
$t_{w(H)}$	SCLK pulse width high	4		µs
$t_{w(L)}$	SCLK pulse width low	4.7		µs
$t_{su(STA)}$	Setup time for start condition	4.7		µs
$t_{h(STA)}$	Start condition hold time after which first clock pulse is generated	4		µs
$t_{su(DAT)}$	Data setup time	250		ns
$t_{h(DAT)}$	Data hold time	0		µs
$t_{su(STOP)}$	Setup time for Stop condition	4		µs
$t_{su(BUF)}$	Time the bus must be free before new transmission can start	4.7		µs
t_v	Clock low to data out valid		900	ns
$t_{h(CH)}$	Data out hold time after clock low	10		ns
f_{SCL}	Clock frequency	0	100	kHz



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FUNCTIONAL DESCRIPTION

LOW DROP OUTPUT REGULATOR (LEDOUT)

The inputs for this regulator can be derived from the VCC or BAT terminals. The output is a fixed voltage of typically 3.3 V with the minimum output capacitance for stable operation of 2.2 µF and is also internally current limited. This output is used for LED drive, power supply source for REG (2.5 V) and bq29330 internal circuit. During normal operation, the regulator limits output current to typically 50 mA. Until the internal regulator circuit is correctly powered, the DSG and CHG FET drives are low (FETs = OFF).

LOW DROP OUTPUT REGULATOR (REG)

The inputs for this regulator can be derived from the LED (3.3 V). The output is typically 2.5 V with the minimum output capacitance for stable operation of 1 µF and is also internally current limited. During normal operation, the regulator limits output current to typically 50 mA.

INITIALIZATION

From a shutdown situation, the bq29330 requires a voltage greater that start-up voltage ($V_{STARTUP}$) applied to the PACK pin to enable its integrated regulator and provide the regulators power source. Once the REG output is stable, the power source of the regulator is switched to VCC.

After the regulator has started, it then continues to operate through the VCC input. If the VCC input is below the minimum operating range, then the bq29330 will not operate if the supply to the PACK input is removed.

If the voltage at VLED falls below about 2.3 V, the internal circuit turns off the FETs and disables all controllable functions including the REG, LEDOUT, and TOUT outputs.

The initial state of the CHG and DSG FET drive is low (OFF) and the ZVCHG FET drive is low (ON).

OVERLOAD DETECTION

The overload detection is used to detect abnormal currents in the discharge direction. This feature is used to protect the pass FETs, cells, and any other inline components from excessive discharge current conditions. The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to the OFF state. The overload sense voltage is set in the OLV register, and delay time is set in the OLD register. The thresholds can be individually programmed from 50 mV to 205 mV in 5-mV steps with the default being 50 mV.

If the RSNS bit in the FUNCTION_CTL register is set to 1, then the voltage threshold, programmable step size, and hysteresis is divided by 2.

SHORT CIRCUIT IN CHARGE AND SHORT CIRCUIT IN DISCHARGE DETECTION

The short current circuit in charge and short circuit in discharge detections are used to detect severe abnormal current in the charge and discharge directions, respectively. This safety feature is used to protect the pass FETs, cells, and any other inline components from excessive current conditions. The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to the OFF state. The short circuit in charge threshold and delay time are set in the SCC register. The short circuit in discharge threshold and delay time are set in the SCD register. The short-circuit thresholds can be programmed from 100 mV to 475 mV in 25-mV steps.

If the RSNS bit in the FUNCTION_CTL register is set to 1, then the voltage threshold, programmable step size, and hysteresis is divided by 2.

OVERLOAD, SHORT CIRCUIT IN CHARGE AND SHORT CIRCUIT IN DISCHARGE DELAY

The overload delay (default = 1 ms) allows the system to momentarily accept a high current condition without disconnecting the supply to the load. The delay time can be increased via the OLD register which can be programmed for a range of 1 ms to 31 ms with 2-ms steps.

The short circuit in charge and short circuit in discharge delays (default = 0 µs) are programmable in the SCC and SCD registers, respectively. These registers can be programmed from 0 µs to 915 µs with 61-µs steps.

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OVERLOAD, SHORT CIRCUIT IN CHARGE AND SHORT CIRCUIT IN DISCHARGE RESPONSE

When an overload, short circuit in charge, or short circuit in discharge fault is detected, the FETs are turned off. The STATUS (b0…b3) register reports the details of overload, short circuit in charge or short-circuit discharge. The respective STATUS (b0…b3) bits are set to 1 and the XALERT output is triggered. This condition is latched until the STATE_CONTROL (b7) is set and then reset. If a FET is turned on after resetting STATE_CONTROL (b0) and the error condition is still present on the system, then the device again enters the protection response state.

2-, 3-, or 4-CELL CONFIGURATION

In a 2-cell configuration, VC1 and VC2 are shorted to VC3. In a 3-cell configuration, VC1 is shorted to VC2.

CELL VOLTAGE

The cell voltage is translated to allow a system host to measure individual series elements of the battery. The series element voltage is translated to a GND-based voltage equal to 0.15 ±0.003 of the series element voltage. This provides a range from 0 to 4.5 V. The translation output is presented between CELL+ and CELL– pins of the bq29330 and is inversely proportional to the input using the following equation.

Where, $V_{(CELLOUT)} = –K \times V_{(CELLIN)} + 0.975$ (V)

Programming CELL_SEL (b1, b0) selects the individual series element. The CELL_SEL (b3, b2) selects the voltage monitor mode, cell monitor, offset, etc.

CALIBRATION OF CELL VOLTAGE MONITOR AMPLIFIER GAIN

The cell voltage monitor amplifier has an offset, and to increase accuracy, this can be calibrated.

The following procedure shows how to measure and calculate the offset as an example.

Step 1

Set CAL1=1, CAL0=1, VMEN=1.

VREF is trimmed to 0.975 V within ±1%; measuring VREF eliminates its error.

Measure internal reference voltage VREF from VCELL directly.

VREF = measured reference voltage

Step 2

Set CAL1=0, CAL0=1, CELL1=0, CELL0=0, VMEN=1.

The output voltage includes the offset and represented by:

$V_{OUT(4-5)} = VREF + (1 + K) \times V_{OS}$ (V)

Where K = CELL Scaling Factor

V_{OS} = Offset voltage at input of the internal operational amplifier

Step 3

Set CAL1=1, CAL0=0, CELL1=0, CELL0=0, VMEN=1.

Measure scaled REF voltage through VCELL amplifier.

The output voltage includes the scale factor error and offset and is represented by:

$V_{(OUTR)} = VREF + (1 + K) \times VOS – K \times VREF$ (V)

Step 4

Calculate $(V_{OUT(4-5)} – V_{(OUTR)}) / VREF$.

The result is the actual scaling factor, K_{ACT} and is represented by:

$K_{ACT} = (V_{OUT(4-5)} – V_{(OUTR)}) / VREF = (VREF + (1 + K) \times V_{OS}) – (VREF + (1 + K) \times V_{OS} – K \times VREF)/VREF = K \times VREF/VREF = K$

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Step 5

Calculate the actual offset value where:

$V_{OS(ACT)} = (V_{(OUTR)} – VREF) / (1 + K_{ACT})$

Step 6

Calibrated cell voltage is calculated by:

$VCn – VC(n+1) = \{ VREF + (1 + K_{ACT}) \times V_{OS(ACT)} – V_{(CELLOUT)}\}/K_{ACT} = \{V_{OUT(4-5)} – V_{(CELLOUT)}\}/K_{ACT}$

To seek greater accuracy, it is better to measure $V_{OS(ACT)}$ for each cell voltage.

Set CAL1=0, CAL0=0, CELL1=0, CELL0=1, VMEN=1.

Set CAL1=0, CAL0=0, CELL1=1, CELL0=0, VMEN=1.

Set CAL1=0, CAL0=0, CELL1=1, CELL0=1, VMEN=1.

Measure $V_{OUT(3-4)}$, $V_{OUT(2-3)}$, $V_{OUT(1-2)}$,

$VC4 – VC5 = \{V_{OUT(4-5)} – V_{(CELLOUT)}\}/K_{ACT}$

$VC3 – VC4 = \{V_{OUT(3-4)} – V_{(CELLOUT)}\}/K_{ACT}$

$VC2 – VC3 = \{V_{OUT(2-3)} – V_{(CELLOUT)}\}/K_{ACT}$

$VC1 – VC2 = \{V_{OUT(1-2)} – V_{(CELLOUT)}\}/K_{ACT}$

BATTERY PACK AND BATTERY STACK MEASUREMENTS

The PACK (battery pack) and VC1 (battery stack) inputs can be translated to the CELL+, CELL– outputs of the bq29330 through control bits in the FUNCTION_CONTROL register. If PACK is set, then the input at the PACK is divided by 18 and presented at the CELL+, CELL– outputs. If the BAT bit is set, then the input to VC1 is divided by 18 and presented at the CELL+, CELL– outputs. If setting both bits at the same time, VC1 is presented at the CELL+, CELL– outputs.

CELL BALANCE CONTROL

The cell balance control allows a small bypass path to be controlled for any one series element. The purpose of this bypass path is to reduce the current into any one cell during charging to bring the series elements to the same voltage. Series resistors placed between the input pins and the positive series element nodes control the bypass current value. Individual series element selection is made using bits 4 through 7 of CELL_SEL register.

Series input resistors between 500 Ω and 1 kΩ are recommended for effective cell balancing.

XALERT (XALERT)

XALERT is driven Low, when WDF, OL, SCC, or SCD OC are detected. To clear XALERT, toggle (from 0, set to 1, then reset to 0) STATE_CONTROL, LTCLR (bit 7), then read the STATUS register.

THERMISTOR DRIVE CIRCUIT (TOUT)

The TOUT pin can be enabled to drive a thermistor from REG. The typical thermistor resistance is 10 kΩ at 25°C. The default state for this is OFF to conserve power. The maximum output impedance is 100 Ω. TOUT is enabled in FUNCTION_CONTROL register (bit 3).

GENERAL PURPOSE OPEN DRAIN DRIVE CIRCUIT (GPOD)

The General Purpose Open Drain output has 1-mA current source drive with a maximum output voltage of 25 V. The OD output is enabled or disabled by OUTPUT_CONTROL register (bit 4) and has a default state of OFF.

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LATCH CLEAR (LTCLR)

When a protection fault occurs, the state is latched. To clear the fault flag, toggle (from 0, set 1, then reset to 0) the LTCLR bit in the STATE_CONTROL register (bit 7). The OL, SCC, SCD, and WDF bits are unlatched by this function. The FETs can now be controlled by programming the OUTPUT_CONTROL register, and the XALERT output can be cleared by reading the STATUS register.

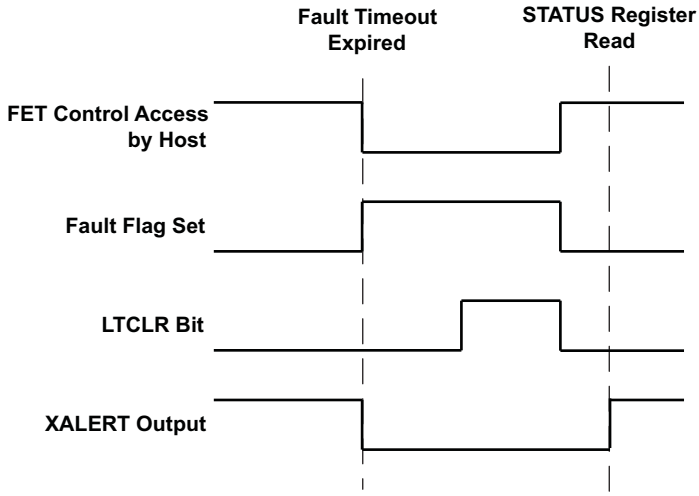

Figure 1. LTCLR and XLAERT Clear Timing

POR and WATCHDOG RESET (XRST)

The XRST pin is activated by activation of the REG output. This holds the host in reset for the duration of the t_{RST} period, allowing the VREG to stabilize before the host is released from reset. When the regulator power is down, XRST is active below the regulator's voltage of 1.8 V. Also, when a watchdog fault is detected, the XRST is also activated to ensure a valid reset of the battery management host.

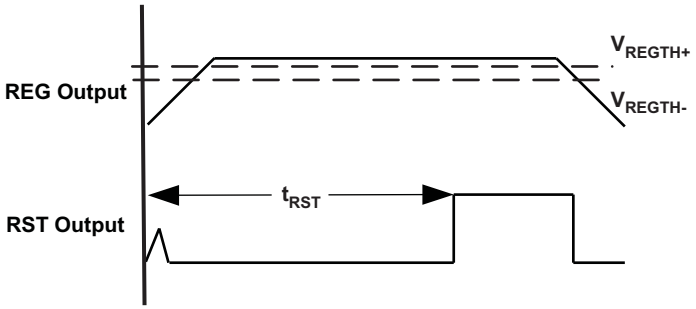

Figure 2. XRST Timing Chart – Power Up and Power Down

WATCHDOG INPUT (WDI)

The WDI input is required as a time base for delay timing when determining fault detection and is used as part of the system watchdog.

Initially, the watchdog monitors the host oscillator start-up; if there is no response from the host within t_{WDINT} of t_{RST} expiring, then the bq29330 turns CHG, DSG, and ZVCHG FETs off. It then activates the XRST output in an attempt to reset the host.

Once the watchdog has been started during this wake-up period, it monitors the host for an oscillation stop condition which is defined as a period of t_{WDWT} where no clock input is received. If an oscillator stop condition is identified, then the watchdog turns the CHG, DSG, and ZVCHG FETs off. The bq29330 then activates the XRST output in an attempt to reset the host.

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If the host clock oscillation is started after the reset, the bq29330 still has the WDF flag set until it is cleared. See the LTCLR section for further details on clearing the fault flags.

During Sleep mode, the watchdog function is not disabled.

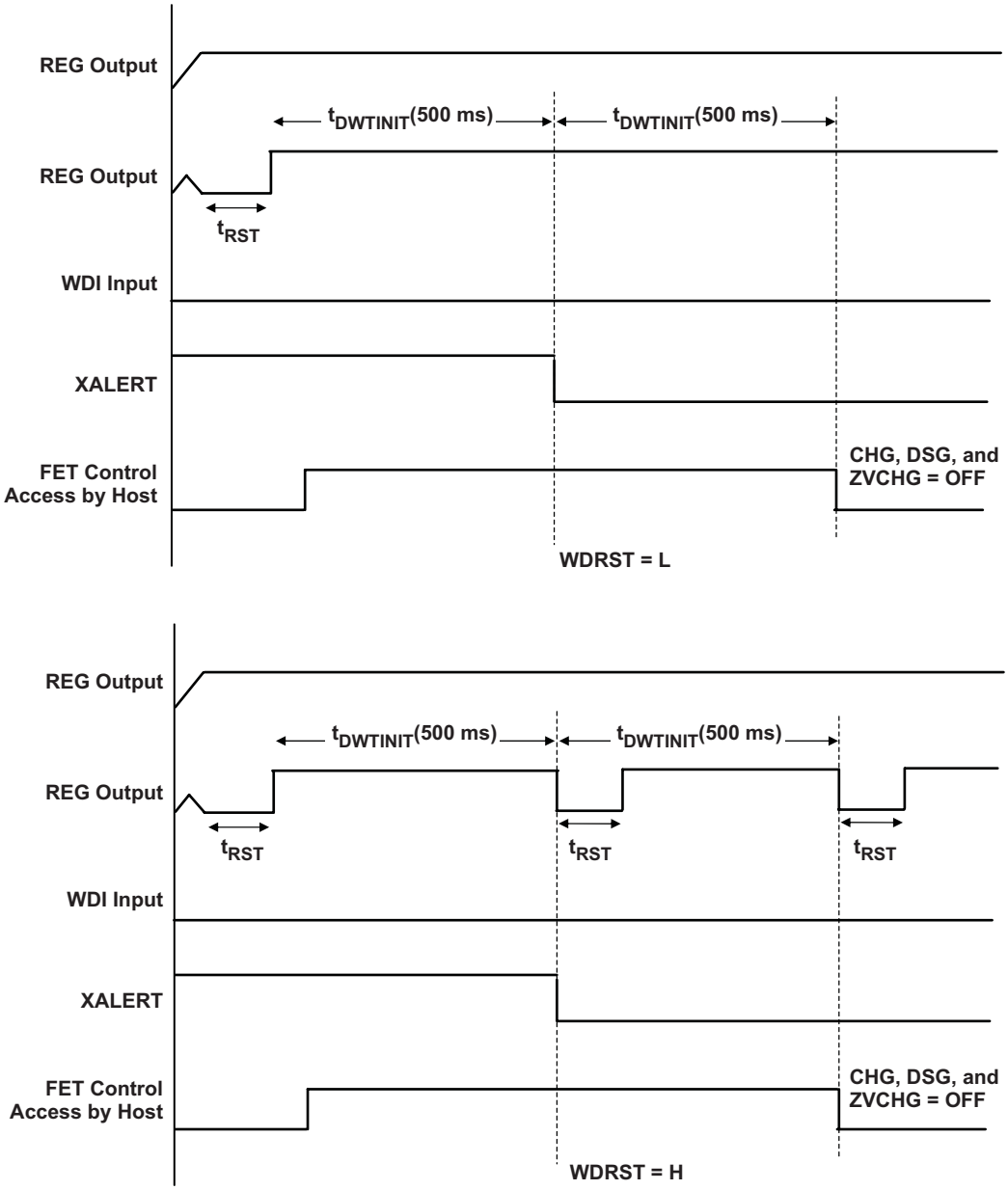

Figure 3. Watchdog Timing Chart – WDI Fault at Start-up

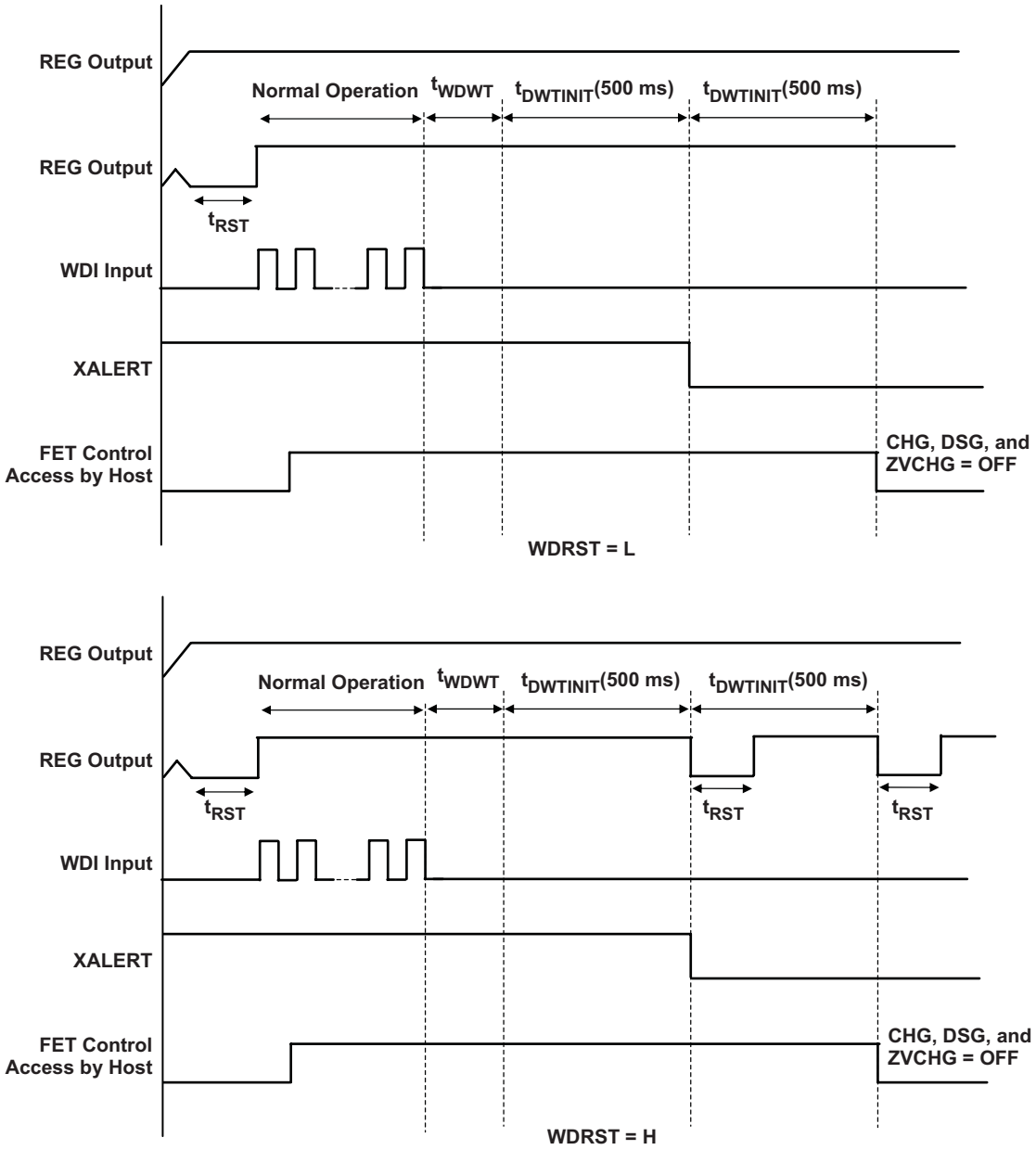

Figure 4. Watchdog Timing Chart – WDI Fault After Startup

DSG and CHG NCH FET DRIVER CONTROL

The bq29330 drives either the DSG or CHG FET off if an OL, SCC, or SCD safety threshold is breached depending on the current direction. The host can force any FET on or off only if the bq29330 integrated protection control allows.

The default-state of the FET drive is off. A host can control the FET drive by programming OUTPUT_CONTROL (b2...b0), where b0 is used to control the discharge FET, b1 is used to control the charge FET, and b2 is used to control the ZVCHG FET. These controls are only valid when not in the initialized state. The CHG drive FET can be powered by PACK and the DSG FET can be powered by BAT.

When the bq29330 powers down, the NCH FET drivers power down to GND causing the FETs to turn off.

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PRECHARGE AND 0 V CHARGING

The bq29330 supports both a charger that has a precharge mode and one that does not. The bq29330 also supports charging even when the battery falls to 0 V. In order to charge, the charge FET (CHG) must be turned on to create a current path. When the V_{BAT} is ~0 V, the $V_{(PACK)}$ is as low as the battery voltage. In this case, the supply voltage for the device is too low to operate.

POWER MODES

The bq29330 has three power modes, normal, sleep, and ship. The following table outlines the operational functions during these power modes.

Table 1. Outlines the Operational Functions

POWER MODE	TO ENTER POWER MODE	TO EXIT POWER MODE	MODE DESCRIPTION
Normal	STATE_CONTROL, SLEEP(b0) = 0 and STATE_CONTROL, SHIP (b1) = 0		The battery is in normal operation with protection, power management and battery monitoring functions available and operating. The supply current of this mode varies as the host can enable and disable various power management features.
Sleep	STATE_CONTROL, SLEEP(b0) = 1 and STATE_CONTROL, SHIP (b1) = 0	STATE_CONTROL, SLEEP(b0) = 0	CHG, DSG, and ZVCHG OFF, OL, SCC, and SCD function is disabled. Cell AMP, GPOD , CELL BAL, and WDF is not disabled
Ship	STATE_CONTROL, SHIP (b1) = 1 and supply at the PACK < V_{WAKE}	Supply voltage to PACK Supply	The bq29330 is completely shut down as in the sleep mode. In addition, the REG output is disabled, I^2C interface is powered down, and memory is not valid.

VOLTAGE BASED EXIT FROM SHUTDOWN

If a voltage greater than $V_{STARTUP}$ is applied to the PACK pin, then the bq29330 exits shutdown and enters normal mode.

COMMUNICATIONS

The I^2C-compatible serial communications provides read and write access to the bq29330 data area. The data is clocked via separate data (SDATA) and clock (SCLK) pins. The bq29330 acts as a slave device and does not generate clock pulses. Communication to the bq29330 can be provided from GPIO pins or an I^2C supporting port of a host system controller. The slave address for the bq29330 is 7 bits, and the value is 0100 000 (0x20).

	(MSB)			I2C Address +R/W bit				(LSB)
	(MSB)			I2C Address (0x20)			(LSB)	
Write	0	1	0	0	0	0	0	0
Read								1

The bq29330 does NOT have the following functions compatible with the I^2C specification.

- The bq29330 is always regarded as a slave.
- The bq29330 does not support the General Code of the I^2C specification, and therefore will not return an ACK but may return a NACK.
- The bq29330 does not support the Address Auto Increment, which allows continuous reading and writing.
- The bq29330 will allow data to be written or read from the same location without re-sending the location address.

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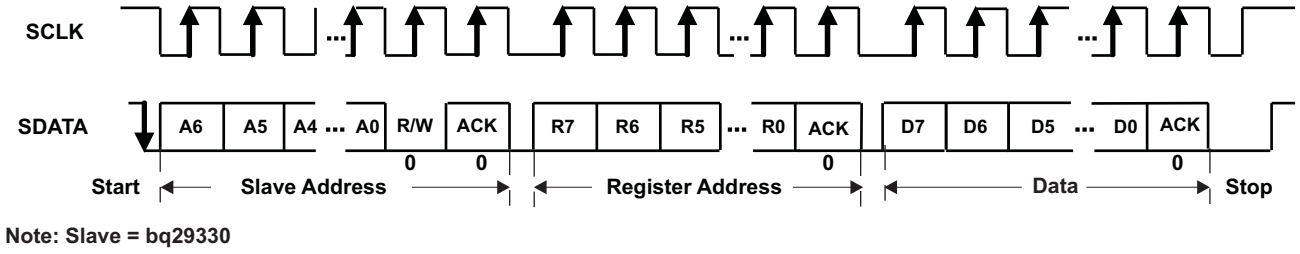

Figure 5. I²C-Bus Write to bq29330

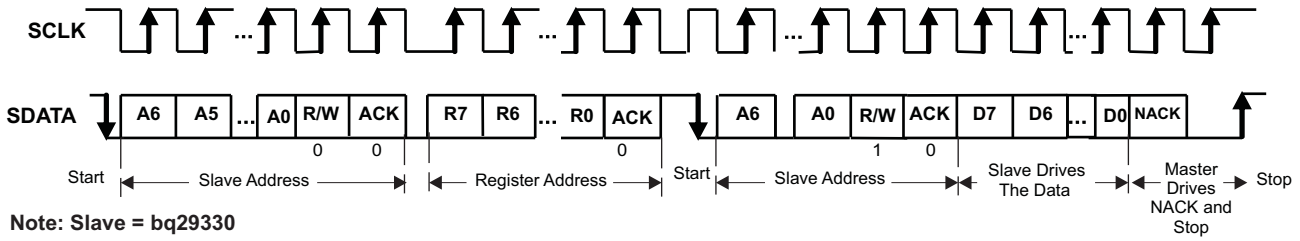

Figure 6. I²C-Bus Read from bq29330: Protocol A

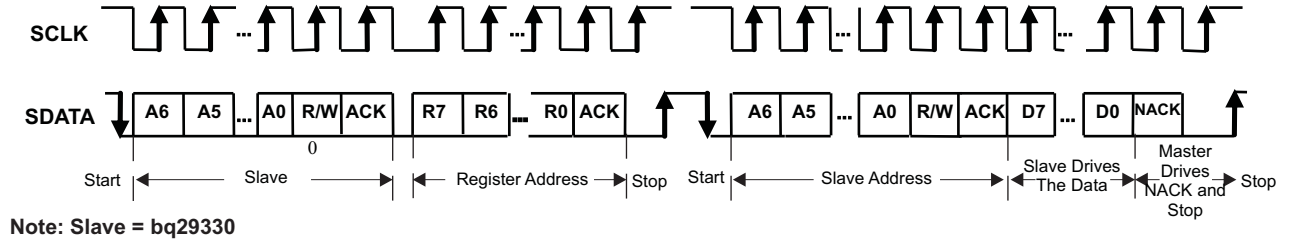

Figure 7. I²C-Bus Read from bq29330: Protocol B

REGISTER MAP

The bq29330 has nine addressable registers. These registers provide status, control, and configuration information for the battery protection system.

NAME	ADDR	TYPE	DESCRIPTION
STATUS	0x00	R	Status register
OUTPUT_CONTROL	0x01	R/W	Output pin control from system host and external pin status
STATE_CONTROL	0x02	R/W	State control
FUNCTION_CONTROL	0x03	R/W	Function control
CELL _SEL	0x04	R/W	Battery cell select for cell translation and balance bypass and select mode for calibration
OLV	0x05	R/W	Overload voltage threshold
OLD	0x06	R/W	Overload delay time
SCC	0x07	R/W	Short circuit in charge current threshold voltage and delay
SCD	0x08	R/W	Short circuit in discharge current threshold voltage and delay

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NAME	ADDR	TYPE	BIT MAP							
			B7	B6	B5	B4	B3	B2	B1	B0
STATUS	0x00	R	0	0	0	ZV	WDF	OL	SCC	SCD
OUTPUT_ CONTROL	0x01	R/W	0	0	PMS_CHG	GPOD	XZV	CHG	DSG	LTCLR
STATE_ CONTROL	0x02	R/W	0	0	0	RSNS	WDRST	WDDIS	SHIP	SLEEP
FUNCTION_ CONTROL	0x03	R/W	0	0	0	0	TOUT	BAT	PACK	VMEN
CELL _SEL	0x04	R/W	CB3	CB2	CB1	CB0	CAL1	CAL0	CELL1	CELL0
OLV	0x05	R/W	0	0	0	OLV4	OLV3	OLV2	OLV1	OLV0
OLD	0x06	R/W	0	0	0	0	OLD3	OLD2	OLD1	OLD0
SCC	0x07	R/W	SCCD3	SCCD2	SCCD1	SCCD0	SCCV3	SCCV2	SCCV1	SCCV0
SCD	0x08	R/W	SCDD3	SCDD2	SCDD1	SCDD0	SCDV3	SCDV2	SCDV1	SCDV0

STATUS: Status register

STATUS REGISTER (0x00)							
7	6	5	4	3	2	1	0
0	0	0	ZV	WDF	OL	SCC	SCD

The STATUS register provides information about the current state of the bq29330.

STATUS b0 (SCD): This bit indicates a short circuit in discharge condition.

0 = Voltage below the short circuit in discharge threshold (default).

1 = Voltage greater than or equal to the short circuit in discharge threshold.

STATUS b1 (SCC): This bit indicates a short circuit in charge condition in the charge direction.

0 = Voltage below the short circuit in charge threshold (default).

1 = Voltage greater than or equal to the short circuit in charge threshold.

STATUS b2 (OL): This bit indicates an overload condition.

0 = Voltage less than or equal to the overload threshold (default).

1 = Voltage greater than overload threshold.

STATUS b3 (WDF): This bit indicates a watchdog fault condition has occurred.

0 = 32-kHz oscillation is normal (default).

1 = 32-kHz oscillation stopped or not started, and the watchdog has timed out.

STATUS b4 (ZV): This bit indicates ZVCHG output is clamped.

0 = ZVCHG pin is not clamped (default).

1 = ZVCHG pin is clamped.

STATUS b5, b6, b7: Reserved

OUTPUT_CONTROL : Output control register

OUTPUT_CONTROL REGISTER (0x01)							
7	6	5	4	3	2	1	0
0	0	PMS_CHG	GPOD	XZV	CHG	DSG	LTCLR

The OUTPUT_CONTROL register controls the outputs of the bq29330 and can show the state of the external pin corresponding to the control.

OUTPUT_ CONTROL b0 (LTCLR): When a fault is latched, this bit releases the fault latch when toggled from 0 to 1 and back to 0 (default =0).

0 = (default)

0->1 ->0 clears the fault latches, allowing STATUS to be cleared on its next read.

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OUTPUT_ CONTROL b1 (DSG): This bit controls the external discharge FET.

0 = Discharge FET is off and is controlled by the system host (default).

1 = Discharge FET is on, and the bq29330 is in normal operating mode.

OUTPUT_ CONTROL b2 (CHG): This bit controls the external charge FET.

0 = Charge FET is off, and is controlled by the system host (default).

1 = Charge FET is on, and the bq29330 is in normal operating mode.

OUTPUT_CONTROL b3(ZV): This bit enables or disables the precharge function.

0 = ZVCHG FET is on, and is controlled by the system host (default).

1 = ZVCHG FET is off, and the bq29330 is in normal operating mode.

OUTPUT_CONTROL b4 (GPOD): This bit enables or disables the GPOD output.

0 = GPOD is high impedance (default).

1 = GPOD output is active (GND).

OUTPUT_CONTROL b5 (PMS_CHG): This bit enables the CHG output for 0-V charge, when PMS terminal is connected to Pack.

0 = CHG FET is off (When PMS = GND, default).

1 = CHG FET is on by connecting CHG and PACK terminal. (When PMS = PACK, default).

STATE_CONTROL : State control register

STATE_CONTROL REGISTER (0x02)							
7	6	5	4	3	2	1	0
0	0	0	RSNS	WDRST	WDDIS	SHIP	SLEEP

The STATE_CTL register controls the outputs of the bq29330 and can be used to clear certain states.

STATE_CONTROL b0 (SLEEP): This bit is used to enter the sleep power mode.

0 = bq29330 exits sleep mode (default).

1 = bq29330 enters the sleep mode.

STATE_CONTROL b1 (SHIP): This bit is used to enter the ship power mode when Pack supply voltage is not applied.

0 = bq29330 is in normal mode (default).

1 = bq29330 enters ship mode when pack voltage is removed.

STATE_CONTROL b2 (WDDIS): This bit is used to enable the watchdog timer.

0 = Watchdog timer is enabled (default).

1 = Watchdog timer is disabled.

STATE_CONTROL b3 (WDRST): This bit is used to enable the reset for GC, when watchdog timer is active.

0 = Reset output is disabled, when watchdog timer is active (default).

1 = 2 Times reset output is enabled, when watchdog timer is active.

STATE_CONTROL b4 (RSNS): This bit sets the OL, SCC, and SCD thresholds into a range suitable for a low sense resistor value by dividing the OLV, SCCV, and SCDV selected voltage thresholds by 2.

0 = Current protection voltage threshold as programmed (default)

1 = Current protection voltage thresholds divided by 2 as programmed

STATE_CONTROL b6..7 (0): These bits are not used and should be set to 0.

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FUNCTION_CONTROL : Function control register

FUNCTION_CTL REGISTER (0x03)							
7	6	5	4	3	2	1	0
0	0	0	0	TOUT	BAT	PACK	VMEN

The FUNCTION_CONTROL register enables and disables features of the bq29330.

FUNCTION_CONTROL b0 (VMEN): This bit enables or disables the cell and battery voltage monitoring function.

0 = Disable voltage monitoring (default). CELL output is pulled down to GND level.

1 = Enable voltage monitoring

FUNCTION_CONTROL b1 (PACK): This bit is used to translate the PACK input to the CELL+, CELL– pins when VMEN = 1. The PACK input voltage is divided by 18 and is presented on CELL+, CELL– pins regardless of the CELL_SEL register settings.

0 = CELL_SEL (b0, b1) settings determine CELL+, CELL– output when VMEN = 1(default).

1 = PACK input translated to CELL output regardless of CELL_SEL (b0, b1) selection when VMEN=1

FUNCTION_CTL b2 (BAT): This bit is used to translate the BAT input to the CELL+, CELL– pins when VMEN=1. The VC5 input voltage is divided by 18 and is presented on CELL+, CELL– regardless of the CELL_SEL register settings.

0 = CELL_SEL (b0, b1) settings determine CELL+, CELL– output when VMEN = 1(default).

1 = BAT input translated to CELL+, CELL– output regardless of CELL_SEL (b0, b1) selection when VMEN = 1

This bit priority is higher than PACK(b1).

FUNCTION_CONTROL b3 (TOUT): This bit controls the power to the thermistor.

0 = Thermistor power is off (default).

1 = Thermistor power is on.

CELL_SEL : Cell select register

CELL_SEL REGISTER (0x04)							
7	6	5	4	3	2	1	0
CB3	CB2	CB1	CB0	CAL1	CAL0	CELL1	CELL0

This register determines cell selection for voltage measurement and translation, cell balancing, and the operational mode of the cell voltage monitoring.

CELL_SEL b0–b1 (CELL0–CELL1): These two bits select the series cell for voltage measurement translation.

CELL1	CELL0	SELECTED CELL
0	0	VC4–VC5, Bottom series element (default)
0	1	VC4–VC3, Second lowest series element
1	0	VC3–VC2, Second highest series element
1	1	VC1–VC2, Top series element

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CELL_SEL b2–b3 (CAL1, CAL0): These bits determine the mode of the voltage monitor block

CAL1	CAL0	SELECTED MODE
0	0	Cell translation for selected cell (default)
0	1	Offset measurement for selected cell
1	0	Monitor the VREF value for gain calibration
1	1	Monitor the V_{REF} directly value for gain calibration, bypassing the translation circuit

CELL_SEL b4–b7 (CB0 – CB3): These 4 bits select the series cell for cell balance bypass path.

CELL_SEL b4 (CB0): This bit enables or disables the bottom series cell balance charge bypass path.

0 = Disable bottom series cell balance charge bypass path (default)

1 = Enable bottom series cell balance charge bypass path

CELL_SEL b5 (CB1): This bit enables or disables the second lowest series cell balance charge bypass path.

0 = Disable series cell balance charge bypass path (default)

1 = Enable series cell balance charge bypass path

CELL_SEL b6 (CB2): This bit enables or disables the second highest cell balance charge bypass path.

0 = Disable series cell balance charge bypass path (default)

1 = Enable series cell balance charge bypass path

CELL_SEL b7 (CB3): This bit enables or disables the highest series cell balance charge bypass path.

0 = Disable series cell balance charge bypass path (default)

1 = Enable series cell balance charge bypass path

OLV: Overload Voltage threshold register

OLV REGISTER (0x05)							
7	6	5	4	3	2	1	0
0	0	0	OLV4	OLV3	OLV2	OLV1	OLV0

OLV (b4–b0): These four bits select the value of the overload threshold with a default of 0000.

OLV (b5–b7): These bits are not used and should be set to 0.

OLV (b4–b0) configuration bits with corresponding voltage threshold(1)							
0x00	–0.050 V	0x08	–0.090 V	0x10	–0.130 V	0x18	–0.170 V
0x01	–0.055 V	0x09	–0.095 V	0x11	–0.135 V	0x19	–0.175 V
0x02	–0.060 V	0x0a	–0.100 V	0x12	–0.140 V	0x1a	–0.180 V
0x03	–0.065 V	0x0b	–0.105 V	0x13	–0.145 V	0x1b	–0.185 V
0x04	–0.070 V	0x0c	–0.110 V	0x14	–0.150 V	0x1c	–0.190 V
0x05	–0.075 V	0x0d	–0.115 V	0x15	–0.155 V	0x1d	–0.195 V
0x06	–0.080 V	0x0e	–0.120 V	0x16	–0.160 V	0x1e	–0.200 V
0x07	–0.085 V	0x0f	–0.125 V	0x17	–0.165 V	0x1f	–0.205 V

(1) If RSNS bit is FUNCTION_CONTROL = 1, then the corresponding voltage threshold is divided by 2.

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OLD: Overload Delay time configuration register

OLD REGISTER (0x07)							
7	6	5	4	3	2	1	0
0	0	0	0	OLD3	OLD2	OLD1	OLD0

OLD(b3–b0): These four bits select the value of the delay time for overload with a default of 0000.							
0x00	1 ms	0x04	9 ms	0x08	17 ms	0x0c	25 ms
0x01	3 ms	0x05	11 ms	0x09	19 ms	0x0d	27 ms
0x02	5 ms	0x06	13 ms	0x0a	21 ms	0x0e	29 ms
0x03	7 ms	0x07	15 ms	0x0b	23 ms	0x0f	31 ms

SCC : Short Circuit In Charge configuration register

SCC REGISTER (0x08)							
7	6	5	4	3	2	1	0
SCCD3	SCCD2	SCCD1	SCCD0	SCCV3	SCCV2	SCCV1	SCCV0

This register selects the short circuit in charge voltage threshold and delay.

SCCV (b3–b0) : These lower nibble bits select the value of the short circuit in charge voltage threshold with 0000 as the default.(1)							
0x00	0.100 V	0x04	0.200 V	0x08	0.300 V	0x0c	0.400 V
0x01	0.125 V	0x05	0.225 V	0x09	0.325 V	0x0d	0.425 V
0x02	0.150 V	0x06	0.250 V	0x0a	0.350 V	0x0e	0.450 V
0x03	0.175 V	0x07	0.275 V	0x0b	0.375 V	0x0f	0.475 V

(1) If RSNS bit is FUNCTION_CTL = 1, then the corresponding voltage threshold is divided by 2.

SCCD (b7–b4): These upper nibble bits select the value of the short circuit in charge delay time. Exceeding the short circuit in charge voltage threshold for longer than this period turns off the CHG and DSG outputs. 0000 is the default.							
0x00	0 µs	0x04	244 µs	0x08	488 µs	0x0c	732 µs
0x01	61 µs	0x05	305 µs	0x09	549 µs	0x0d	793 µs
0x02	122 µs	0x06	366 µs	0x0a	610 µs	0x0e	854 µs
0x03	183 µs	0x07	427 µs	0x0b	671 µs	0x0f	915 µs

SCD : Short Circuit In Discharge configuration register

SCD REGISTER (0x08)							
7	6	5	4	3	2	1	0
SCDD3	SCDD2	SCDD1	SCDD0	SCDV3	SCDV2	SCDV1	SCDV0

This register selects the short circuit in discharge voltage threshold and delay.

SCDV(b3–b0) : These lower nibble bits select the value of the short circuit in discharge voltage threshold with 0000 as the default.(1)							
0x00	–0.100 V	0x04	–0.200 V	0x08	–0.300 V	0x0c	–0.400 V
0x01	–0.125 V	0x05	–0.225 V	0x09	–0.325 V	0x0d	–0.425 V
0x02	–0.150 V	0x06	–0.250 V	0x0a	–0.350 V	0x0e	–0.450 V
0x03	–0.175 V	0x07	–0.275 V	0x0b	–0.375 V	0x0f	–0.475 V

(1) If RSNS bit is FUNCTION_CTL = 1, then the corresponding voltage threshold is divided by 2.

SCCD (b7–b4): These upper nibble bits select the value of the short circuit in charge delay time. Exceeding the Short Circuit in charge voltage threshold for longer than this period will turn off the CHG and DSG outputs. 0000 is the default.							
0x00	0 µs	0x04	244 µs	0x08	488 µs	0x0c	732 µs
0x01	61 µs	0x05	305 µs	0x09	549 µs	0x0d	793 µs
0x02	122 µs	0x06	366 µs	0x0a	610 µs	0x0e	854 µs
0x03	183 µs	0x07	427 µs	0x0b	671 µs	0x0f	915 µs

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REVISION HISTORY

Changes from Original (September 2005) to Revision A **Page**

- Changed package name From: SSOP(DBT) To: TSSOP(DBT) in the Ordering Information Table 2
- Changed the SCLK pin description From: Open-drain bi-directional serial interface clock with internal 10-kΩ pullup to V_{REG} To: Open-drain serial interface clock with internal 10-kΩ pullup to V_{REG} 4
- Changed Supply Current 2 From: XALERT, SCLK, SDATA. ZVCHG = off, Input WDI, To: XALERT, SCLK, SDATA. ZVCHG = off, WDI = 32 kHz, ... 7
- Changed Calibration of Cell Voltage Monitor Amplifier Gain, Step 3 - From: Set CAL1=1, CAL0=1, CELL1=0, CELL0=0, VMEN=1. To: Set CAL1=1, CAL0=0, CELL1=0, CELL0=0, VMEN=1. 12

Changes from Revision A (December 2005) to Revision B **Page**

- Deleted the QFN(RHB) package from the Ordering Information Table, the Package Option Pin Diagrams, and the Pin Functions table. 2

Changes from Revision B (August 2006) to Revision C **Page**

- Changed BAT Pin description From: Charge pump, charge N-CH FET gate drive To: Device power supply input 3
- Changed ELECTRICAL CHARACTERISTICS - CURRENT PROTECTION DETECTION section - positive and negative values were not properly displayed. 8
- Changed Figure 3 - Watchdog Timing Chart – WDI Fault at Start-up 15
- Added Figure 4 - Watchdog Timing Chart – WDI Fault After Startup 16

Changes from Revision C (March 2009) to Revision D **Page**

- Added the RSM package to the Ordering Information Table 2
- Added the RSM pin out package illustration. 3

Changes from Revision D (July 2009) to Revision E **Page**

- Changed the device numbers in the Ordering Information Table From: bq29330ADBT and bq29330ARSM To: bq29330DBT and bq29330RSM 2
- Added Thermal Information 2
- Changed the AC Timing Requiremenst Table, f_{SCL} - Clock frequency MAX value From: 400 kHz To: 100 kHz 10

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ29330DBT	Active	Production	TSSOP (DBT) | 30	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29330
BQ29330DBT.A	Active	Production	TSSOP (DBT) | 30	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29330
BQ29330DBTG4	Active	Production	TSSOP (DBT) | 30	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29330
BQ29330DBTR	Active	Production	TSSOP (DBT) | 30	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29330
BQ29330DBTR.A	Active	Production	TSSOP (DBT) | 30	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29330
BQ29330DBTRG4	Active	Production	TSSOP (DBT) | 30	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29330

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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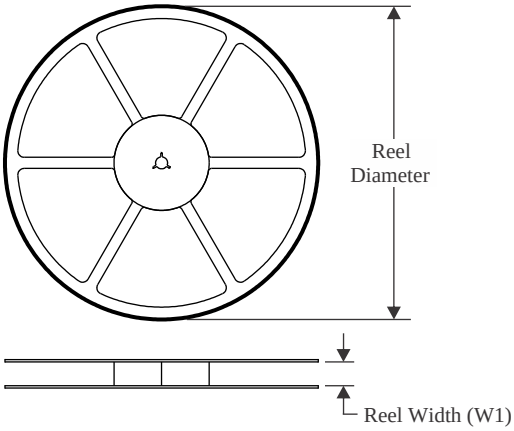
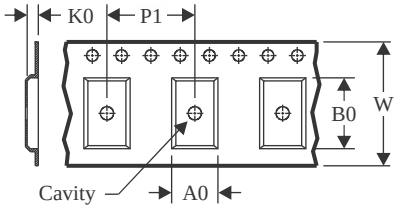
TAPE AND REEL INFORMATION

REEL DIMENSIONS

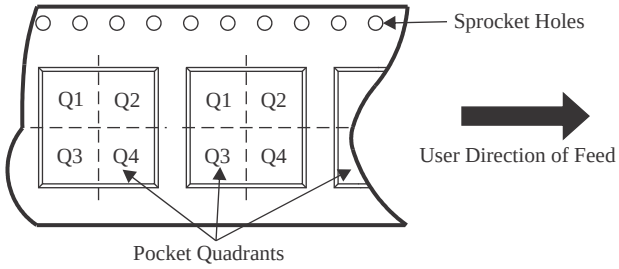


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

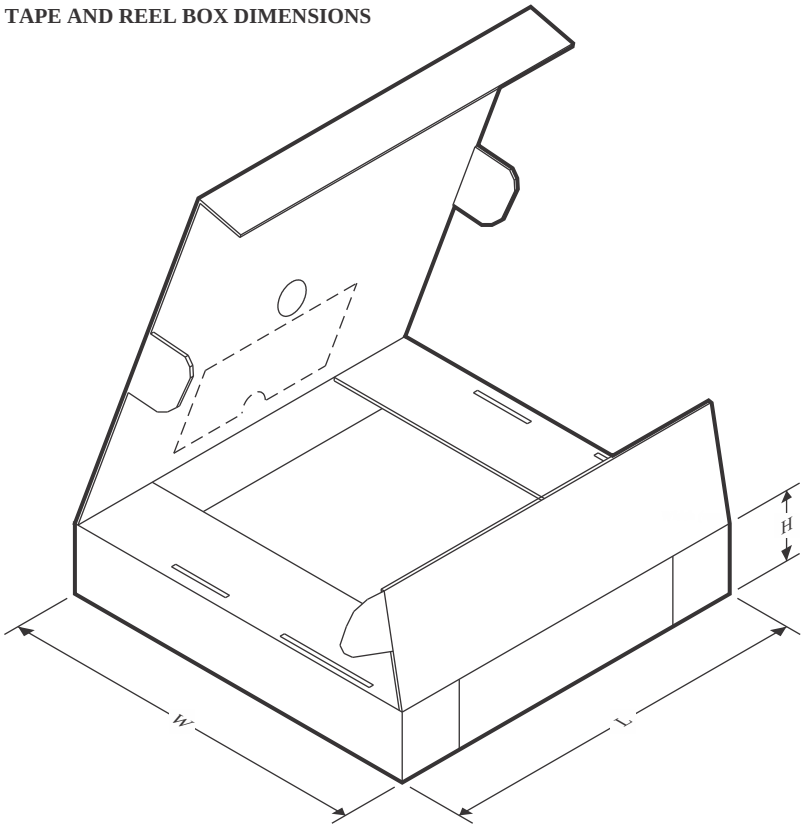
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29330DBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

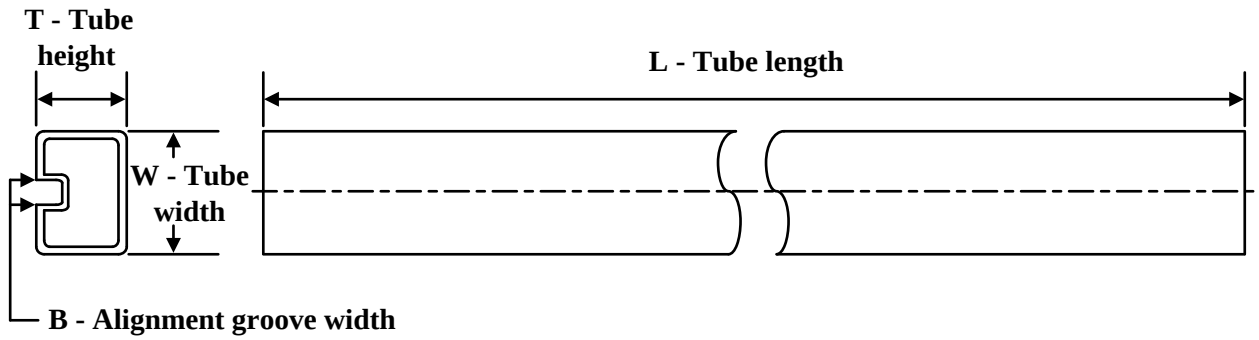
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29330DBTR	TSSOP	DBT	30	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

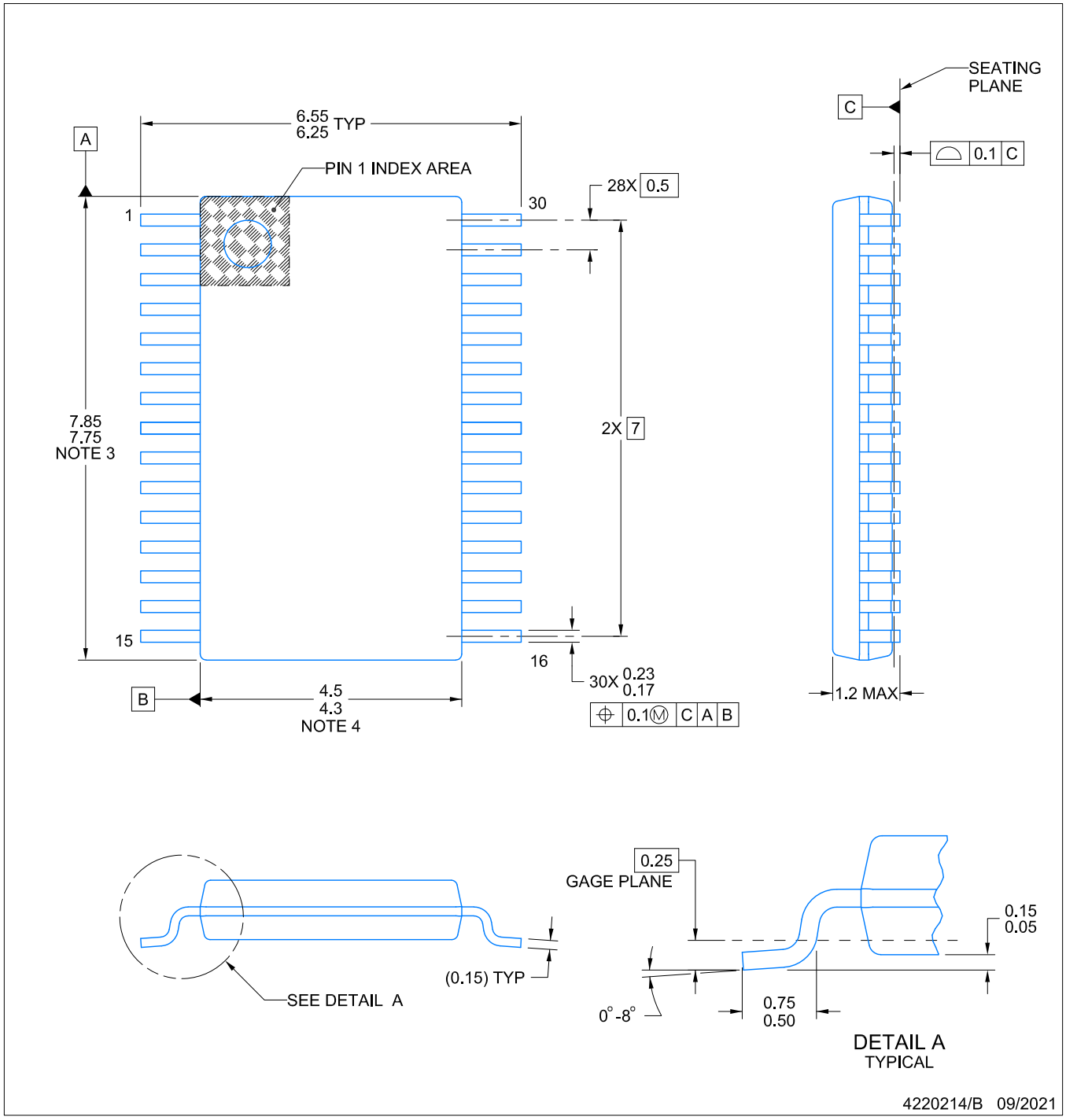
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ29330DBT	DBT	TSSOP	30	60	530	10.2	3600	3.5
BQ29330DBT.A	DBT	TSSOP	30	60	530	10.2	3600	3.5
BQ29330DBTG4	DBT	TSSOP	30	60	530	10.2	3600	3.5

PACKAGE OUTLINE

DBT0030A

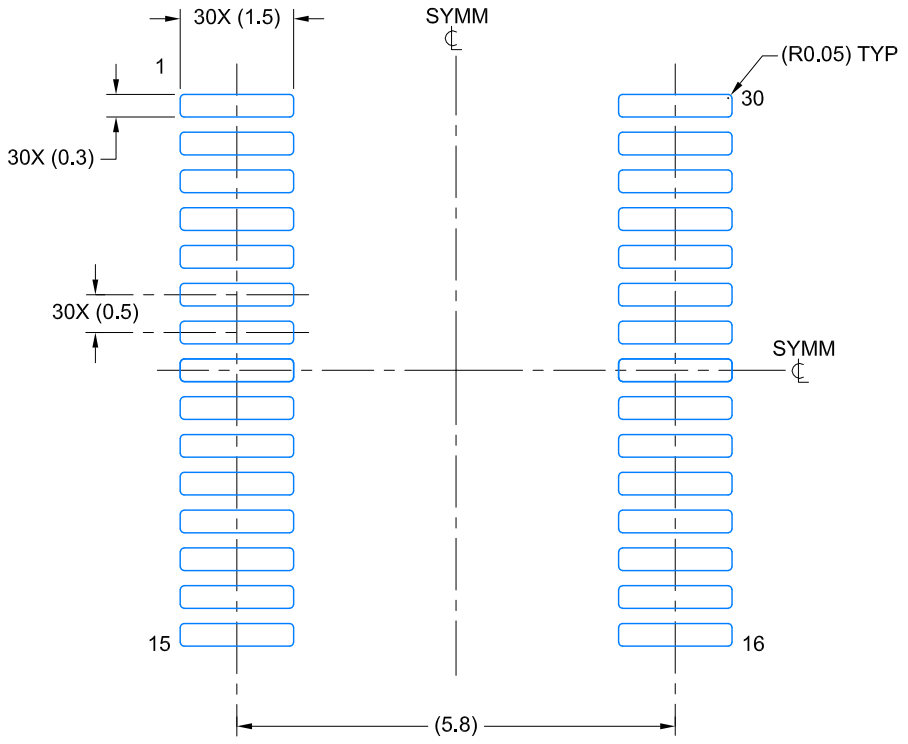
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

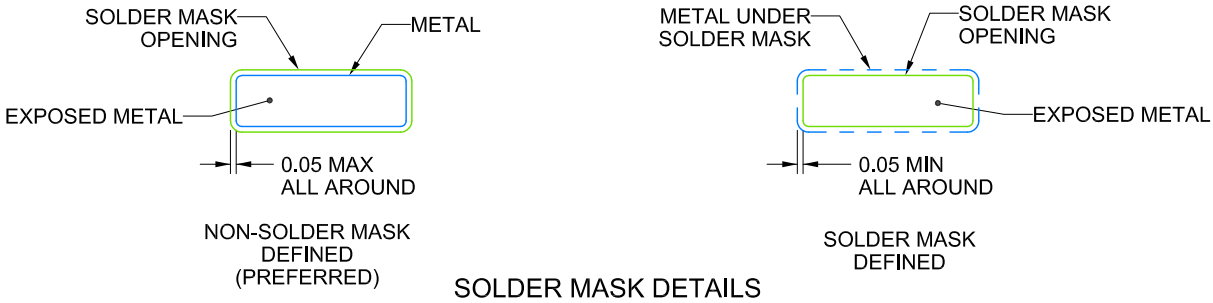


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

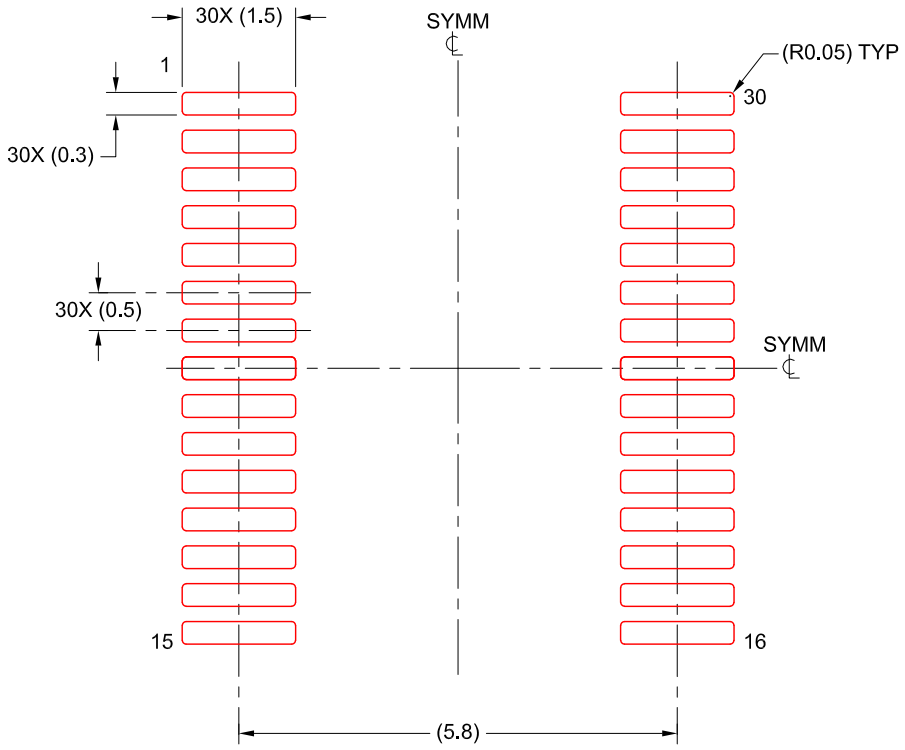


SOLDER MASK DETAILS

4220214/B 09/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220214/B 09/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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