OVERVOLTAGE AND OVERCURRENT PROTECTION IC AND Li+ CHARGER FRONT-END PROTECTION IC

FEATURES

- **Provides Protection for Three Variables:**
  - **Input Overvoltage, with Rapid Response in < 1 µs**
  - **User-Programmable Overcurrent with Current Limiting**
  - **Battery Overvoltage**
- **30V Maximum Input Voltage**
- **Supports up to 1.5A Input Current**
- **Robust Against False Triggering Due to Current Transients**
- **Thermal Shutdown**
- **Enable Input**
- **Status Indication – Fault Condition**

- **5.5V LDO Mode Voltage Regulation**
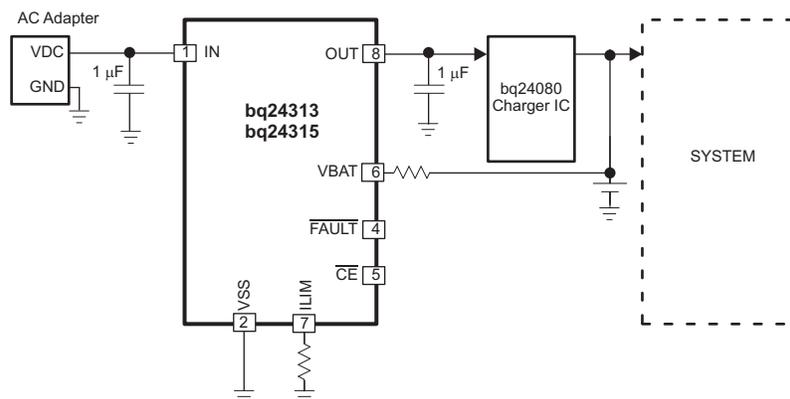- **Available in Space-Saving Small 8 Lead 2mm ×2mm SON**

APPLICATIONS

- **Mobile Phones and Smart Phones**
- **PDAs**
- **MP3 Players**
- **Low-Power Handheld Devices**
- **Bluetooth™ Headsets**

DESCRIPTION

The bq24313 and bq24315 are highly integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current, and the battery voltage. The output acts as a linear regulator. The output is regulated to $V_{O(REG)}$ for inputs between $V_{O(REG)}$ and the overvoltage threshold. If an input overvoltage condition occurs, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable.

The IC can be controlled by a processor and also provides status information about fault conditions to the host.

APPLICATION SCHEMATIC

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION[1]

DEVICE[2]	OVP THRESHOLD	PACKAGE	MARKING
bq24313DSG	10.5V	2mm x 2mm SON	NXQ
bq24315DSG	5.85 V	2mm x 2mm SON	CGM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) To order a 3000 piece reel add R to the part number, or to order a 250 piece reel add T to the part number.

PACKAGE DISSIPATION RATINGS

DESIGNATOR	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$
DSG	2×2 SON	5°C/W	75°C/W

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	PIN	VALUE	UNIT
V_I	Input voltage	IN (with respect to VSS)	−0.3 to 30	V
		OUT (with respect to VSS)	−0.3 to 12	
		ILIM, $\overline{FAULT}$, $\overline{CE}$, VBAT (with respect to VSS)	−0.3 to 7	
I_I	Input current	IN	2	A
I_O	Output current	OUT	2	A
	Output sink current	$\overline{FAULT}$	15	mA
ESD	Withstand Voltage	All (Human Body Model per JESD22-A114-E)	2000	V
		All (Machine Model per JESD22-A115-E)	200	V
		All (Charge Device Model per JESD22-C101-C)	500	V
		IN(IEC 61000-4-2) (with IN bypassed to the VSS with a 1-µF low-ESR ceramic capacitor)	15 (Air Discharge) 8 (Contact)	kV
T_J	Junction temperature		−40 to 150	°C
T_{stg}	Storage temperature		−65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	3.3	30	V
I_{IN}	Input current, IN pin		1.5	A
I_{OUT}	Output current, OUT pin		1.5	A
$R_{(ILIM)}$	OCP Programming resistor	15	90	kΩ
T_J	Junction temperature	−40	125	°C

Product Folder Link(s): *bq24313 bq24315*

ELECTRICAL CHARACTERISTICS

over junction temperature range –40°C to 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IN							
UVLO	Undervoltage lock-out, input power detected threshold	$\overline{CE}$ = Low, V_{IN} increasing from 0V to 3V		2.6	2.7	2.8	V
$V_{hys(UVLO)}$	Hysteresis on UVLO	$\overline{CE}$ = Low, V_{IN} decreasing from 3V to 0V		200	260	300	mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	$\overline{CE}$ = Low. Time measured from V_{IN} 0V → 5V 1µs rise-time, to output turning ON			8		ms
I_{DD}	Operating current	$\overline{CE}$ = Low, No load on OUT pin, V_{IN} = 5V, $R_{(ILIM)}$ = 25kΩ			400	600	µA
I_{STDBY}	Standby current	$\overline{CE}$ = High, V_{IN} = 5V			65	95	µA
INPUT TO OUTPUT CHARACTERISTICS							
V_{DO}	Drop-out voltage IN to OUT	$\overline{CE}$ = Low, V_{IN} = 5V, I_{OUT} = 1A			170	280	mV
OUPUT VOLTAGE REGULATION							
$V_{O(REG)}$	Output voltage	$\overline{CE}$ = Low, V_{IN} = 6.5V, I_{OUT} = 1A	bq24313	5.67	5.85	6.03	V
		$\overline{CE}$ = Low, V_{IN} = 5.7V, I_{OUT} = 1A	bq24315	5.3	5.5	5.7	
INPUT OVERVOLTAGE PROTECTION							
V_{OVP}	Input overvoltage protection threshold	$\overline{CE}$ = Low, V_{IN} increasing from 5V to 11V	bq24313	10.2	10.5	10.8	V
			bq24315	5.71	5.85	6.00	
$t_{PD(OVP)}$	Input OV propagation delay[1]	$\overline{CE}$ = Low			200		ns
$V_{hys(OVP)}$	Hysteresis on OVP	$\overline{CE}$ = Low, V_{IN} decreasing from 11V to 5V	bq24313	60	120	180	mV
			bq24315	20	60	110	
$t_{ON(OVP)}$	Recovery time from input overvoltage condition	$\overline{CE}$ = Low, Time measured from V_{IN} 7.5V → 5V, 1µs fall-time			8		ms
INPUT OVERCURRENT PROTECTION							
I_{OCP}	Input overcurrent protection threshold range			300		1500	mA
I_{OCP}	Input overcurrent protection threshold	$\overline{CE}$ = Low, $R_{(ILIM)}$ = 24.9kΩ, 3 V ≤ V_{IN} < V_{OVP} − $V_{hys(OVP)}$		900	1000	1100	mA
$K_{(ILIM)}$	Adjustable current limit factor				25		A = kΩ
$t_{BLANK(OCP)}$	Blanking time, input overcurrent detected				176		µs
$t_{REC(OCP)}$	Recovery time from input overcurrent condition				64		ms
BATTERY OVERVOLTAGE PROTECTION							
BV_{OVP}	Battery overvoltage protection threshold	$\overline{CE}$ = Low, V_{IN} > 4.4V		4.30	4.35	4.4	V
$V_{hys(Bovp)}$	Hysteresis on BV_{OVP}	$\overline{CE}$ = Low, V_{IN} > 4.4V		200	275	320	mV
$I_{(VBAT)}$	Input bias current on VBAT pin	$V_{(VBAT)}$ = 4.4V, T_J = 25°C				10	nA
$t_{DGL(Bovp)}$	Deglitch time, battery overvoltage detected	$\overline{CE}$ = Low, V_{IN} > 4.4V. Time measured from $V_{(VBAT)}$ rising from 4.1V to 4.4V to $\overline{FAULT}$ going low.			176		µs
THERMAL PROTECTION							
$T_{J(OFF)}$	Thermal shutdown temperature				140	150	°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis				20		°C
LOGIC LEVELS ON $\overline{CE}$							
V_{IL}	Low-level input voltage			0		0.4	V
V_{IH}	High-level input voltage			1.4			V
I_{IL}	Low-level input current	$V_{(/CE)}$ = 0V				1	µA

(1) Not tested in production. Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range –40°C to 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	$V_{(/CE)} = 1.8V$			15	µA
LOGIC LEVELS ON FAULT						
V_{OL}	Output low voltage	$I_{SINK} = 5mA$			0.2	V
I_{lkg}	Leakage current, $\overline{FAULT}$ pin HI-Z	$V_{(/FAULT)} = 5V$			10	µA
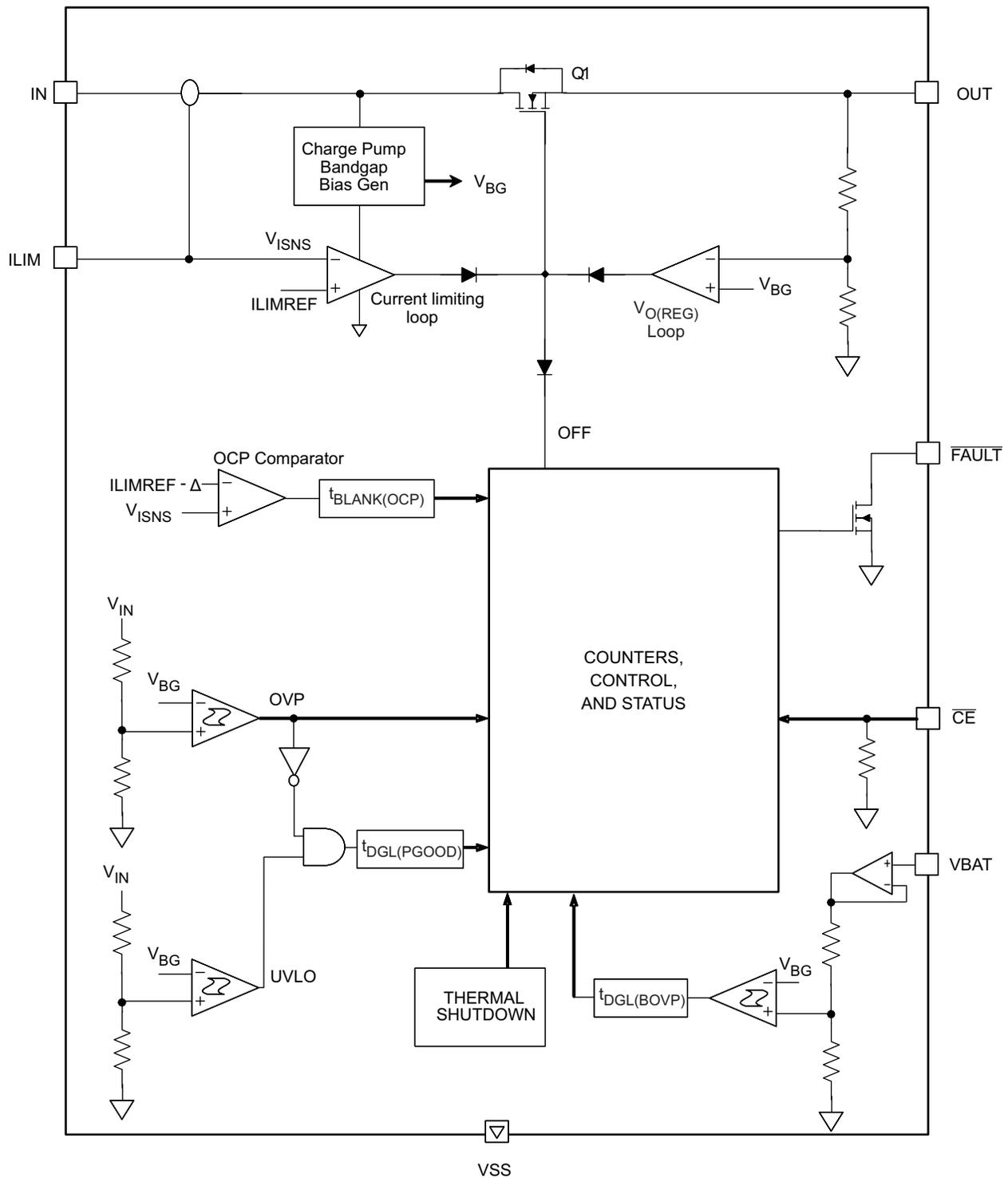
Figure 1. Simplified Block Diagram

bq24313
bq24315

TERMINAL FUNCTIONS

| TERMINAL		I/O	DESCRIPTION
NAME	DSG		
IN	1	I	Input power. Connect IN to the external DC supply. Bypass IN to VSS with a 1µF ceramic capacitor (minimum).
VSS	2	–	Ground terminal
NC	3		This pin may have internal circuits used for test purposes. Do not make any external connection to this pin for normal operation.
$\overline{\text{FAULT}}$	4	O	Open-drain, device status output. $\overline{\text{FAULT}}$ = Low indicates that the input FET Q1 is off due to input overvoltage, input overcurrent, battery overvoltage, or thermal shutdown. $\overline{\text{FAULT}}$ is high impedance during normal operation. Connect a pullup resistor from $\overline{\text{FAULT}}$ to the desired logic level voltage rail.
$\overline{\text{CE}}$	5	I	Chip enable active low input. Connect $\overline{\text{CE}}$ = High to disable the IC and turn the input FET off. Connect $\overline{\text{CE}}$ = low for normal operation. $\overline{\text{CE}}$ is internally pulled down.
VBAT	6	I	Battery voltage sense input. Connect to the battery pack positive terminal through a resistor.
ILIM	7	I/O	Input overcurrent threshold programming. Connect a resistor from ILIM to VSS to set the overcurrent threshold.
OUT	8	O	Output terminal to the charging system. Connect OUT to the external load circuitry. Bypass OUT to VSS with a 1µF ceramic capacitor (minimum).
Thermal PAD		–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. The VSS pin must be connected to ground at all times.

DSG Package
(Top View)

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Product Folder Link(s): *bq24313 bq24315*
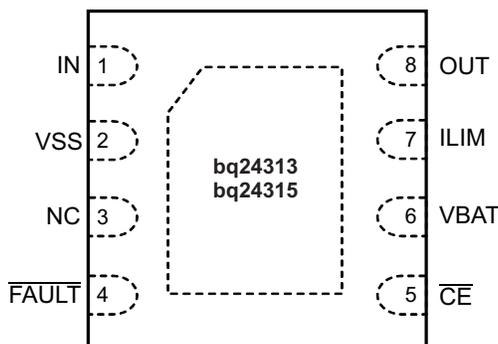
TYPICAL OPERATING PERFORMANCE

Test conditions (unless otherwise noted) for typical operating performance: V_{IN} = 5 V, C_{IN} = 1 μF, C_{OUT} = 1 μF, $R_{(ILIM)}$ = 25 kΩ, R_{BAT} = 100 kΩ, T_A = 25°C, V_{PU} = 3.3V (see Figure 22 for the Typical Application Circuit)

NORMAL POWER-ON SHOWING SOFT-START
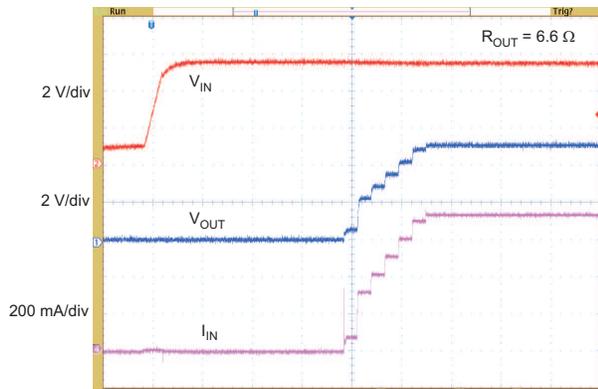
Figure 2.

OVP AT POWER-ON
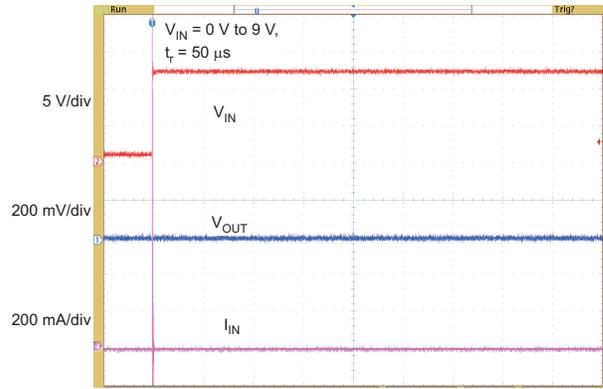
Figure 3.

OVP RESPONSE FOR INPUT STEP
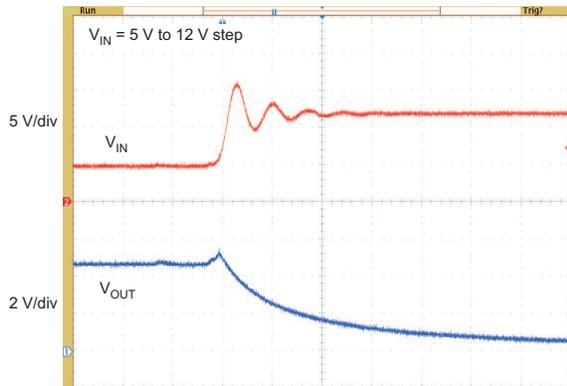
Figure 4.

OVP RESPONSE FOR INPUT STEP
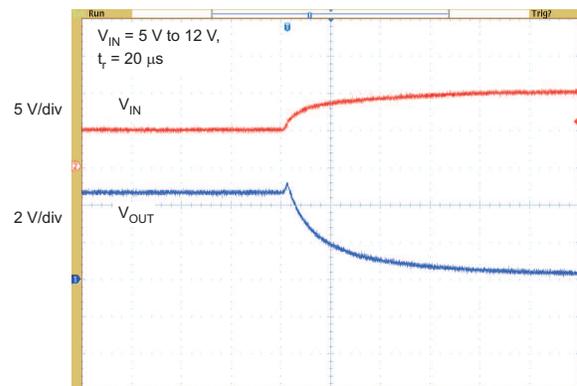
Figure 5.

RECOVERY FROM OVP
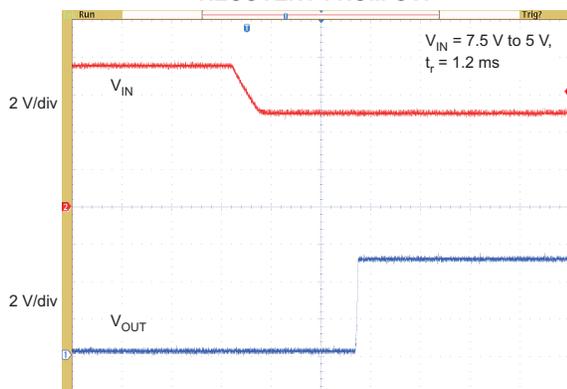
Figure 6.

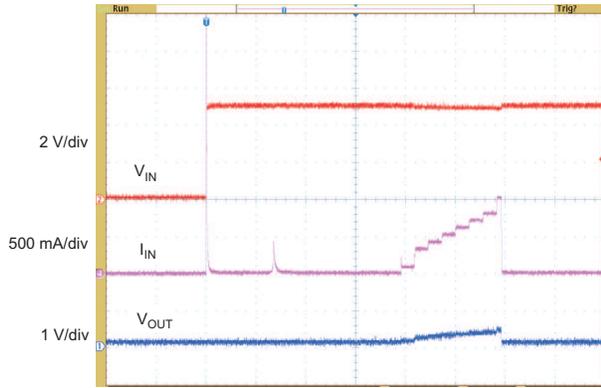**OCP, POWERING UP INTO A SHORT CIRCUIT ON OUT, COUNTER COUNTS TO 15 BEFORE SWITCHING OFF THE DEVICE**

Figure 7.

bq24313
bq24315

TEXAS
INSTRUMENTS
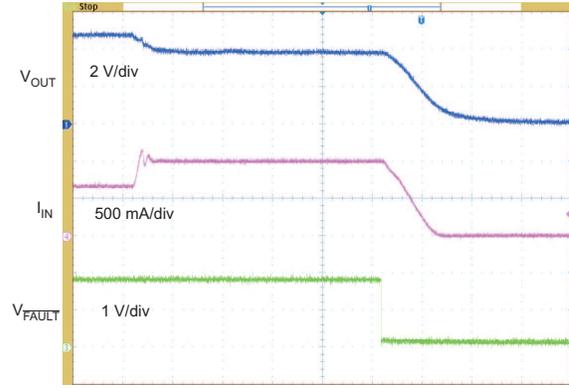
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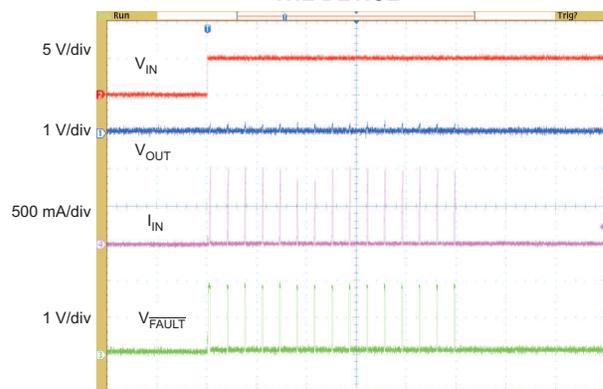
TYPICAL OPERATING PERFORMANCE (continued)

OCP, ZOOM-IN ON THE FIRST CYCLE OF FIGURE 7

Figure 8.

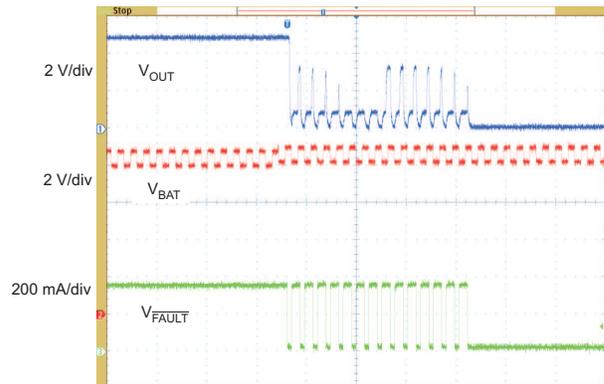**R$_{OUT}$ SWITCHES FROM 6.6Ω TO 3.3Ω,SHOWS CURRENT LIMITING AND SOFT-STOP**

Figure 9.

BAT-OVP, V$_{(VBAT)}$ STEPS FROM 4 V TO 4.5 V,SHOWS t$_{DGL(BAT-OVP)}$ AND SOFT STOP
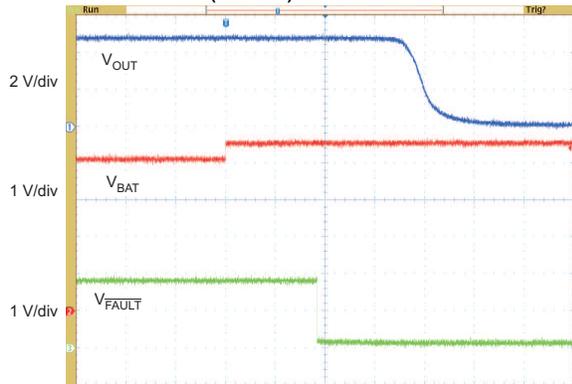
Figure 10.

BAT-OVP, V$_{(VBAT)}$ CYCLES BETWEEN 4 V AND 4.5 V,SHOWS BAT-OVP COUNTER

Figure 11.
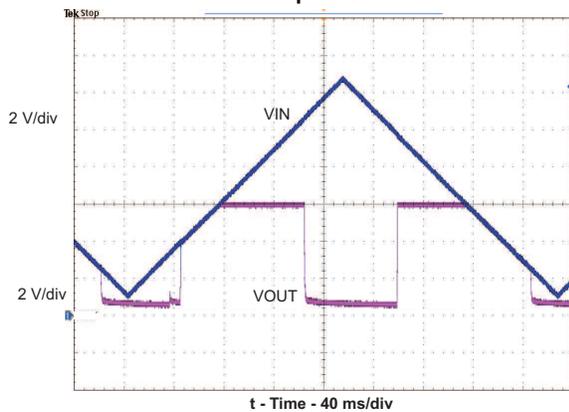
INPUT VOLTAGE RAMP-UP / RAMP-DOWN bq24313

Figure 12.

UNDERVOLTAGE LOCKOUT vs FREE-AIR TEMPERATURE
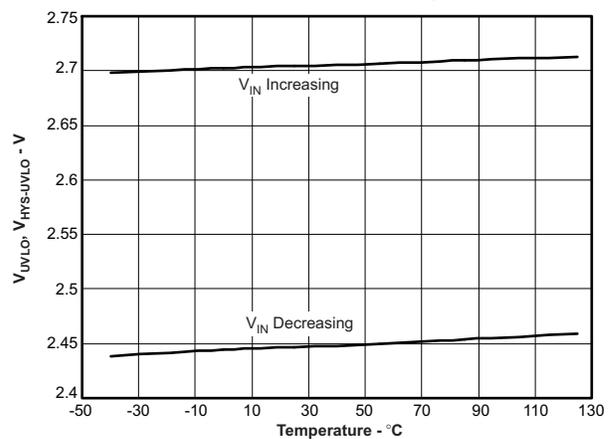

Figure 13.

TYPICAL OPERATING PERFORMANCE (continued)
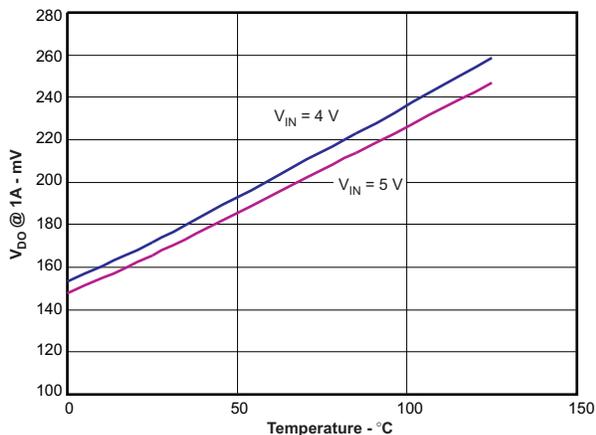
DROPOUT VOLTAGE (IN to OUT)
vs
FREE-AIR TEMPERATURE

Figure 14.

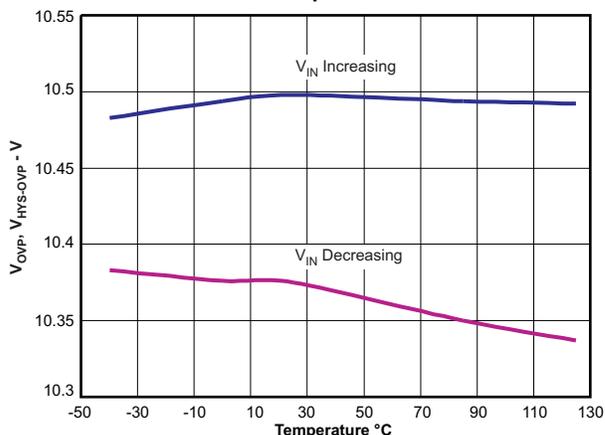**OVERVOLTAGE PROTECTION THRESHOLD**
vs
FREE-AIR TEMPERATURE
bq24313

Figure 15.

OVERVOLTAGE THRESHOLD PROTECTION
vs
FREE-AIR TEMPERATURE
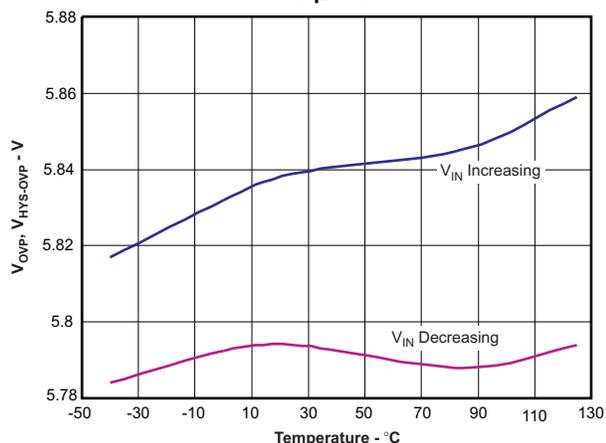**bq24315**

Figure 16.

INPUT OVERCURRENT PROTECTION
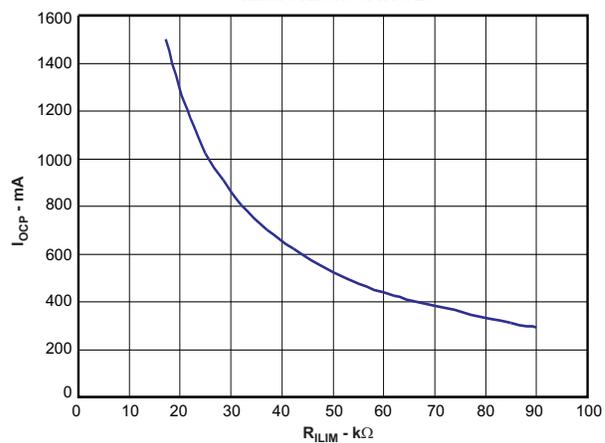**vs**
ILIM RESISTANCE

Figure 17.

TYPICAL OPERATING PERFORMANCE (continued)

**INPUT OVERCURRENT PROTECTION
vs
FREE-AIR TEMPERATURE**

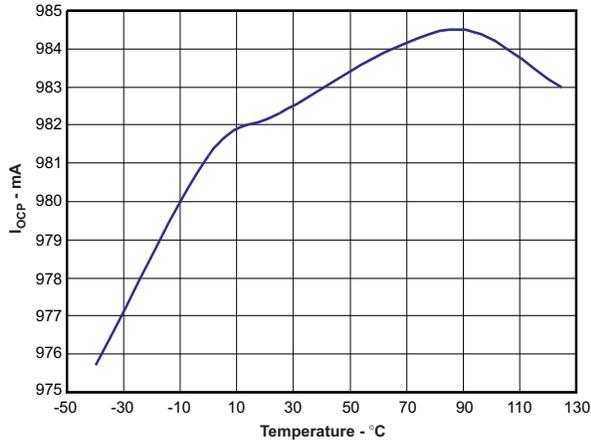Figure 18.

**BATTERY OVERVOLTAGE PROTECTION
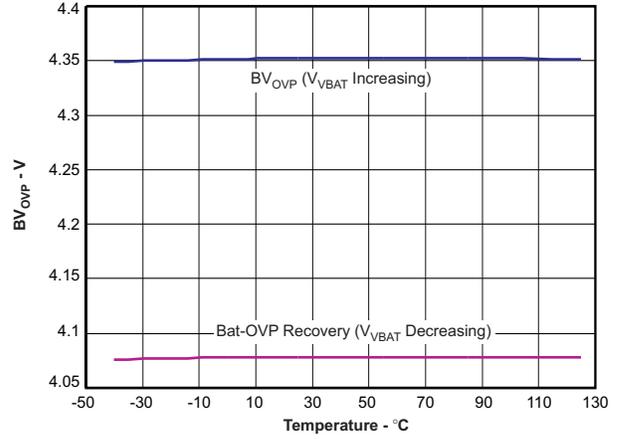vs
FREE-AIR TEMPERATURE**

Figure 19.

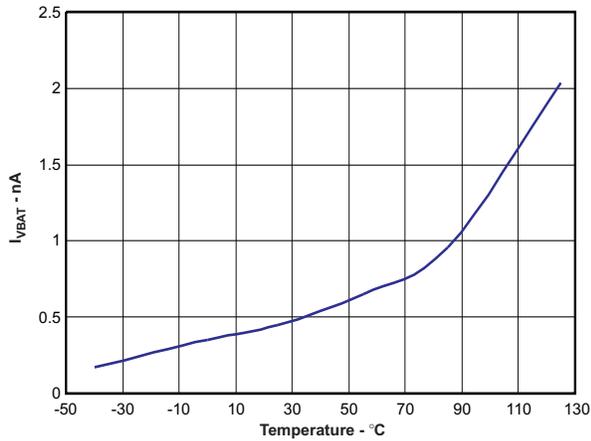**LEAKAGE CURRENT (VBAT Pin)
vs
FREE-AIR TEMPERATURE**

Figure 20.
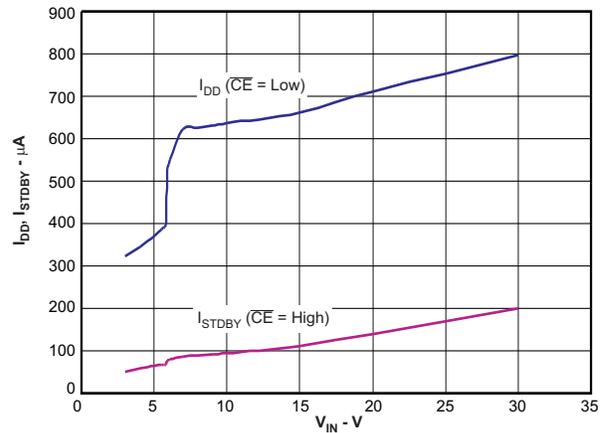
**SUPPLY CURRENT
vs
INPUT VOLTAGE**

Figure 21.

Product Folder Link(s): *bq24313 bq24315*
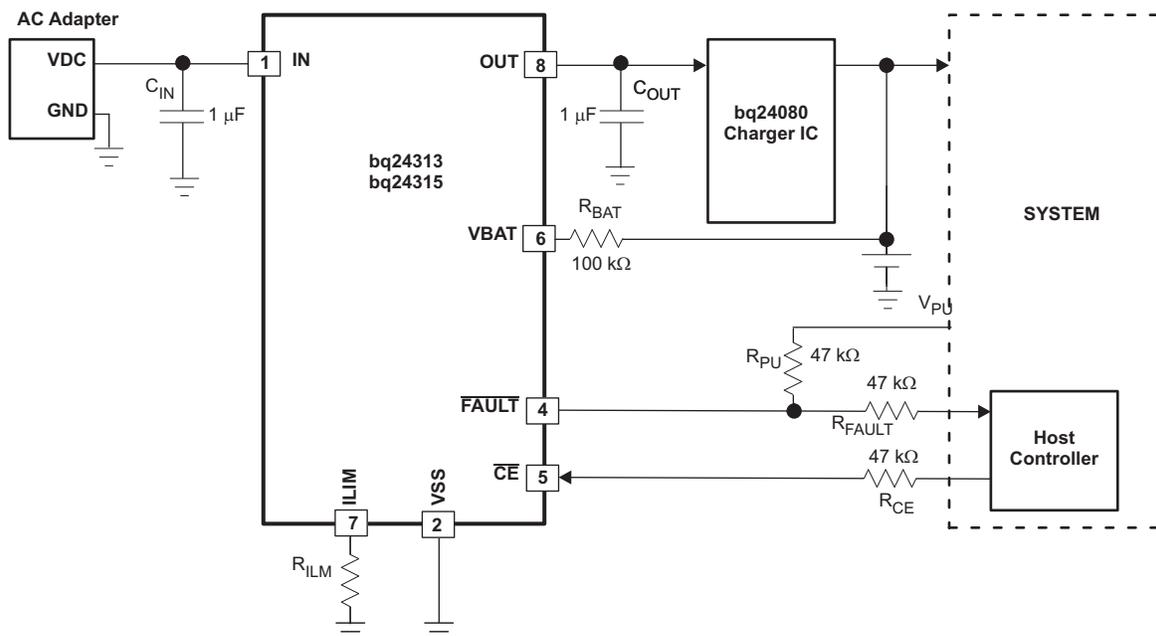
TYPICAL APPLICATION CIRCUIT

$V_{OVP} = 5.85V$, $I_{OCP} = 1000mA$, $BV_{OVP} = 4.35V$

Figure 22.

DETAILED FUNCTIONAL DESCRIPTION

The bq24313 and bq24315 are integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current and the battery voltage. For an input overvoltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. For an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. If the battery voltage rises to an unsafe level, the IC disconnects power from the charging circuit until the battery voltage returns to an acceptable value. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable. The IC can be controlled by a processor, and also provides status information about fault conditions to the host.

POWER DOWN

The device remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold UVLO. The FET Q1 connected between IN and OUT pins is off, and the status output, $\overline{FAULT}$, is set to Hi-Z.

POWER-ON RESET

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset. The IC then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are safe, FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, instead it will go into protection mode and indicate a fault on the $\overline{FAULT}$ pin.

OPERATION

The device continuously monitors the input voltage, the input current, and the battery voltage as described in detail in the following sections.

Input Overvoltage Protection

While the input voltage is less than $V_{O(REG)}$, the output voltage tracks the input voltage (less the drop due to the $R_{DS(on)}$ of Q1). When the input voltage is between $V_{O(REG)}$ and V_{OVP}, the device functions as a linear regulator and regulates the output voltage to 5.5V. If the input voltage rises above V_{OVP}, the internal FET Q1 is turned off, removing power to the output. The response is rapid, with the FET turning off in less than a microsecond. The $\overline{FAULT}$ pin is driven low. When the input voltage returns below $V_{OVP} − V_{hys(OVP)}$ (but is still above UVLO), the FET Q1 is turned on again after a deglitch time of $t_{ON(OVP)}$ to ensure that the input supply has stabilized.

Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor $R_{(ILIM)}$ connected from the ILIM pin to VSS. Figure 17 shows the OCP threshold as a function of $R_{(ILIM)}$, and may be approximated by the following equation: $I_{OCP} = 25 \div R_{(ILIM)}$ (current in A, resistance in kΩ)

If the load current tries to exceed the I_{OCP} threshold, the device limits the current for a blanking duration of $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate. However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, the FET Q1 is turned off for a duration of $t_{REC(OCP)}$, and the $\overline{FAULT}$ pin is driven low. The FET is then turned on again after $t_{REC(OCP)}$ and the current is monitored all over again. Each time an OCP fault occurs, an internal counter is incremented. If 15 OCP faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{CE}$ pin.

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly, resulting in a "soft-stop".

Battery Overvoltage Protection

The battery overvoltage threshold BV_{OVP} is internally set to 4.35V. If the battery voltage exceeds the BV_{OVP} threshold, the FET Q1 is turned off, and the $\overline{FAULT}$ pin is driven low. The FET is turned back on once the battery voltage drops to $BV_{OVP} − V_{hys(Bovp)}$. Each time a battery overvoltage fault occurs, an internal counter is incremented. If 15 such faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{CE}$ pin. For a battery overvoltage fault, Q1 is gradually switched OFF.

Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET Q1 is turned off, and the $\overline{FAULT}$ pin is driven low. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} − T_{J(OFF-HYS)}$.

Enable Function

The IC has an enable pin which can be used to enable or disable the device. When the $\overline{CE}$ pin is driven high, the internal FET is turned off. When the $\overline{CE}$ pin is low, the FET is turned on if other conditions are safe. The OCP counter and the Bat-OVP counter are both reset when the device is disabled and re-enabled. The $\overline{CE}$ pin has an internal pulldown resistor and can be left floating. Note that the $\overline{FAULT}$ pin functionality is also disabled when the $\overline{CE}$ pin is high.

Fault Indication

The $\overline{FAULT}$ pin is an active-low open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting $\overline{CE}$ high. With $\overline{CE}$ low, the $\overline{FAULT}$ pin goes low whenever any of these events occurs:

• Input overvoltage
• Input overcurrent
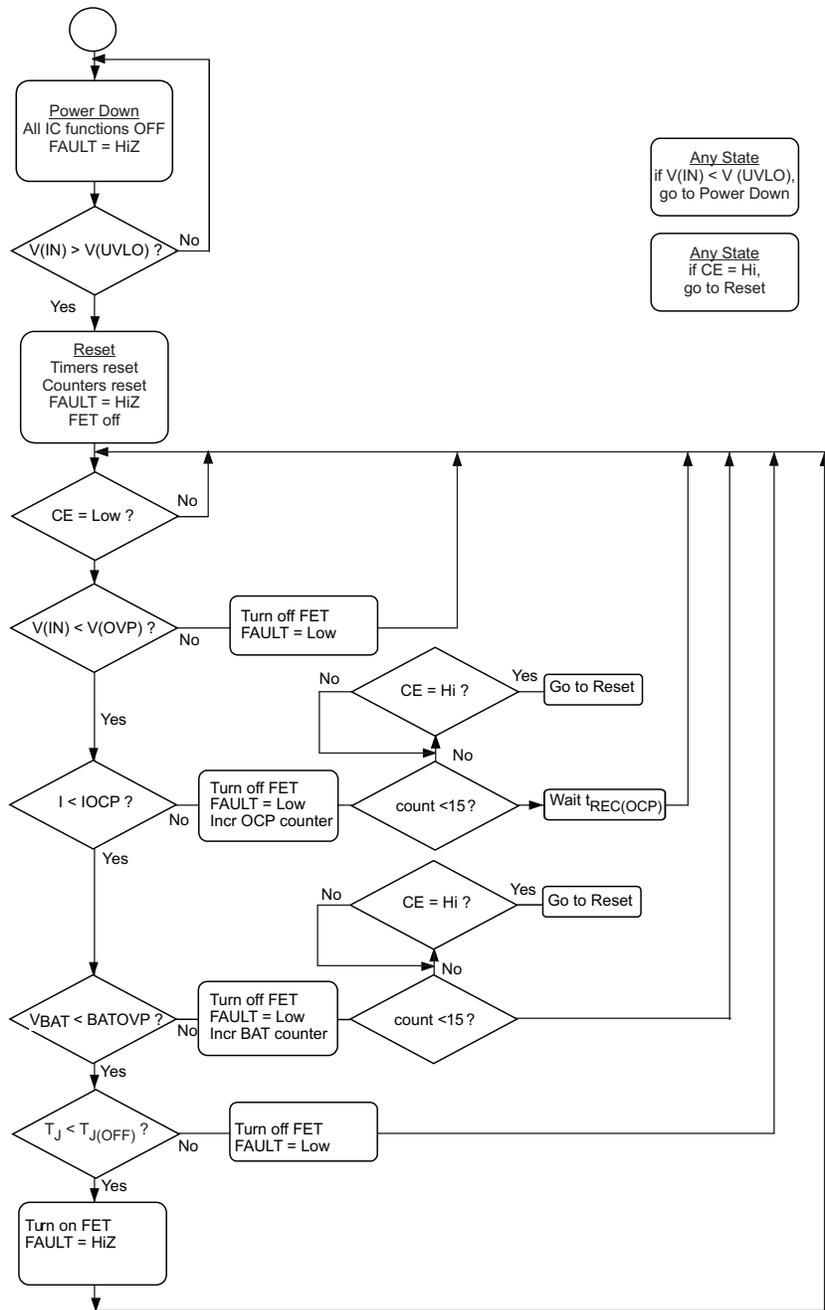• Battery overvoltage
• IC Overtemperature

Figure 23. Flow Diagram

APPLICATION INFORMATION (WITH REFERENCE TO FIGURE 22)

Selection of R_{BAT}

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the bq24315 can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of a failure of the IC. In the interests of safety, R_{BAT} should have a high value. The problem with a large R_{BAT} is that the voltage drop across this resistor, due to the VBAT bias current $I_{(VBAT)}$, causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35V BV_{OVP} threshold.

Choosing R_{BAT} in the range 100kΩ to 470kΩ is a good compromise. In the event of an IC failure, with R_{BAT} equal to 100kΩ, the maximum current flowing into the battery would be (30V − 3V) ÷ 100kΩ = 246μA, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100kΩ results in a worst-case voltage drop of $R_{BAT} \times I_{(VBAT)}$ = 1mV. This is negligible to compared to the internal tolerance of 50mV on BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

Selection of R_{CE}, R_{FAULT}, and R_{PU}

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the $\overline{CE}$ pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor should be greater than V_{IH} of the bq24315 $\overline{CE}$ pin. The drop across the resistor is given by $R_{CE} \times I_{IH}$.

The $\overline{FAULT}$ pin is an open-drain output that goes low during OV, OC, battery-OV, and OT events. If the application does not require monitoring of the $\overline{FAULT}$ pin, it can be left unconnected. But if the $\overline{FAULT}$ pin has to be monitored, it should be pulled high externally through R_{PU}, and connected to the host through R_{FAULT}. R_{FAULT} prevents damage to the host controller if the bq24315 fails (see above). The resistors should be of high value, in practice values between 22kΩ and 100kΩ should be sufficient.

Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 22 is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is recommended that a ceramic capacitor of at least 1μF be used at the input of the device. It should be located in close proximity to the IN pin.

C_{OUT} in Figure 22 is also important: If a fast (< 1μs rise time) overvoltage transient occurs at the input, the current that charges C_{OUT} causes the device's current-limiting loop to start, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. C_{OUT} should also be a ceramic capacitor of at least 1μF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

Powering Accessories

In some applications, the equipment that the protection IC resides in may be required to provide power to an accessory (e.g. a cellphone may power a headset or an external memory card) through the same connector pins that are used by the adapter for charging. Figure 24 and Figure 25 illustrate typical charging and accessory-powering scenarios:
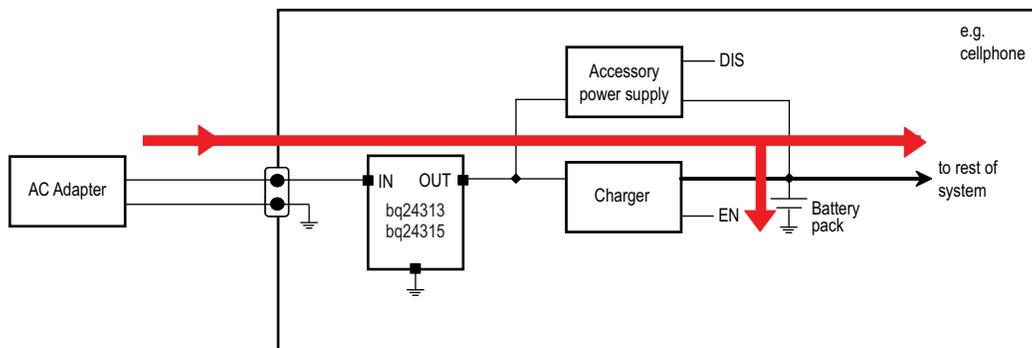
Figure 24. Charging - The Red Arrows Show the Direction of Current Flow
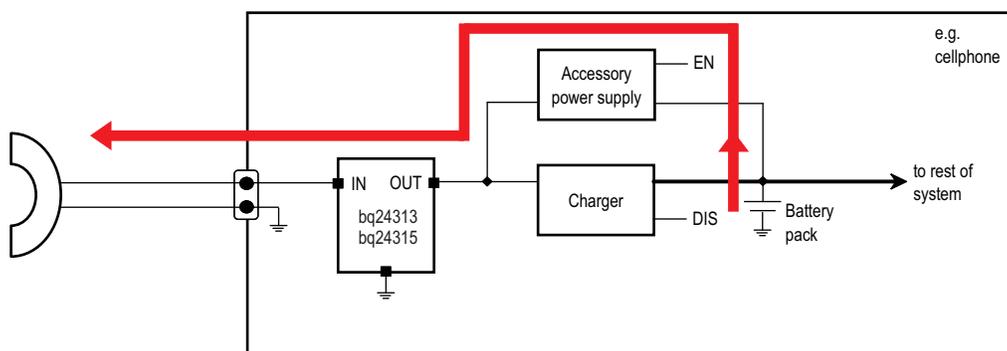

Figure 25. Powering an Accessory - The Red Arrows Show the Direction of Current Flow

In the second case, when power is being delivered to an accessory, the bq24313/bq24315 device is required to support current flow from the OUT pin to the IN pin.

If V_{OUT} > UVLO + 0.7V, FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1. Q1 remains ON as long as V_{OUT} > UVLO − $V_{hys(UVLO)}$ + $R_{DS(on)}$ × $I_{(ACCESSORY)}$. Within this voltage range, the reverse current capability is the same as the forward capability, 1.5A. It should be noted that there is no overcurrent protection in this direction.

PCB Layout Guidelines:

- This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for high voltages.
- The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.
- C_{IN} and C_{OUT} should be located close to the IC. Other components like $R_{(ILIM)}$ and R_{BAT} should also be located close to the IC.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24313DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	NXQ
BQ24313DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXQ
BQ24313DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXQ
BQ24313DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	NXQ
BQ24313DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXQ
BQ24313DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXQ
BQ24315DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	CGM
BQ24315DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGM
BQ24315DSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGM
BQ24315DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGM
BQ24315DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGM
BQ24315DSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGM
BQ24315DSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	CGM
BQ24315DSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGM
BQ24315DSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CGM

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24313DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24313DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24315DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24315DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24315DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24313DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ24313DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ24315DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ24315DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
BQ24315DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG 8

2 x 2, 0.5 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224783/A

A · 2.1 / 1.9 · B

PIN 1 INDEX AREA

2.1 / 1.9

0.32 / 0.18

0.4 / 0.2
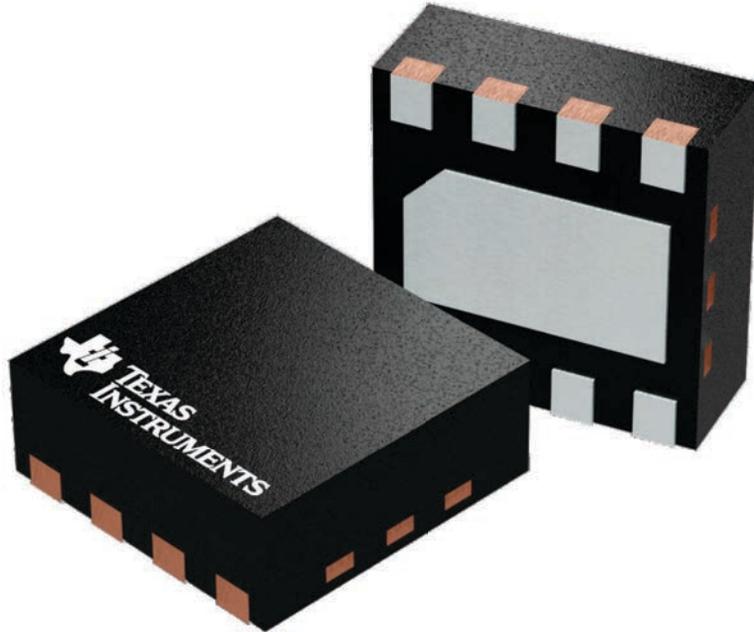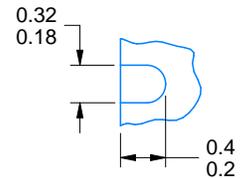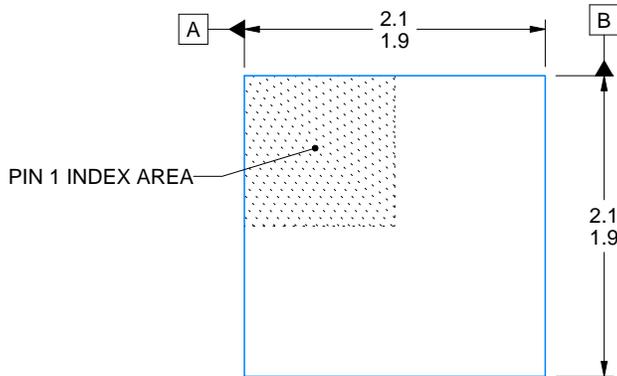
ALTERNATIVE TERMINAL SHAPE
TYPICAL

0.8 / 0.7

C

SEATING PLANE

0.05 / 0.00

⌒ | 0.08 | C
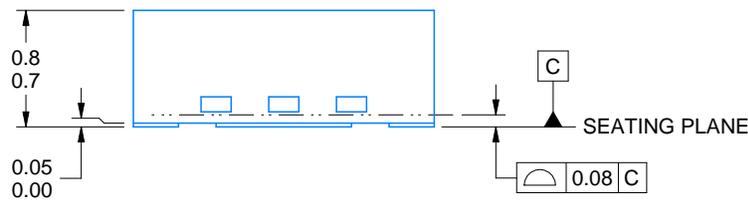
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

EXPOSED THERMAL PAD

0.9 ± 0.1

4   5

6X 0.5

2X 1.5

9

1.6 ± 0.1

(DIM A) TYP

1   8

PIN 1 ID
(45° X 0.25)

8X 0.4 / 0.2

8X 0.32 / 0.18

⊕	0.1 Ⓜ	C	A	B
	0.05 Ⓜ	C		
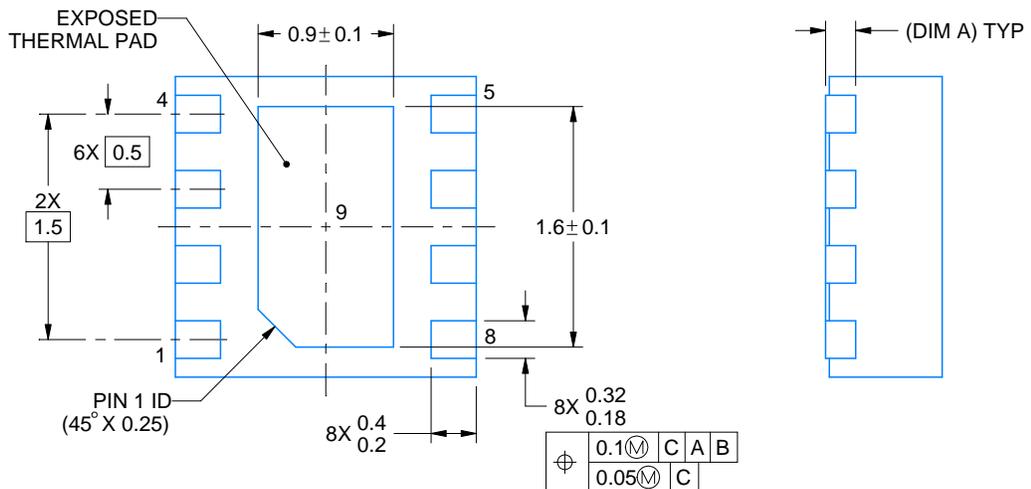
4218900/E   08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

8X (0.5)

(0.9)

(⌀ 0.2) VIA
TYP

1

8

8X (0.25)

SYMM
℄

9

(0.55)

(1.6)

6X (0.5)

4

5

(R0.05) TYP

SYMM
℄

(1.9)
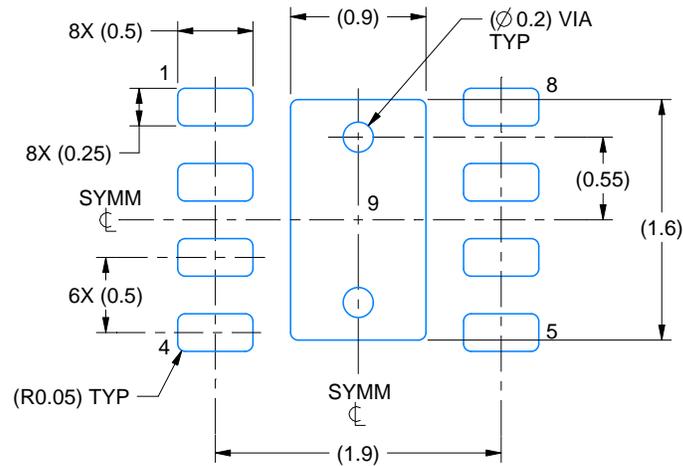
LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
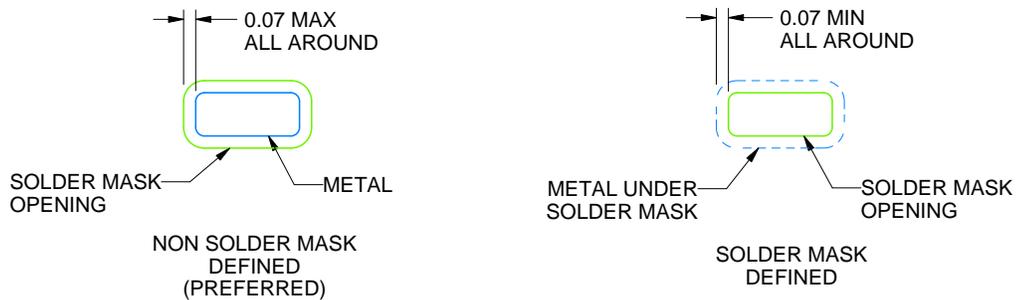
SOLDER MASK DETAILS

4218900/E   08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

8X (0.5)

1

8X (0.25)

SYMM
℄

SYMM ℄

METAL

8

(0.45)

9

6X (0.5)

4

(R0.05) TYP

(0.9)

(0.7)

5

(1.9)
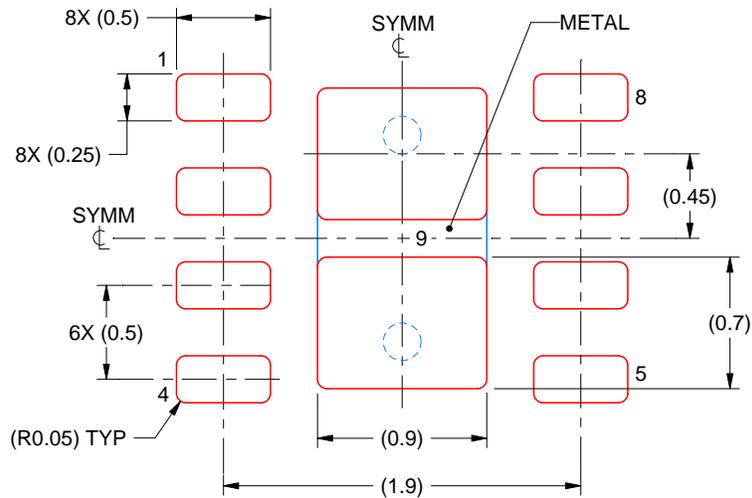
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E   08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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