

### DESCRIPTION

The MP5611 is a triple-output converter across a 2.9 to 5.2V input voltage ( $V_{IN}$ ) range designed for small-size AMOLED (active matrix organic light-emitting diode) display power supplies.

The MP5611 integrates a boost converter for ELVDD, an inverting buck-boost (IBB) converter for ELVSS, and another boost converter for AVDD. The one wire digital control pin (CTRL) can program the ELVSS, ELVDD, and AVDD voltages following digital protocol.

The MP5611 supports an independent start-up sequence for AVDD and ELVDD via the separated enable pins (EN\_AVDD and CTRL). It also integrates an optional fast discharge function after the IC has been disabled.

The device features rich protections, including  $V_{IN}$  under-voltage lockout (UVLO), cycle-by-cycle current limit protection, thermal shutdown protection, short output protection, and over-current protection (OCP) for AVDD and ELVDD.

The fully integrated synchronous rectification solution with low on resistance improves total system efficiency, minimizes external components, and reduces PCB layout size.

The MP5611 is available in a TQFN-16 (3mmx3mm) package.

### FEATURES

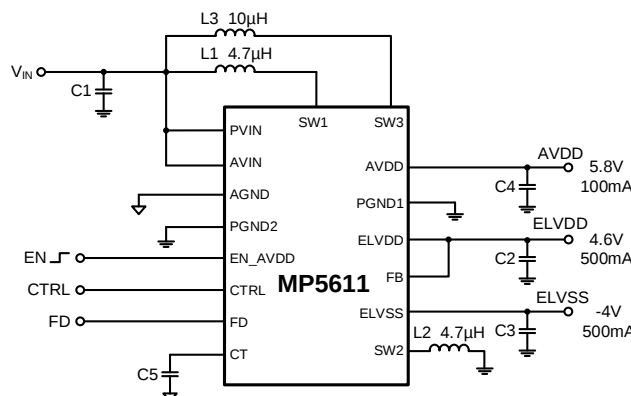
- 2.9 to 5.2V Input Voltage ( $V_{IN}$ ) Range
- Triple Output AVDD, ELVDD, ELVSS
- High Accuracy for Output Voltage ( $V_{OUT}$ )
- Good Line and Load Regulation
- Configurable  $V_{ELVDD}$  = 4.6V to 5.2V, Default 4.6V
- Configurable  $V_{ELVSS}$  = -1.4V to -6.4V, Default -4V
- 500mA Output Current ( $I_{OUT}$ ) for ELVDD and ELVSS
- Configurable  $V_{AVDD}$  = 5V to 7.7V, Default 5.8V
- 100mA  $I_{OUT}$  for AVDD
- Respective Enable for AVDD and ELVDD
- Soft Start (SS)
- Active Fast Discharge Function
- Cycle-by-Cycle Current Limit Protection
- AVDD Output Over-Current Protection (OCP) 90mA to 270mA
- ELVDD Output OCP 80mA to 650mA
- Output Short-to-GND Protection
- Over-Temperature Protection (OTP)
- Available in a TQFN-16 (3mmx3mm) Package

### APPLICATIONS

- AMOLED Smartphones
- AMOLED Displays

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### TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package           | Top Marking | MSL Rating |
|--------------|-------------------|-------------|------------|
| MP5611GQT    | TQFN-16 (3mmx3mm) | See Below   | 1          |

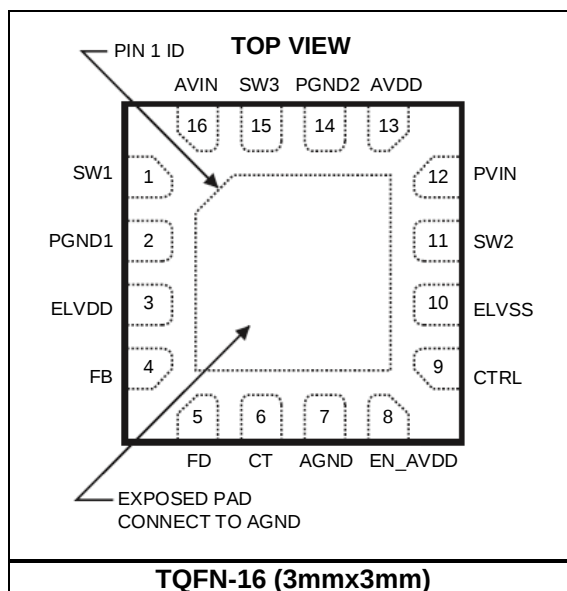
\* For Tape & Reel, add suffix -Z (e.g. MP5611GQT-Z).

## TOP MARKING

**BKHY**  
**LLL**

BKH: Product code  
Y: Year code  
LLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin #       | Name    | Description                                                                                     |
|-------------|---------|-------------------------------------------------------------------------------------------------|
| 1           | SW1     | Switching node of the ELVDD boost converter.                                                    |
| 2           | PGND1   | Power ground of the ELVDD boost converter.                                                      |
| 3           | ELVDD   | Output of the ELVDD boost converter.                                                            |
| 4           | FB      | Feedback. ELVDD output voltage ( $V_{OUT}$ ) sense pin.                                         |
| 5           | FD      | Fast discharge enable and disable during shutdown. Pull this pin high to enable fast discharge. |
| 6           | CT      | ELVSS transition time configured pin.                                                           |
| 7           | AGND    | Analog ground.                                                                                  |
| 8           | EN_AVDD | AVDD boost converter enable pin. Pull this pin high to enable the AVDD converter.               |
| 9           | CTRL    | Digital control. This pin also enables the ELVDD and ELVSS converter.                           |
| 10          | ELVSS   | Output of the ELVSS inverting buck-boost (IBB) converter.                                       |
| 11          | SW2     | Switching node of the ELVSS IBB converter.                                                      |
| 12          | PVIN    | Power supply of the ELVSS IBB converter.                                                        |
| 13          | AVDD    | Output of the AVDD boost converter.                                                             |
| 14          | PGND2   | Power ground of the AVDD boost converter.                                                       |
| 15          | SW3     | Switching node of the AVDD boost converter.                                                     |
| 16          | AVIN    | Power supply for internal circuit.                                                              |
| Exposed pad |         | Exposed pad. Connect this pin to AGND.                                                          |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                          |                 |
|--------------------------------------------------------------------------|-----------------|
| $V_{IN}$ , SW1 .....                                                     | -0.3V to +5.3V  |
| SW3, AVDD .....                                                          | -0.3V to +10V   |
| ELVSS .....                                                              | -7.5V to +0.3V  |
| SW2 .....                                                                | -7.5V to +5.3V  |
| All other pins .....                                                     | -0.3V to +5.3V  |
| Junction temperature .....                                               | 150°C           |
| Lead temperature .....                                                   | 260°C           |
| Storage temperature .....                                                | -65°C to +150°C |
| Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup> |                 |
| TQFN-16 (3mmx3mm) .....                                                  | 2.1W            |

## ESD Ratings

|                                  |                    |
|----------------------------------|--------------------|
| Human body model (HBM) .....     | $\pm 1.5\text{kV}$ |
| Charged device model (CDM) ..... | $\pm 2\text{kV}$   |

## Recommended Operating Conditions <sup>(3)</sup>

|                                        |                 |
|----------------------------------------|-----------------|
| Supply voltage ( $V_{IN}$ ) .....      | 2.9V to 5.2V    |
| Operating junction temp ( $T_J$ ) .... | -40°C to +125°C |

|                                          |                                 |                                 |
|------------------------------------------|---------------------------------|---------------------------------|
| <b>Thermal Resistance <sup>(4)</sup></b> | <b><math>\theta_{JA}</math></b> | <b><math>\theta_{JC}</math></b> |
| TQFN-16 (3mmx3mm) .....                  | 60                              | 12                              |

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) –  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 3.7V$ ,  $V_{ELVDD}/ELVSS/AVDD = \text{default}$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.

| Parameter                                                  | Symbol                   | Condition                                                 | Min  | Typ                | Max  | Units |
|------------------------------------------------------------|--------------------------|-----------------------------------------------------------|------|--------------------|------|-------|
| General                                                    |                          |                                                           |      |                    |      |       |
| Operating input voltage                                    | V <sub>IN</sub>          |                                                           | 2.9  |                    | 5.2  | V     |
| Shutdown current                                           | I <sub>SD</sub>          | EN_AVDD = CTRL = 0V                                       |      | 0.1                |      | μA    |
| Quiescent supply current                                   | I <sub>Q</sub>           | V <sub>IN</sub> = 3.7V, ELVDD switching                   |      | 1.6                | 3    | mA    |
| Input under-voltage lockout (UVLO) threshold               | V <sub>IN_UVLO</sub>     | Rising edge                                               |      |                    | 2.65 | V     |
| Input UVLO hysteresis                                      |                          |                                                           |      | 300                |      | mV    |
| EN_AVDD/FD high voltage                                    | V <sub>EN_HIGH</sub>     | Rising V <sub>EN</sub>                                    | 1.35 |                    |      | V     |
| EN_AVDD/FD low voltage                                     | V <sub>EN_LOW</sub>      | Falling V <sub>EN</sub>                                   |      |                    | 0.4  | V     |
| EN_AVDD pull-down resistor                                 | R <sub>DOWN</sub>        |                                                           |      | 500                |      | kΩ    |
| Over-temperature protection (OTP) threshold <sup>(5)</sup> | T <sub>SD</sub>          |                                                           |      | 150                |      | °C    |
| Thermal protection hysteresis <sup>(5)</sup>               |                          |                                                           |      | 25                 |      | °C    |
| Boost Converter ELVDD                                      |                          |                                                           |      |                    |      |       |
| ELVDD voltage                                              | V <sub>ELVDD</sub>       |                                                           |      | 4.6                |      | V     |
| ELVDD voltage variation                                    |                          | T <sub>A</sub> = 25°C, no load                            | -0.5 |                    | +0.5 | %     |
|                                                            |                          | -40°C to +85°C, no load                                   | -0.8 |                    | +0.8 | %     |
| Low-side MOSFET (LS-FET) on resistance                     | R <sub>ON_LS_ELVDD</sub> | I <sub>SW1</sub> = 200mA                                  |      | 160                |      | mΩ    |
| High-side MOSFET (HS-FET) on resistance                    | R <sub>ON_HS_ELVDD</sub> | I <sub>SW1</sub> = 200mA                                  |      | 320                |      | mΩ    |
| Switching frequency                                        | f <sub>SW1</sub>         |                                                           |      | 1.35               |      | MHz   |
| Current limit                                              | I <sub>LIMIT1</sub>      |                                                           |      | 1.5                |      | A     |
| Output over-current protection (OCP) threshold             | I <sub>OCP_ELVDD</sub>   | I <sub>OCP_ELVDD</sub> = 650mA                            |      | 650                |      | mA    |
| Short protection threshold                                 |                          | During operation                                          |      | 80                 |      | %     |
| Short protection detection time                            |                          | During operation                                          |      | 1                  |      | ms    |
| ELVDD sense threshold                                      | V <sub>TELVDD</sub>      | Increasing ELVDD-FB                                       |      | 350                |      | mV    |
| Feedback (FB) sense threshold                              | V <sub>TFB</sub>         | Decreasing ELVDD-FB                                       |      | 250                |      | mV    |
| ELVDD/FB leakage current                                   | I <sub>LEAKAGE</sub>     | CTRL = FD = 0V                                            |      |                    | 5    | μA    |
| FB pull-down resistor                                      | R <sub>DOWN_FB</sub>     |                                                           |      | 4                  |      | MΩ    |
| Active discharge resistance                                | R <sub>DS_ELVDD</sub>    | CTRL = 0V, I <sub>ELVDD</sub> = 1mA                       |      | 75                 |      | Ω     |
| Load regulation <sup>(5)</sup>                             |                          | 1mA < I <sub>ELVDD</sub> < 300mA                          |      | 0.2                |      | %/A   |
| Line regulation <sup>(5)</sup>                             |                          | 2.9V < V <sub>IN</sub> < 4.3V, I <sub>ELVDD</sub> = 200mA |      | 0.015              |      | %V    |
|                                                            |                          | 2.9V < V <sub>IN</sub> < 5.2V, I <sub>ELVDD</sub> = 200mA |      | 1.5 <sup>(6)</sup> |      |       |

# ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 3.7V$ ,  $V_{ELVDD/ELVSS/AVDD} = \text{default}$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.

| Parameter                                        | Symbol                    | Condition                                                                                  | Min  | Typ                 | Max  | Units |
|--------------------------------------------------|---------------------------|--------------------------------------------------------------------------------------------|------|---------------------|------|-------|
| Buck-Boost Converter ELVSS                       |                           |                                                                                            |      |                     |      |       |
| ELVSS default output voltage (V <sub>OUT</sub> ) | V <sub>ELVSS</sub>        |                                                                                            |      | -4                  |      | V     |
| ELVSS V <sub>OUT</sub> range                     |                           |                                                                                            | -6.4 |                     | -1.4 | V     |
| ELVSS regulation                                 |                           | T <sub>A</sub> = 25°C, no load                                                             | -30  |                     | +30  | mV    |
|                                                  |                           | -40°C to +85°C, no load                                                                    | -50  |                     | +50  | mV    |
| LS-FET on resistance                             | R <sub>ON_LS_EL</sub> VSS | I <sub>SW2</sub> = 200mA                                                                   |      | 200                 |      | mΩ    |
| HS-FET on resistance                             | R <sub>ON_HS_EL</sub> VSS | I <sub>SW2</sub> = 200mA                                                                   |      | 350                 |      | mΩ    |
| Switching frequency                              | f <sub>SW2</sub>          |                                                                                            |      | 1.7                 |      | MHz   |
| Current limit                                    | I <sub>LIMIT2</sub>       |                                                                                            | 2    | 3                   |      | A     |
| Short protection threshold at start-up           | V <sub>ELVSS_SCP</sub>    | At start-up                                                                                |      | 250                 |      | mV    |
| Short protection threshold during operation      |                           | Voltage drop from normal ELVSS                                                             |      | 600                 |      | mV    |
| Short protection detection time                  | t <sub>SCP2</sub>         | At start-up                                                                                |      | 12.5                |      | ms    |
|                                                  |                           | During operation                                                                           |      | 1                   |      | ms    |
| ELVSS leakage current                            | I <sub>LEAKAGE</sub>      | CTRL = FD = 0V                                                                             |      | 0.01                | 5    | μA    |
| ELVSS discharge resistance                       | R <sub>DC_EL</sub> VSS    | CTRL = 0V, I <sub>ELVSS</sub> = 1mA                                                        |      | 150                 |      | Ω     |
| CT output impedance                              | R <sub>CT</sub>           |                                                                                            | 130  | 300                 | 490  | kΩ    |
| CT comparator                                    |                           |                                                                                            |      | 50                  |      | mV    |
| Load regulation <sup>(5)</sup>                   |                           | 1mA < I <sub>ELVSS</sub> < 300mA                                                           |      | 1.5                 |      | %/A   |
| Line regulation <sup>(5)</sup>                   |                           | 2.9V < V <sub>IN</sub> < 5.2V, I <sub>ELVSS</sub> = 200mA                                  |      | 0.45                |      | %V    |
|                                                  |                           | 2.9V < V <sub>IN</sub> < 5.2V, I <sub>ELVSS</sub> = 200mA with an external rectifier diode |      | 0.08 <sup>(7)</sup> |      |       |
| Boost Converter AVDD                             |                           |                                                                                            |      |                     |      |       |
| AVDD default voltage                             | V <sub>AVDD</sub>         |                                                                                            |      | 5.8                 |      | V     |
| AVDD voltage range                               |                           |                                                                                            | 5    |                     | 7.7  | V     |
| AVDD regulation                                  |                           | -40°C to +85°C, no load                                                                    | -1   |                     | +1   | %     |
| LS-FET on resistance                             | R <sub>ON_LS_A</sub> VDD  | I <sub>SW3</sub> = 200mA                                                                   |      | 500                 |      | mΩ    |
| HS-FET on resistance                             | R <sub>ON_HS_A</sub> VDD  | I <sub>SW3</sub> = 200mA                                                                   |      | 1400                |      | mΩ    |
| Switching frequency                              | f <sub>SW3</sub>          |                                                                                            |      | 1.35                |      | MHz   |
| Current limit                                    | I <sub>LIMIT3</sub>       |                                                                                            |      | 0.5                 |      | A     |
| Output OCP threshold                             | I <sub>OCP_A</sub> VDD    | I <sub>OCP_A</sub> VDD = 210mA                                                             |      | 210                 |      | mA    |
| Short protection threshold                       |                           | During operation                                                                           |      | 90                  |      | %     |
| Short protection detection time                  |                           | During operation                                                                           |      | 1                   |      | ms    |
| AVDD leakage current                             | I <sub>LEAKAGE</sub>      | CTRL = FD = 0V                                                                             |      | 2.8                 | 5.6  | μA    |
| Active discharge resistance                      | R <sub>DS_A</sub> VDD     | CTRL = 0V, I <sub>AVDD</sub> = 1mA                                                         |      | 30                  |      | Ω     |
| Load regulation <sup>(5)</sup>                   |                           | 1mA < I <sub>AVDD</sub> < 100mA                                                            |      | 0.08                |      | %/A   |
| Line regulation <sup>(5)</sup>                   |                           | 2.9V < V <sub>IN</sub> < 5.2V, I <sub>AVDD</sub> = 50mA                                    |      | 0.015               |      | %/V   |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 3.7V$ ,  $V_{ELVDD}/ELVSS/AVDD = \text{default}$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.

| Parameter                                         | Symbol      | Condition | Min  | Typ | Max | Units      |
|---------------------------------------------------|-------------|-----------|------|-----|-----|------------|
| <b>CTRL Interface</b>                             |             |           |      |     |     |            |
| Logic high voltage                                | $V_H$       |           | 1.35 |     |     | V          |
| Logic low voltage                                 | $V_L$       |           |      |     | 0.4 | V          |
| Pull-down resistor                                | R           |           |      | 500 |     | k $\Omega$ |
| Initialization time                               | $t_{INIT}$  |           |      | 340 | 470 | $\mu s$    |
| Shutdown period <sup>(5)</sup>                    | $t_{OFF}$   |           | 30   |     | 80  | $\mu s$    |
| Pulse high-level period <sup>(5)</sup>            | $t_{HIGH}$  |           | 2    | 10  | 25  | $\mu s$    |
| Pulse low-level period <sup>(5)</sup>             | $t_{LOW}$   |           | 2    | 10  | 25  | $\mu s$    |
| Data storage and acceptance period <sup>(5)</sup> | $t_{STORE}$ |           | 30   |     | 80  | $\mu s$    |

### Notes:

5) Guaranteed by characterization. Not tested in production.

6) When  $V_{IN}$  is between 4.3V and 4.5V, ELVDD line regulation increases since  $V_{IN}$  is close to ELVDD's  $V_{OUT}$ .

7) To improve ELVSS line regulation in heavy load when  $V_{IN} < 3.5V$ , use an external Schottky diode as a rectifier between ELVSS and SW2.

## TIMING DIAGRAM

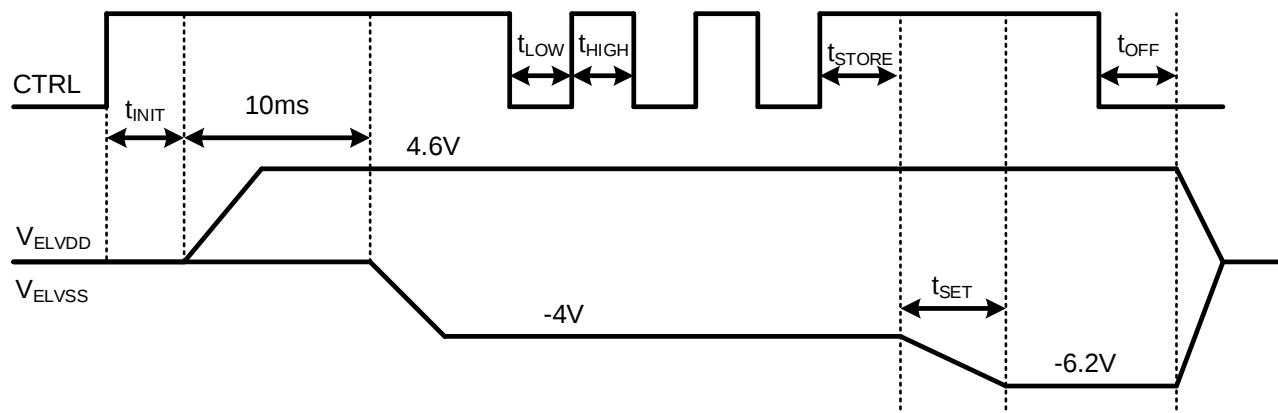
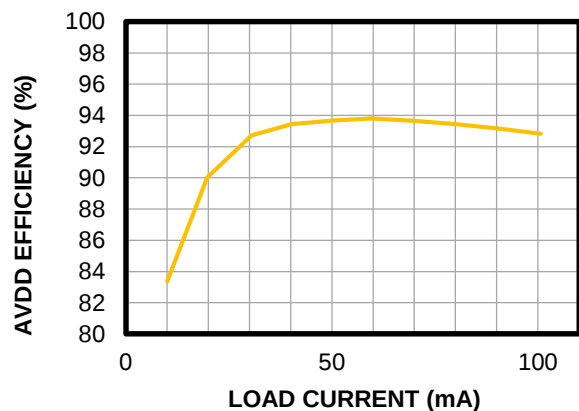


Figure 1: Digital Interface (CTRL) Timing Diagram

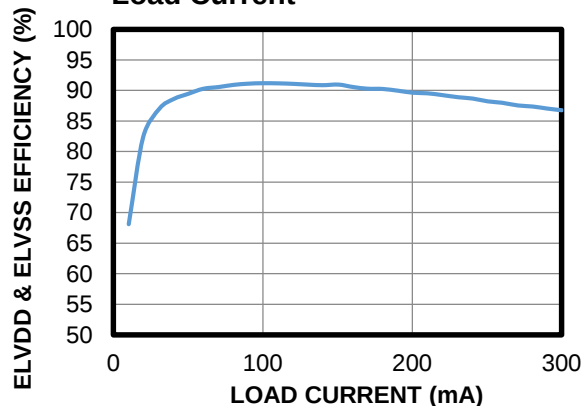
# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 3.7V$ ,  $V_{ELVDD}/V_{ELVSS}/V_{AVDD} = \text{default}$ ,  $L1 = L2 = 4.7\mu H$ ,  $L3 = 10\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

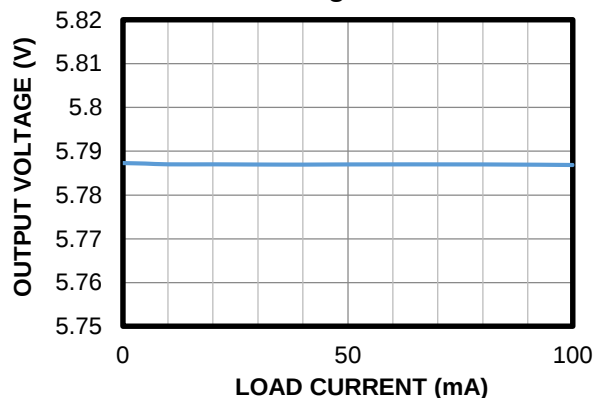
## AVDD Efficiency vs. Load Current



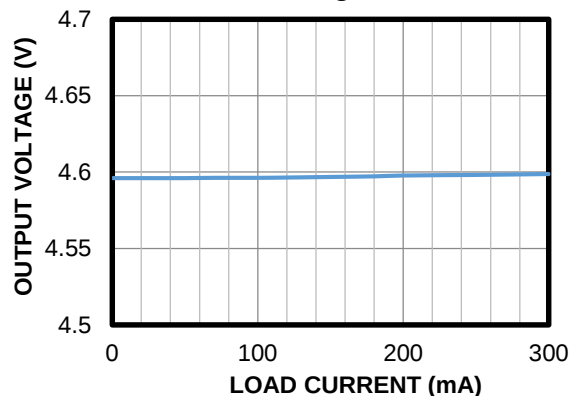
## ELVDD & ELVSS Efficiency vs. Load Current



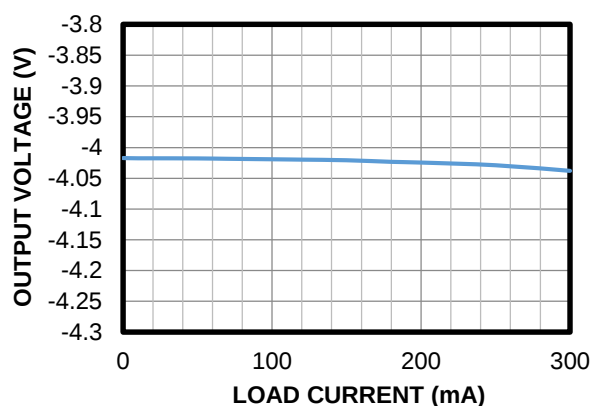
## AVDD Load Regulation



## ELVDD Load Regulation

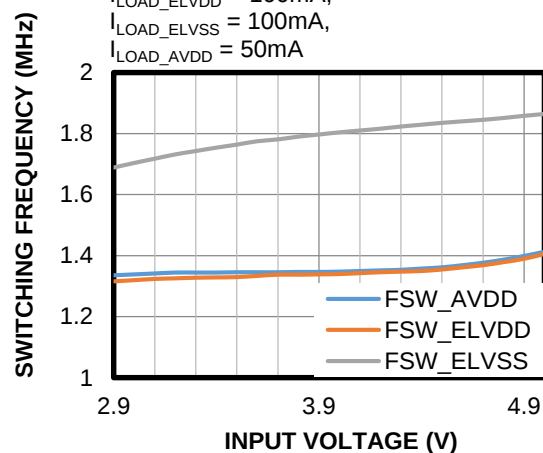


## ELVSS Load Regulation



## Switching Frequency vs. $V_{IN}$

$I_{LOAD\_ELVDD} = 100mA$ ,  
 $I_{LOAD\_ELVSS} = 100mA$ ,  
 $I_{LOAD\_AVDD} = 50mA$

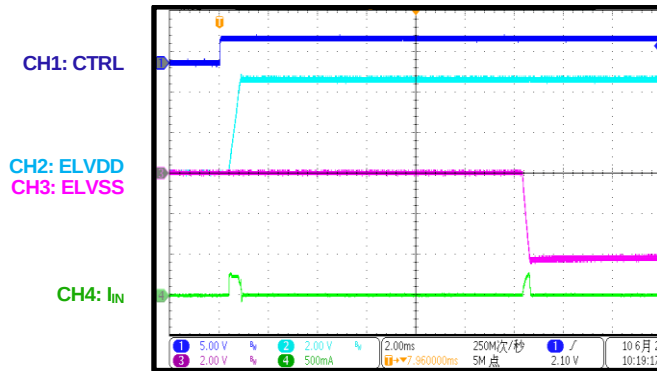


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3.7V$ ,  $V_{ELVDD}/ELVSS/AVDD = \text{default}$ ,  $L1 = L2 = 4.7\mu H$ ,  $L3 = 10\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

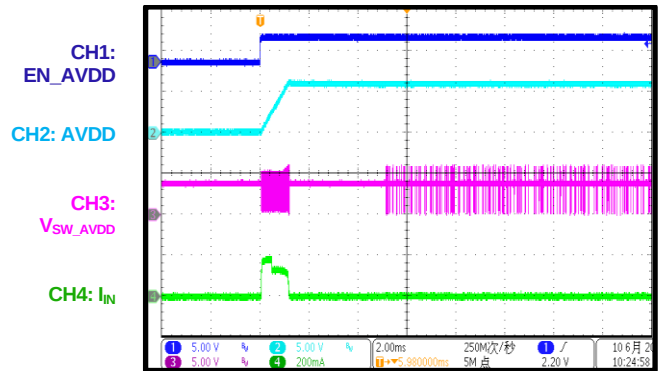
## EVLDD and ELVSS Start-Up

$I_{LOAD} = 0mA$



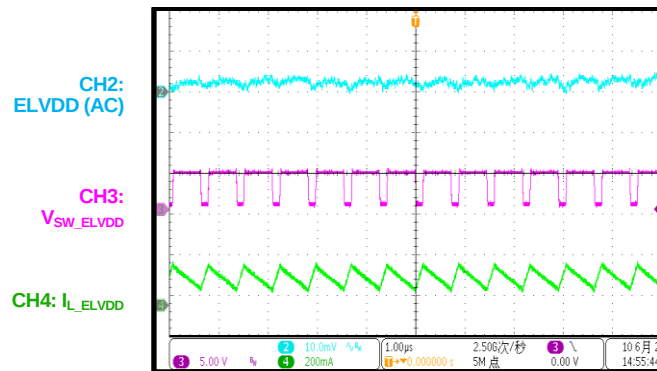
## AVDD Start-Up

$I_{LOAD} = 0mA$



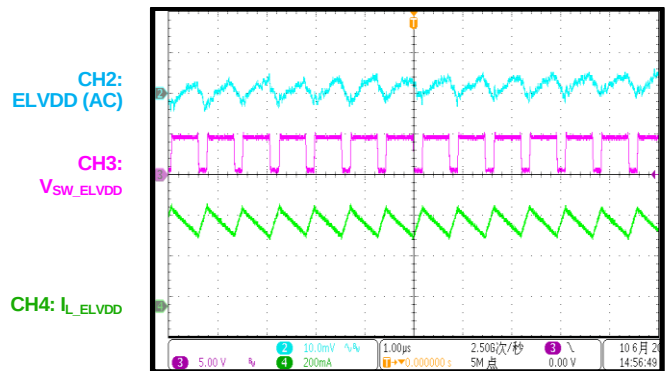
## ELVDD Steady State

$I_{LOAD} = 100mA$



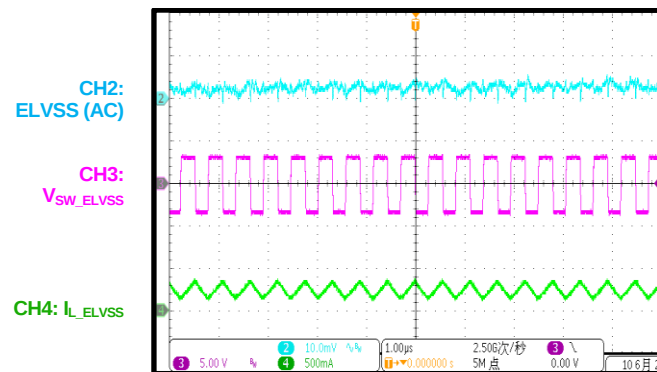
## ELVDD Steady State

$I_{LOAD} = 300mA$



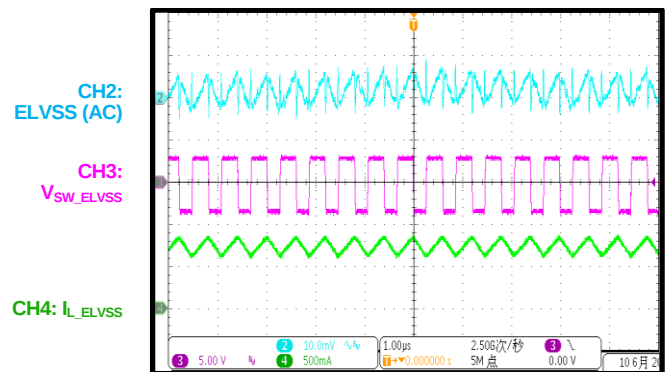
## ELVSS Steady State

$I_{LOAD} = 100mA$



## ELVSS Steady State

$I_{LOAD} = 300mA$

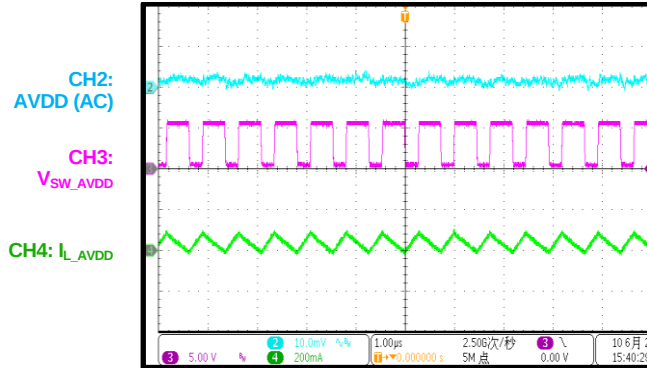


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3.7V$ ,  $V_{ELVDD}/V_{ELVSS}/V_{AVDD} = \text{default}$ ,  $L1 = L2 = 4.7\mu H$ ,  $L3 = 10\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

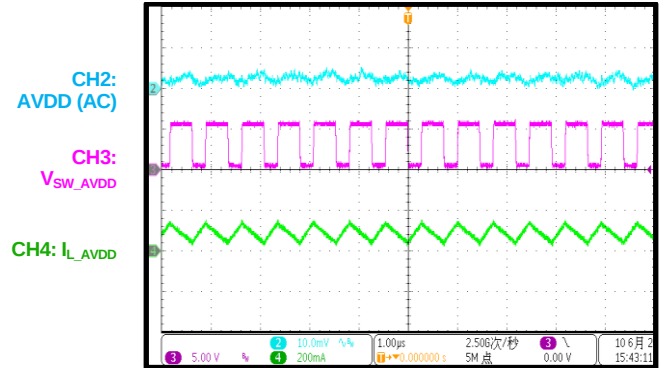
## AVDD Steady State

$I_{LOAD} = 20mA$



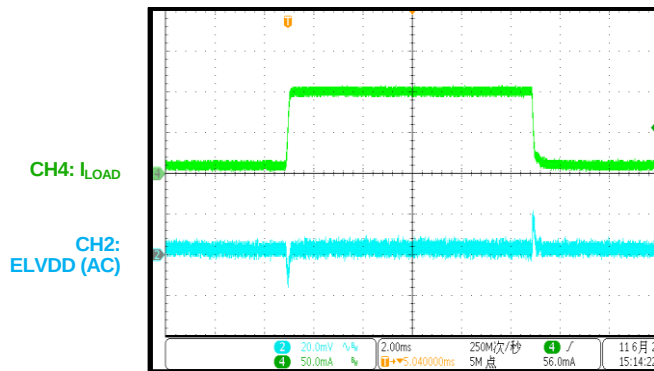
## AVDD Steady State

$I_{LOAD} = 50mA$



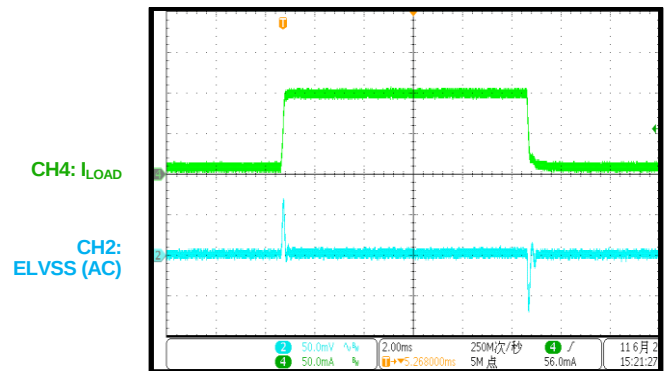
## ELVDD Load Transient Response

$I_{LOAD} = 10mA \text{ to } 100mA \text{ in } 180\mu s$



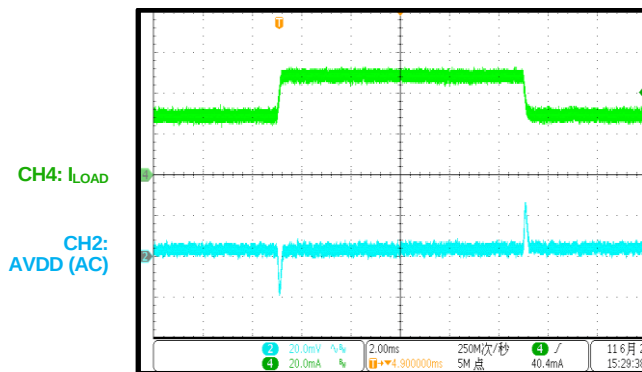
## ELVSS Load Transient Response

$I_{LOAD} = 10mA \text{ to } 100mA \text{ in } 180\mu s$

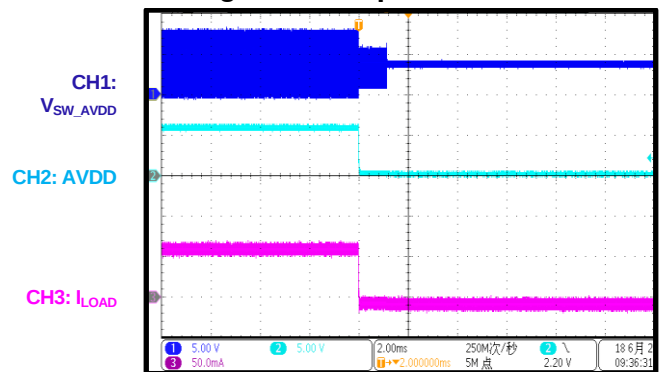


## AVDD Load Transient Response

$I_{LOAD} = 30mA \text{ to } 50mA \text{ in } 180\mu s$



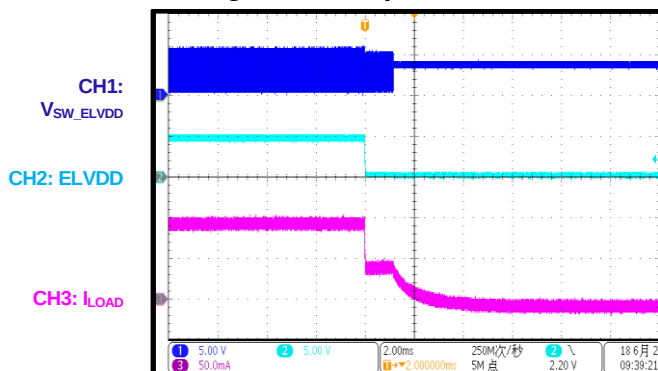
## AVDD Short to GND Protection during Normal Operation



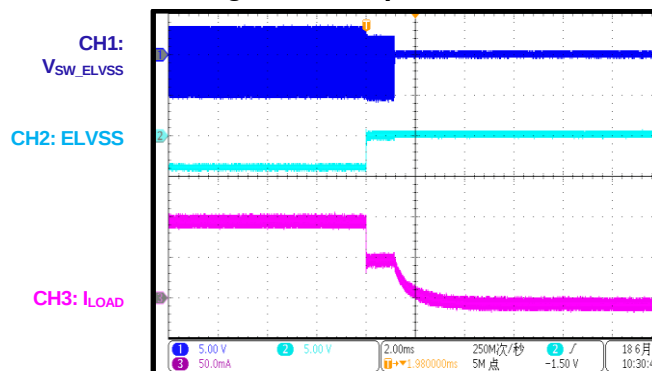
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 3.7V$ ,  $V_{ELVDD}/V_{ELVSS}/V_{AVDD} = \text{default}$ ,  $L1 = L2 = 4.7\mu H$ ,  $L3 = 10\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

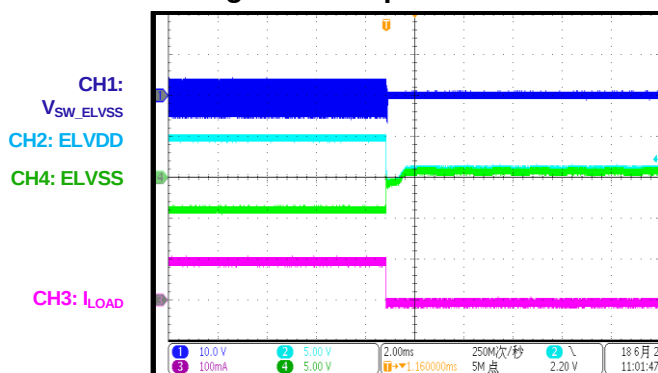
## ELVDD Short to GND Protection during Normal Operation



## ELVSS Short to GND Protection during Normal Operation



## ELVDD Short to ELVSS Protection during Normal Operation



# FUNCTIONAL BLOCK DIAGRAM

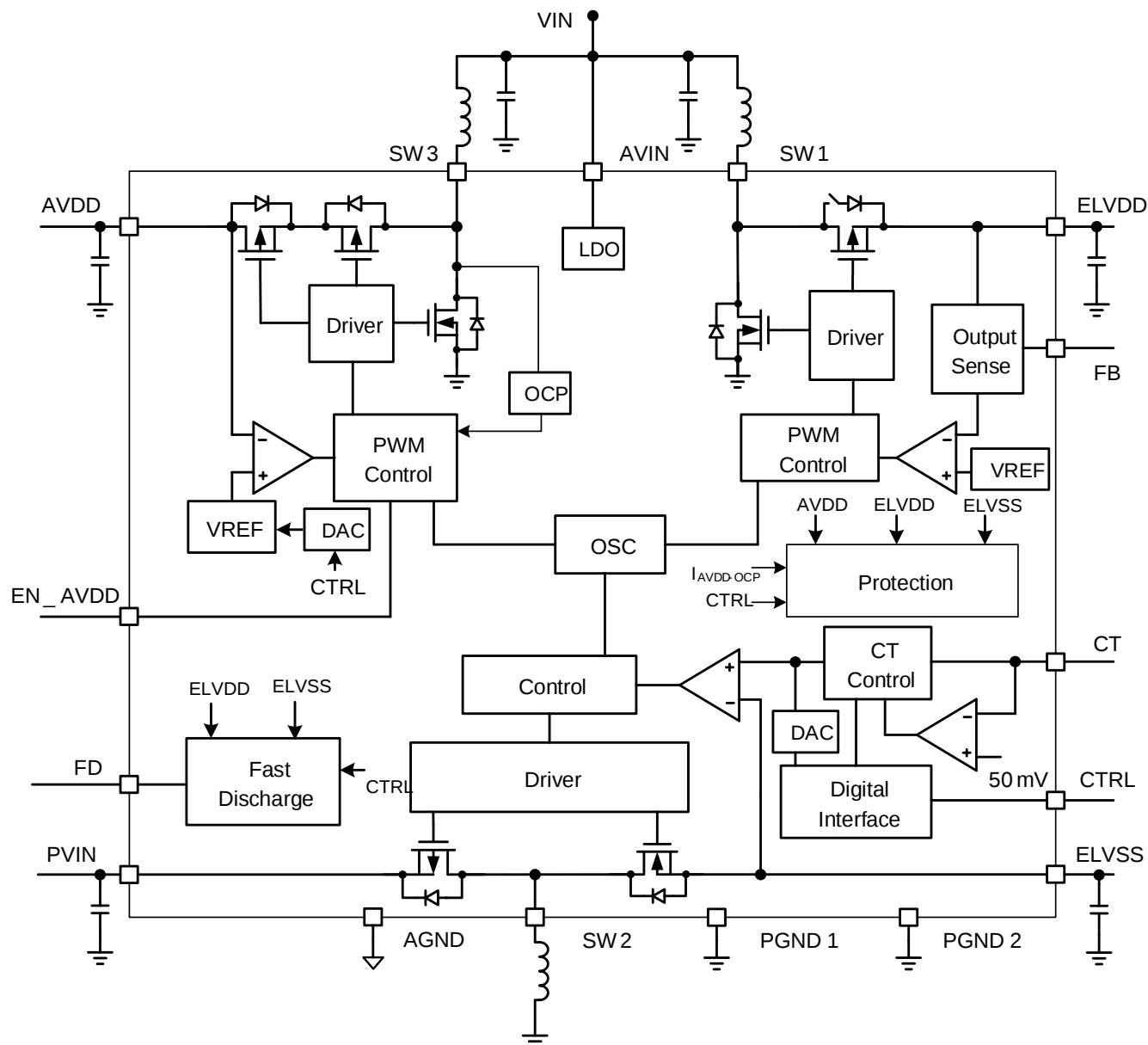


Figure 2: Functional Block Diagram

## OPERATION

The MP5611 is a triple-output converter designed for small-size AMOLED (active matrix organic light-emitting diode) display power supplies. It integrates a boost converter for ELVDD, an inverting buck-boost (IBB) converter for ELVSS, and another boost converter for AVDD. The one wire digital control pin (CTRL) can program the ELVSS, ELVDD, and AVDD voltages following digital protocol.

### Feedback (FB) Connection for ELVDD

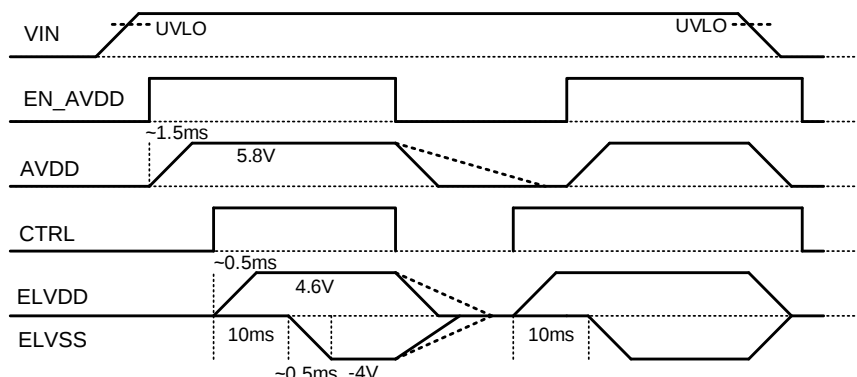
If the FB pin is floating or tied to GND, or  $(V_{ELVDD} - V_{FB}) > 350\text{mV}$ , then the ELVDD boost converter's output voltage ( $V_{OUT}$ ) is sensed via the ELVDD pin directly. To improve the ELVDD  $V_{OUT}$  sense performance, externally connect FB

to the main ELVDD output capacitor's positive terminal. In this case, when  $(V_{ELVDD} - V_{FB}) < 250\text{mV}$ ,  $V_{OUT}$  is sensed via FB pin with better sense accuracy.

### Fast Discharge Function

Pull the FD pin high to enable the active fast discharge function when the MP5611 shuts down. By connecting FD to GND, all outputs are high-impedance when the IC shuts down. When FD is pulled high, the fast discharge function can also be disabled by applying 81 pulses to the CTRL pin.

Figure 3 shows the start-up/shutdown sequence, where the solid line is with active discharge enabled and the dotted line is without active discharge enabled.



**Figure 3: Start-Up/Shutdown Sequence with and without Active Discharge Enable**

### Configuring the ELVSS Transition Time

When ELVSS is controlled by the CTRL pulse, the voltage transition time can be configured by the capacitor on the CT pin ( $C_{EXTERNAL}$ ), which can be estimated using Equation (1):

$$t (\mu\text{s}) = 3 \times R_{INTERNAL} (\text{k}\Omega) \times C_{EXTERNAL} (\text{nF}) \quad (1)$$

Where  $R_{INTERNAL} = 300\text{k}\Omega$ .  $C_{EXTERNAL}$  e.g. 100nF is about 90ms of the transition time.

### Digital Interface (CTRL)

The CTRL pin has two functions:

1. CTRL is the digital interface that configures the output of ELVSS, ELVDD, and AVDD, as well as the output over-current (OC) limit. The number of pulse signal's rising edges applied on the CTRL pin is counted for configuring the corresponding item to a certain value (see Table 1 on page 13).

2. CTRL is also ELVDD and ELVSS's enable signal. Once CTRL pulls high, ELVDD starts up to the default value. After 10ms, ELVSS establishes to its default value (see the Timing Diagram section on page 6).

The reset information for ELVSS, ELVDD, and AVDD follows:

- A power cycle resets all settings to default.
- CTRL is low, and lasts for a set time to reset ELVDD and ELVSS to the default value.
- EN\_AVDD can enable/disable AVDD.
- EN\_AVDD and CTRL are both pulled low to reset AVDD and all registers to the default value.

Table 1: CTRL Configuration Table

| Pulse # | ELVSS |
|---------|-------|
| 1       | -6.4V |
| 2       | -6.3V |
| 3       | -6.2V |
| 4       | -6.1V |
| 5       | -6V   |
| 6       | -5.9V |
| 7       | -5.8V |
| 8       | -5.7V |
| 9       | -5.6V |
| 10      | -5.5V |
| 11      | -5.4V |
| 12      | -5.3V |
| 13      | -5.2V |
| 14      | -5.1V |
| 15      | -5V   |
| 16      | -4.9V |
| 17      | -4.8V |
| 18      | -4.7V |
| 19      | -4.6V |
| 20      | -4.5V |
| 21      | -4.4V |
| 22      | -4.3V |
| 23      | -4.2V |
| 24      | -4.1V |
| 25      | -4V   |
| 26      | -3.9V |
| 27      | -3.8V |
| 28      | -3.7V |
| 29      | -3.6V |
| 30      | -3.5V |
| 31      | -3.4V |
| 32      | -3.3V |
| 33      | -3.2V |
| 34      | -3.1V |
| 35      | -3V   |
| 36      | -2.9V |
| 37      | -2.8V |
| 38      | -2.7V |
| 39      | -2.6V |
| 40      | -2.5V |
| 41      | -2.4V |
| 42      | -2.3V |
| 43      | -2.2V |
| 44      | -2.1V |
| 45      | -2V   |
| 46      | -1.9V |
| 47      | -1.8V |
| 48      | -1.7V |
| 49      | -1.6V |
| 50      | -1.5V |
| 51      | -1.4V |

| Pulse # | AVDD                            |
|---------|---------------------------------|
| 52      | +5V                             |
| 53      | +5.1V                           |
| 54      | +5.2V                           |
| 55      | +5.3V                           |
| 56      | +5.4V                           |
| 57      | +5.5V                           |
| 58      | +5.6V                           |
| 59      | +5.7V                           |
| 60      | +5.8V                           |
| 61      | +5.9V                           |
| 62      | +6V                             |
| 63      | +6.1V                           |
| 64      | +6.2V                           |
| 65      | +6.3V                           |
| 66      | +6.4V                           |
| 67      | +6.5V                           |
| 68      | +6.6V                           |
| 69      | +6.7V                           |
| 70      | +6.8V                           |
| 71      | +6.9V                           |
| 72      | +7V                             |
| 73      | +7.1V                           |
| 74      | +7.2V                           |
| 75      | +7.3V                           |
| 76      | +7.4V                           |
| 77      | +7.5V                           |
| 78      | +7.6V                           |
| 79      | +7.7V                           |
| Pulse # | V <sub>OUT</sub> Fast Discharge |
| 0       | Controlled by FD                |
| 80      | On                              |
| 81      | Off                             |
| Pulse # | 250mV Detection                 |
| 0       | Off                             |
| 82      | On                              |
| 83      | Off                             |
| Pulse # | ELVDD                           |
| 0       | 4.6V                            |
| 84      | 4.6V                            |
| 85      | 4.7V                            |
| 86      | 4.8V                            |
| 87      | 4.9V                            |
| 88      | 5V                              |
| 89      | 5.1V                            |
| 90      | 5.2V                            |
| Pulse # | OCP (ELVDD)                     |
| 0       | 650mA                           |
| 91      | 80mA                            |
| 92      | 175mA                           |
| 93      | 270mA                           |
| 94      | 365mA                           |

| Pulse # | OCP (ELVDD) |
|---------|-------------|
| 95      | 460mA       |
| 96      | 555mA       |
| 97      | 650mA       |
| Pulse # | OCP (AVDD)  |
| 0       | 210mA       |
| 98      | 90mA        |
| 99      | 120mA       |
| 100     | 150mA       |
| 101     | 180mA       |
| 102     | 210mA       |
| 103     | 240mA       |
| 104     | 270mA       |

### Diode Mode when $V_{IN} \approx ELVDD$

When the input voltage ( $V_{IN}$ ) is close to ELVDD, the MP5611 operates in diode mode. In this mode, the ELVDD boost converter's high-side MOSFET (HS-FET) is disabled, and its body diode operates as a rectifier to regulate  $V_{OUT}$ . Note that the converter must work in continuous conduction mode (CCM) to achieve proper output regulation in diode mode.

### ELVDD Over-Current Protection (OCP)

The MP5611 supports ELVDD over-current protection (OCP). If ELVDD's output current ( $I_{OUT}$ ) exceeds 650mA (default) or the threshold configured via the CTRL signal, and lasts for 1ms, then OCP is triggered and the IC shuts down until CTRL or the power resets.

### AVDD OCP

The MP5611 supports AVDD OCP. When AVDD's  $I_{OUT}$  exceeds 210mA (default) or the threshold configured via the CTRL signal, and lasts for 1ms, then OCP is triggered and the IC shuts down until EN\_AVDD or the power resets.

### Short Output Voltage ( $V_{OUT}$ ) Protection

The MP5611 features complete short protection functions, including AVDD, ELVDD, ELVSS short to GND protection, as well as ELVDD short to ELVSS protection.

The conditions required for the short protection functions follow:

1. If ELVDD does not reach its regulated voltage within 10ms after ELVDD is enabled (CTRL = high), all output voltages shut down

(for ELVDD short to GND protection at start-up).

2. If ELVSS does not reach its regulated voltage within 12.5ms after ELVSS is enabled (22.5ms after CTRL = high), all output voltages shut down (for ELVSS short to GND protection at start-up).
3. If  $ELVSS > 250mV$  when ELVSS is enabled (10ms after CTRL = high), ELVDD and ELVSS shut down, and AVDD operates normally (for ELVDD short to ELVSS protection).
4. If AVDD decreases to 90% of its configured voltage for 1ms, all output voltages shut down (for AVDD short to GND protection during operation).
5. If ELVDD decreases to 80% of its configured voltage for 1ms, all output voltages shut down (for ELVDD short to GND protection during operation).
6. If ELVSS increases to  $>600mV$  for 1ms, all output voltages shut down (for ELVSS short to GND protection during operation).

### Thermal Shutdown

To prevent the IC from operating at exceedingly high temperatures, thermal shutdown is implemented by monitoring the silicon die temperature. When the die temperature exceeds the upper threshold ( $T_{ST}$ ), the IC shuts down. Once the die temperature drops below the lower threshold, the IC restarts and resumes normal operation. The hysteresis is 25°C.

## APPLICATION INFORMATION

### Selecting the Inductor

It is recommended to use the ELVDD and ELVSS converters with 4.7 $\mu$ H inductors, and the AVDD boost converter with a 10 $\mu$ H inductor (see Table 2).

For a given inductance, the inductor DC current rating should be at least 40% greater than the maximum input peak inductor current for most applications. The inductor's DC resistance should be as small as possible for higher efficiency.

### Selecting the Capacitor

Table 2 shows the recommended capacitors. Lower capacitance may lead to increased

voltage ripple. Generally, the lower  $I_{OUT}$ , the lower the required capacitance. It is recommended to use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients.

### Optional ELVSS External Rectifier Diode

Using an external Schottky diode as a rectifier for ELVSS can be beneficial for improving ELVSS line regulation in heavy load when  $V_{IN} < 3.5V$ . If necessary, a B0530WS Schottky diode in an SOD-323 package is sufficient. Connect this diode between ELVSS and SW2 (see the dotted box in Figure 4 on page 16).

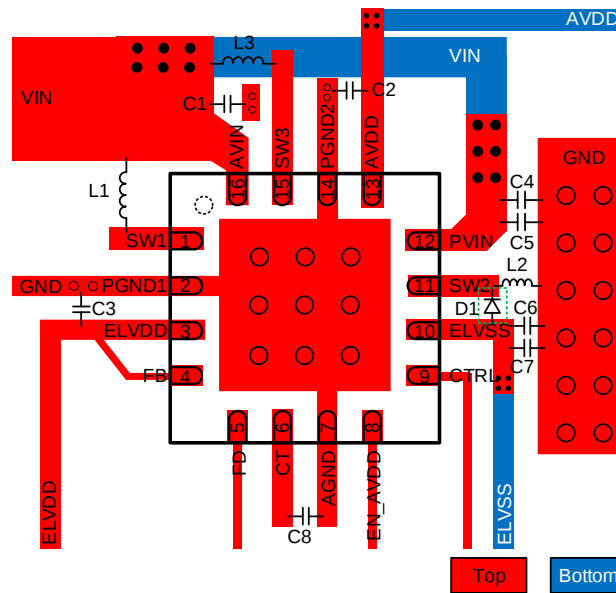
**Table 2: Recommended Inductors and Capacitors**

| Ref                                       | Value          | Manufacturer | Manufacturer PN   |
|-------------------------------------------|----------------|--------------|-------------------|
| L <sub>SW1</sub> , L <sub>SW2</sub>       | 4.7 $\mu$ H    | Coilcraft    | XFL4020-4R7ML     |
| L <sub>SW3</sub>                          | 10 $\mu$ H     | Coilmaster   | MMPP252012-100N   |
| C <sub>IN</sub>                           | 3 x 10 $\mu$ F | Murata       | GRM21BR71A106KE51 |
| C <sub>O_AVDD</sub> , C <sub>O_ELVD</sub> | 10 $\mu$ F     | Murata       | GRM21BR71A106KE51 |
| C <sub>O_ELVS</sub>                       | 2 x 10 $\mu$ F | Murata       | GRM21BR71A106KE51 |
| C <sub>CT</sub>                           | 100nF          | Murata       | GRM155B11A104KA01 |

### PCB Layout Guidelines

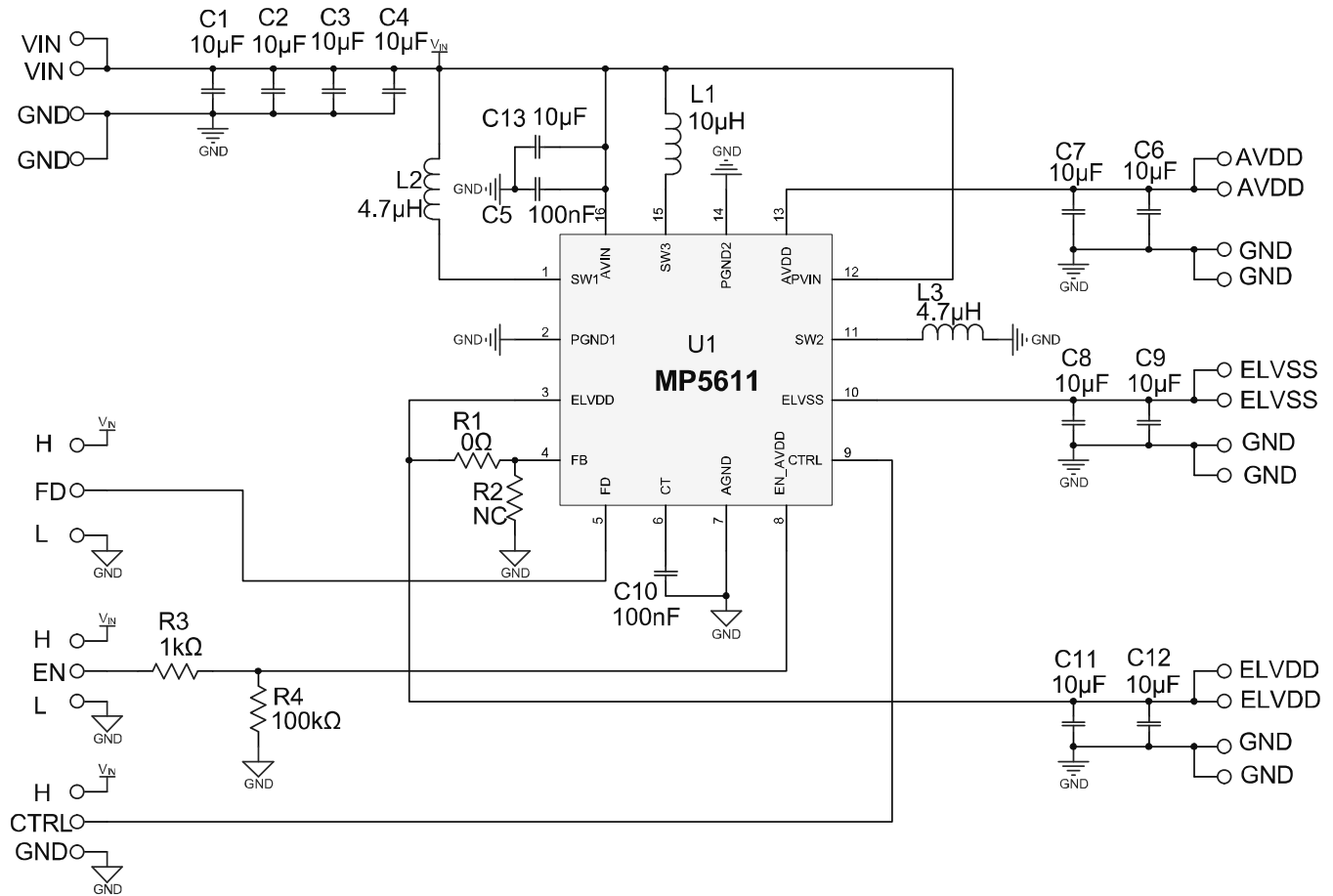
Efficient PCB layout and placement of the high-frequency switching path are critical to prevent noise and electromagnetic interference (EMI). For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the input capacitors on PVIN and AVIN as close as possible to the device.
2. Place the output capacitors on AVDD, ELVDD, and ELVSS as close as possible to the device.
3. Use short and wide traces to connect the input capacitors on PVIN and AVIN.
4. Use short and wide traces to connect the output capacitors on AVDD, ELVDD, and ELVSS.
5. Connect the CT capacitor's negative terminal directly to the AGND pin.
6. Keep the loop between SW2, L2, the PVIN input capacitor, the ELVSS output capacitor, and GND as short as possible due to the high-frequency pulse current.
7. Connect the IC's exposed thermal pad to AGND, PGND1, and PGND2.



**Figure 4: Recommended PCB Layout**

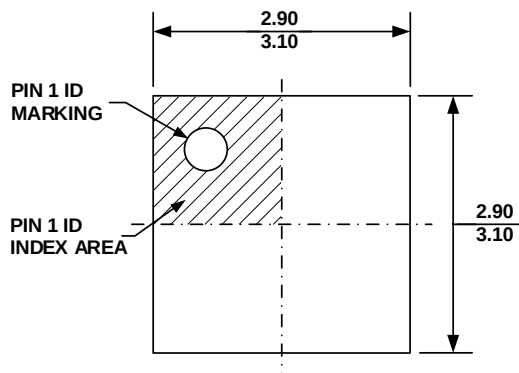
# **TYPICAL APPLICATION CIRCUIT**



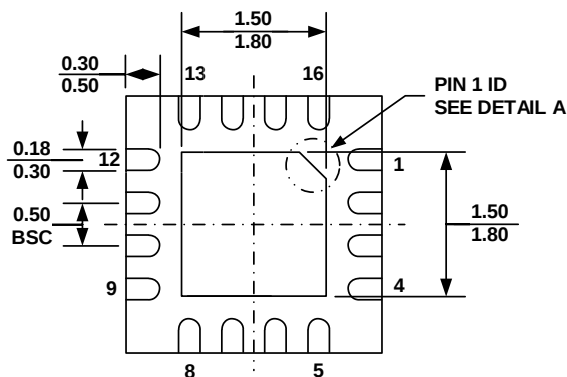
**Figure 5: Typical Application Circuit**

# PACKAGE INFORMATION

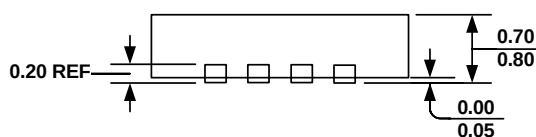
## TQFN-16 (3mmx3mm)



**TOP VIEW**

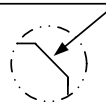


**BOTTOM VIEW**



**SIDE VIEW**

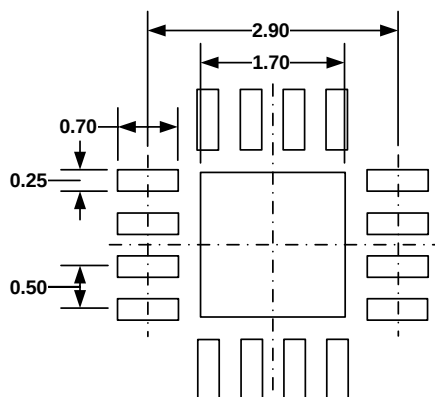
PIN 1 ID OPTION A  
0.30x45° TYP.



PIN 1 ID OPTION B  
R0.20 TYP.



**DETAIL A**

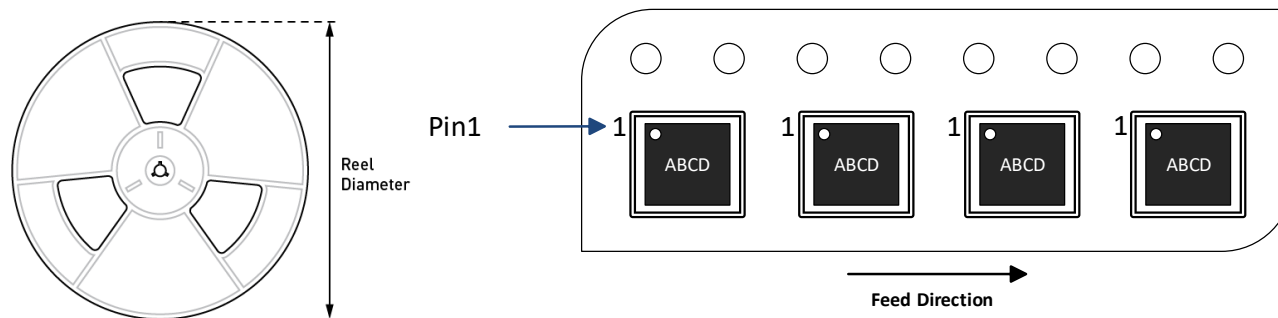


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION WEED-4.
- 5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MP5611GQT-Z | TQFN-16 (3mmx3mm)   | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                |

**REVISION HISTORY**

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 12/16/2021    | Initial Release | -             |

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