

CDx4HC4511, CD74HCT4511 BCD-to-7 Segment Latch/Decoder/Drivers

1 Features

- 2-V to 6-V V_{CC} operation ('HC4511)
- 4.5-V to 5.5-V V_{CC} operation (CD74HCT4511)
- High-output sourcing capability
 - 7.5 mA at 4.5 V (CD74HCT4511)
 - 10 mA at 6 V ('HC4511)
- Input latches for BCD code storage
- Lamp test and blanking capability
- Balanced propagation delays and transition times
- Significant power reduction compared to LSTTL logic IC's
- 'HC4511
 - High noise immunity,
 N_{IL} or $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5$ V
- CD74HCT4511
 - Direct LSTTL input logic compatibility, $V_{IL} = 0.8$ V Maximum, $V_{IH} = 2$ V minimum
 - CMOS input compatibility, $I_I \leq 1\mu\text{A}$ at V_{OL} , V_{OH}

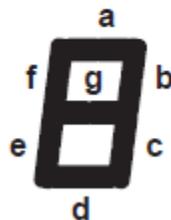
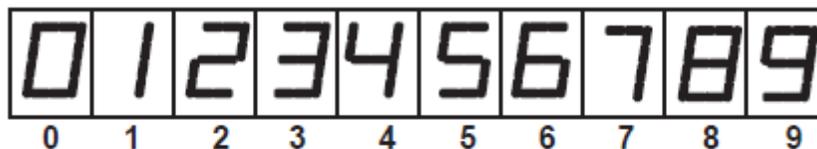
2 Description

The CD54HC4511, CD74HC4511, and CD74HCT4511 are BCD-to-7 segment latch/decoder/drivers with four address inputs (D_0 – D_3), an active-low blanking (\overline{BL}) input, lamp-test (\overline{LT}) input, and a latch-enable (\overline{LE}) input that, when high, enables the latches to store the BCD inputs. When \overline{LE} is low, the latches are disabled, making the outputs transparent to the BCD inputs.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
CD54HC4511	J (CDIP, 16)	24.38 mm × 6.92 mm
CD74HC4511	N (PDIP, 16)	19.31 mm × 6.35 mm
	D (SOIC, 16)	9.90 mm × 3.90 mm
	PW (TSSOP, 16)	5.00 mm × 4.40 mm
CD74HCT4511	N (PDIP, 16)	19.31 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Display



Table of Contents

1 Features	1	6 Parameter Measurement Information	8
2 Description	1	7 Detailed Description	10
3 Revision History	2	7.1 Overview.....	10
4 Pin Configuration and Functions	3	7.2 Functional Block Diagram.....	10
5 Specifications	4	7.3 Device Functional Modes.....	10
5.1 Absolute Maximum Ratings.....	4	8 Power Supply Recommendations	11
5.2 Recommended Operating Conditions for 'HC4511 ⁽¹⁾	4	9 Layout	11
5.3 Recommended Operating Conditions for CD74HCT4511 ⁽¹⁾	4	9.1 Layout Guidelines.....	11
5.4 Thermal Information.....	5	10 Device and Documentation Support	12
5.5 'HC4511 Electrical Characteristics.....	5	10.1 Receiving Notification of Documentation Updates..	12
5.6 CD74HCT4511 Electrical Characteristics.....	5	10.2 Support Resources.....	12
5.7 'HC4511 Timing Requirements.....	6	10.3 Trademarks.....	12
5.8 Switching Characteristics.....	6	10.4 Electrostatic Discharge Caution.....	12
5.9 CD74HCT4511 Timing Requirements.....	7	10.5 Glossary.....	12
5.10 CD74HCT4511 Switching Characteristics.....	7	11 Mechanical, Packaging, and Orderable Information	12
5.11 Operating Characteristics.....	7	11.1 Tape and Reel Information.....	13
		11.2 Mechanical Data.....	14

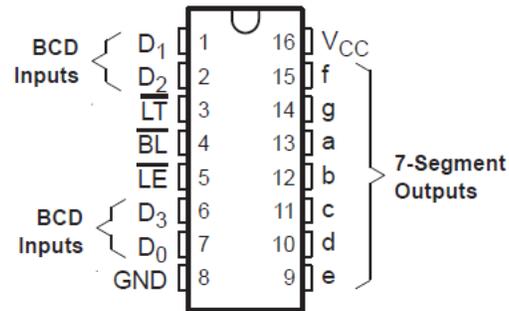
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2003) to Revision E (August 2022) Page

- Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards..... 1

4 Pin Configuration and Functions



J, N, D, PW package
16-Pin CDIP, PDIP, SOIC, TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	- 0.5	7	V
I _{IK}	Input diode current	V _I < - 0.5 V or V _I > V _{CC} + 0.5 V ⁽¹⁾		±20 mA
I _{OK}	Output diode current	V _O < - 0.5 V or V _O > V _{CC} + 0.5 V ⁽¹⁾		±20 mA
I _O	Output source or sink current per output pin	V _O = 0 to V _{CC}		±25 mA
Continuous current through V _{CC} or GND				±50 mA
T _J	Junction temperature			150 °C
T _{stg}	Storage temperature range	- 65	150	°C
Lead temperature (During Soldering)		At distance 1/16 ± 1/32 in (1.59 ± 0.79 mm) from case for 10 s maximum		265 °C
		Unit inserted into a PC board (minimum thickness 1/16 in, 1.59 mm) (with solder contacting lead tips only)		300 °C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

5.2 Recommended Operating Conditions for 'HC4511⁽¹⁾

		T _A = 25°C		T _A = - 55°C to 125°C		T _A = - 40°C to 85°C		UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	6	2	6	2	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5		1.5		V
		V _{CC} = 4.5 V		3.15		3.15		
		V _{CC} = 6 V		4.2		4.2		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5		V
		V _{CC} = 4.5 V		1.35		1.35		
		V _{CC} = 6 V		1.8		1.8		
V _I	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
t _t	Input transition rise/fall time	V _{CC} = 2 V		1000		1000		ns
		V _{CC} = 4.5 V		500		500		
		V _{CC} = 6 V		400		400		

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

5.3 Recommended Operating Conditions for CD74HCT4511⁽¹⁾

		T _A = - 55°C to 125°C		T _A = - 55°C to 125°C		T _A = - 40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		2		V
V _{IL}	Low-level input voltage	0.8		0.8		0.8		
V _I	Input voltage	V _{CC}		V _{CC}		V _{CC}		V
V _O	Output voltage	V _{CC}		V _{CC}		V _{CC}		V

5.3 Recommended Operating Conditions for CD74HCT4511⁽¹⁾ (continued)

		T _A = – 55°C to 125°C		T _A = – 55°C to 125°C		T _A = – 40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _t	Input transition (rise and fall) time	500		500		500		ns

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number [SCBA004](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		D (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	
R _{θJA}	Package thermal impedance	67	73	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 'HC4511 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		T _A = – 55°C to 125°C		T _A = – 40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High level output voltage	V _I = V _{IH} or V _{IL}	I _{OH} = –20 μA	2 V	1.9	1.9	1.9	V		
			4.5 V	4.4	4.4	4.4			
			6 V	5.9	5.9	5.9			
			I _{OH} = –4 mA	4.5 V	3.98	3.7		3.84	
			I _{OH} = –5.2 mA	6 V	5.48	5.2		5.34	
V _{OL} Low level output voltage	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V	0.1	0.1	0.1	V		
			4.5 V	0.1	0.1	0.1			
			6 V	0.1	0.1	0.1			
			I _{OL} = 4 mA	4.5 V	0.26	0.4		0.33	
			I _{OL} = 5.2 mA	6 V	0.26	0.4		0.33	
I _I Input leakage current V	V _I = V _{CC} or 0	6 V	±0.1		±1		±1	μA	
I _{CC} Supply current	V _I = V _{CC} or 0, I _O = 0	6 V	8		160		80	μA	
C _i Input Capacitance		2 V to 6 V	10		10		10	pF	

5.6 CD74HCT4511 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = – 55°C to 125°C		T _A = – 40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH} High level output voltage	V _I = V _{IH} or V _{IL}	I _{OH} = –20 μA	4.5 V	4.4		4.4	4.4		V	
				I _{OH} = –4 mA	3.98		3.7	3.84		
V _{OL} Low level output voltage	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5 V		0.1		0.1		V	
				I _{OL} = 4 mA		0.26		0.4		
I _I Input leakage current V	V _I = V _{CC} to GND	5.5 V		±0.1			±1		μA	
I _{CC} Supply current	V _I = V _{CC} or 0, I _O = 0	5.5 V		8			160		80	μA
ΔI _{CC} ⁽¹⁾ Supply-Current Change	LT, LE inputs held at V _{CC} – 2.1 V	4.5 V to 5.5 V	100	540	735		675		μA	
	BL, Dn inputs held at V _{CC} – 2.1 V		100	108	147		135			

5.6 CD74HCT4511 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -55°C to 125°C		T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C _i Input Capacitance					10		10		10	pF

- (1) Additional supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

5.7 'HC4511 Timing Requirements

	V _{CC}	T _A = 25°C		T _A = -55°C to 125°C		T _A = -40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, \overline{LE} low	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t _{su} Setup time, BCD inputs before $\overline{LE}\uparrow$	2 V	60		90		75		ns
	4.5 V	12		18		15		
	6 V	10		15		13		
t _h Hold time, BCD inputs before $\overline{LE}\uparrow$	2 V	3		3		3		ns
	4.5 V	3		3		3		
	6 V	3		3		3		

5.8 Switching Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		UNIT	
					MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{pd}	D _n	Output	C _L = 50 pF	2 V		300		450		375	ns		
				4.5 V		60		90		75			
				6 V		51		77		64			
			C _L = 15 pF	5 V		25							
				2 V	C _L = 50 pF	2 V		270		405			340
						4.5 V		54		81			68
	6 V		46				69		58				
	C _L = 15 pF	5 V		23									
		B \overline{L}	Output	C _L = 50 pF	2 V		220		330			275	
					4.5 V		44		66			55	
	6 V					37		56		47			
	C _L = 15 pF			5 V		18							
				2 V	C _L = 50 pF	2 V		160		240			200
						4.5 V		32		48			40
	6 V		27				41		34				
	C _L = 15 pF	5 V		13									
Any		C _L = 50 pF	2 V		75		110		95				
			4.5 V		15		22		19				
	6 V			13		19		16					

5.9 CD74HCT4511 Timing Requirements

		T _A = 25°C		T _A = – 55°C TO 125°C		T _A = – 40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, \overline{LE} low	16		24		20		ns
t _{su}	Setup time, BCD inputs before \overline{LE} ↑	16		24		20		ns
t _h	Hold time, BCD inputs before \overline{LE} ↑	5		5		5		ns

over operating free-air temperature range (unless otherwise noted)

5.10 CD74HCT4511 Switching Characteristics

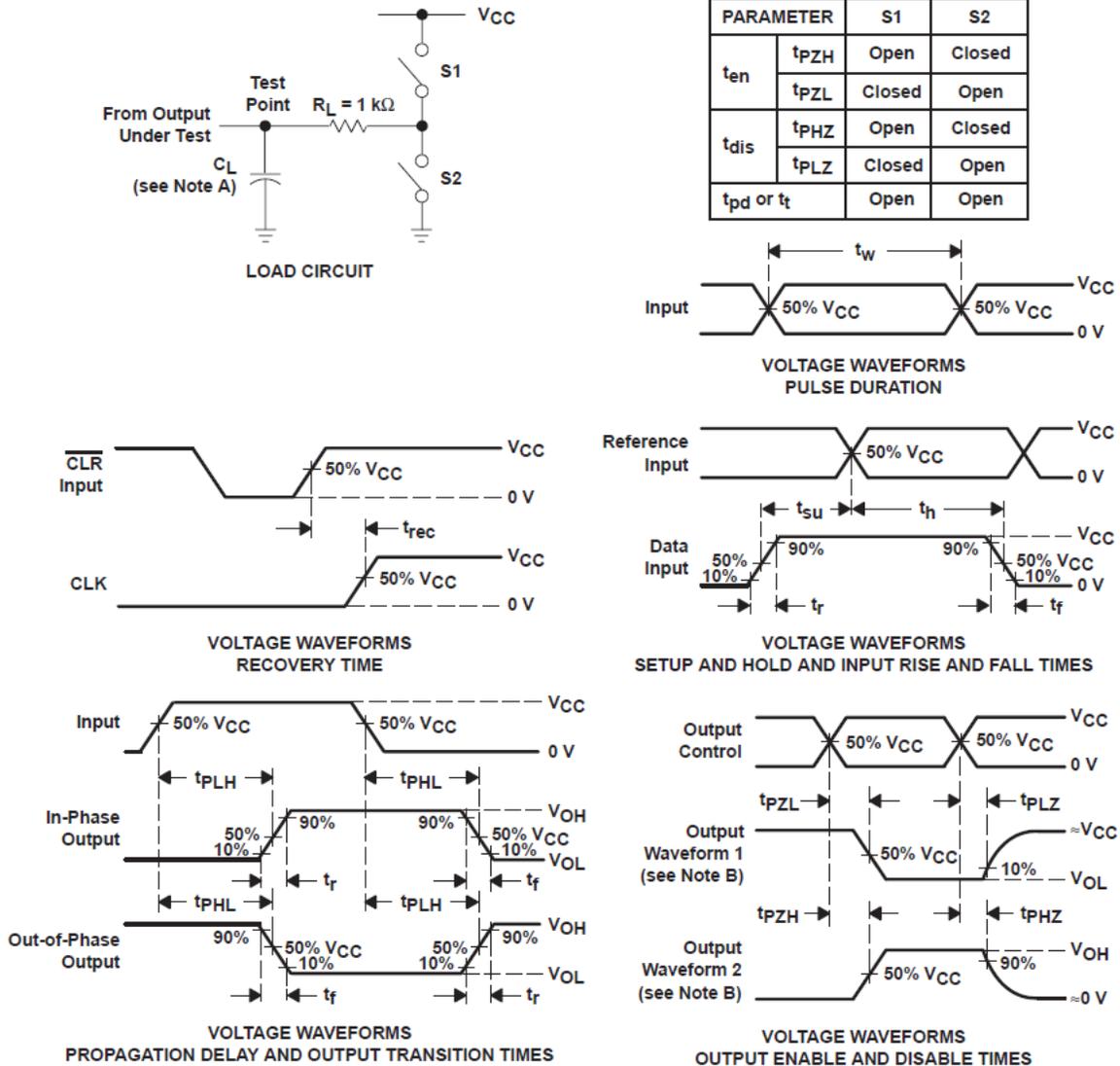
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = – 55°C to 125°C		T _A = – 40°C to 85°C		UNIT	
					MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{pd}	D _n	Output	C _L = 50 pF	4.5 V			60		90		75	ns	
			C _L = 15 pF	5 V			25						
	\overline{LE}	Output	C _L = 50 pF	4.5 V				54		81			68
			C _L = 15 pF	5 V			23						
	\overline{BL}	Output	C _L = 50 pF	4.5 V					44		66		55
			C _L = 15 pF	5 V			18						
	\overline{LT}	Output	C _L = 50 pF	4.5 V					33		50		41
			C _L = 15 pF	5 V			13						
t _t		Any	C _L = 50 pF	4.5 V			15		22		19	ns	

5.11 Operating Characteristics

PARAMETER ⁽¹⁾			TYP	UNIT
C _{pd}	Power dissipation capacitance	'HC4511	114	pF
		CD74HCT4511	110	

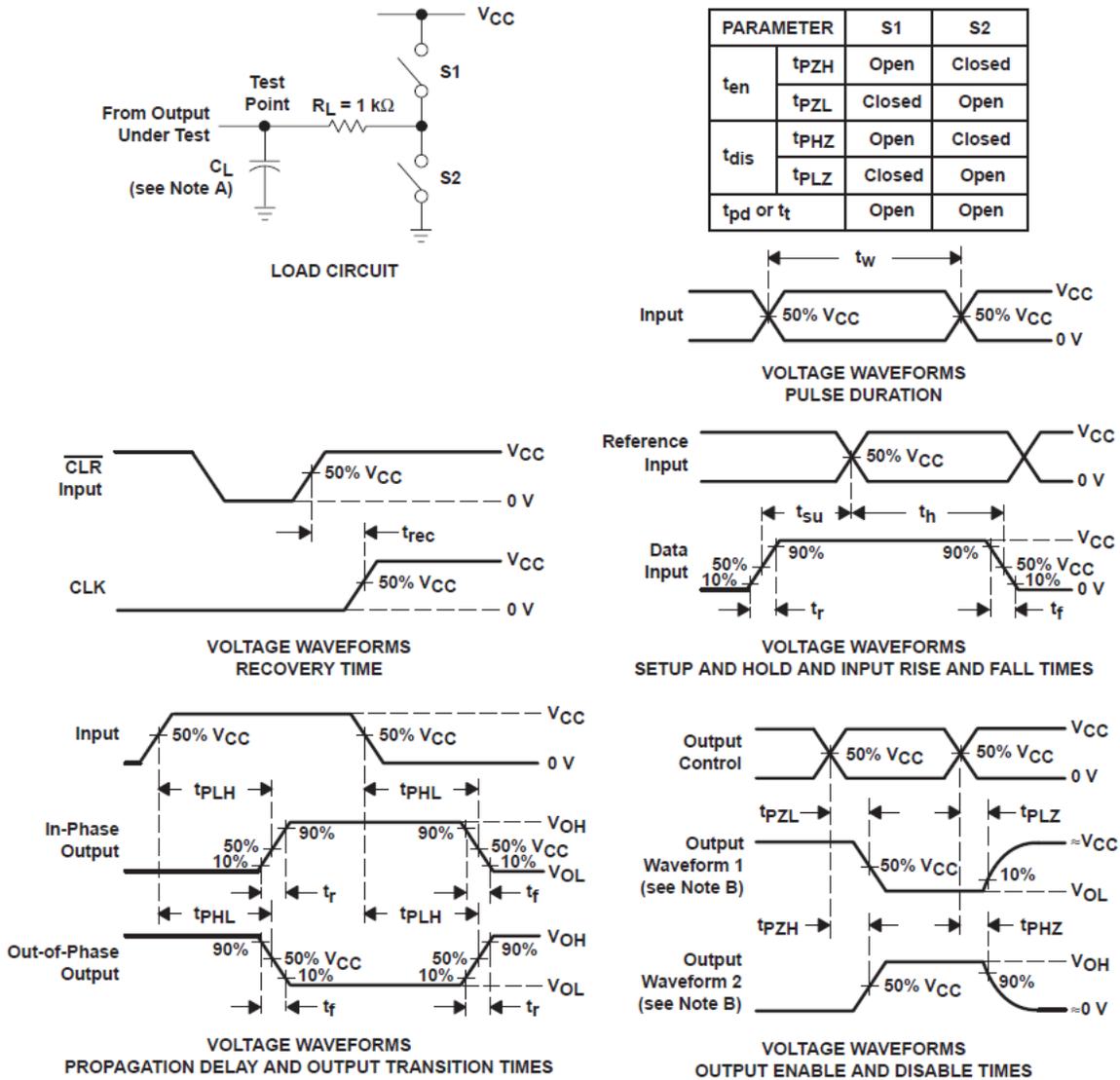
- (1) C_{pd} is used to determine the dynamic power consumption, per package.
 $P_D = C_{pd} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$ where:
 f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

6 Parameter Measurement Information



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.
 D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 E. The outputs are measured one at a time with one input transition per measurement.
 F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 G. t_{PZL} and t_{PZH} are the same as t_{en} .
 H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 6-1. 'HC4511



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 E. The outputs are measured one at a time with one input transition per measurement.
 F. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 G. t_{pZL} and t_{pZH} are the same as t_{en} .
 H. t_{pLH} and t_{pHL} are the same as t_{pd} .

Figure 6-2. CD74HCT4511

7 Detailed Description

7.1 Overview

The CD54HC4511, CD74HC4511, and CD74HCT4511 are BCD-to-7 segment latch/decoder/drivers with four address inputs (D_0 – D_3), an active-low blanking (\overline{BL}) input, lamp-test (\overline{LT}) input, and a latch-enable (\overline{LE}) input that, when high, enables the latches to store the BCD inputs. When \overline{LE} is low, the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors, but are capable of sourcing (at standard V_{OH} levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

7.2 Functional Block Diagram

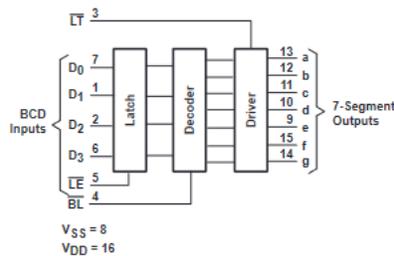


Figure 7-1. Function Diagram

7.3 Device Functional Modes

Table 7-1. Function Table

INPUTS ⁽¹⁾							OUTPUTS ⁽²⁾							
\overline{LE}	\overline{BL}	\overline{LT}	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	t	t	t	t	t	t	t	t

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't care = Depends on BCD code previously applied when \overline{LE} = L (NOT): Display is blank for all illegal input codes (BCD > HLLH).

(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

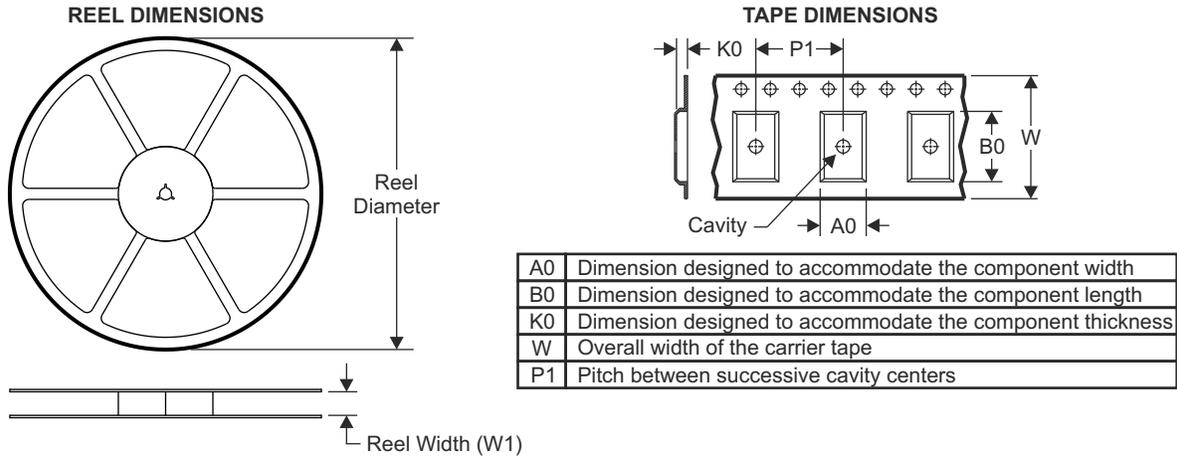
10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

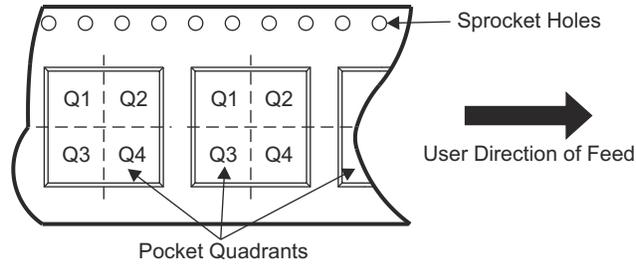
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

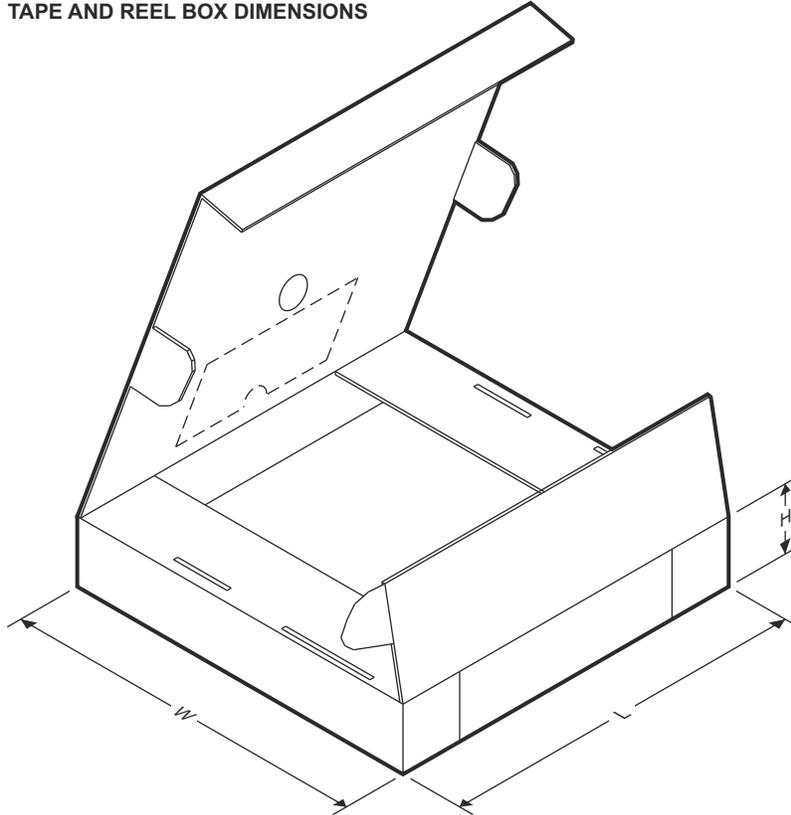


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



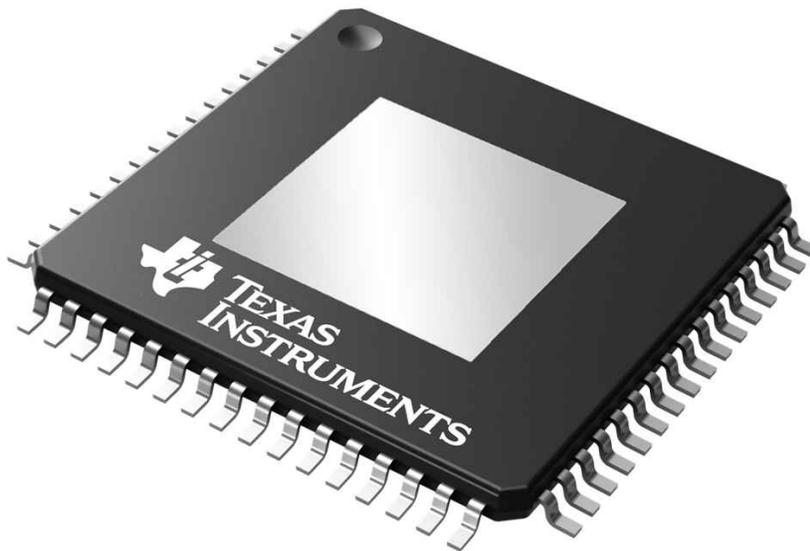
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTAS6584QDKQ1	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTAS6584QPHDRQ1	HTQFP	PHD	64	1000	350.0	350.0	43.0

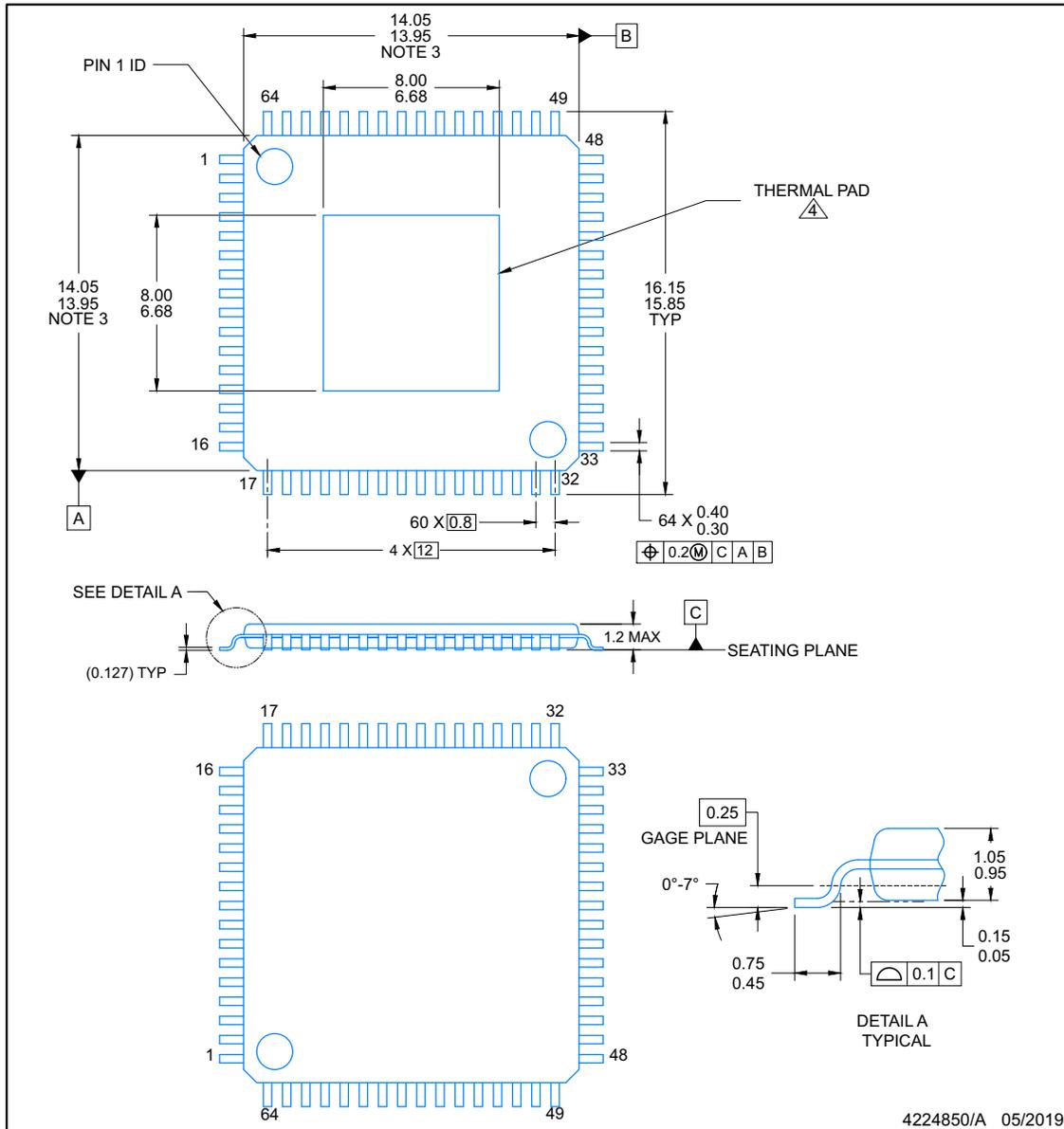
11.2 Mechanical Data



PACKAGE OUTLINE
HTQFP - 1.2 mm max height

PHD0064B

PLASTIC QUAD FLATPACK



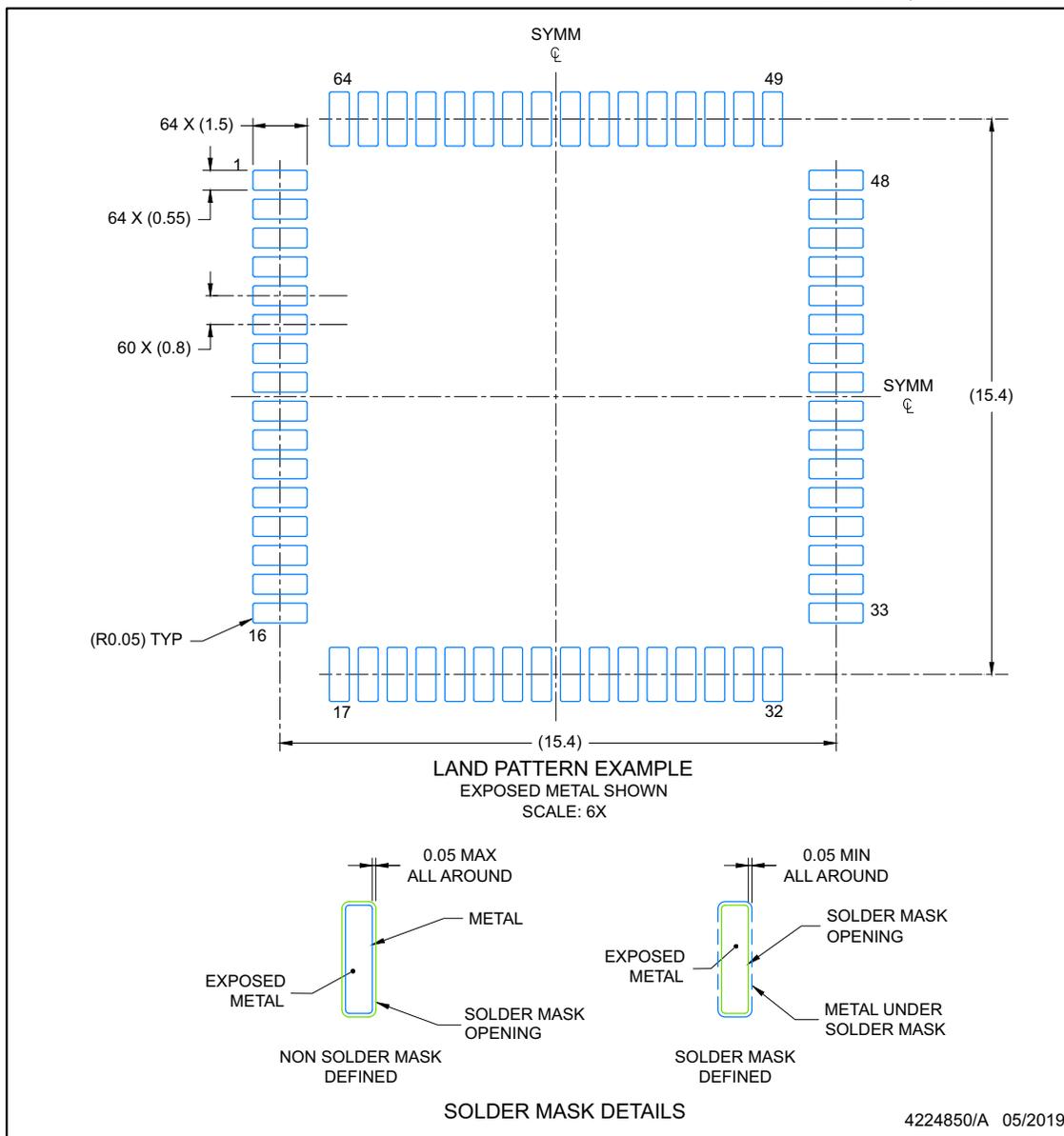
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.

EXAMPLE BOARD LAYOUT
HTQFP - 1.2 mm max height

PHD0064B

PLASTIC QUAD FLATPACK



NOTES: (continued)

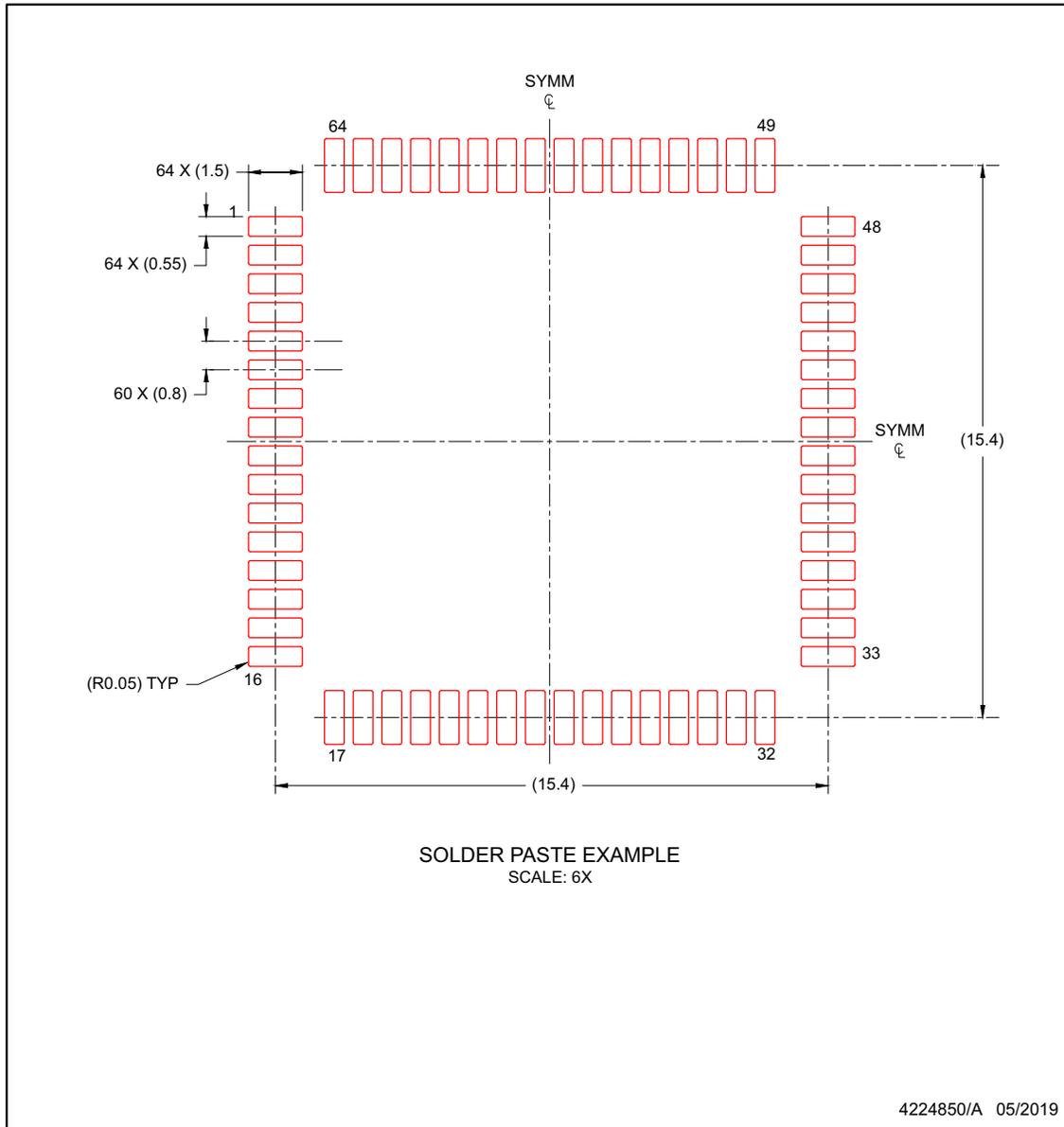
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PHD0064B

HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8773301EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A
CD54HC4511F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A
CD54HC4511F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A
CD74HC4511E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4511E
CD74HC4511E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4511E
CD74HC4511EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4511E
CD74HC4511M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC4511M
CD74HC4511M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC4511M
CD74HC4511M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M
CD74HC4511M96G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M
CD74HC4511M96G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M
CD74HC4511PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511
CD74HC4511PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511
CD74HC4511PWRE4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511
CD74HC4511PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511
CD74HC4511PWT	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	HJ4511
CD74HCT4511E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4511E
CD74HCT4511E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4511E

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HC4511, CD74HC4511 :

- Catalog : [CD74HC4511](#)
- Military : [CD54HC4511](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4511M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4511M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4511PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4511M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC4511M96G4	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC4511PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

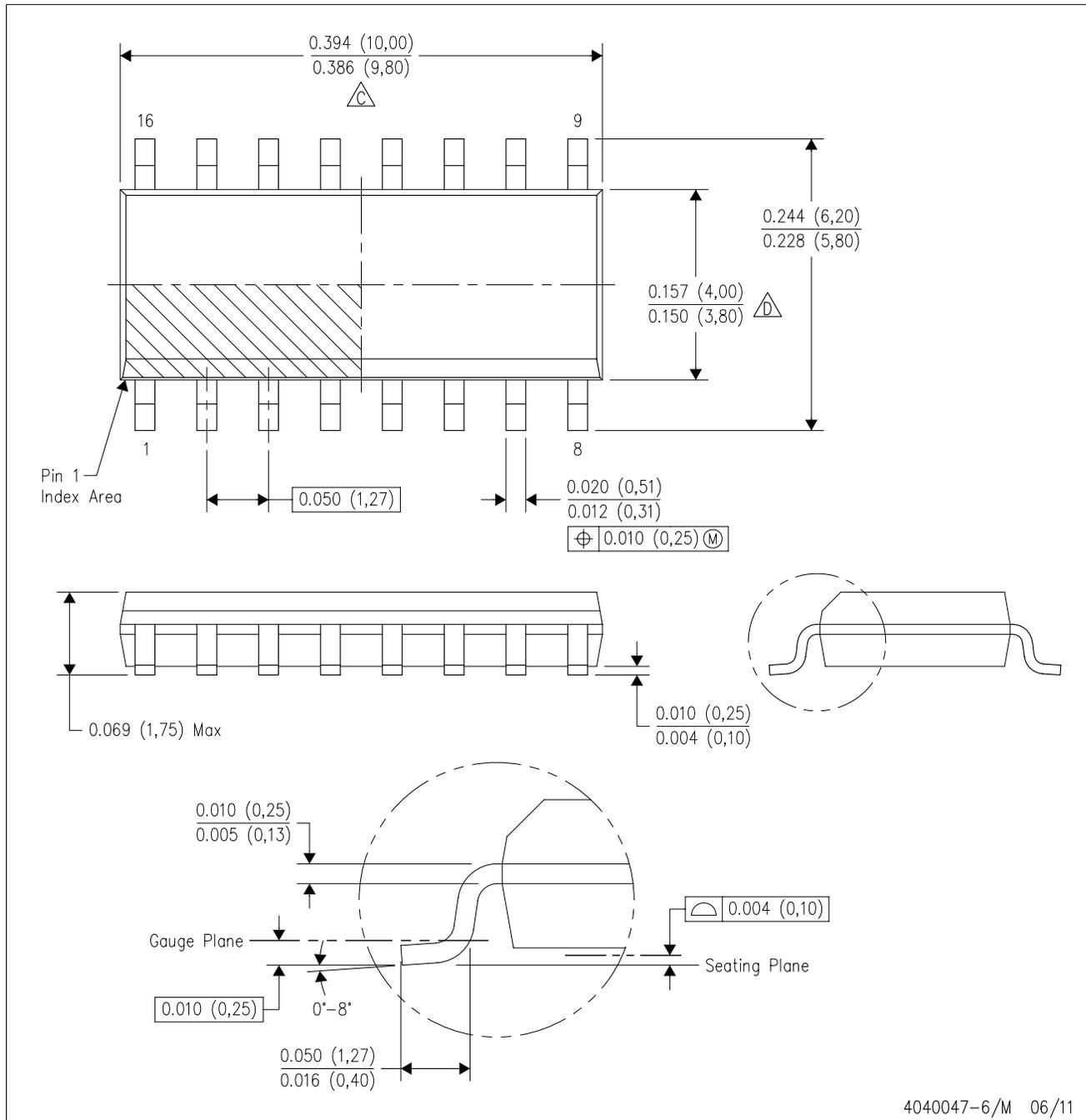
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511E.A	N	PDIP	16	25	506	13.97	11230	4.32

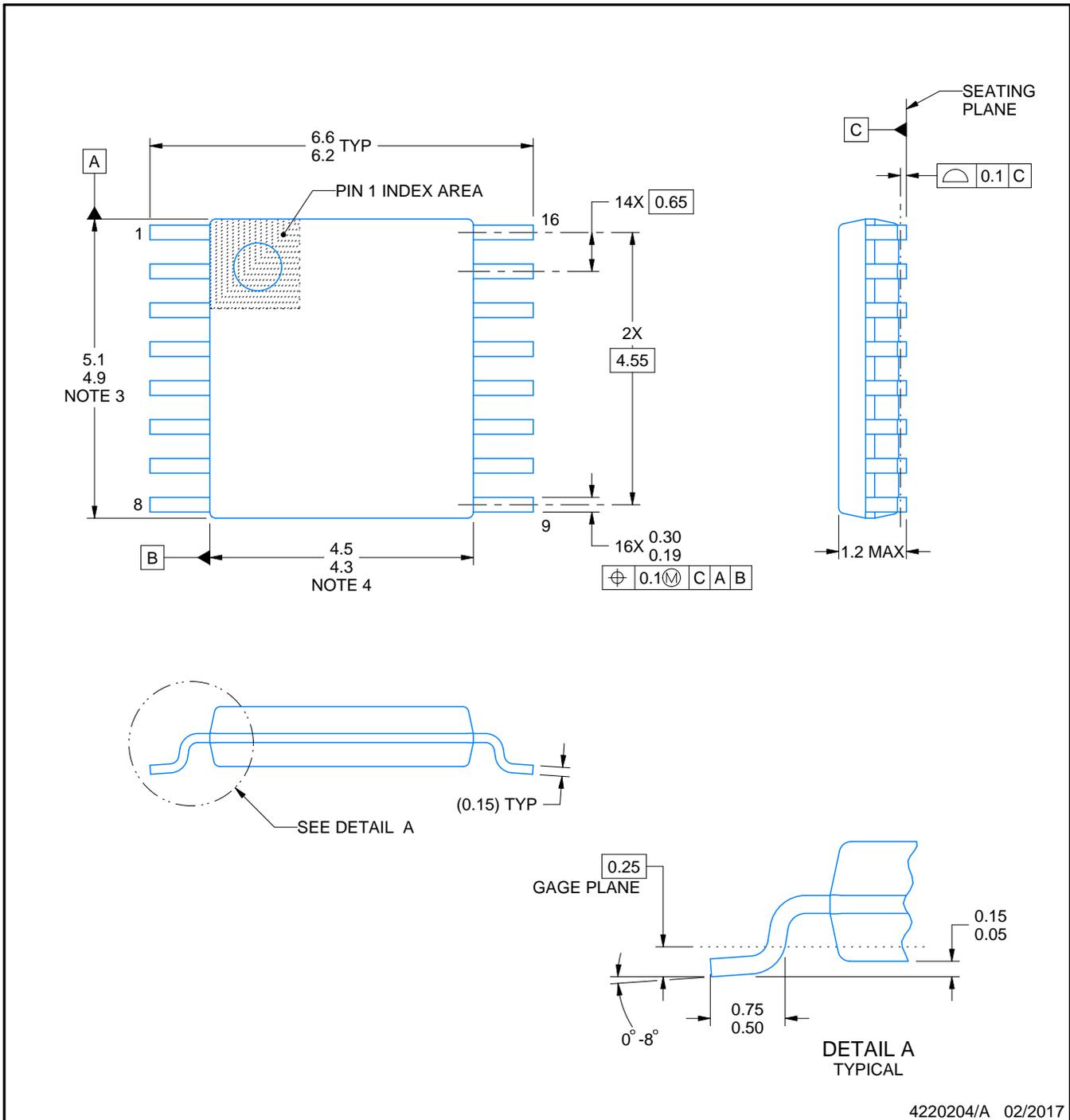
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

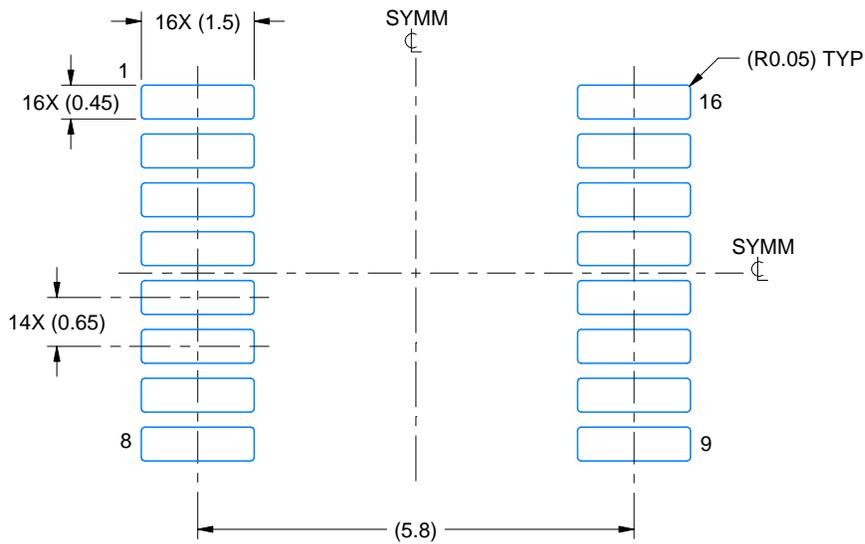
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

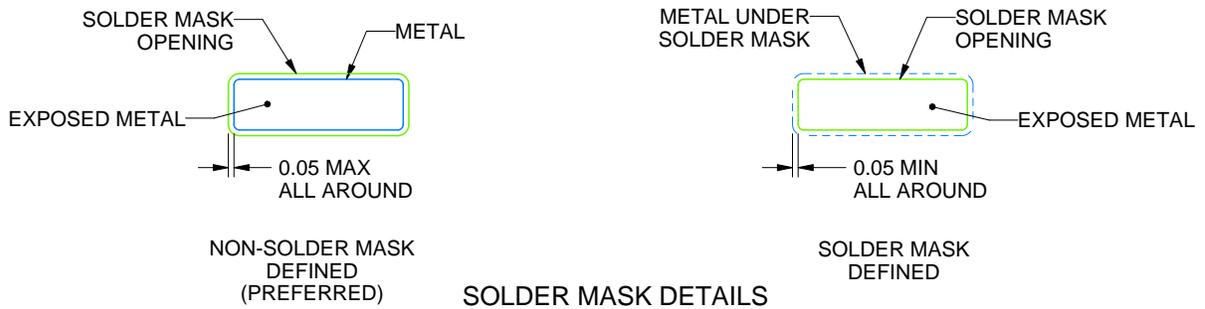
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

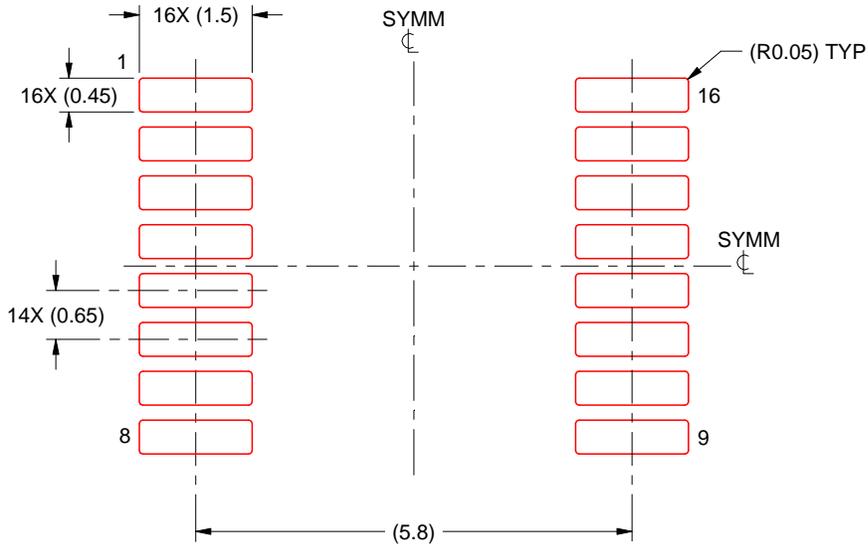
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

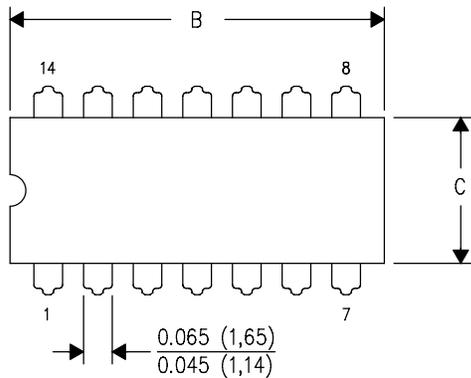
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

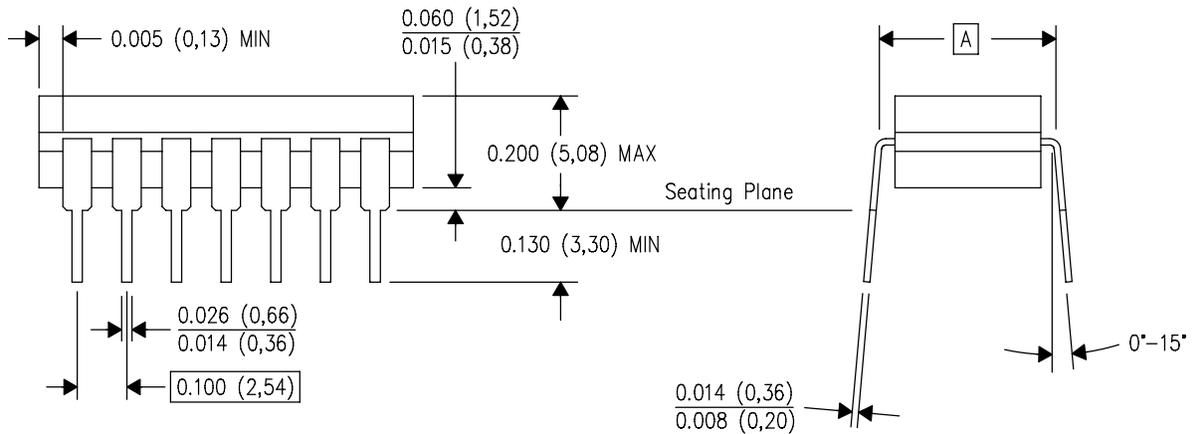
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



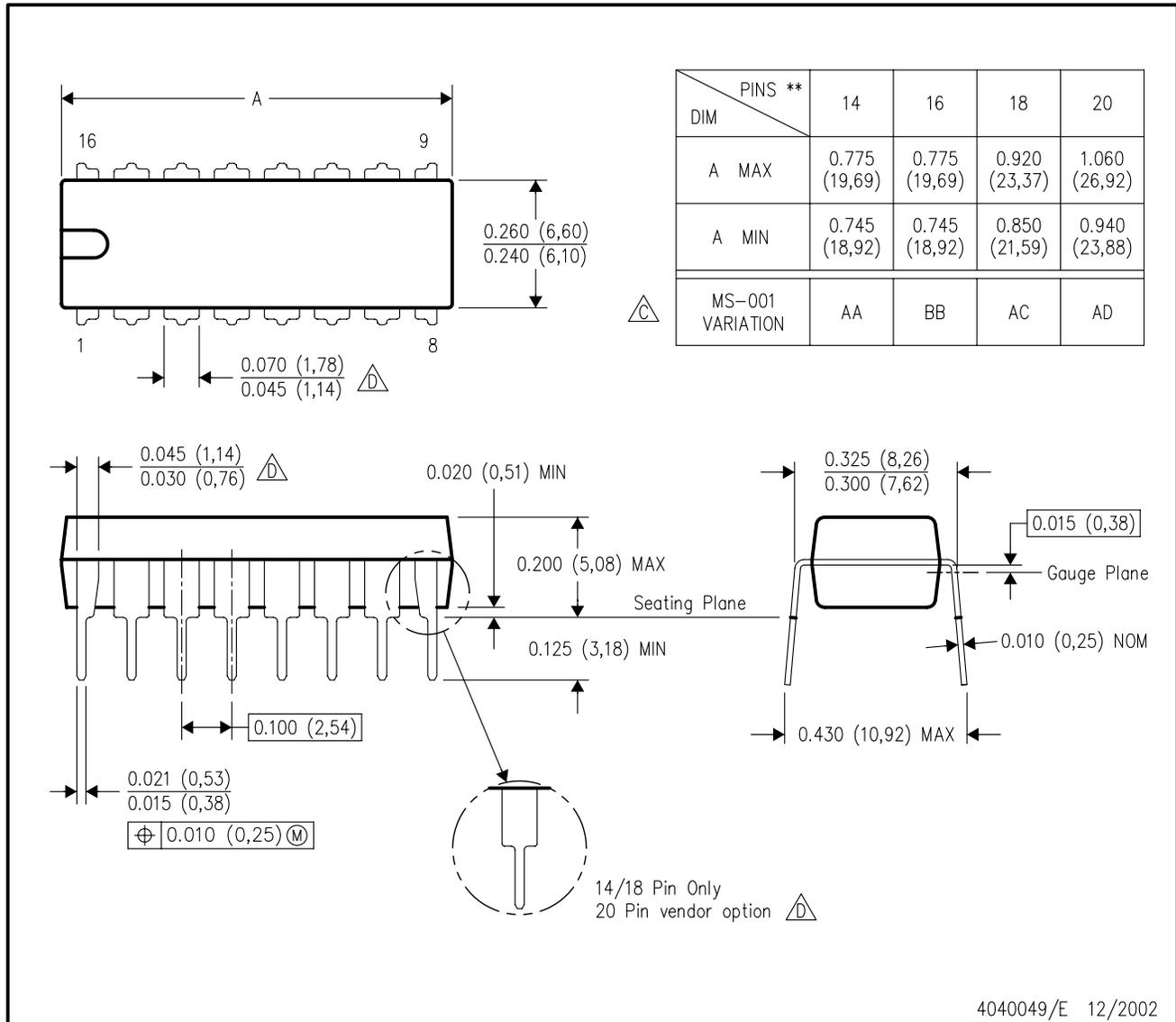
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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