MP6614

35V, H-Bridge DC Motor Driver with SOIC-8 Package

DESCRIPTION

The MP6614 is an H-bridge motor driver designed to drive reversible motors. The device can drive one DC motor, one winding of a stepper motor, or other loads. The H-bridge integrates four N-channel power MOSFETs, and an internal charge pump generates the required gate driver voltages.

The MP6614 operates across a 5V to 35V input supply (V_{IN}) range. It can deliver up to 2A of continuous current (I_{OUT}), depending on the thermal and PCB layout.

The MP6614 provides a pulse-width modulation (PWM) input interface that is compatible with industry-standard devices. A brake is applied to stop the motor, and a very low standby circuit current can be achieved when the device is disabled.

An internal current-sense circuit provides an output voltage (V_{ISEN}) that is proportional to the load current (I_{OUT}). In addition, cycle-by-cycle current regulation and limiting are provided. These features do not require a low-ohmic shunt resistor.

Internal protection features include over-current protection (OCP), short-circuit protection (SCP), under-voltage lockout (UVLO), and over-temperature protection (OTP).

The MP6614 requires a minimal number of readily available, standard external components. The MP6614 is available in a SOIC-8EP package.

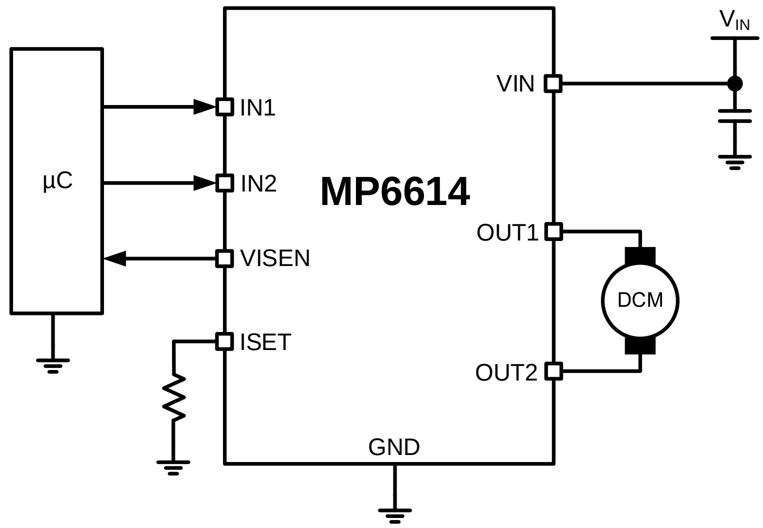
FEATURES

- Wide 5V to 35V Operating Input Voltage (V_{IN}) Range
- Internal Full H-Bridge Driver Supports 100% Duty Cycle
- 2A Continuous Output Current (I_{OUT})
- Low On Resistance ($R_{DS(ON)}$) per MOSFET:
  - 280mΩ High-Side MOSFET (HS-FET)
  - 220mΩ Low-Side MOSFET (LS-FET)
- Simple, Versatile Logic Interfaces
- 3.3V and 5V Compatible Logic Supply
- Cycle-by-Cycle Current Regulation and Limiting
- Low Standby Circuit Current
- Over-Current Protection (OCP)
- Thermal Shutdown
- Under-Voltage Lockout (UVLO)
- Internal Charge Pump
- Available in a Thermally Enhanced, Surface-Mounted SOIC-8EP Package

APPLICATIONS

- Solenoid Drivers
- Brushed DC Motor Drivers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6614GN	SOIC-8EP	*See Below*	2a

* For Tape & Reel, add suffix -Z (e.g. MP6614GN-Z).

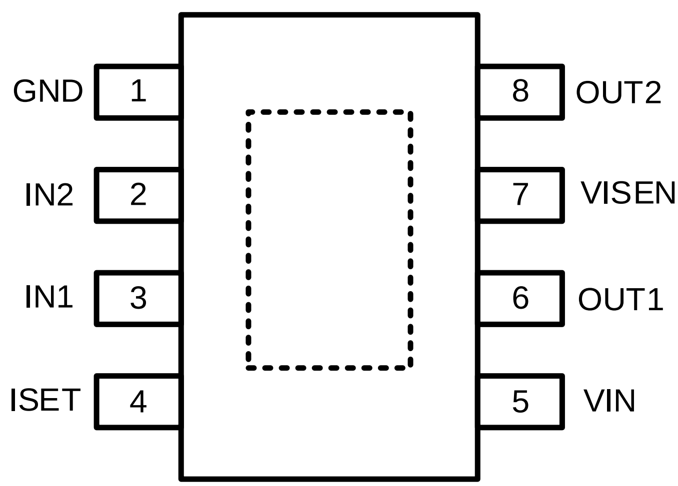
TOP MARKING

MP6614
LLLLLLLL
MPSYWW

MP6614: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE

TOP VIEW



SOIC-8EP

PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	IN2	**Input 2.** Internal pull-down resistor 1.
3	IN1	**Input 1.** Internal pull-down resistor 2.
4	ISET	**Output current-setting resistor.** Connect a resistor between the ISET pin and ground to set the current limit and the VISEN pin's output voltage.
5	VIN	**Supply voltage.** Place an input capacitor connected to the VIN pin to minimize voltage spikes at the input.
6	OUT1	**Output terminal 1.**
7	VISEN	**Current-sense output voltage.**
8	OUT2	**Output terminal 2.**
EP	GND	**Exposed pad.** Connect the exposed pad to GND.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ....-0.3V to +38V
Output voltages (V_{OUT1}, V_{OUT2})............................
....-0.3V to V_{IN} + 0.3V
ISET voltage (V_{ISET}) ....-0.3V to +5V
All other pins to GND ....-0.3V to +6V
Continuous power dissipation........(T_A = 25°C) (2)
SOIC-8EP 2.6W
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) 1KV
Charged device model (CDM) 750V

Recommended Operating Conditions (3)

V_{IN}..5V to 35V
Continuous output current (I_{OUT}) .... ±2A
Load current (I_{VISEN}) .... ±2mA
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
SOIC-8EP	48	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may produce an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7, a 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Input supply voltage	V_{IN}		5		35	V
Start-up threshold	V_{IN_ON}	V_{IN} rising edge		4.4	4.7	V
Shutdown hysteresis	V_{IN_HYS}			0.2		V
IC Supply						
Shutdown current	I_{IN_SD}	IN1 = IN2 = 0		0.1	1	µA
Operating current		IN1 or IN2 = 1, no load current		1.3	2.5	mA
		50kHz PWM, no load current		1.6	3	mA
Input Logic (IN1 and IN2)						
Input high voltage	V_{IH}		1.5			V
Input low voltage	V_{IL}				0.4	V
Input high current	I_{IH}	V_{IH} = 5V			50	µA
Input low current	I_{IL}	V_{IL} = 0V	-5		+5	µA
Input pull-down resistance	R_{PD}			300		kΩ
Sleep entry time		IN1 = 0V, IN2 = 0V for 2ms		2	5	ms
Sleep recovery time		IN1 or IN2 or both = high		250	500	µs
Switching Frequency						
Externally applied pulse-width modulation (PWM) frequency	F_{PWM}				100	kHz
Power MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 100mA, T_A = 25°C		280	350	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	I_{OUT} = 100mA, T_A = 25°C		220	280	mΩ
Minimum on time				250		ns
Output enable time	t_1				200	ns
Output disable time	t_2				200	ns
Delay time	t_3				420	ns
	t_4				300	ns
Output rise time		R_{LOAD} = 20Ω		20	100	ns
Output fall time		R_{LOAD} = 20Ω		20	100	ns
Dead time				200		ns
Protections						
Over-current (OC) threshold			3.3	4	4.7	A
Over-current protection (OCP) retry time	t_{OCR}			1		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
OC deglitch time [5]				500		ns
Thermal shutdown				160		°C
Thermal shutdown hysteresis				25		°C
Current Control						
Off time after the load current reaches the current trip threshold (I_{TRIP})	t_{ITRIP}	After I_{TRIP}		15		µs
Blanking time				800		ns
ISET current	I_{ISET}	I_{OUT} = 1A	90	100	110	µA/A
Rising current trip voltage	V_{ITRIP_R}	At the VISEN pin	2.92	3	3.08	V
Falling current trip voltage	V_{ITRIP_F}	At the VISEN pin	2.34	2.4	2.46	V
VISEN Output Voltage						
VISEN output voltage accuracy	ΔV_{ISEN}	0.1V < V_{ISET} < 0.5V	-10		+10	%
		V_{ISET} > 0.5V	-5		+5	%

Note:

5) Guaranteed by design.

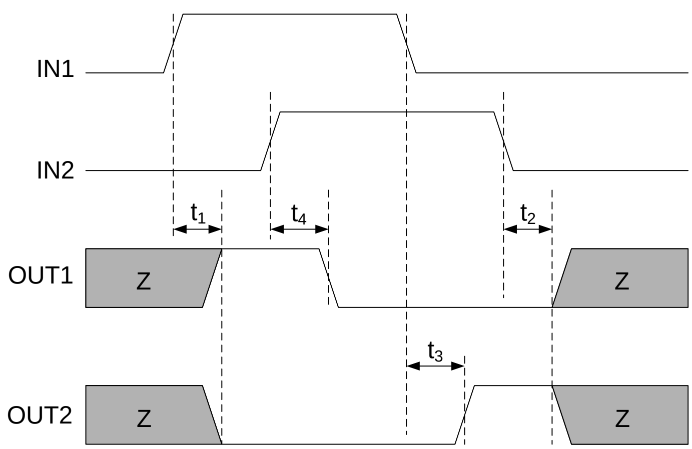
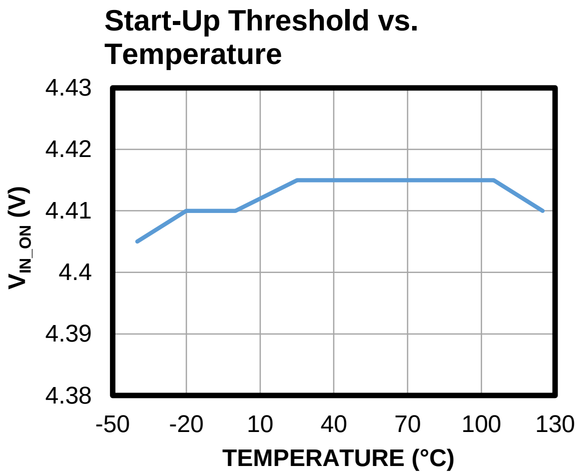
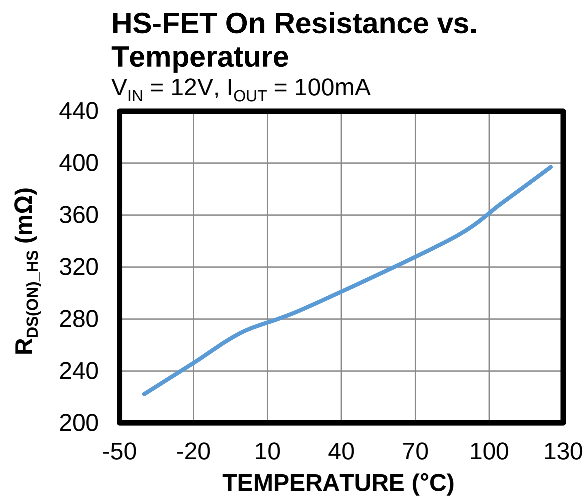


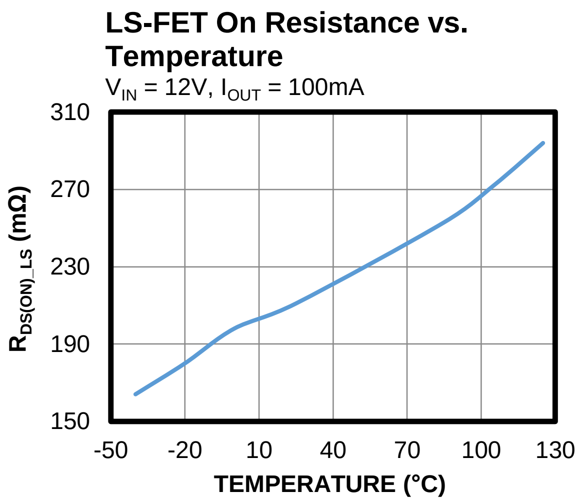
Figure 1: Input/Output Timing Diagram

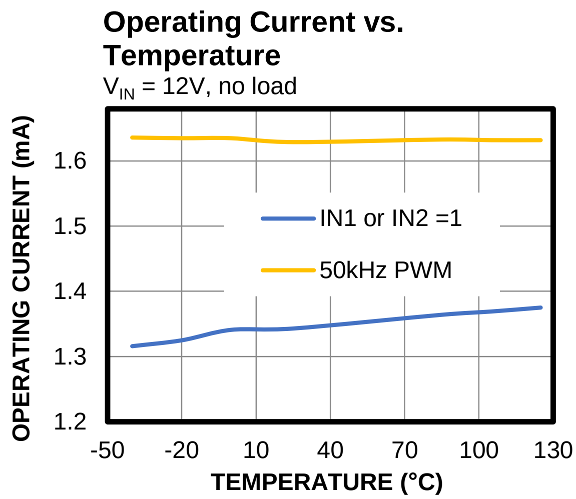
TYPICAL CHARACTERISTICS

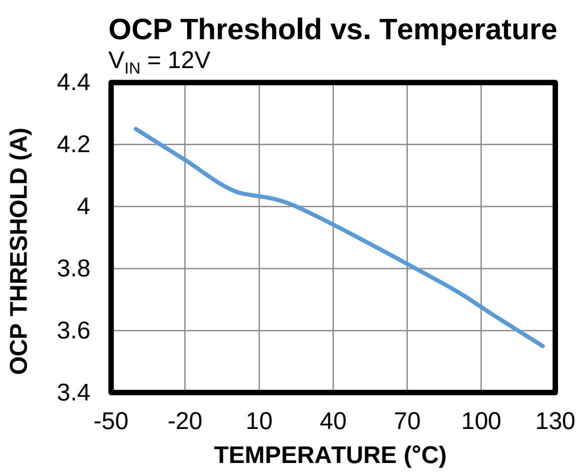
V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

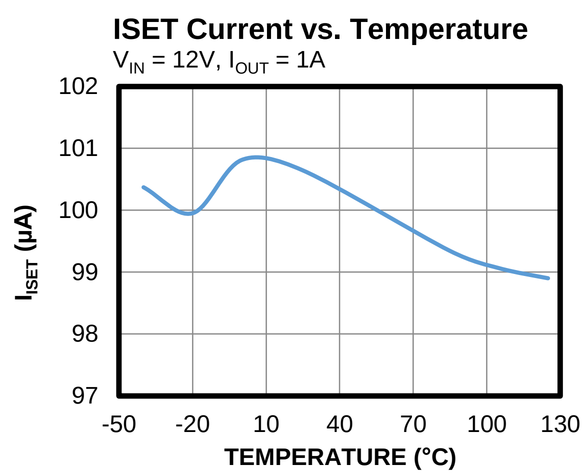






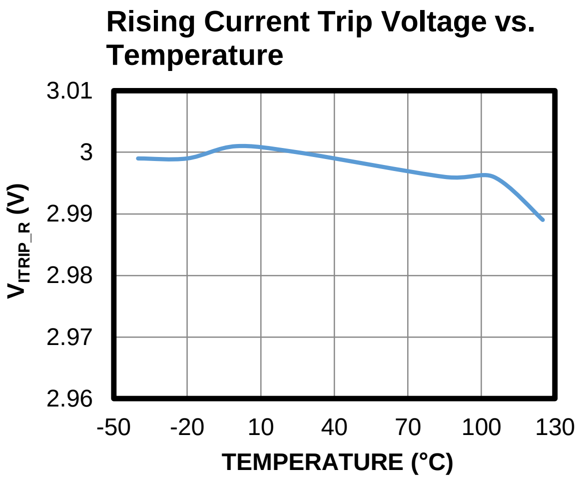


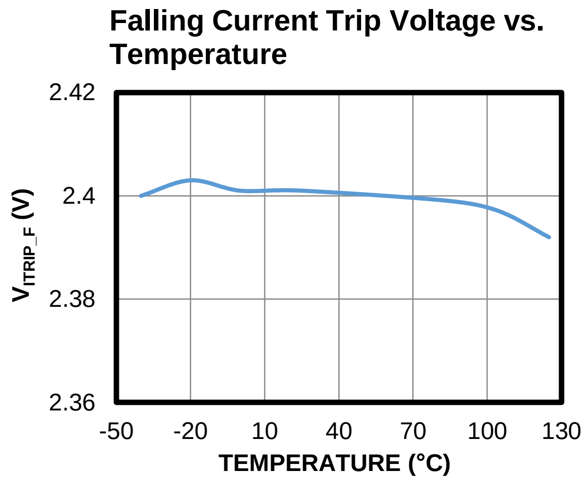




TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

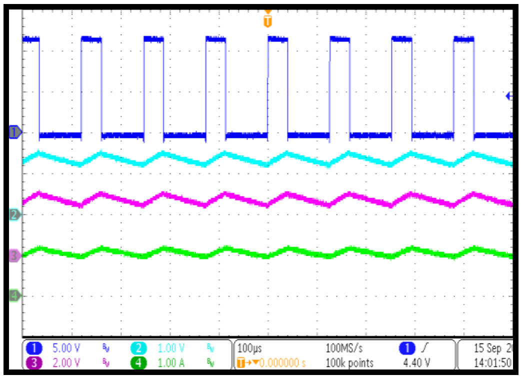




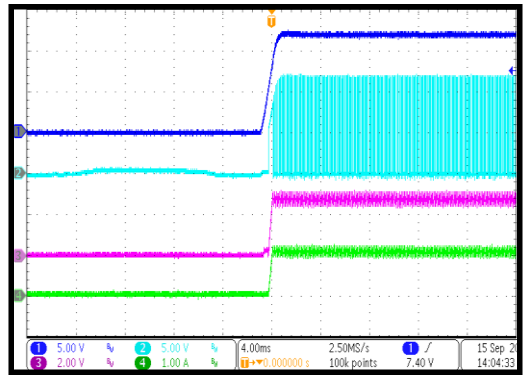
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{IN1} = 3.3V, V_{IN2} = 0V, I_{OUT} = 1.2A, output current-setting resistor = 12.5kΩ, T_A = 25°C, resistor + inductor load: 3Ω + 1.5mH between OUT1 and OUT2, unless otherwise noted.

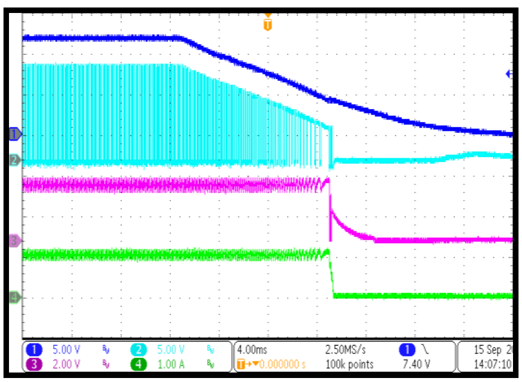
Steady State



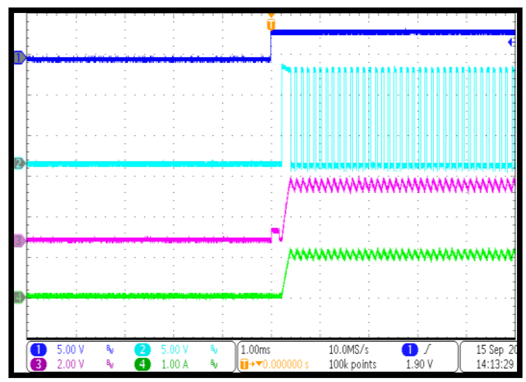
Power Ramping Up



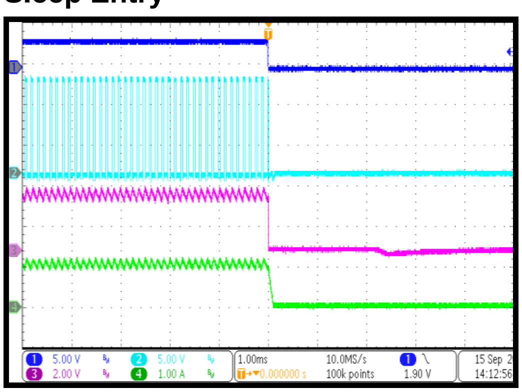
Power Ramping Down



Sleep Recovery



Sleep Entry



FUNCTIONAL BLOCK DIAGRAM

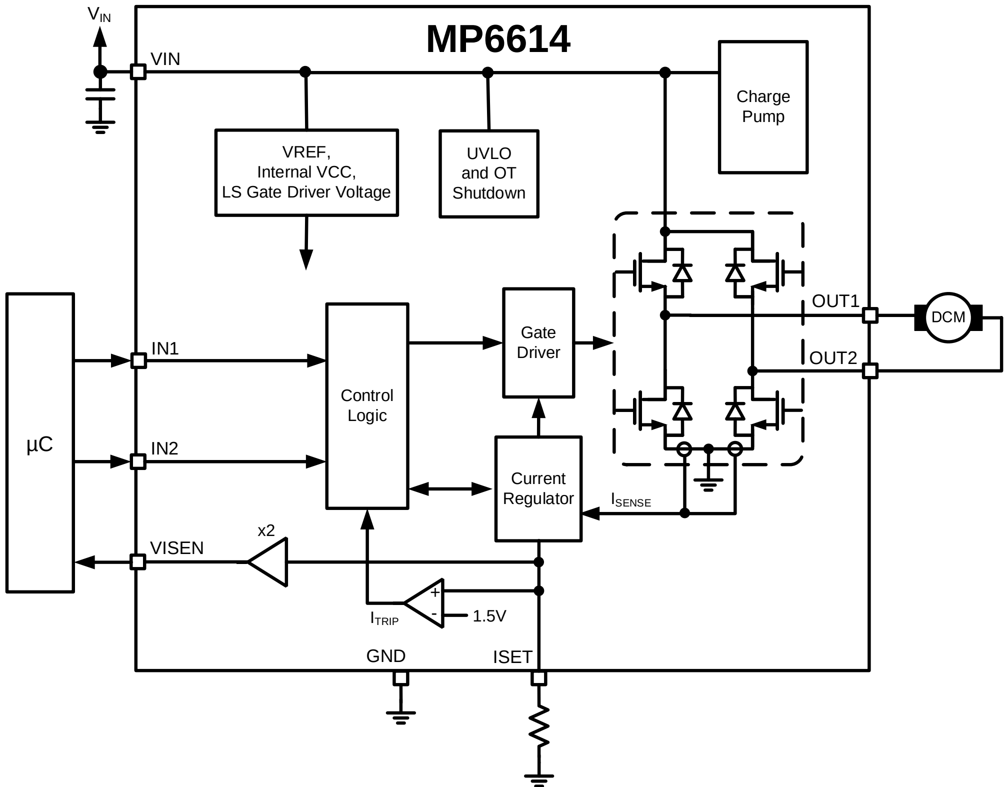


Figure 2: Functional Block Diagram

OPERATION

The MP6614 is an H-bridge motor driver designed to drive bipolar stepper motors, brushed DC motors, solenoids, and other loads. It integrates four N-channel power MOSFETs with a 2A continuous output current (I_{OUT}) capability. The device operates across a wide 5V to 35V input voltage (V_{IN}) range.

Current Sensing

The current flowing into the two low-side MOSFETs (LS-FETs) is sensed via an internal current-sense circuit. A voltage proportional to I_{OUT} is sourced on the VISEN pin.

The VISEN output voltage (V_{ISEN}) is twice the voltage on the ISET pin (V_{ISET}), which is set via a resistor connected between ISET and ground. For a 1A I_{OUT}, a 100µA current is sourced into the resistor connected to ISET. For example, if a 10kΩ resistor is connected between ISET and ground, V_{ISET} is 1V/A of I_{OUT}, and V_{ISEN} is 2V/A of I_{OUT}.

When one of the LS-FETs turns on, current is sensed, including during slow decay (brake) mode.

The load current applied to VISEN (I_{VISEN}) should remain below 2mA, with a maximum 500pF capacitance.

Current Regulation and Limiting

The current in the outputs is limited using constant off-time pulse width modulation (PWM) control circuitry.

Figure 3 shows the current regulation and limiting operation. A diagonal pair of MOSFETs turns on and drives current through the load. The current increases in the load, which is sensed by the internal current-sense circuit.

If the load current reaches the current trip threshold, the H-bridge switches to slow decay mode, with the two LS-FETs turned on.

An off time occurs after the load current reaches the current trip threshold (I_{TRIP}). After (t_{ITRIP}), if the load current falls at least 20% below the current trip threshold (I_{TRIP}), the MOSFETs are re-enabled and the cycle repeats.

If the current still does not reach 20% below I_{TRIP}, t_{ITRIP} is extended until the current falls to 20% below I_{TRIP}.

I_{TRIP} is reached when V_{ISET} reaches 1.5V. For example, with a 10kΩ resistor connected between ISET and ground, V_{ISET} is 1V/A of I_{OUT}. Once the current reaches 1.5A, V_{ISET} reaches 1.5V, V_{ISEN} reaches 3V, and a current trip occurs.

Blanking Time

Current spikes often occur during start-up due to the body diode's reverse-recovery current or the load's shunt capacitance. This current spike requires filtering to prevent it from erroneously shutting down the high-side MOSFET (HS-FET). An internal, fixed blanking time blanks the current-sense comparator's output when the outputs are switched. This blanking time also sets the HS-FET's minimum on time.

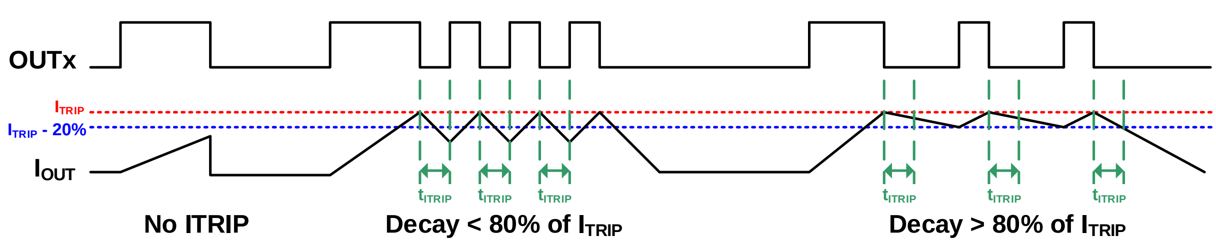


Figure 3: Current Regulation and Limiting Operation

Input Logic

The MP6614 is controlled by a PWM input interface that is compatible with industry-standard devices. Table 1 shows the MP6614's input logic:

Table 1: Input Logic

IN1	IN2	OUT1	OUT2	Function (DC Motor)
L	L	Hi-Z	Hi-Z	Coast (enter sleep mode after 2ms)
L	H	L	H	Reverse current (OUT2 to OUT1)
H	L	H	L	Forward current (OUT1 to OUT2)
H	H	L	L	Brake (low-side slow decay)

nSLEEP Operation

If the input pins (IN1 and IN2) remain low for 2ms, then the MP6614 enters a low-power sleep mode. In this state, all unnecessary internal circuitry shuts down. If the device starts up while both inputs are low, then the MP6614 immediately enters sleep mode. If either IN1 or IN2 are pulled high for a minimum 50ns, the device exits sleep mode and resumes normal operation after 250µs.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through each MOSFET by reducing the gate driver voltage to the MOSFET. If the MOSFET's current limit condition lasts longer than the over-current (OC) deglitch time, all the MOSFETs in the H-bridge are disabled. The driver remains disabled for the OCP retry time (t_{OCR}) and then is re-enabled automatically.

OC conditions such as a short to ground, supply, or across the motor winding are sensed on both high-side (HS) and low-side (LS) devices, resulting in an OC shutdown.

Note that OCP does not use the current-sense circuitry used for PWM current control, and it is independent of the ISET resistance.

Junction Over-Temperature Protection (OTP)

If the IC's junction temperature (T_J) exceeds safe limits, the device stops switching. Once T_J drops to a safe temperature, the IC resumes normal operation.

Input Under-Voltage Lockout (UVLO) Protection

If V_{IN} drops below the under-voltage lockout (UVLO) threshold, all the circuitry in the device is disabled, and the internal logic resets. Operation resumes once V_{IN} exceeds the UVLO threshold.

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the supply bypass capacitors as close to the IC as possible.
2. Place multiple thermal vias under the exposed pad to improve thermal dissipation. This allows heat to move between the IC and a plane located on the PCB's backside.
3. Place as many GND vias near the input capacitors as possible to improve thermal performance.

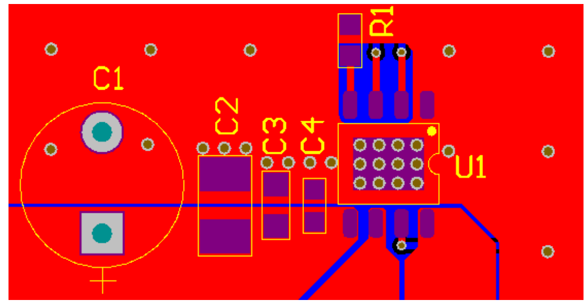
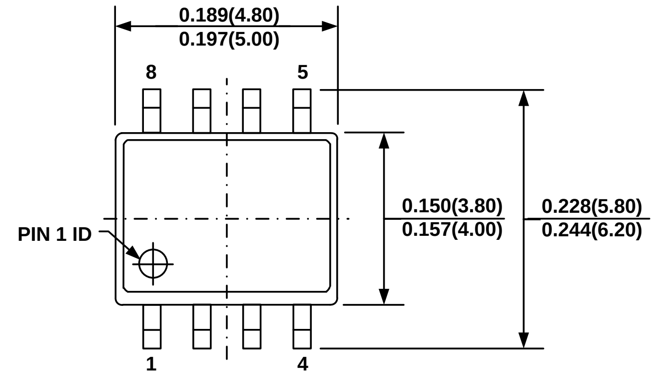


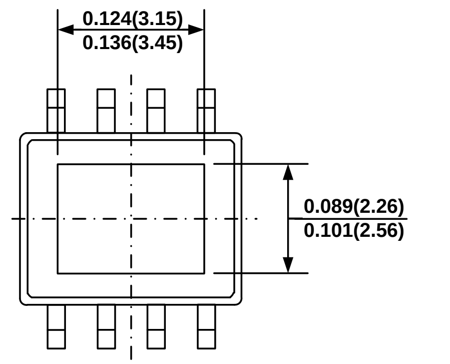
Figure 4: Recommended PCB Layout

PACKAGE INFORMATION

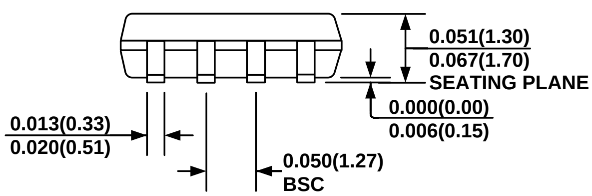
SOIC-8EP



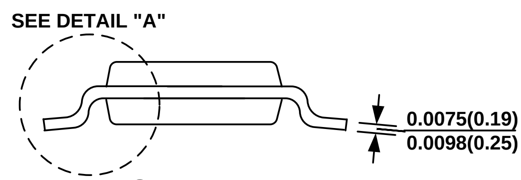
TOP VIEW



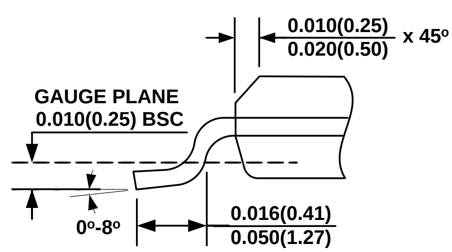
BOTTOM VIEW



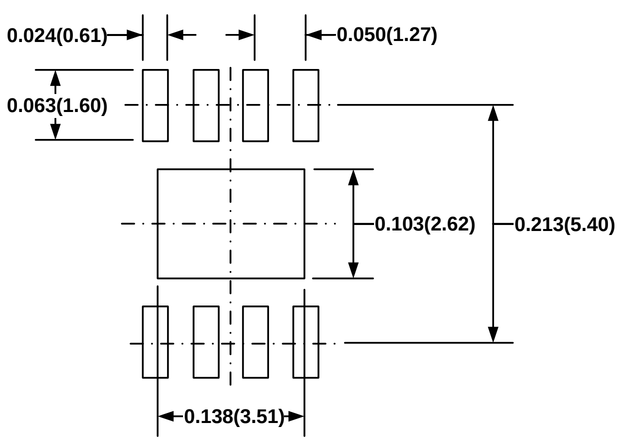
FRONT VIEW



SIDE VIEW



DETAIL "A"

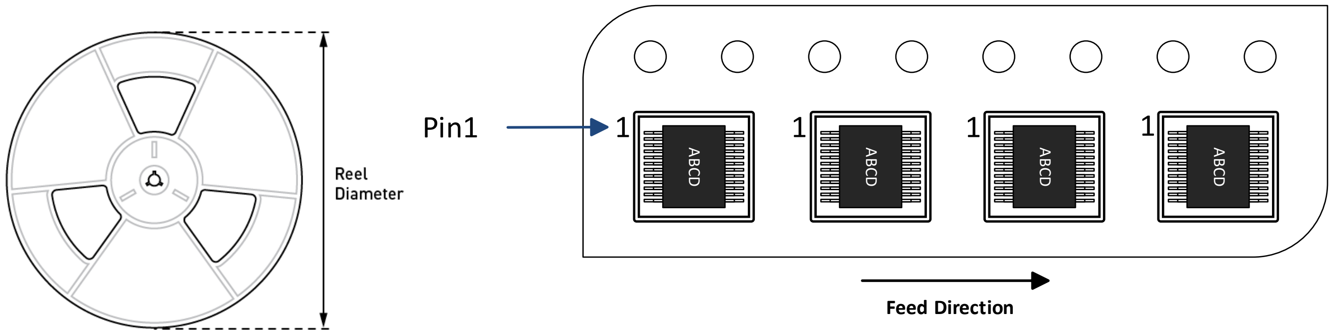


RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6614GN-Z	SOIC-8EP	2500	100	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/24/2023	Initial Release	-