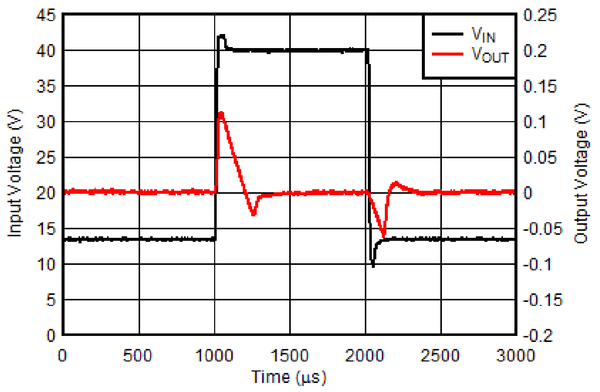
TPS7B84-Q1 Automotive, 150mA, 40V, Adjustable, Low-Dropout Regulator

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Input voltage range: 3V to 40V (42V max)
- Output voltage range:
  - Adjustable output: 1.2V to 18V
  - Fixed output: 3.3V and 5V
- Output current: up to 150mA
- Output voltage accuracy: ±0.75% (max)
- Low dropout voltage:
  - 225mV (max) at 150mA ($V_{OUT} \geq 3.3V$)
- Low quiescent current:
  - 18µA (typ)
  - 4µA (max) when disabled
- Excellent line transient response:
  - ±2% V_{OUT} deviation during cold-crank
  - ±2% V_{OUT} deviation (1V/µs V_{IN} slew rate)
- Stable with a 2.2µF or larger capacitor
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Package options:
  - DRB (8-pin VSON), $R_{\theta JA}$: 50.8°C/W
  - DCY (4-pin SOT-223), $R_{\theta JA}$: 85.5°C/W

2 Applications

- Reconfigurable instrument clusters
- Body control modules (BCM)
- Always-on, battery-connected applications:
  - Automotive gateways
  - Remote keyless entries (RKE)



Line Transient Response (3V/µs V_{IN} Slew Rate)

3 Description

The TPS7B84-Q1 is a low-dropout linear regulator designed to connect to the battery in automotive applications. The device has an input voltage range extending to 40V, which allows the device to withstand transients (such as load dump) that are anticipated in automotive systems. With only an 18µA quiescent current, the device is an optimal solution for powering always-on components such as microcontrollers (MCUs) and controller area network (CAN) transceivers in standby systems.

The TPS7B84-Q1 has both fixed and adjustable output types. The wide output voltage range allows the device to generate the bias voltage for silicon carbide (SiC) gate drivers and microphones as well as power MCUs and processors.

The device has state-of-the-art transient response that allows the output to quickly react to changes in load or line (for example, during cold-crank conditions). Additionally, the device has a novel architecture that minimizes output overshoot when recovering from dropout. During normal operation, the device has a tight DC accuracy of ±0.75% over line, load, and temperature.

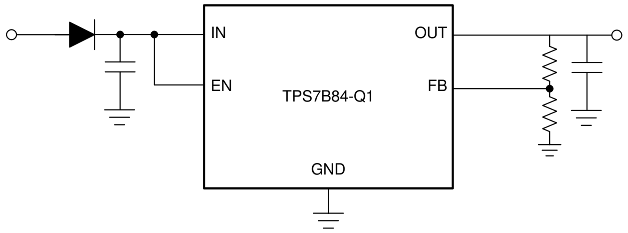
The device is available in both a SOT223 package and a small VSON package with wettable flanks that facilitates a compact printed circuit board (PCB) design. The low thermal resistance enables sustained operation despite significant dissipation across the device.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7B84-Q1	DRB (VSON, 8)	3mm × 3mm
	DCY (SOT-223, 4)	6.5mm × 7mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

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4 Pin Configuration and Functions

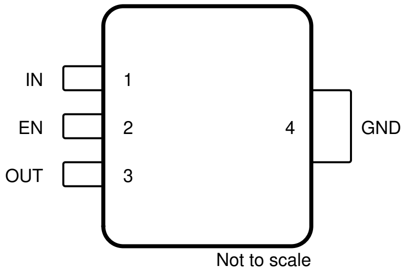


Figure 4-1. DCY Package, 4-Pin SOT-223, Top View

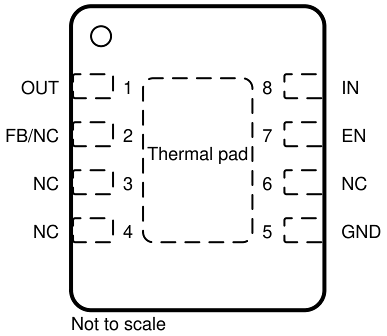


Figure 4-2. DRB Package, 8-Pin VSON, Top View

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	DCY	DRB		
EN	2	7	I	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). To ensure the device is enabled, the EN pin must be driven above the logic high level (V_{IH}). This pin should not be left floating as this pin is high impedance if it is left floating the part may enable or disable.
GND	4	5	G	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
FB/NC	—	2	I	Feedback pin when using an external resistor divider or an NC pin when using the device with a fixed output voltage. When using the adjustable device this pin must be connected through a resistor divider to the output for the device to function.
NC	—	3, 4, 6	—	No internal connection. Connect these pins to GND for the best thermal performance.
IN	1	8	I	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input Capacitor* section. Place the input capacitor as close to the input of the device as possible.
OUT	3	1	O	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Output Capacitor* section. Place the output capacitor as close to output of the device as possible. If using a high ESR capacitor, decouple the output with a 100-nF ceramic capacitor.
Thermal pad	—	Pad	—	Thermal pad. Connect the pad to GND for the best possible thermal performance. See the *Layout* section for more information.

(1) I = input; O = output; G = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN	Unregulated input	–0.3	42	V
EN	Enable input	–0.3	42	V
OUT	Regulated output	–0.3	V_{IN} + 0.3(2)	V
FB	Feedback	–0.3	20	V
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* isnot implied. Exposure to absolute-maximum-rated conditions for extended periods may affect devicereliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 20 V, whichever is smaller.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	3		40	V
V_{OUT}	Output voltage	1.2		18	V
I_{OUT}	Output current	0		150	mA
F_{EN}	Enable pin frequency(1)			5	kHz
V_{EN}	High voltage (I/O)	0		40	V
C_{OUT}	Output capacitor(3)	2.2		220	µF
ESR	Output capacitor ESR requirements(4)	0.001		2	Ω
C_{IN}	Input capacitor(2)	0.1	1		µF
T_J	Operating junction temperature	–40		150	°C

(1) Minimum pulse time on the EN pin is 100 µs.
(2) For robust EMI performance the minimum input capacitance is 500 nF.
(3) Effective output capacitance of 1 µF minimum required for stability.
(4) If using a large ESR capacitor it is recommended to decouple this with a 100-nF ceramic capacitor to improve transient performance.

5.4 Thermal Information

THERMAL METRIC(1) (2)		TPS7B84-Q1		Unit
		DRB (VSON)	DCY	
		8 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(3)	50.8	85.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.6	46.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.9	11.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.9	11	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	11	°C/W

(1) The thermal data is based on the JEDEC standard high K profile,JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered tothe thermal land pattern. Also, correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics,see the Semiconductor and IC PackageThermal Metrics application report.
(3) The 1s0p $R_{\theta JA}$ is 212.7°C/W for the DRB package and 168.8°C/W for the DCY package.

5.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Regulated output accuracy	V_{IN} = V_{OUT} + 500 mV to 40 V, I_{OUT} = 100 µA to 150 mA (2) (1)	T_J = 25ºC	–0.5		0.5	%
			T_J = –40°C to +150ºC	–0.75		0.75	
V_{OUT}	Regulated output accuracy DCY	V_{IN} = V_{OUT} + 500 mV to 40 V, I_{OUT} = 100 µA to 150 mA (2) (1)	T_J = 25ºC	–0.75		0.75	%
			T_J = –40°C to +150ºC	–1		1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	Change in percent of output voltage	V_{IN} = V_{OUT} + 500 mV to 40 V, I_{OUT} = 100 µA			0.2	%
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	Change in percent of output voltage	V_{IN} = V_{OUT} + 500 mV, I_{OUT} = 100 µA to 150 mA, V_{OUT} ≥ 3.3 V			0.2	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation (Adjustable output only)	Change in percent of output voltage	V_{IN} = V_{OUT} + 500 mV, I_{OUT} = 100 µA to 150 mA, V_{OUT} < 3.3 V			0.3	%
ΔV_{OUT}	Load transient response settling time(4) (5)	C_{OUT} = 10 µF	C_{OUT} = 10 µF			100	µs
	Load transient response overshoot, undershoot(5)		I_{OUT} = 45 mA to 105 mA	–2%		10%	$\%V_{OUT}$
			I_{OUT} = 0 mA to 150 mA	–10%			
I_Q	Quiescent current	V_{IN} = V_{OUT} + 500 mV to 40 V, I_{OUT} = 0 mA (2)	T_J = 25ºC		18	21	µA
			T_J = –40°C to +150ºC			26	
		I_{OUT} = 500 µA (2)	T_J = –40°C to +150ºC			35	
$I_{SHUTDOWN}$	Shutdown supply current (I_{GND})	V_{EN} = 0 V	T_J = 25ºC			2.5	µA
			T_J = –40°C to +150ºC			4	
V_{DO}	Dropout voltage (DCY package)	I_{OUT} ≤ 1 mA, V_{OUT} ≥ 3.3 V, V_{IN} = $V_{OUT(NOM)}$ x 0.95				47	mV
		I_{OUT} = 105 mA, V_{OUT} ≥ 3.3 V, V_{IN} = $V_{OUT(NOM)}$			130	180	
		I_{OUT} = 150 mA, V_{OUT} ≥ 3.3 V, V_{IN} = $V_{OUT(NOM)}$			160	230	

5.5 Electrical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage (fixed output DRB package)	$I_{OUT} \leq 1$ mA, $V_{OUT} \geq 3.3$ V, $V_{IN} = V_{OUT(NOM)}$ x 0.95			43	mV
		I_{OUT} = 105 mA, $V_{OUT} \geq 3.3$ V, $V_{IN} = V_{OUT(NOM)}$		125	175	
		I_{OUT} = 150 mA, $V_{OUT} \geq 3.3$ V, $V_{IN} = V_{OUT(NOM)}$		155	225	
V_{DO}	Dropout voltage adjustable output DRB package	$I_{OUT} \leq 1$ mA, V_{IN} = 3 V, V_{FB} = 0.61 V(3)			43	mV
	Dropout voltage adjustable output	I_{OUT} = 105 mA, V_{IN} = 3 V, V_{FB} = 0.61 V(3)		140	195	
		I_{OUT} = 150 mA, V_{IN} = 3 V, V_{FB} = 0.61 V(3)		175	245	
V_{FB}	Feedback voltage	Reference voltage for FB	0.645	0.65	0.655	V
I_{FB}	Feedback current		-10		10	nA
$V_{UVLO(RISING)}$	Rising input supply UVLO	V_{IN} rising	2.6	2.7	2.82	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO	V_{IN} falling	2.38	2.5	2.6	V
$V_{UVLO(HYST)}$	V_{UVLO} hysteresis			230		mV
V_{IL}	Enable logic input low level				0.7	V
V_{IH}	Enable logic input high level		2			V
I_{EN}	EN pin current	$V_{EN} = V_{IN}$ = 13.5 V			50	nA
I_{CL}	Output current limit	$V_{IN} = V_{OUT(nom)}$ + 1 V, V_{OUT} short to 90% x $V_{OUT(NOM)}$	180	220	260	mA
PSRR	Power-supply ripple rejection	$V_{IN} - V_{OUT}$ = 500 mV, frequency = 1 kHz, I_{OUT} = 150 mA		55		dB
V_n	Output noise voltage	V_{OUT} = 3.3 V, BW = 10 Hz to 100 kHz		280		μV_{RMS}
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			20		°C

(1) Power dissipation is limited to 2W for IC production testing purposes. The power dissipation can be higher during normal operation. Please see the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150℃.
(2) For adjustable devices this parameter is tested in unity gain, so resistor divider tolerances and current is not included.
(3) Dropout is not measured for $V_{IN} \leq$ 3 V.
(4) The settling time is measured from when I_{OUT} is stepped from 45mA to 105 mA to when the output voltage recovers to $V_{OUT} = V_{OUT(nom)}$ - 5 mV.
(5) This specification is specified by design.

5.6 Typical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)

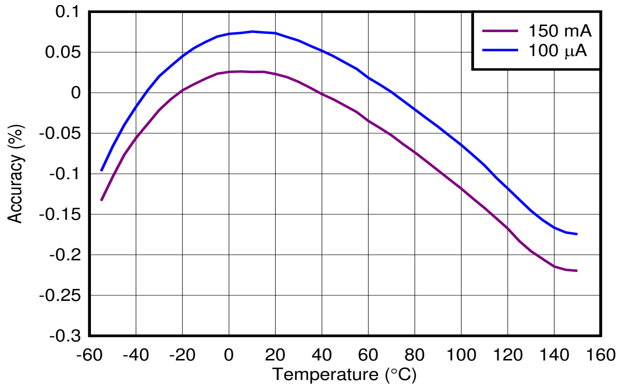
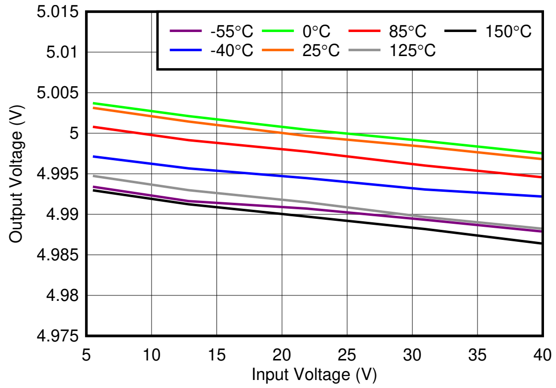
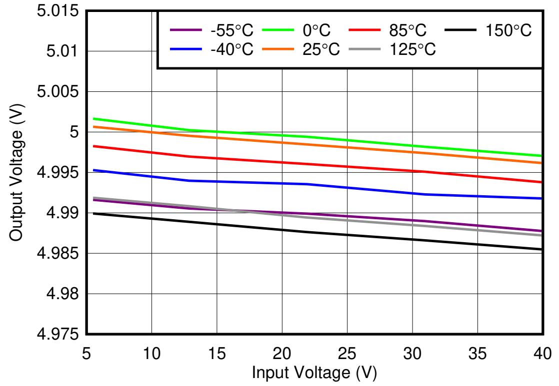


Figure 5-1. Accuracy vs Temperature



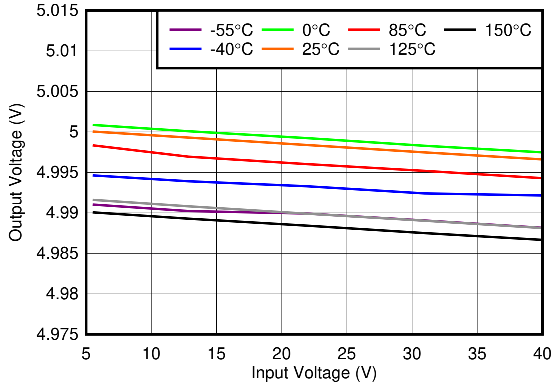
V_{OUT} = 5 V, I_{OUT} = 150 mA

Figure 5-2. Line Regulation vs V_{IN}



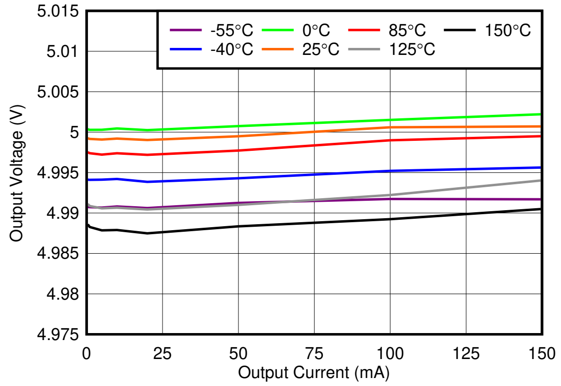
V_{OUT} = 5 V, I_{OUT} = 5 mA

Figure 5-3. Line Regulation vs V_{IN}



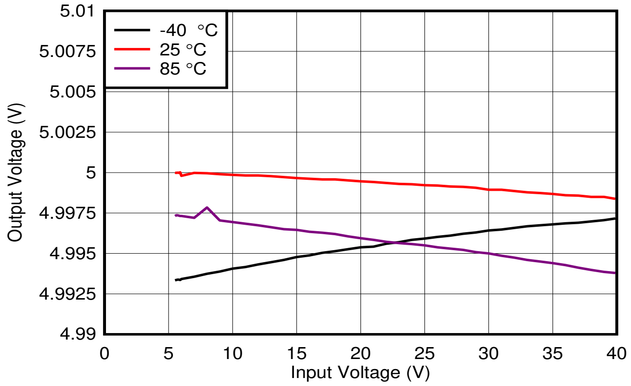
V_{OUT} = 5 V, I_{OUT} = 1 mA

Figure 5-4. Line Regulation vs V_{IN}



V_{OUT} = 5 V

Figure 5-5. Load Regulation vs I_{OUT}

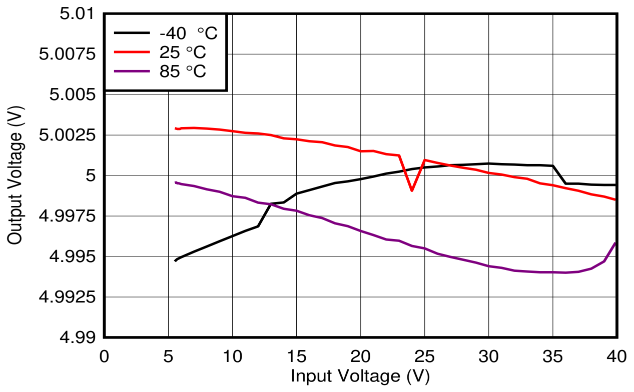


C_{OUT} = 10 µF

Figure 5-6. Line Regulation at 50 mA

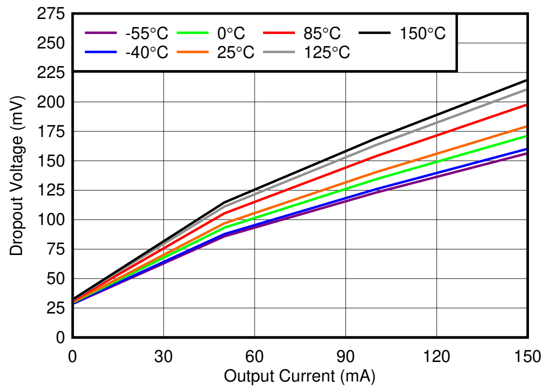
5.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



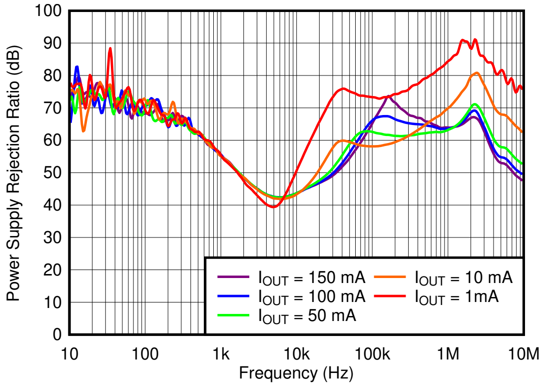
C_{OUT} = 10 µF

Figure 5-7. Line Regulation at 100 mA



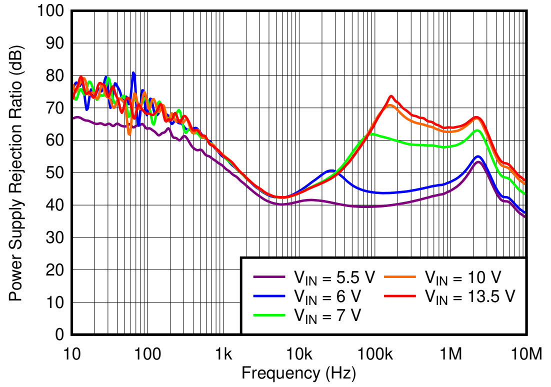
V_{IN} = 3 V

Figure 5-8. Dropout Voltage (V_{DO}) vs I_{OUT}



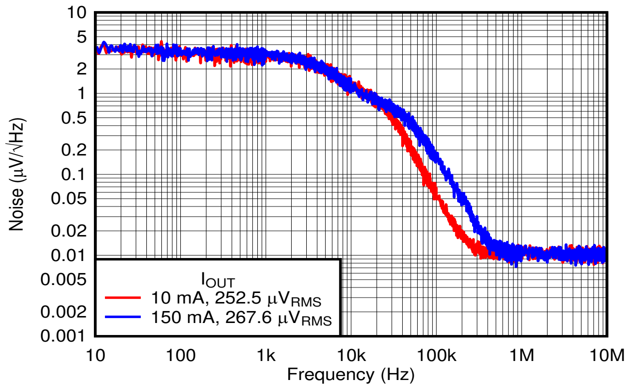
C_{OUT} = 10 µF (X7R 50 V), V_{OUT} = 5 V

Figure 5-9. PSRR vs Frequency and I_{OUT}



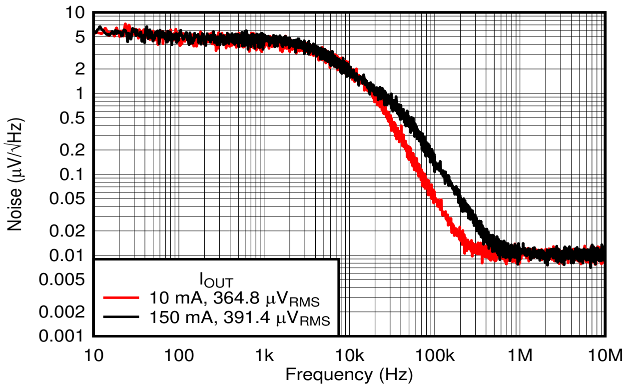
C_{OUT} = 10 µF (X7R 50 V), I_{OUT} = 150 mA, V_{OUT} = 5 V

Figure 5-10. PSRR vs Frequency and V_{IN}



V_{OUT} = 3.3 V, C_{OUT} = 10 µF

Figure 5-11. Noise vs Frequency at 3.3 V

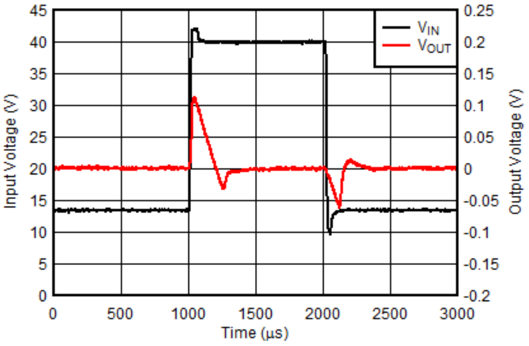


V_{OUT} = 5 V, C_{OUT} = 10 µF

Figure 5-12. Noise vs Frequency at 5.0 V

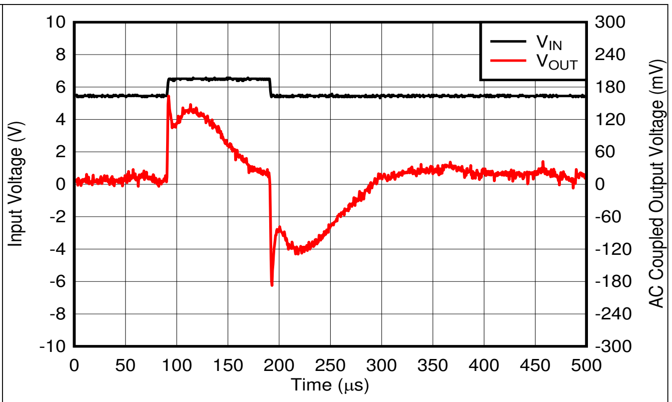
5.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



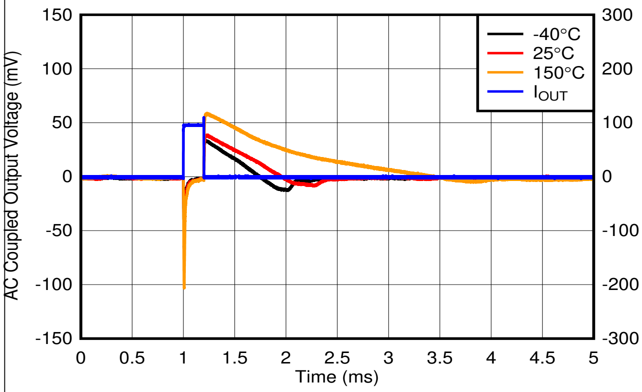
V_{OUT} = 5 V, I_{OUT} = 1 mA, V_{IN} = 13.5 V to 40 V, slew rate = 2.7 V/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 5-13. Line Transients at 13.5 V to 40 V



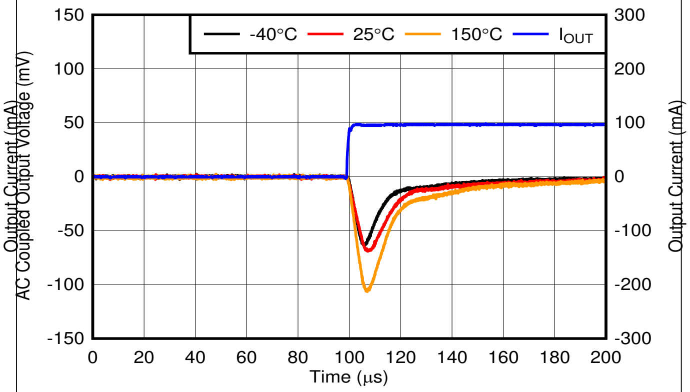
V_{OUT} = 5 V, V_{IN} = 5.5 V to 6.5 V, t_{rise} = 1 µs, C_{OUT} = 10 µF

Figure 5-14. Line Transients at 5.5 V to 6.5 V



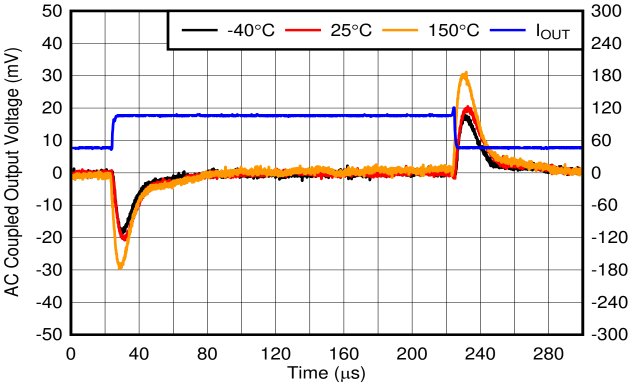
V_{OUT} = 5 V, I_{OUT} = 0 mA to 100 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 5-15. Load Transient, No Load to 100 mA



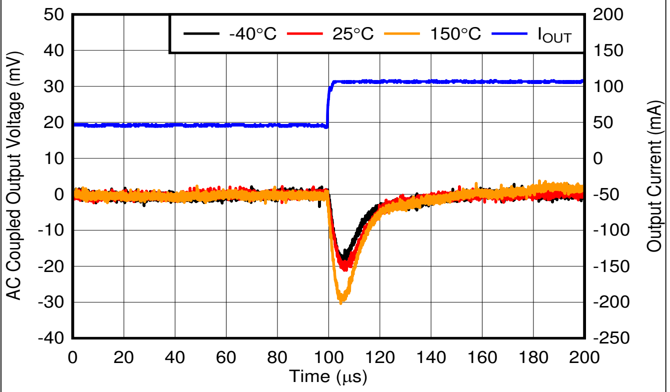
V_{OUT} = 5 V, I_{OUT} = 0 mA to 100 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 5-16. Load Transient, No Load to 100-mA Rising Edge



V_{OUT} = 5 V, I_{OUT} = 45 mA to 105 mA, slew rate = 0.1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 5-17. Load Transient, 45 mA to 105 mA

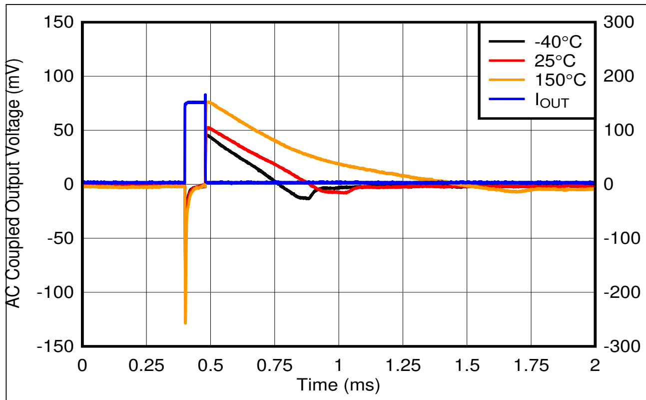


V_{OUT} = 5 V, I_{OUT} = 45 mA to 105 mA, slew rate = 0.1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 5-18. Load Transient, 45-mA to 105-mA Rising Edge

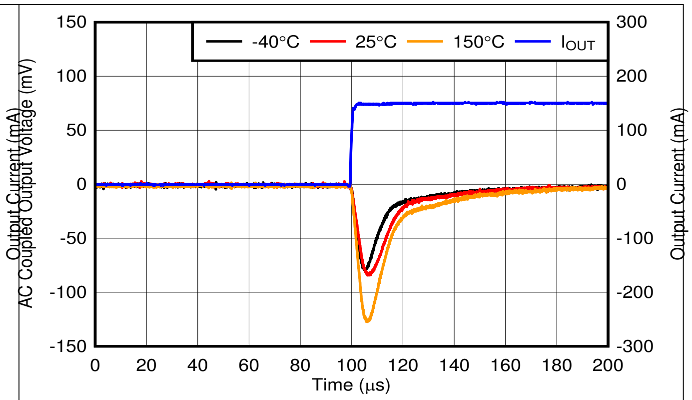
5.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



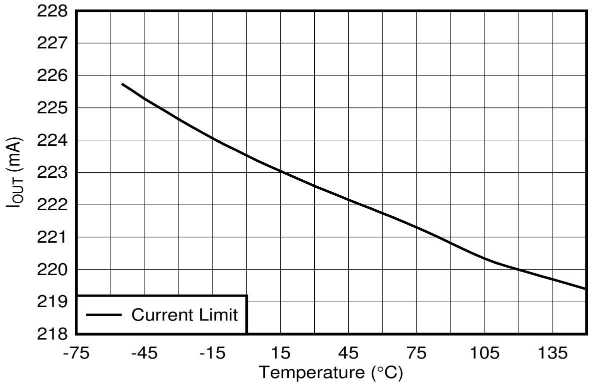
V_{OUT} = 5 V, I_{OUT} = 0 mA to 150 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 5-19. Load Transient, No Load to 150 mA



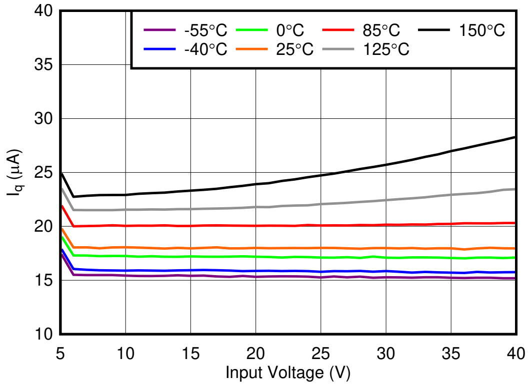
V_{OUT} = 5 V, I_{OUT} = 0 mA to 150 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 5-20. Load Transient, No Load to 150-mA Rising Edge



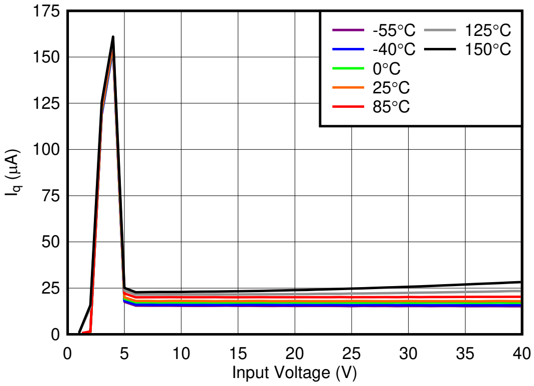
V_{IN} = V_{OUT} + 1 V, V_{OUT} = 90% × $V_{OUT(NOM)}$

Figure 5-21. Output Current Limit vs Temperature



V_{OUT} = 5 V

Figure 5-22. Quiescent Current (I_Q) vs V_{IN}



V_{OUT} = 5 V

Figure 5-23. Quiescent Current (I_Q) vs V_{IN}

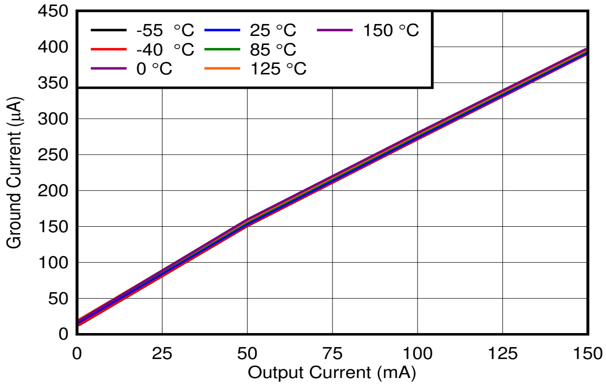
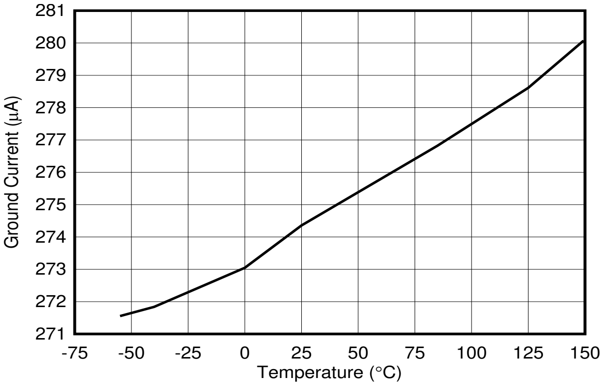


Figure 5-24. Ground Current (I_{GND}) vs I_{OUT}

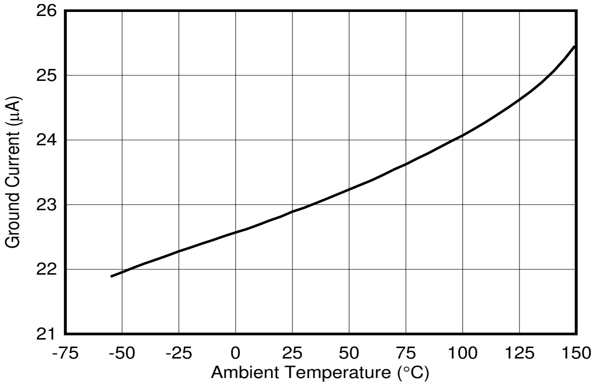
5.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



I_{OUT} = 100 mA

Figure 5-25. Ground Current



I_{OUT} = 500 µA

Figure 5-26. Ground Current

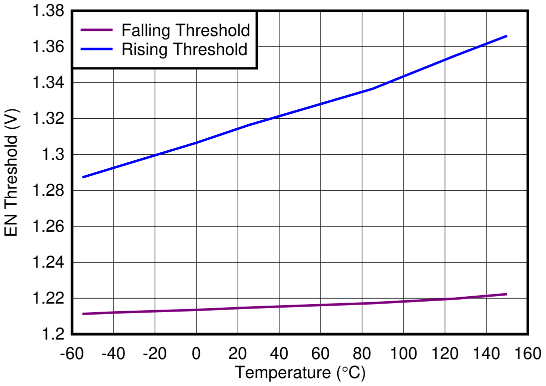


Figure 5-27. EN Threshold vs Temperature

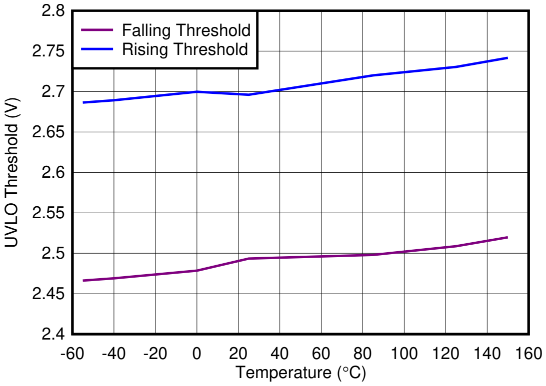
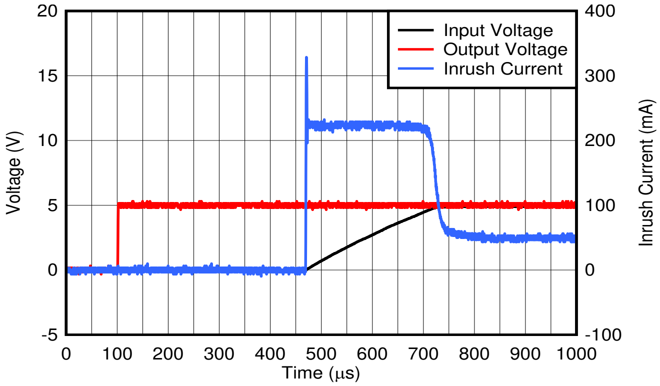
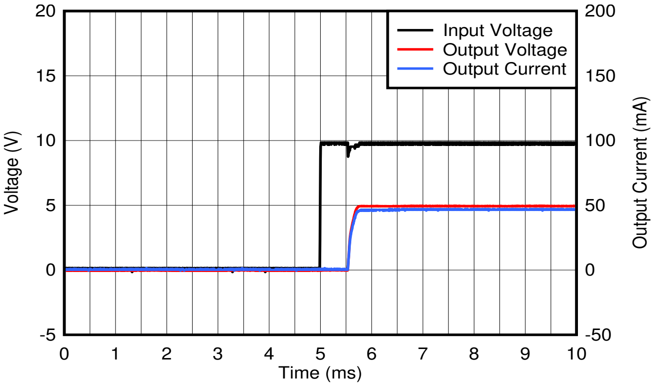


Figure 5-28. Undervoltage Lockout (UVLO) Threshold vs Temperature



V_{IN} = 13.5 V, C_{OUT} = 10 µF

Figure 5-29. Startup Plot With EN



C_{OUT} = 10 µF

Figure 5-30. Startup Plot

5.6 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)

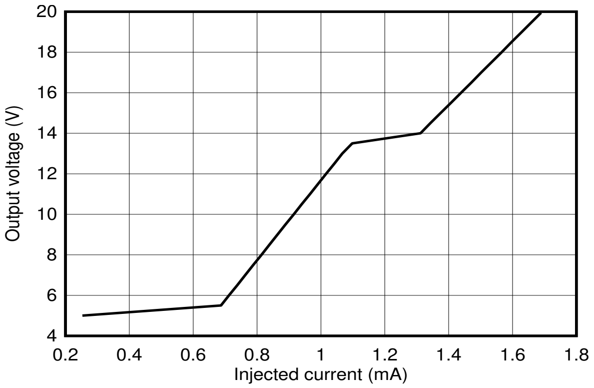


Figure 5-31. Output Voltage vs Injected Current

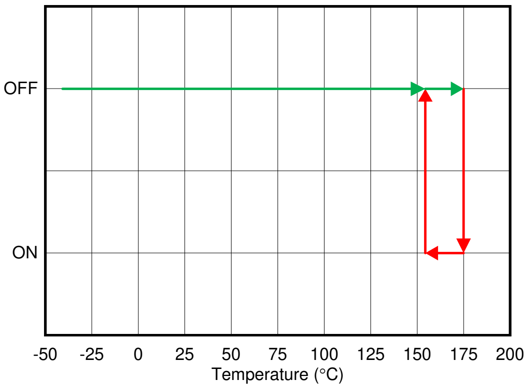


Figure 5-32. Thermal Shutdown

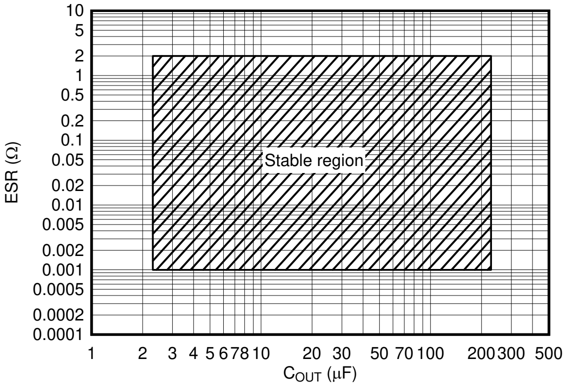


Figure 5-33. Stability ESR vs C_{OUT}

6 Detailed Description

6.1 Overview

The TPS7B84-Q1 is a low-dropout linear regulator (LDO) designed to connect to the battery in automotive applications. The device has an input voltage range extending to 40 V, which allows the device to withstand transients (such as load dumps) that are anticipated in automotive systems. With only a 18-μA quiescent current at light loads, the device is an optimal solution for powering always-on components.

The device has a state-of-the-art transient response that allows the output to quickly react to changes in the load or line (for example, during cold-crank conditions). Additionally, the device has a novel architecture that minimizes output overshoot when recovering from dropout. During normal operation, the device has a tight DC accuracy of ±0.75% over line, load, and temperature.

6.2 Functional Block Diagrams

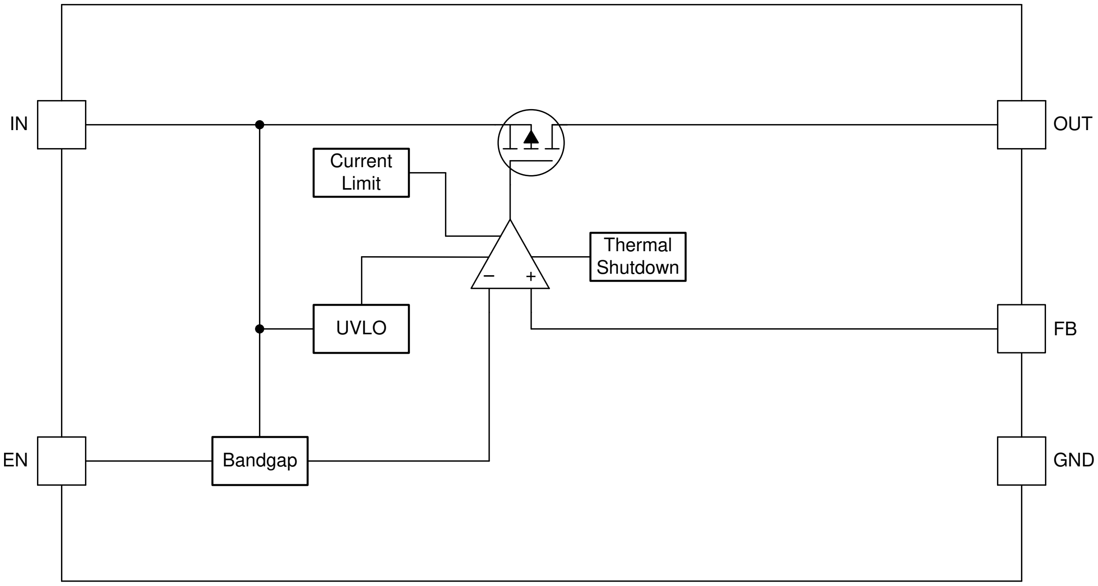


Figure 6-1. Adjustable Output Block Diagram

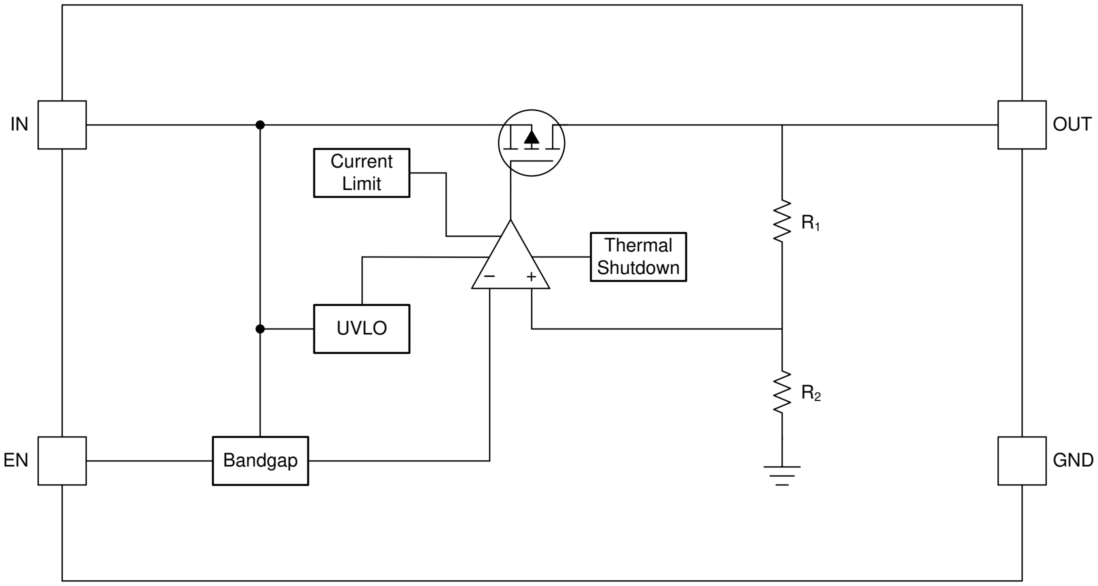


Figure 6-2. Fixed Output Block Diagram

6.3 Feature Description

6.3.1 Enable (EN)

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

6.3.2 Undervoltage Lockout

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

6.3.3 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brickwall scheme. In a high-load current fault, the brickwall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{CL}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 6-3 shows a diagram of the current limit.

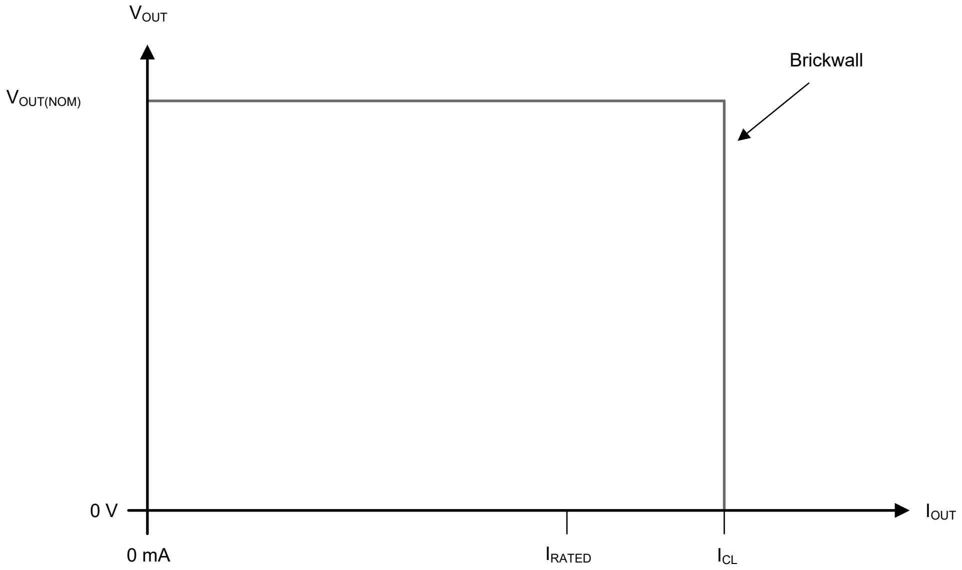


Figure 6-3. Current Limit

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Input and Output Capacitor Selection

The TPS7B84-Q1 requires an output capacitor of 2.2 µF or larger (1 µF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001 Ω and 2 Ω. For the best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.1.2 Adjustable Device Feedback Resistor Selection

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \tag{1}$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \tag{2}$$

7.1.3 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, connect an optional feed-forward capacitor (C_{FF}) from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. Using a higher-capacitance C_{FF} is permissible but start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z. C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. The following equations calculate C_{FF} zero and pole frequencies.

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \tag{3}$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \tag{4}$$

7.1.4 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{5}$$

7.1.5 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \le V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

7.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \tag{6}$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{7}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.6.1 Thermal Performance Versus Copper Area

The most used thermal resistance parameter, $R_{\theta JA}$, is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table in the *Specifications* section is determined by the JEDEC standard (see Figure 7-1), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

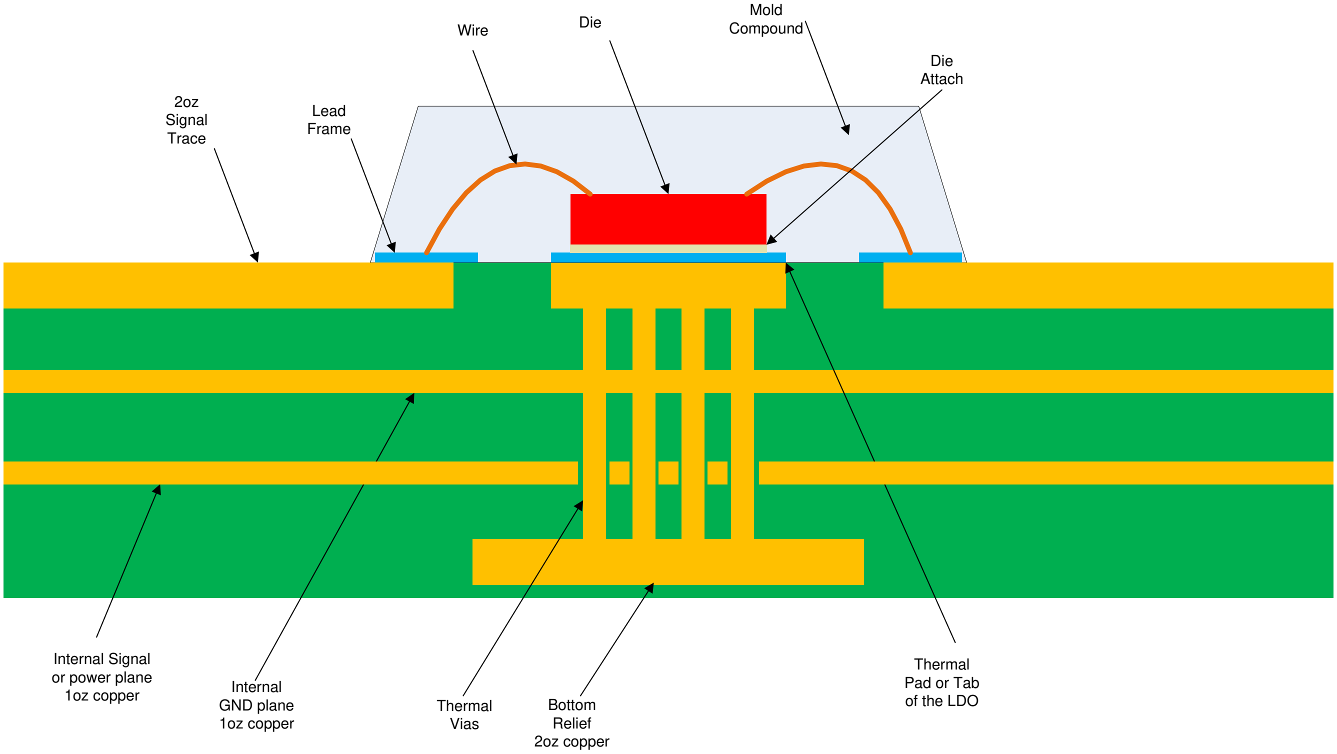


Figure 7-1. JEDEC Standard 2s2p PCB

Figure 7-2 through Figure 7-4 depict the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness. These plots are generated with a 101.6-mm x 101.6-mm x 1.6-mm PCB of two and four layers. For the four-layer board, the inner planes use a 1-oz copper thickness. Outer layers are simulated with both a 1-oz and 2-oz copper thickness. A 4 x 4 array of thermal vias of 300-µm drill diameter and 25-µm Cu plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

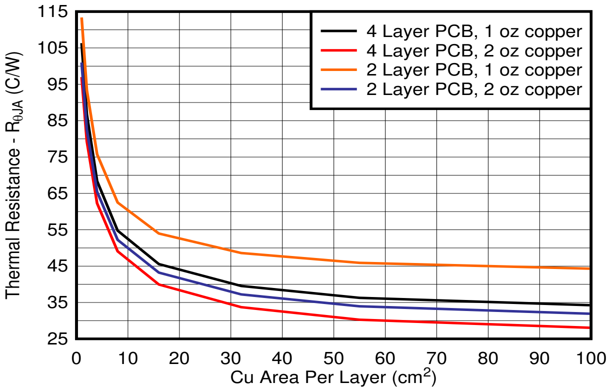


Figure 7-2. $R_{\theta JA}$ vs Copper Area 2s2p DRB Package

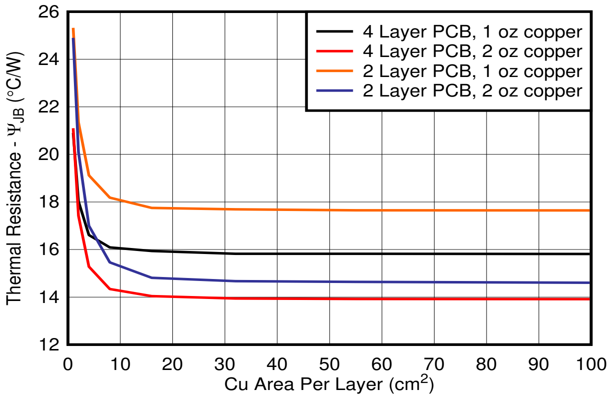


Figure 7-3. ψ_{JB} vs Copper Area 2s2p DRB Package

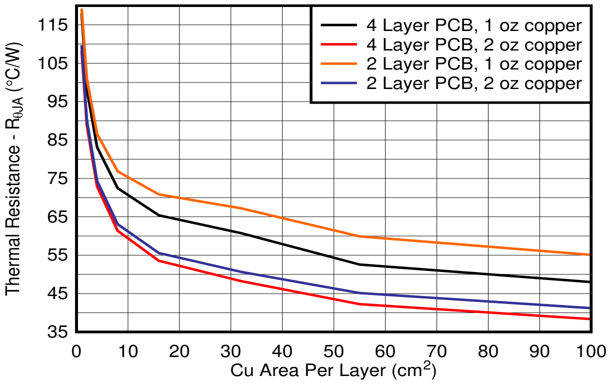


Figure 7-4. $R_{\theta JA}$ vs Copper Area 2s2p DCY Package

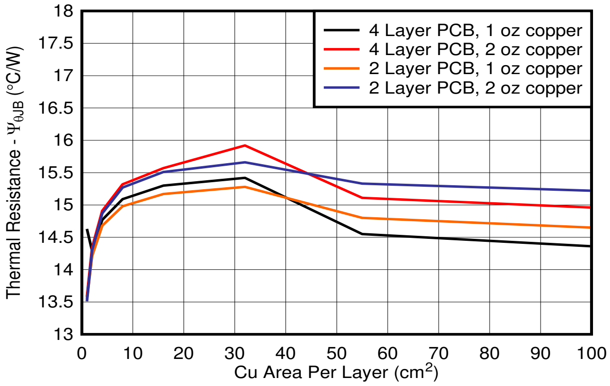


Figure 7-5. ψ_{JB} vs Copper Area 2s2p DCY Package

7.1.6.2 Power Dissipation vs Ambient Temperature

Figure 7-6 is based off of a JESD51-7 4 layer high-K board. The allowable power dissipation was estimated using the following equation. As disscussed in the *An empirical analysis of the impact of board layout on LDO thermal performance* application report, thermal dissipation can be improved in the JEDEC high-K layout by adding top layer copper and increasing the number of thermal vias. If a good thermal layout is used, the allowable thermal dissipation can be improved by up to 50%.

$$T_A + R_{\theta JA}\,x\,P_D \le 150\,°C \tag{8}$$

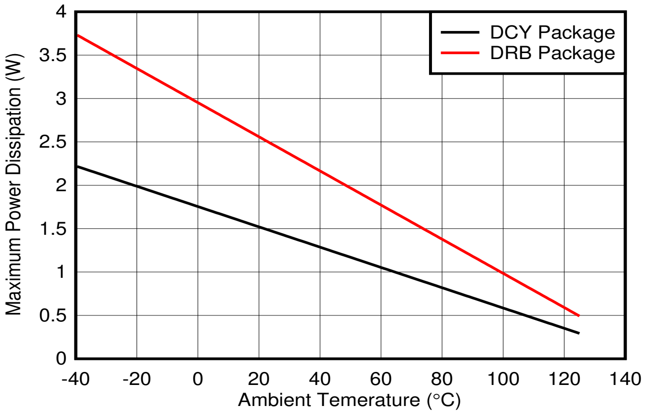


Figure 7-6. TPS7B84-Q1 Allowable Power Dissipation

7.1.7 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the linear regulator junction temperatures when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the printed circuit board (PCB) surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{9}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \tag{10}$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use the metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2 Typical Application

Figure 7-7 shows a typical application circuit for the TPS7B84-Q1. Use different values of external components, depending on the end application. An application may require a larger output capacitor during fast load steps in order to prevent a reset from occurring. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

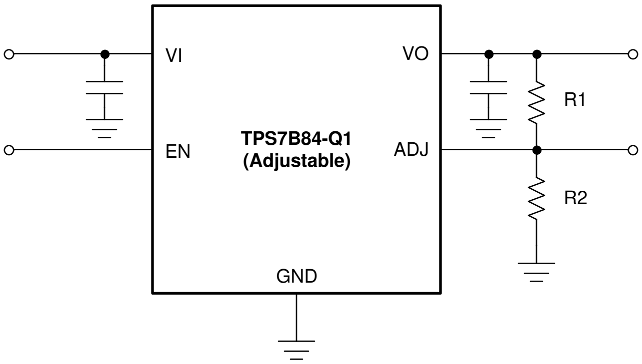


Figure 7-7. Typical Application Schematic for the TPS7B84-Q1

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the input parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6 V to 40 V
Output voltage	5 V
Output current	100 mA
Output capacitor	10 µF

7.2.2 Detailed Design Procedure

7.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 1 µF. The voltage rating must be greater than the maximum input voltage.

7.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value must be between 2.2 µF and 200 µF and the ESR range must be between 1 mΩ and 2 Ω. For this design a low ESR, 10-µF ceramic capacitor was used to improve transient performance.

7.2.3 Application Curves

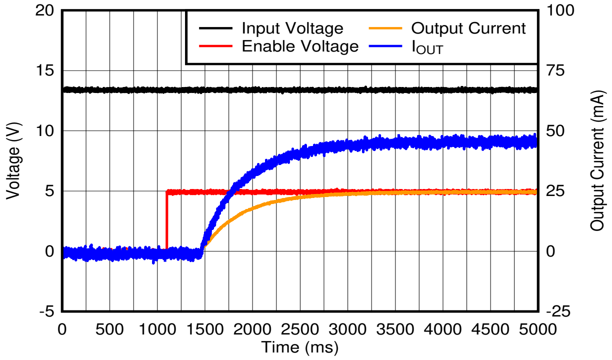


Figure 7-8. Power-Up Waveform

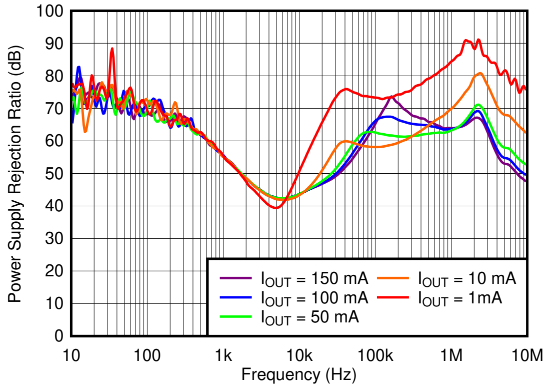


Figure 7-9. PSRR

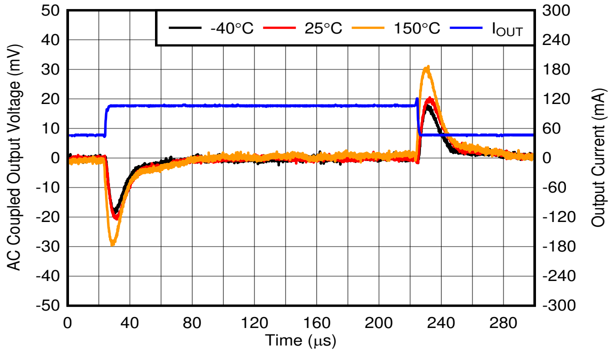


Figure 7-10. Transient Response

7.3 Power Supply Recommendations

This device is designed for operation from an input voltage supply with a range between 3 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B84-Q1, add an electrolytic capacitor and a ceramic bypass capacitor at the input.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. TI also recommends a ground reference plane either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7B84-Q1 are available at the end of this document and at www.ti.com.

7.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

As depicted in Figure 7-11 and Figure 7-12 , place the input and output capacitors close to the device for the layout of the TPS7B84-Q1. In order to enhance the thermal performance, place as many vias as possible around the device. These vias improve the heat transfer between the different GND planes in the PCB.

To improve ac performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place each capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces to connect the capacitors because these can negatively impact system performance and may even cause instability.

If possible, and to ensure the maximum performance specified in this document, use the same layout pattern used for the TPS7B84-Q1 evaluation board, available at www.ti.com.

7.4.2 Layout Examples

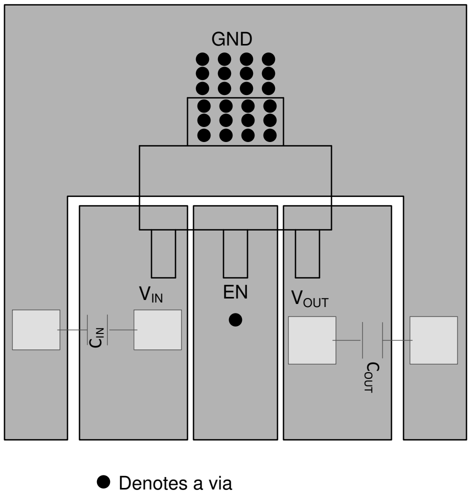


Figure 7-11. SOT-223 (DCY) Layout

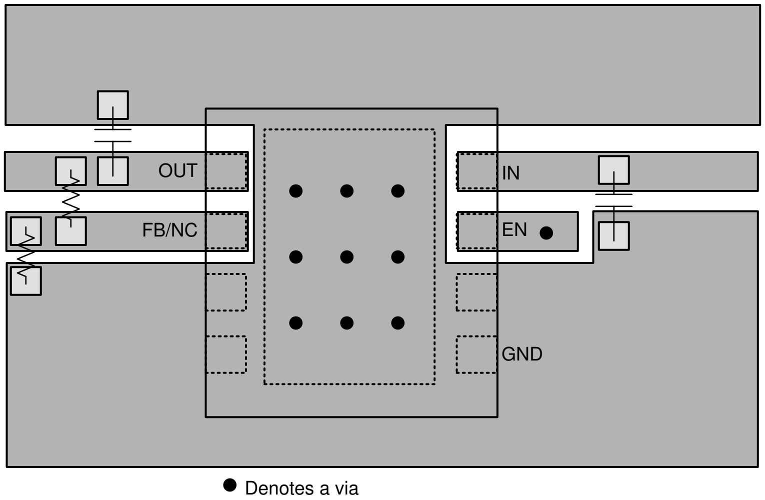


Figure 7-12. VSON (DRB) Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT(1)	DESCRIPTION
TPS7B84**xxQ(W)yyyRQ1**	**xx** is the nominal output voltage (for example, 33 = 3.3V; 50 = 5.0V; 01 = Adjustable). **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **W** indicates the package has wettable flanks. **yyy** is the package designator. **R** is the package quantity. R is for reel (3000 pieces). **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2020) to Revision B (May 2025) **Page**

- Added *01 = Adjustable* to xx description in *Device Nomenclature* table.. 26

Changes from Revision * (April 2020) to Revision A (November 2020) **Page**

- Changed document status from advance information to production data.. 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B8401QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8401
TPS7B8401QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8401
TPS7B8433QDCYRQ1	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	7B8433
TPS7B8433QDCYRQ1.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8433
TPS7B8433QDCYRQ1M3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7B8433
TPS7B8433QDCYRQ1M3.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7B8433
TPS7B8433QDCYRQ1W	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7B8433
TPS7B8433QDCYRQ1W.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7B8433
TPS7B8433QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8433
TPS7B8433QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8433
TPS7B8450QDCYRQ1	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	7B8450
TPS7B8450QDCYRQ1.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8450
TPS7B8450QDCYRQ1M3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7B8450
TPS7B8450QDCYRQ1M3.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7B8450
TPS7B8450QDCYRQ1W	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7B8450
TPS7B8450QDCYRQ1W.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7B8450
TPS7B8450QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8450
TPS7B8450QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8450
TPS7B8480QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8480
TPS7B8480QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7B8480

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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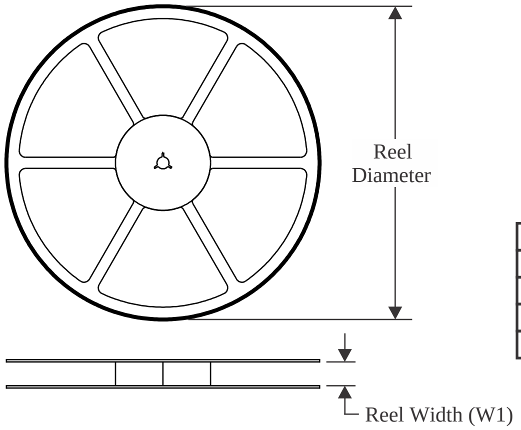
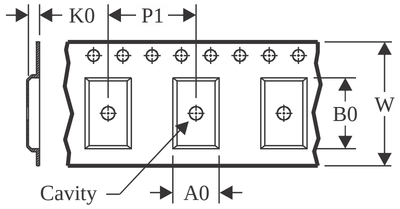
TAPE AND REEL INFORMATION

REEL DIMENSIONS

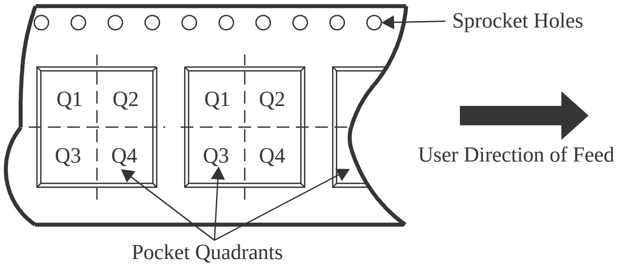


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

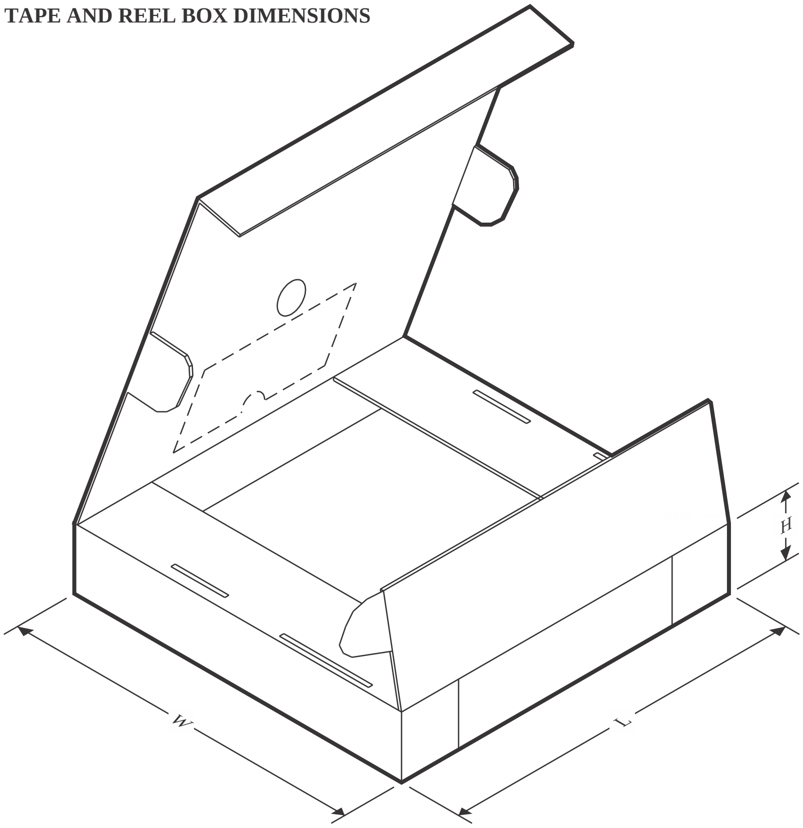
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8401QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7B8433QDCYRQ1	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS7B8433QDCYRQ1M3	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS7B8433QDCYRQ1W	SOT-223	DCY	4	2500	330.0	16.4	7.05	7.4	1.9	8.0	16.0	Q3
TPS7B8433QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7B8450QDCYRQ1	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS7B8450QDCYRQ1M3	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS7B8450QDCYRQ1W	SOT-223	DCY	4	2500	330.0	16.4	7.05	7.4	1.9	8.0	16.0	Q3
TPS7B8450QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7B8480QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8401QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS7B8433QDCYRQ1	SOT-223	DCY	4	2500	366.0	364.0	50.0
TPS7B8433QDCYRQ1M3	SOT-223	DCY	4	2500	366.0	364.0	50.0
TPS7B8433QDCYRQ1W	SOT-223	DCY	4	2500	366.0	364.0	50.0
TPS7B8433QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS7B8450QDCYRQ1	SOT-223	DCY	4	2500	340.0	340.0	38.0
TPS7B8450QDCYRQ1M3	SOT-223	DCY	4	2500	340.0	340.0	38.0
TPS7B8450QDCYRQ1W	SOT-223	DCY	4	2500	340.0	340.0	38.0
TPS7B8450QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS7B8480QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

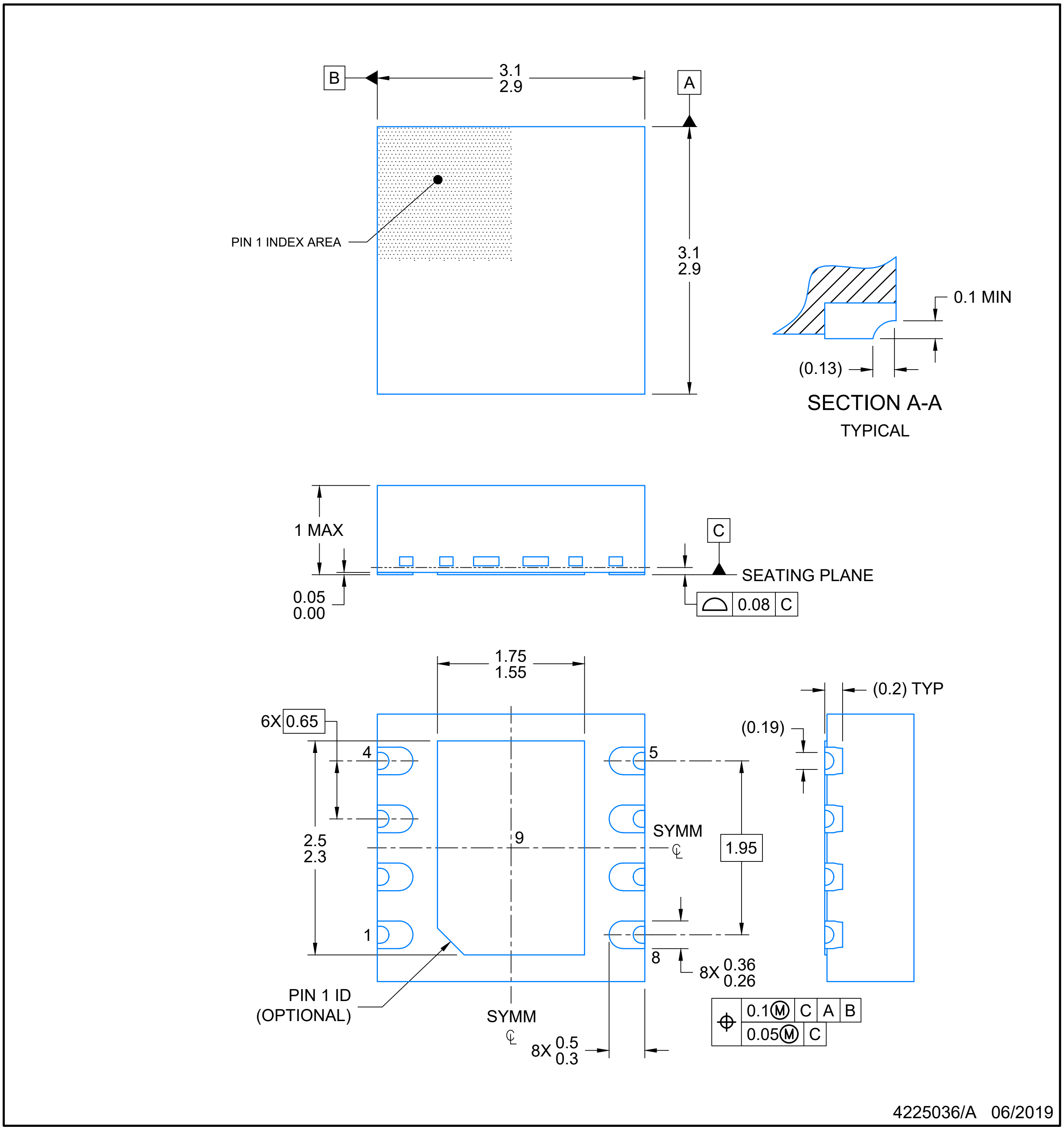
GENERIC PACKAGE VIEW

DRB 8 **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

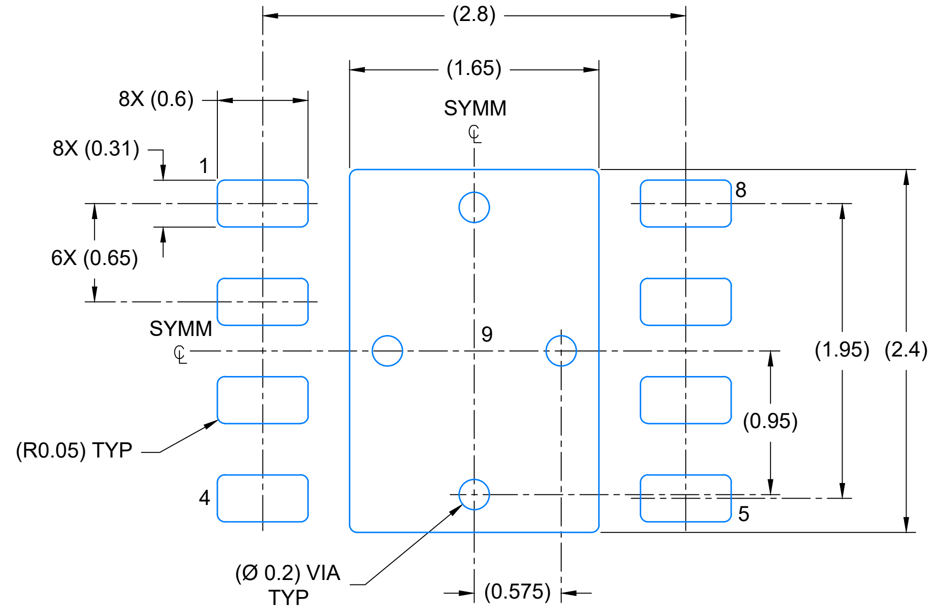
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

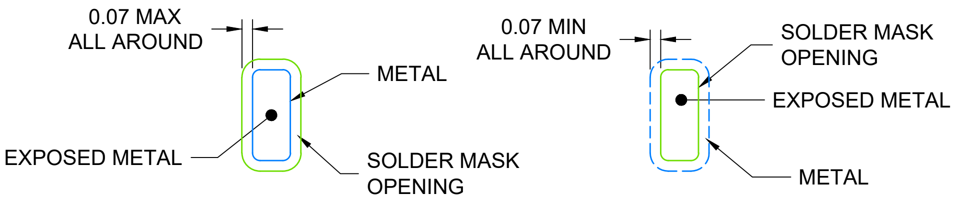


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

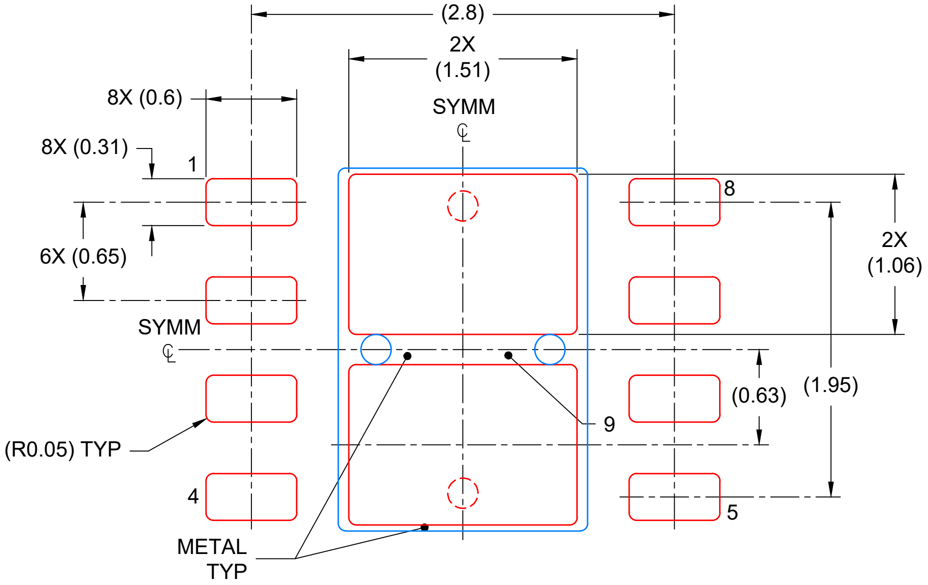
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



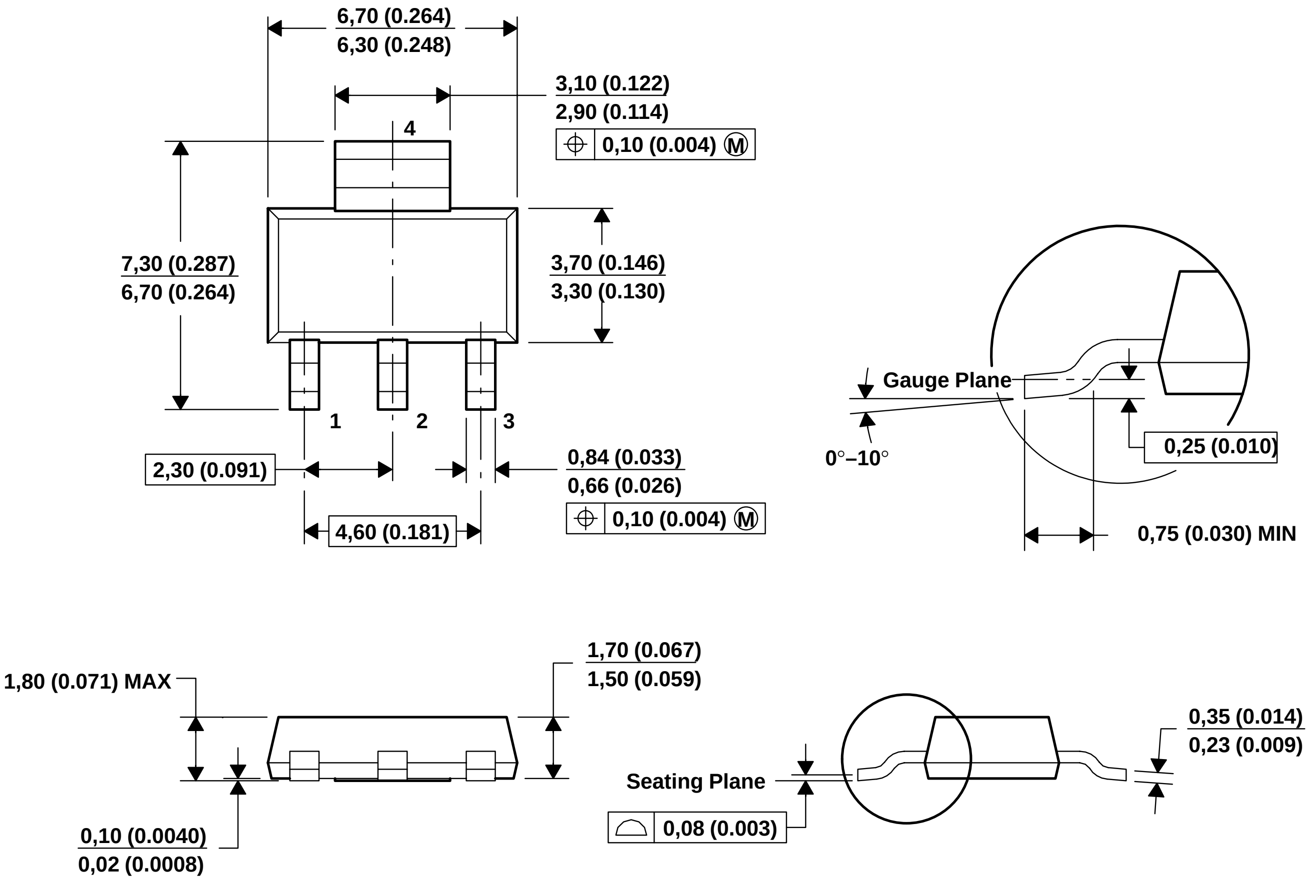
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DCY (R-PDSO-G4) PLASTIC SMALL-OUTLINE



4202506/B 06/2002

NOTES:
- A. All linear dimensions are in millimeters (inches).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC TO-261 Variation AA.

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