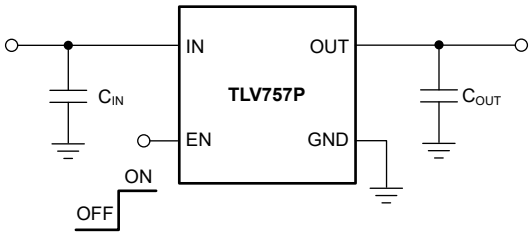
TLV757P 1A, Low I_Q, Small-Size, Low-Dropout Regulator

1 Features

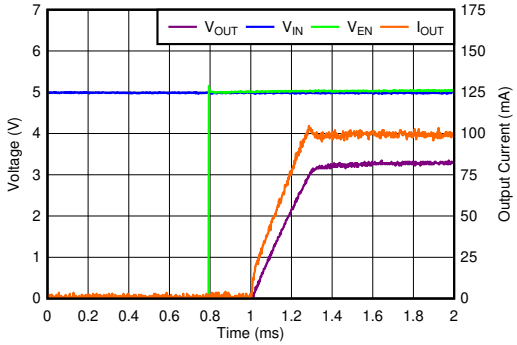
- SOT-23 (DYD) package with 60.3°C/W $R_{\theta JA}$ available
- Input voltage range: 1.45V to 5.5V
- Available in fixed-output voltages:
  - 0.6V to 5V (50mV steps)
- Low I_Q: 25µA (typical)
- Low dropout:
  - 425mV (maximum) at 1A ($3.3V_{OUT}$)
- Output accuracy: 1% (maximum)
- Built-in soft-start with monotonic V_{OUT} rise
- Foldback current limit
- Active output discharge
- High PSRR: 45dB at 100kHz
- Stable with a 1µF ceramic output capacitor
- Packages:
  - 2.9mm × 2.8mm SOT-23-5 (DBV)
  - 2.9mm × 2.8mm SOT-23-5 (DYD) with thermal pad
  - 2mm × 2mm WSON-6 (DRV)

2 Applications

- Set-top boxes, TV, and gaming consoles
- Portable and battery-powered equipment
- Desktops, notebooks, and ultrabooks
- Tablets and remote controls
- White goods and appliances
- Grid infrastructure and protection relays
- Camera modules and image sensors



Typical Application



Start-Up Waveform

3 Description

The TLV757P low-dropout regulator (LDO) is an ultra-small, low quiescent current LDO that sources 1A with good line and load transient performance. The TLV757P is optimized for a wide variety of applications by supporting an input voltage range from 1.45V to 5.5V. To minimize cost and solution size, the device is offered in fixed output voltages ranging from 0.6V to 5V. This range supports the lower core voltages of modern microcontrollers (MCUs). Additionally, the TLV757P has a low I_Q with enable functionality to minimize standby power. This device features an internal soft-start to lower the inrush current. This feature provides a controlled voltage to the load and minimizes the input voltage drop during start-up. When shutdown, the device actively pulls down the output to quickly discharge the outputs and provides a known start-up state.

The TLV757P is stable with small ceramic output capacitors allowing for a small overall solution size. A precision band-gap and error amplifier provides a typical accuracy of 1%. All device versions have integrated thermal shutdown, current limit, and undervoltage lockout (UVLO). The TLV757P has an internal foldback current limit that helps reduce thermal dissipation during short-circuit events.

The TLV757 is available in the popular SON and SOT23-5 packages. This device is also available in a thermally enhanced SOT23-5 package (DYD) with a thermal pad. This package provides significantly reduced thermal resistance compared to a standard SOT23-5 package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLV757P	DRV (WSON, 6)	2mm × 2mm
	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DYD (SOT-23, 5)	2.9mm × 1.6mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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Table of Contents

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4 Pin Configuration and Functions

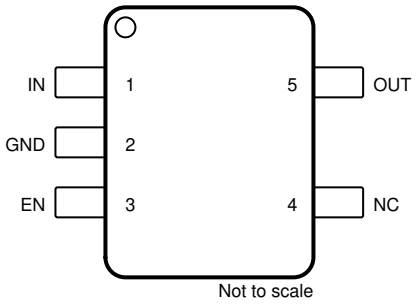

Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

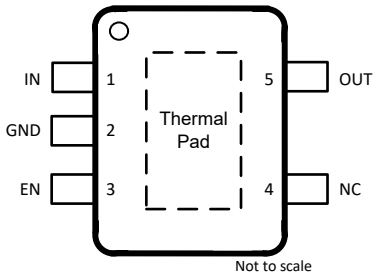

Figure 4-2. DYD Package, 5-Pin SOT-23 With Exposed Thermal Pad (Top View)

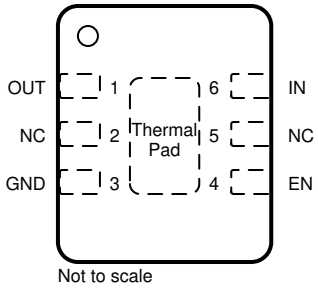

Figure 4-3. DRV Package, 6-Pin WSON With Exposed Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DBV	DYD	DRV		
EN	3	3	4	I	Enable pin. Drive EN greater than V_{HI} to turn on the regulator. Drive EN less than V_{LO} to place the LDO into shutdown mode.
GND	2	2	3	—	Ground pin.
IN	1	1	6	I	Input pin. A capacitor with a value of 1µF or larger is required from this pin to ground.(1) See the *Input and Output Capacitor Selection* section for more information.
NC	4	4	2, 5	—	No internal connection.
OUT	5	5	1	O	Regulated output voltage pin. A capacitor with a value of 1µF or larger is required from this pin to ground.(1) See the *Input and Output Capacitor Selection* section for more information.
Thermal pad	—	Pad	Pad	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

(1) Make sure the nominal input and output capacitance are greater than 0.47µF. Throughout this document the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 0.47µF.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage,V_{IN}	–0.3	6.0	V
Enable voltage, V_{EN}	–0.3	6.0	V
Output voltage, V_{OUT}	–0.3	V_{IN} + 0.3(2)	V
Operating junction temperature range, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3V or 6.0V, whichever is smaller

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.45		5.5	V
V_{OUT}	Output voltage	0.6		5.0	V
V_{EN}	Enable voltage	0		5.5	V
I_{OUT}	Output current	0		1	A
C_{IN}	Input capacitor	1			µF
C_{OUT}	Output capacitor	1		200	µF
f_{EN}	Enable toggle frequency			10	kHz
T_J	Junction temperature	–40		125	°C

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5.4 Thermal Information

PCB	THERMAL METRIC(1) (2)		TLV757			UNIT
			DYD (SOT-23)	DBV (SOT-23)	DRV (SON)	
			5 PINS	5 PINS	6 PINS	
EVM	$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.3	100.8	N/A	°C/W
	ψ_{JT}	Junction-to-top characterization parameter	14.2	23.3	N/A	°C/W
	ψ_{JB}	Junction-to-board characterization parameter	35.9	67.8	N/A	°C/W
JEDEC	$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.5	231.1	100.2	°C/W
	$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	119.8	118.4	108.5	°C/W
	$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	64.4	64.3	°C/W
	ψ_{JT}	Junction-to-top characterization parameter	16.7	28.4	10.4	°C/W
	ψ_{JB}	Junction-to-board characterization parameter	44.9	63.8	64.8	°C/W
	$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	34.3	N/A	34.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) JEDEC thermal metrics apply to JEDEC standard PCB (2s2p, no vias to internal plane and bottom layer). EVM metrics apply to the LP087A EVM with an exposed pad SOT-23-5 (DYD) layout.

5.5 Electrical Characteristics

over operating free-air temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT} + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.45		5.5	V
V_{OUT}	Output voltage			0.6		5.0	V
	Output accuracy	–40°C ≤ T_J ≤ 85°C, V_{OUT} ≥ 1V		–1		1	%
		–40°C ≤ T_J ≤ 85°C, 0.6V ≤ V_{OUT} < 1V		–10		10	mV
		V_{OUT} ≥ 1V		–1.5		1.5	%
		0.6V ≤ V_{OUT} < 1V		–15		15	mV
$(\Delta_{VOUT})_{\Delta VIN}$	Line regulation	V_{OUT} + 0.5V(1) ≤ V_{IN} ≤ 5.5V			2		mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0.1mA ≤ I_{OUT} ≤ 1A, V_{IN} ≥ 2.4V	DRV package		0.044		V/A
			DBV package		0.060		
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0.1 mA ≤ I_{OUT} ≤ 1A, V_{IN} ≥ 2.4V	DYD package		0.069		V/A
I_{GND}	Ground current	T_J = 25°C			25	31	µA
		–40°C ≤ T_J ≤ +85°C				33	
		–40°C ≤ T_J ≤ +125°C				40	
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4V, 1.45V ≤ V_{IN} ≤ 5.5V			0.1	1	µA
I_{CL}	Output current limit	V_{IN} = V_{OUT} + $V_{DO(MAX)}$ + 0.25V	V_{OUT} = V_{OUT} - 0.2V, V_{OUT} ≤ 1.5V	1.2	1.55	1.78	A
			V_{OUT} = 0.9 x V_{OUT}, 1.5V < V_{OUT} ≤ 4.5V				
I_{SC}	Short circuit current limit	V_{OUT} = 0V, V_{IN} = V_{OUT} + $V_{DO(MAX)}$ + 0.25V			755		mA

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5.5 Electrical Characteristics (continued)

over operating free-air temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT} + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	I_{OUT} = 1A, –40°C ≤ T_J ≤ +85°C	0.6V ≤ V_{OUT} < 0.8V		1350	1400	mV
			0.8V ≤ V_{OUT} < 1V		1200	1300	
			0.8V ≤ V_{OUT} < 1V, DYD package		1225	1325	
			1V ≤ V_{OUT} < 1.2V		1100	1150	
			1V ≤ V_{OUT} < 1.2V, DYD package		1125	1175	
			1.2V ≤ V_{OUT} < 1.5V		1000	1050	
			1.2V ≤ V_{OUT} < 1.5V, DYD package		1025	1075	
			1.5V ≤ V_{OUT} < 1.8V		700	800	
			1.5V ≤ V_{OUT} < 1.8V, DYD package		725	825	
			1.8V ≤ V_{OUT} < 2.5V		650	750	
			1.8V ≤ V_{OUT} < 2.5V, DYD package		650	775	
			2.5V ≤ V_{OUT} < 3.3V		500	600	
			2.5V ≤ V_{OUT} < 3.3V, DYD package		525	625	
			3.3V ≤ V_{OUT} < 5.0V		300	425	
			3.3V ≤ V_{OUT} < 5.0V, DYD package		300	450	
		I_{OUT} = 1A, –40°C ≤ T_J ≤ +125°C	0.6V ≤ V_{OUT} < 0.8V			1450	
			0.8V ≤ V_{OUT} < 1V			1350	
			0.8V ≤ V_{OUT} < 1V, DYD package			1375	
			1V ≤ V_{OUT} < 1.2V			1200	
			1V ≤ V_{OUT} < 1.2V, DYD package			1225	
			1.2V ≤ V_{OUT} < 1.5V			1100	
			1.2V ≤ V_{OUT} < 1.5V, DYD package			1125	
			1.5V ≤ V_{OUT} < 1.8V			850	
			1.5V ≤ V_{OUT} < 1.8V, DYD package			875	
			1.8V ≤ V_{OUT} < 2.5V			800	
			1.8V ≤ V_{OUT} < 2.5V, DYD package			825	
			2.5V ≤ V_{OUT} < 3.3V			650	
			2.5V ≤ V_{OUT} < 3.3V, DYD package			675	
			3.3V ≤ V_{OUT} < 5.0V			475	
			3.3V ≤ V_{OUT} < 5.0V, DYD package			500	
PSRR	Power supply rejection ratio	f = 1kHz, V_{IN} = V_{OUT} + 1V, I_{OUT} = 50mA			52		dB
		f = 100kHz, , V_{IN} = V_{OUT} + 1 V, I_{OUT} = 50mA			46		
		f = 1MHz, , V_{IN} = V_{OUT} + 1V, I_{OUT} = 50mA			52		
V_n	Output noise voltage	BW = 10Hz to 100kHz, V_{OUT} = 1.2V, I_{OUT} = 1A			71.5		μV_{RMS}
V_{UVLO}	Undervoltage lockout	V_{IN} rising		1.21	1.3	1.44	V
$V_{UVLO, HYST}$	Undervoltage lockout hysteresis	V_{IN} falling			40		mV
t_{STR}	Startup time				550		µs
V_{HI}	EN pin high voltage (enabled)			1			V
V_{LO}	EN pin low voltage (enabled)					0.3	V
I_{EN}	Enable pin current	V_{IN} = 5.5V, EN = 5.5V			10		nA
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 3.3V (P version only)			95		Ω
T_{SD}	Thermal shutdown	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			155		°C

(1) V_{IN} = 1.45V for V_{OUT} < 0.9V

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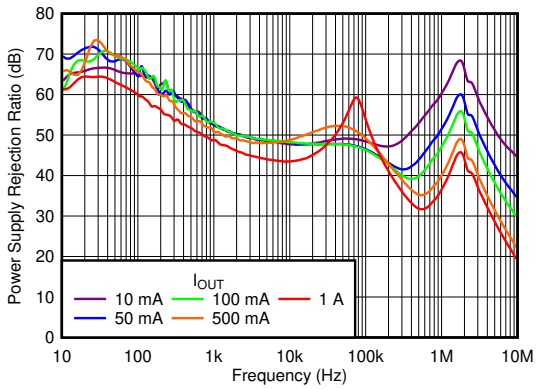
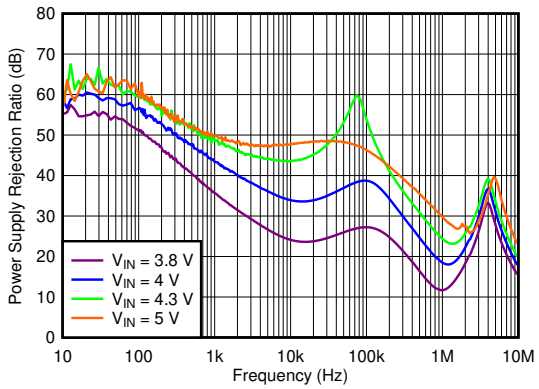
5.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



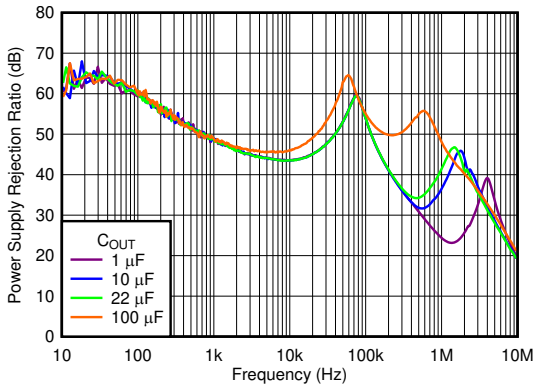
V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 1µF

Figure 5-1. PSRR vs I_{OUT}



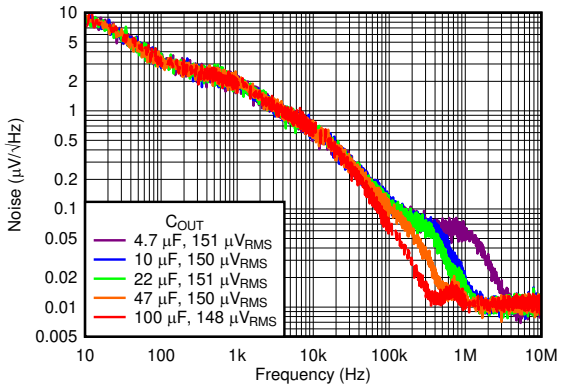
V_{OUT} = 3.3V, C_{OUT} = 1µF, I_{OUT} = 1A

Figure 5-2. PSRR vs V_{IN}



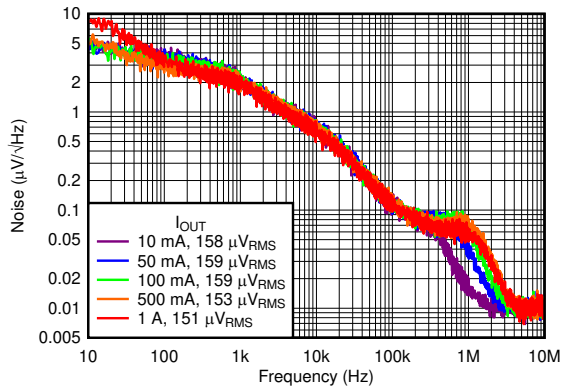
V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 1µF

Figure 5-3. PSRR vs C_{OUT}



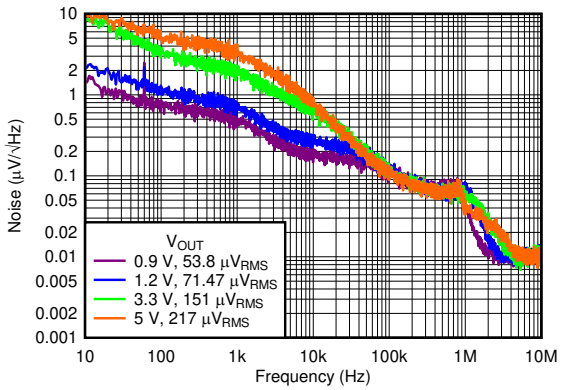
V_{OUT} = 3.3V, I_{OUT} = 1A, V_{RMS} BW = 10Hz to 100kHz

Figure 5-4. Output Spectral Noise Density



V_{OUT} = 3.3V, C_{OUT} = 1µF, V_{RMS} BW = 10Hz to 100kHz

Figure 5-5. Output Spectral Noise Density



I_{OUT} = 1A, C_{OUT} = 1µF, V_{RMS} BW = 10Hz to 100kHz

Figure 5-6. Output Noise vs Frequency and V_{OUT}

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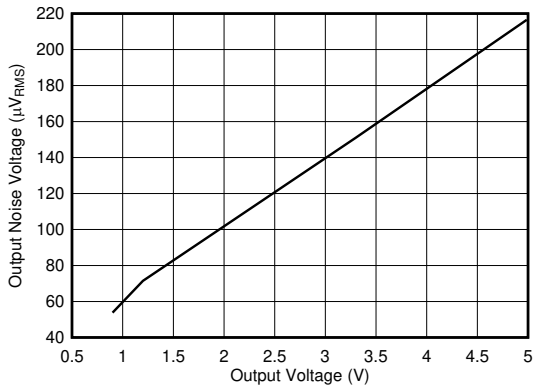
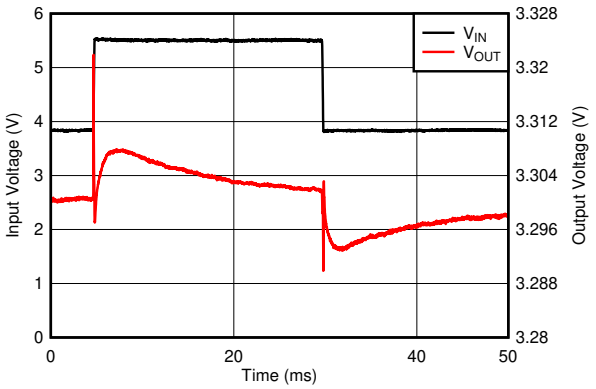
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



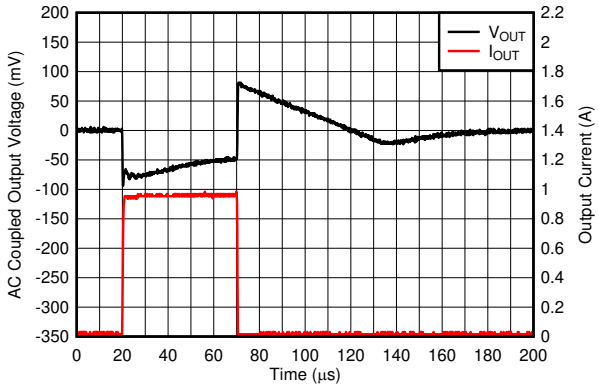
I_{OUT} = 1A, C_{OUT} = 1µF, V_{RMS} BW = 10Hz to 100kHz

Figure 5-7. Output Noise Voltage vs V_{OUT}



V_{OUT} = 3.3V, C_{OUT} = 1µF, V_{IN} slew rate = 1V/µs

Figure 5-8. Line Transient



V_{IN} = 5V, V_{OUT} = 3.3V, C_{OUT} = 1µF, I_{OUT} slew rate = 1A/µs

Figure 5-9. 3.3V, 1mA to 1A Load Transient

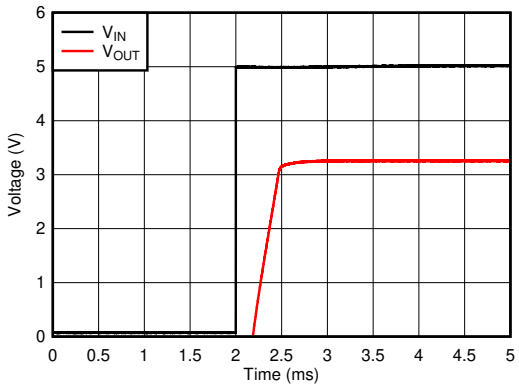


Figure 5-10. V_{IN} = V_{EN} Power-Up

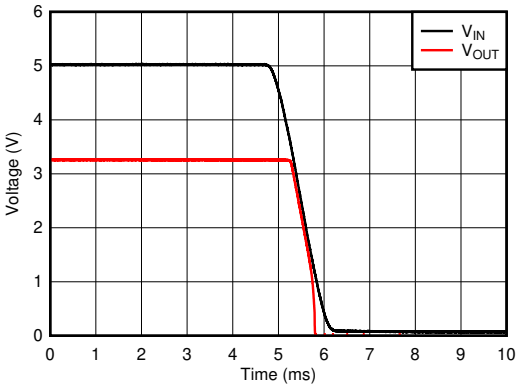
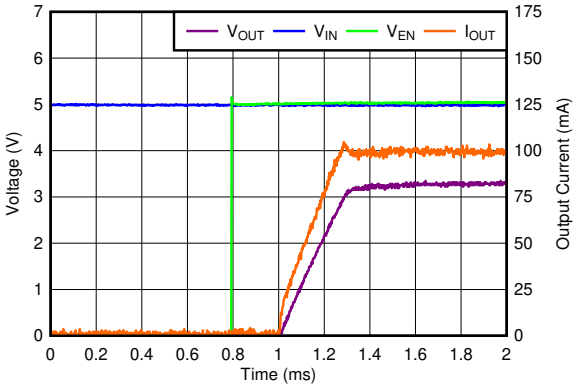


Figure 5-11. V_{IN} = V_{EN} Shutdown



V_{IN} = 5V, I_{OUT} = 100mA, V_{EN} slew rate = 1V/µs, V_{OUT} = 3.3V

Figure 5-12. EN Start-Up

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5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)

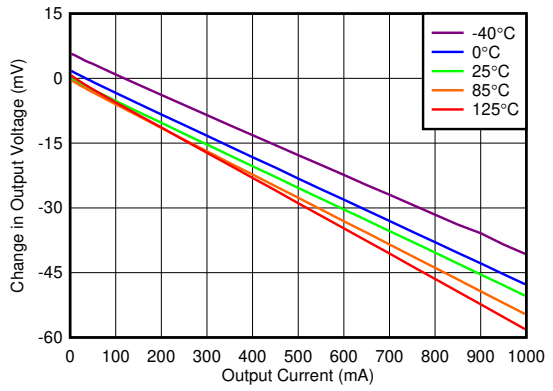


Figure 5-13. Load Regulation vs I_{OUT}

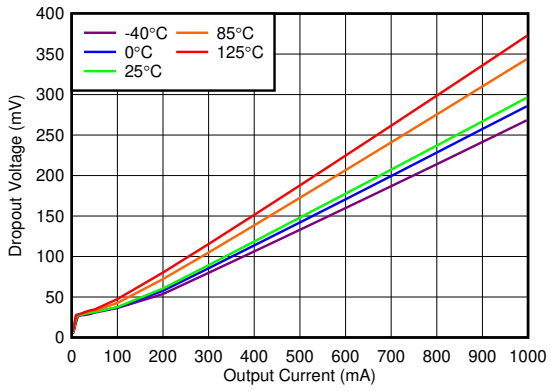


Figure 5-14. 3.3V Dropout Voltage vs I_{OUT}

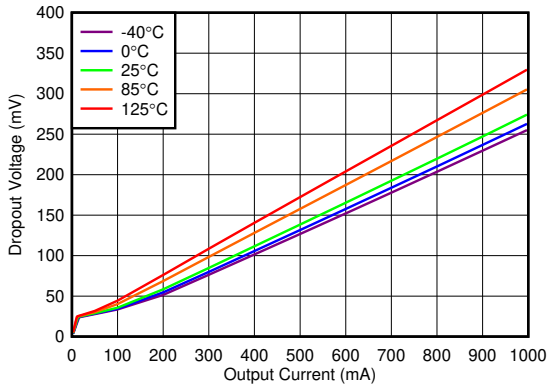
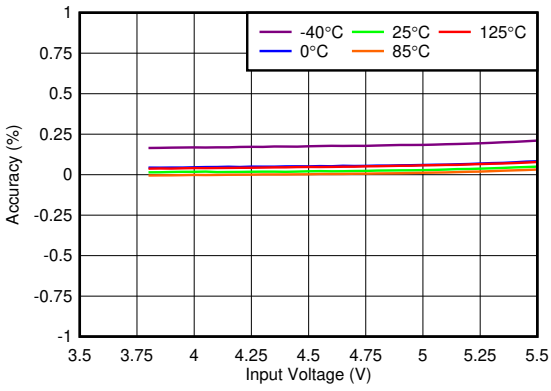
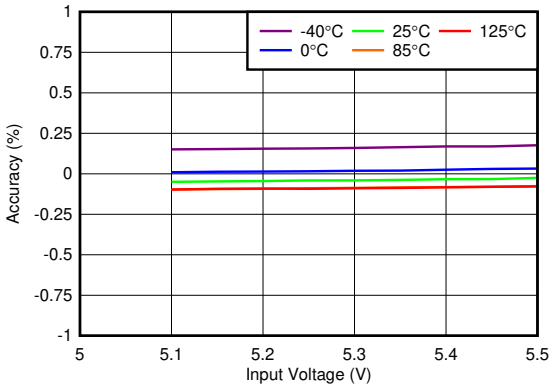


Figure 5-15. 5.0V Dropout Voltage vs I_{OUT}



V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 5-16. 3.3V Regulation vs V_{IN} (Line Regulation)



I_{OUT} = 1mA, V_{OUT} = 5V

Figure 5-17. 5.0V Accuracy vs V_{IN} (Line Regulation)

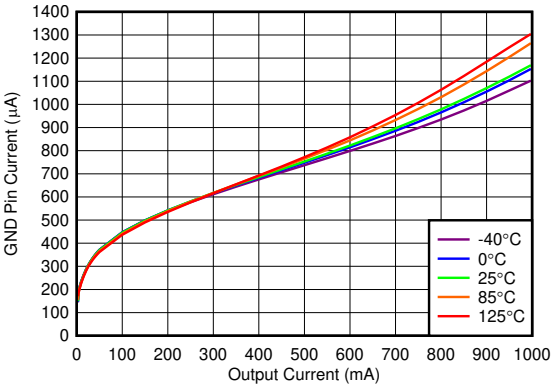


Figure 5-18. I_{GND} vs I_{OUT}

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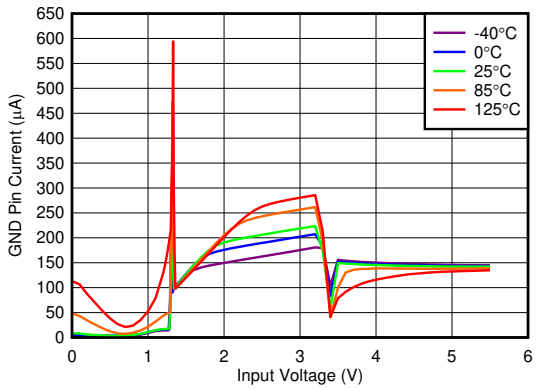
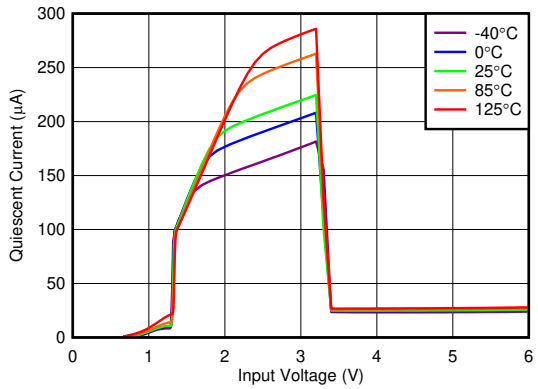
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 5-19. I_{GND} vs V_{IN}



V_{OUT} = 3.3V, I_{OUT} = 0mA

Figure 5-20. I_{GND} vs V_{IN}

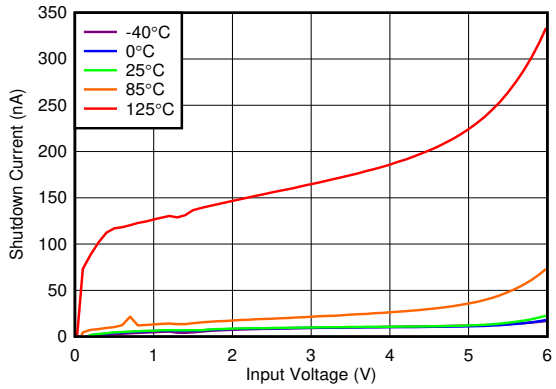


Figure 5-21. I_{SHDN} vs V_{IN}

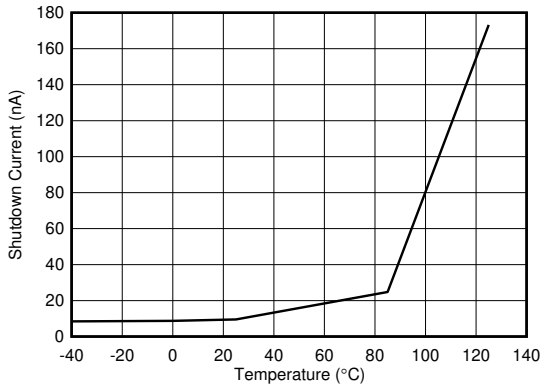


Figure 5-22. I_{SHDN} vs Temperature

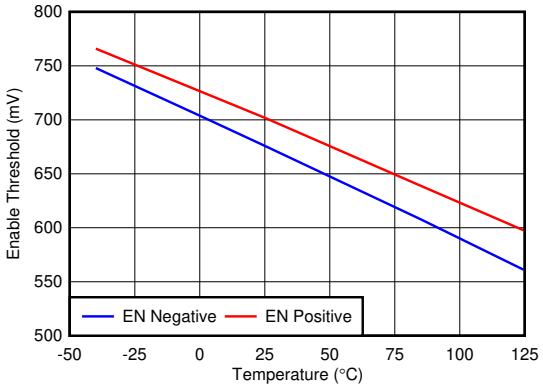
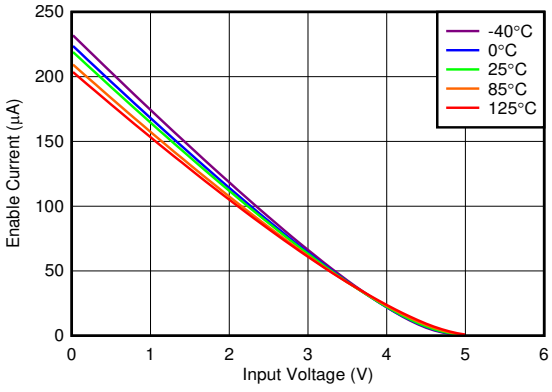


Figure 5-23. Enable Threshold vs Temperature



V_{EN} = 5.5V

Figure 5-24. I_{EN} vs V_{IN}

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5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)

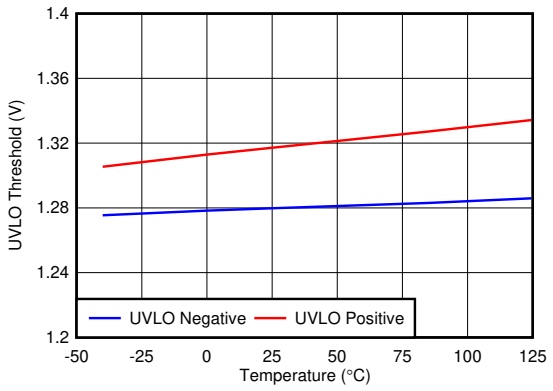


Figure 5-25. UVLO Threshold vs Temperature

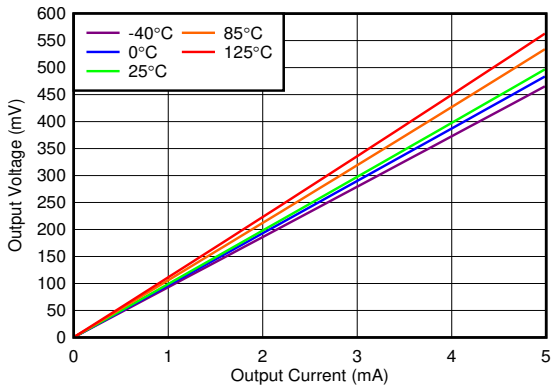


Figure 5-26. I_{OUT} vs V_{OUT} Pulldown Resistor

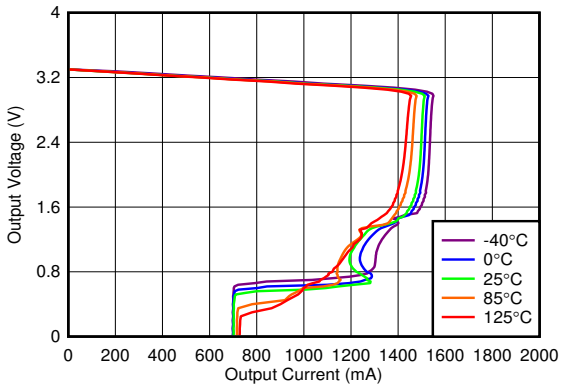


Figure 5-27. 3.3V Foldback Current Limit vs I_{OUT}

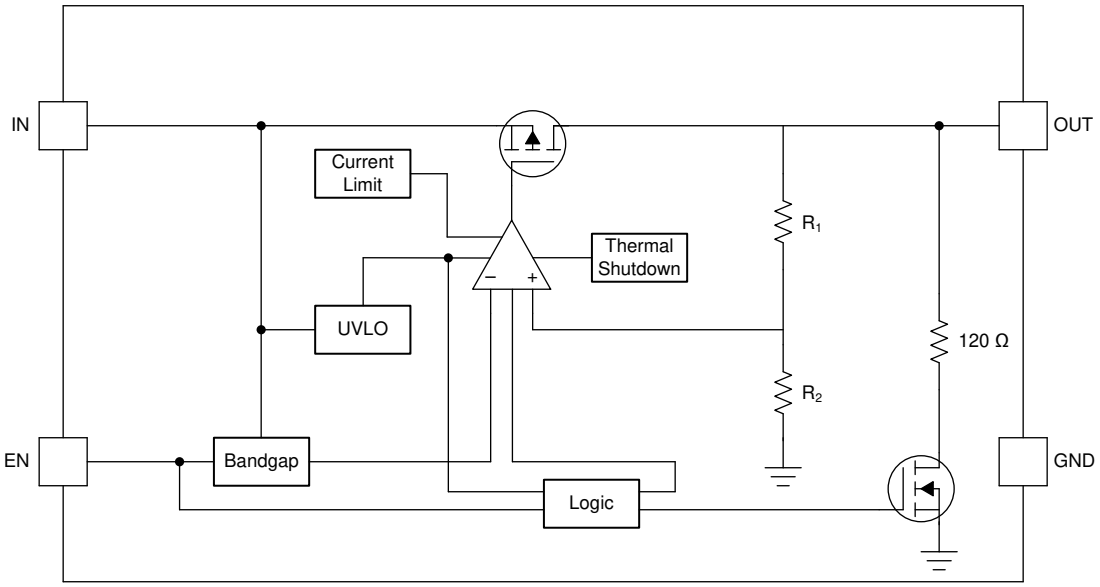
6 Detailed Description

6.1 Overview

The TLV757P is a next-generation, low-dropout regulator (LDO). This device consumes low quiescent current and delivers excellent line and load transient performance. The TLV757P is optimized for a wide variety of applications by supporting an input voltage range from 1.4V to 5.5V. To minimize cost and solution size, the device is offered in fixed output voltages ranging from 0.6V to 5V. This range supports the lower core voltages of modern microcontrollers (MCUs).

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature is –40°C to +125°C.

6.2 Functional Block Diagram



A. R_2 = 550kΩ, R_1 = adjustable.

6.3 Feature Description

6.3.1 Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). This circuit makes sure the device does not exhibit unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_{IN} is less than V_{UVLO}, the output is connected to ground with a 120Ω pulldown resistor.

6.3.2 Enable (EN)

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed V_{HI}. Turn off the device by forcing the EN pin below V_{LO}. If shutdown capability is not required, connect EN to IN.

The device has an internal pull-down that connects a 120Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120Ω pulldown resistor. Equation 1 calculates the time constant τ:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

The EN pin is independent of the input pin. However, if the EN pin is driven to a higher voltage than V_{IN}, the current into the EN pin increases. This effect is illustrated in Figure 5-24. When the EN voltage is higher than

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the input voltage there is an increased current flow into the EN pin. If this increased flow causes problems in the application, sequence the EN pin after V_{IN} is high, or tie EN to V_{IN}. If EN is driven to a higher voltage than V_{IN}, limit the frequency on EN to below 10kHz.

6.3.3 Internal Foldback Current Limit

The TLV757P has an internal current limit that protects the regulator during fault conditions. The current limit is a hybrid scheme with brick wall until the output voltage is less than 0.4 × $V_{OUT(NOM)}$. When the voltage drops below 0.4 × $V_{OUT(NOM)}$, a foldback current limit is implemented that scales back the current as the output voltage approaches GND. When the output shorts, the LDO supplies a typical current of I_{SC}. The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output is shorts, the PMOS pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}] until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown.

The foldback current-limit circuit limits the current that is allowed through the device to current levels lower than the minimum current limit at nominal V_{OUT} current limit (I_{CL}) during start up. See Figure 5-27 for typical current limit values. If the output is loaded by a constant-current load during start up, or if the output voltage is negative when the device is enabled, then the load current demanded by the load potentially exceeds the foldback current limit. Thus, causing the device to possibly not rise to the full output voltage. For constant-current loads, disable the output load until the output rises to the nominal voltage.

Excess inductance causes the current limit to oscillate. Minimize the inductance to keep the current limit from oscillating during a fault condition.

6.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 165°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit cycles on and off. This cycling limits regulator dissipation, which protects the circuit from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the device into thermal shutdown degrades device reliability.

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6.4 Device Functional Modes

Table 6-1 lists a comparison between the normal, dropout, and disabled modes of operation.

Table 6-1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal(1)	$V_{IN} > V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout(1)	$V_{IN} < V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	—	$T_J < T_{SD}$
Disabled(2)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{LO}$	—	$T_J > T_{SD}$

(1) Make sure all table conditions are met.
(2) The device is disabled when any condition is met.

6.4.1 Normal Operation

The device regulates to the nominal output voltage when all of the following conditions are met.

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device degrades because the pass transistor is in a triode state and no longer controls the output voltage of the LDO. Line or load transients in dropout result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, right after being in a normal regulation state, but not during start-up), the pass transistor is driven as hard as possible when the control loop is out of balance. During the normal time required for the device to regain regulation, $V_{IN} \geq V_{OUT(NOM)} + V_{DO}$, V_{OUT} overshoots $V_{OUT(NOM)}$ during fast transients.

6.4.3 Disabled

The output is shut down by forcing the enable pin below V_{LO}. When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal switch from the output to ground. The active pulldown is on when sufficient input voltage is provided.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Input and Output Capacitor Selection

The TLV757P requires an output capacitance of 0.47µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in capacitance value and equivalent series resistance (ESR) over temperature. When selecting a capacitor for a specific application, consider the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. As a general rule, make sure ceramic capacitors are derated by 50%. For best performance, use an output capacitance value no greater than 200µF.

Place a 1µF or greater capacitor on the input pin of the LDO. Some input supplies have a high impedance. Placing a capacitor on the input supply reduces the input impedance. The input capacitor counteracts reactive input sources and improves transient response and PSRR. If the input supply has high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are expected, or if the device is located several inches from the input power source.

7.1.2 Dropout Voltage

The TLV757P uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass transistor. V_{DO} scales linearly with the output current because the PMOS transistor functions like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation. See Figure 5-14 and Figure 5-15 for typical dropout values.

7.1.3 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output overshoots on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up when the slew rate and voltage levels are in the correct range; see Figure 7-1. Use an enable signal to avoid this condition.

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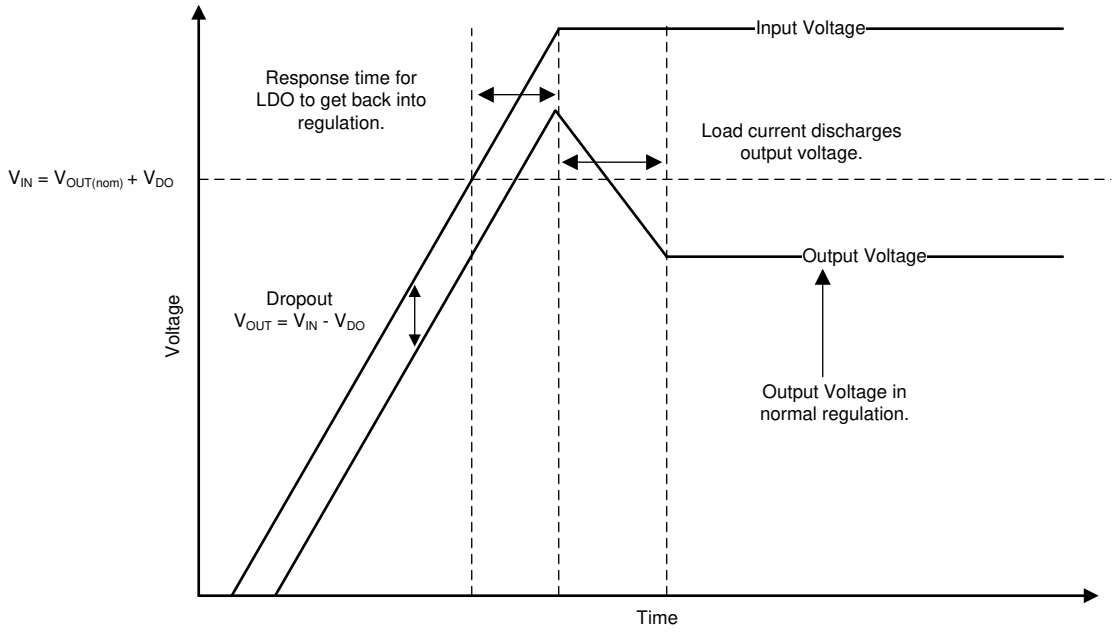

Figure 7-1. Start-Up Into Dropout

Line transients out of dropout also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass transistor and bring the gate back to the correct voltage for proper regulation. Figure 7-2 illustrates what is happening internally with the gate voltage and how overshoot is caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to give the pass transistor the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation, which causes the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

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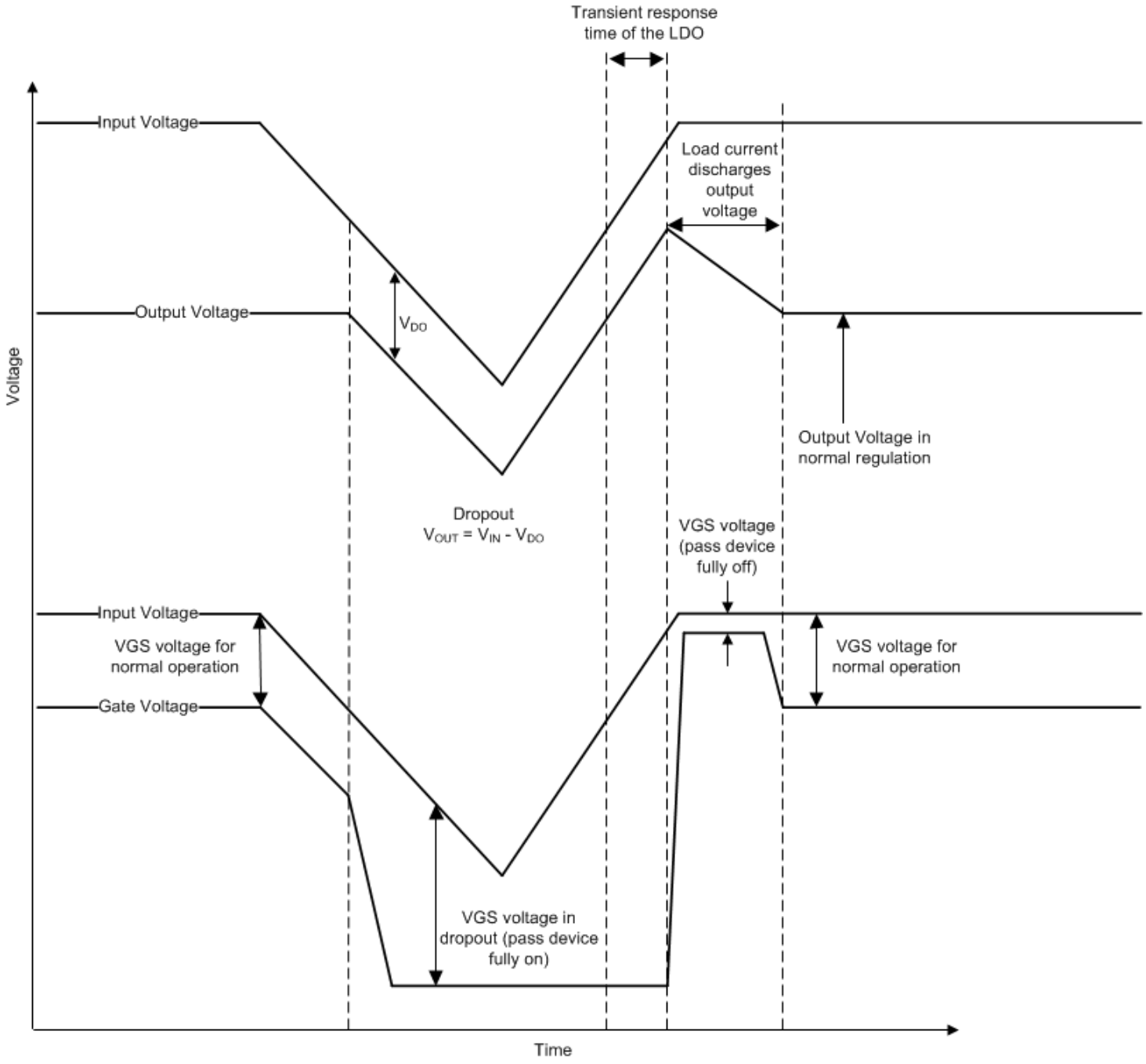

Figure 7-2. Line Transients From Dropout

7.1.4 Reverse Current

As with most LDOs, excessive reverse current potentially damages this device.

Reverse current flows through the body diode on the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current occurs are outlined in this section, all of which exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3V$:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Figure 7-3 shows one approach of protecting the device.

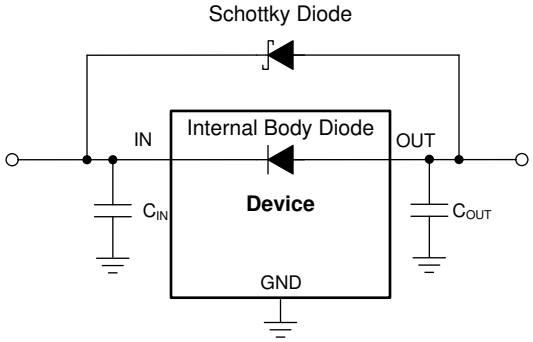

Figure 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Make sure the PCB area around the regulator is as free of other heat-generating devices as possible that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Minimize power dissipation to achieve greater efficiency. This minimizing process is achieved by selecting the correct system voltage rails. Proper selection helps obtain the minimum input-to-output voltage differential. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, solder the thermal pad to a copper pad area under the device. Make sure this pad area contains an array of plated vias that conduct heat to inner plane areas or to a bottom-side copper plane.

The maximum allowable junction temperature (T_J) determines the maximum power dissipation for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB, device package, and the temperature of the ambient air (T_A), according to Equation 3.

$$T_J = T_A + R_{\theta JA} \times P_D \quad (3)$$

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Unfortunately, this thermal resistance ($R_{\theta JA}$) is dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ value is only used as a relative measure of package thermal performance. $R_{\theta JA}$ is the sum of the WSON package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

7.1.5.1 Estimating Junction Temperature

The JEDEC standard recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not thermal resistances, but offer practical and relative means of estimating junction temperatures. These psi metrics are independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are shown in the *Thermal Information* table and are used in accordance with Equation 4.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \quad (4)$$

where:

- P_D is the power dissipated as shown in Equation 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

7.2 Typical Application

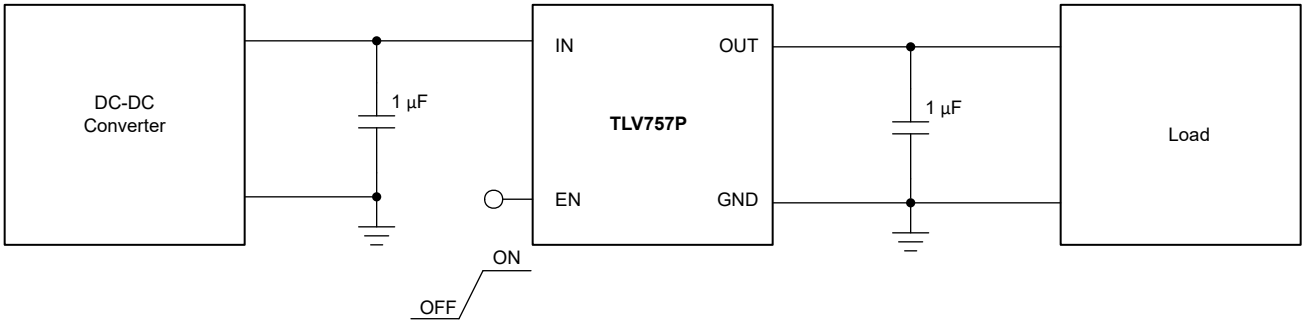

Figure 7-4. TLV757P Typical Application

7.2.1 Design Requirements

Table 7-1 lists the design requirements for this application.

Table 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.5V
Output voltage	1.8V
Input current	700mA (maximum)
Output load	600mA DC
Maximum ambient temperature	70°C

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7.2.2 Detailed Design Procedure

7.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During start-up, the input current is higher as a result of the inrush current charging the output capacitor. Use Equation 5 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (5)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

7.2.2.2 Thermal Dissipation

Junction temperature is determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use Equation 6 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ and add the ambient temperature (T_A) to calculate the junction temperature (T_J) as Equation 7 shows.

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (6)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (7)$$

If the ($T_{J(MAX)}$) value does not exceed 125°C, calculate the maximum ambient temperature as Equation 8 shows. Equation 9 calculates the maximum ambient temperature with a value of 82.916°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (8)$$

$$T_{A(MAX)} = 125°C - 100.2 \times (2.5V - 1.8V) \times (0.6A) = 82.916°C \quad (9)$$

7.2.3 Application Curves

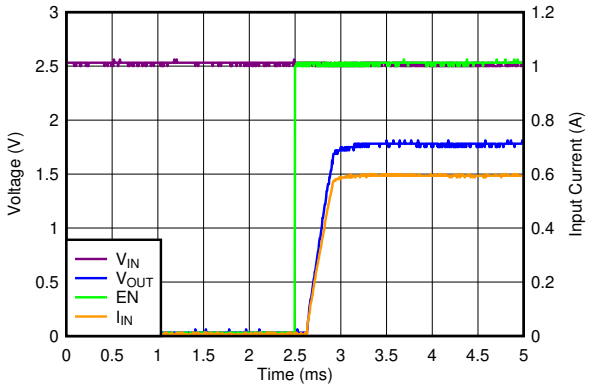
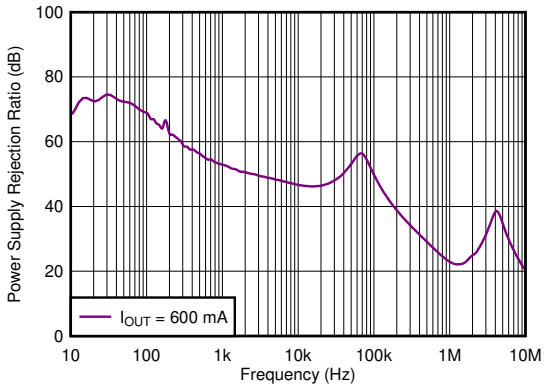


Figure 7-5. Start-Up With a 600mA Load



V_{IN} = 2.5V, V_{OUT} = 1.8V, I_{OUT} = 600mA

Figure 7-6. PSRR (2.5V to 1.8V at 600mA)

7.3 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV757P. If the input source is reactive, use multiple input capacitors in parallel with the 1µF input capacitor to lower the input supply impedance over frequency.

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7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close as possible to the device.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- For packages with thermal pads, solder the thermal pad to copper to achieve best thermal resistance. Thermal resistance increases significantly when the thermal pad is not soldered.

7.4.2 Layout Examples

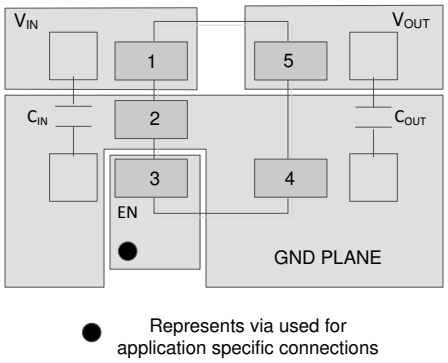

Figure 7-7. Layout Example: DBV Package

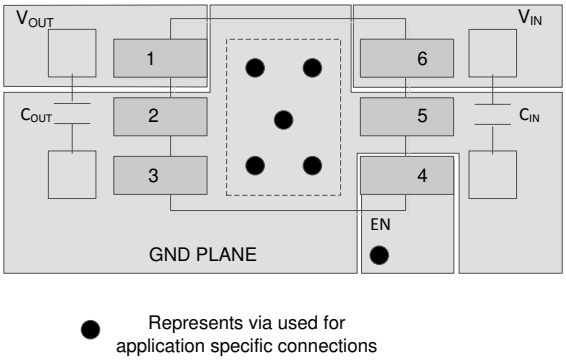

Figure 7-8. Layout Example: DRV Package

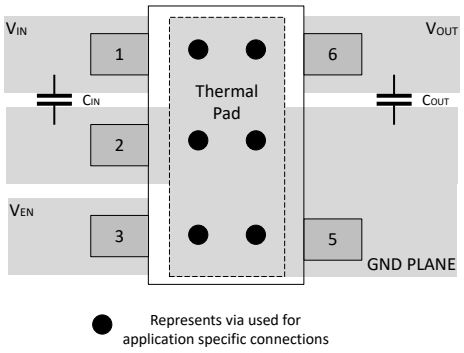

Figure 7-9. Layout Example: DYD Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TLV757**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 50mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V). **P** indicates an active output discharge feature. All members of the TLV757P family actively discharge the output when the device is disabled. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.6V to 5V in 50mV increments are available. Contact the factory for details and availability.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2023) to Revision C (March 2024)	Page
• Changed DYD package from *Preview* to *Production Data*	1
• Added SOT-23 (DYD) package bullet to *Features* section	1
• Added last bullet item to *Layout Guidelines* section	21
• Added *Layout Example: DYD Package* figure	21

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Changes from Revision A (December 2017) to Revision B (December 2023) **Page**

- Changed DBV package from *Preview* to *Production Data* (active)..... 1
- Added DYD package as Preview..... 1
- Added links to *Applications* section..... 1
- Added package discussion to *Description* section..... 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV75709PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1H8F
TLV75709PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1H8F
TLV75709PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HGH
TLV75709PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HGH
TLV75710PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FEF
TLV75710PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FEF
TLV75710PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HHH
TLV75710PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HHH
TLV75712PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FFF
TLV75712PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1FFF
TLV75712PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HIH
TLV75712PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HIH
TLV75712PDYDR	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3DVH
TLV75712PDYDR.A	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3DVH
TLV75715PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FGF
TLV75715PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1FGF
TLV75715PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HJH
TLV75715PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HJH
TLV75715PDRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HJH
TLV75715PDRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HJH
TLV75718PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FHF
TLV75718PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FHF
TLV75718PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HKH
TLV75718PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HKH
TLV75718PDYDR	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3DWH
TLV75718PDYDR.A	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3DWH
TLV75719PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1H7F
TLV75719PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1H7F
TLV75719PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HLH

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV75719PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HLH
TLV75725PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FIF
TLV75725PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FIF
TLV75725PDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FIF
TLV75725PDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FIF
TLV75725PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HMH
TLV75725PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HMH
TLV75725PDYDR	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3DXH
TLV75725PDYDR.A	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3DXH
TLV75728PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FJF
TLV75728PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1FJF
TLV75728PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HNH
TLV75728PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HNH
TLV75728PDRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HNH
TLV75728PDRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HNH
TLV75728PDYDR	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3DZH
TLV75728PDYDR.A	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3DZH
TLV75729PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1H9F
TLV75729PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1H9F
TLV75730PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1GHF
TLV75730PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GHF
TLV75730PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HOH
TLV75730PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HOH
TLV75730PDRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HOH
TLV75730PDRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HOH
TLV75730PDYDR	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3E1H
TLV75730PDYDR.A	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3E1H
TLV75733PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FKF
TLV75733PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1FKF
TLV75733PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HPH
TLV75733PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HPH

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV75733PDRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HPH
TLV75733PDRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HPH
TLV75733PDYDR	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3E2H
TLV75733PDYDR.A	Active	Production	SOT-23 (DYD) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3E2H
TLV75740PDRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HQH
TLV75740PDRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HQH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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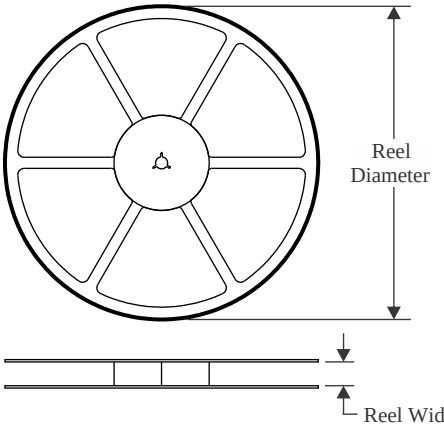
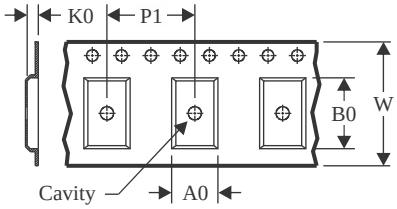
TAPE AND REEL INFORMATION

REEL DIMENSIONS

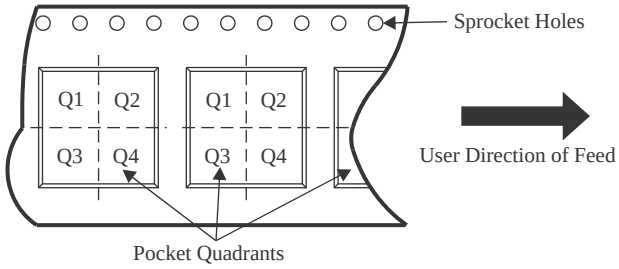


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

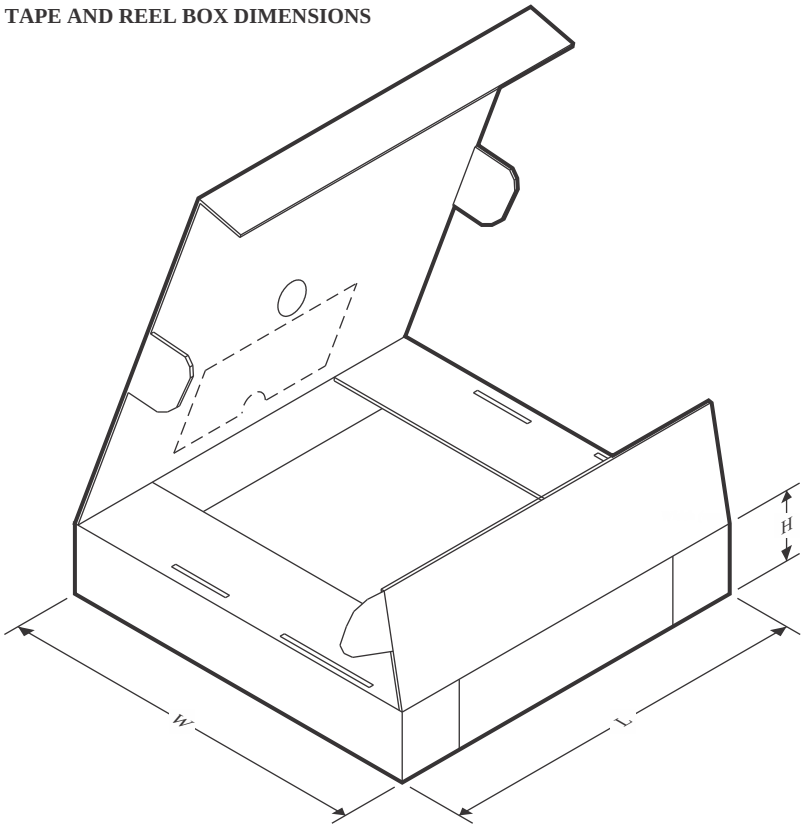


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75709PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75709PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75710PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75710PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75710PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75712PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75712PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75712PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75712PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75715PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75715PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75715PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75715PDRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75718PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75718PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75718PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75719PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75719PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75719PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75725PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75725PDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75725PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75725PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75728PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75728PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75728PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75728PDRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75728PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75729PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75729PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75730PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75730PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75730PDRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75730PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75733PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75733PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75733PDRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75733PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75740PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75709PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75709PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75710PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75710PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75710PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75712PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75712PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75712PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75712PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75715PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75715PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75715PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75715PDRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75718PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV75718PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75718PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75719PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75719PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

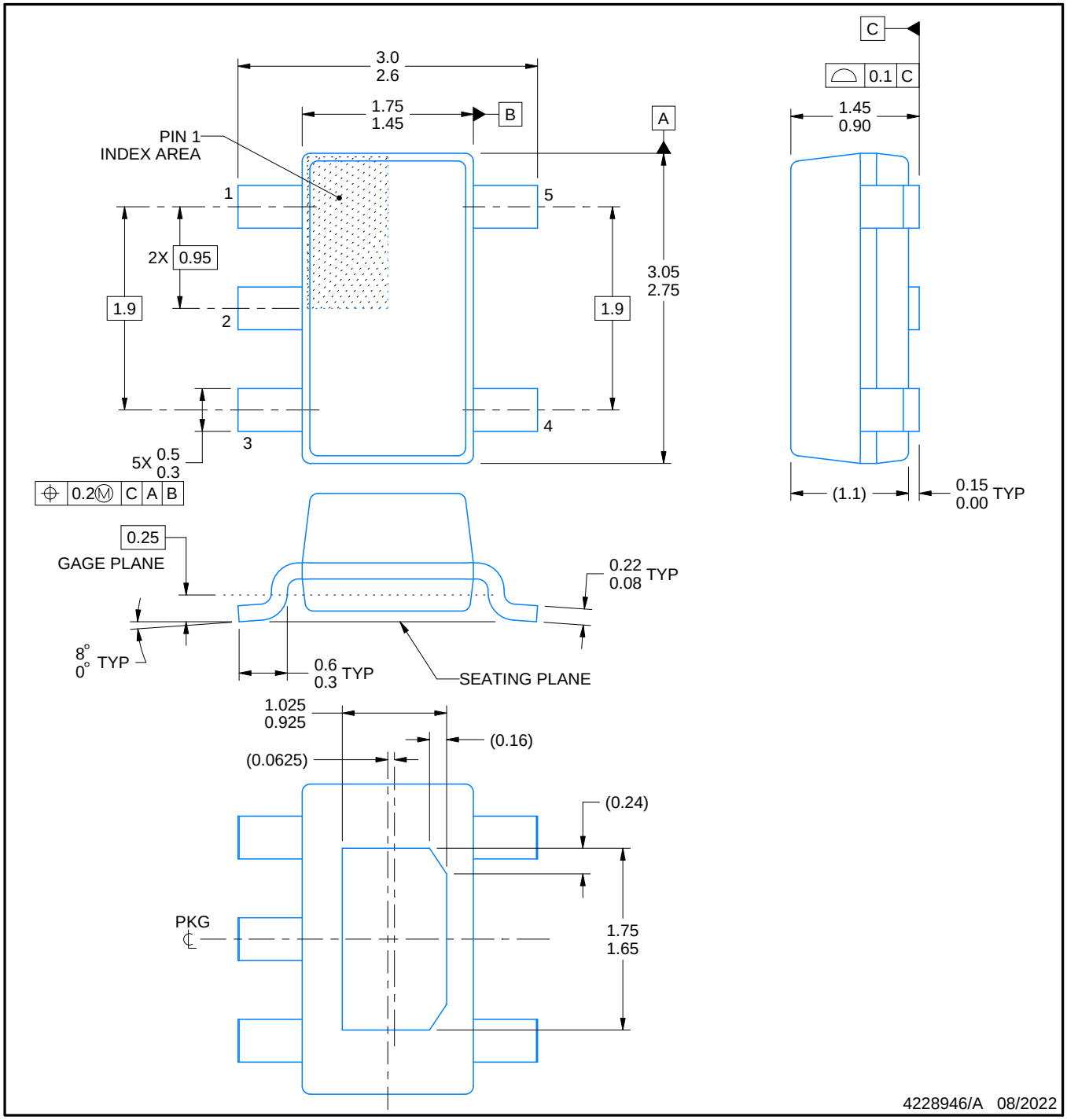
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75719PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75725PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV75725PDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75725PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75725PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75728PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75728PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75728PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75728PDRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75728PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75729PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75729PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75730PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV75730PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75730PDRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75730PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75733PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV75733PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75733PDRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75733PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75740PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DYD0005A

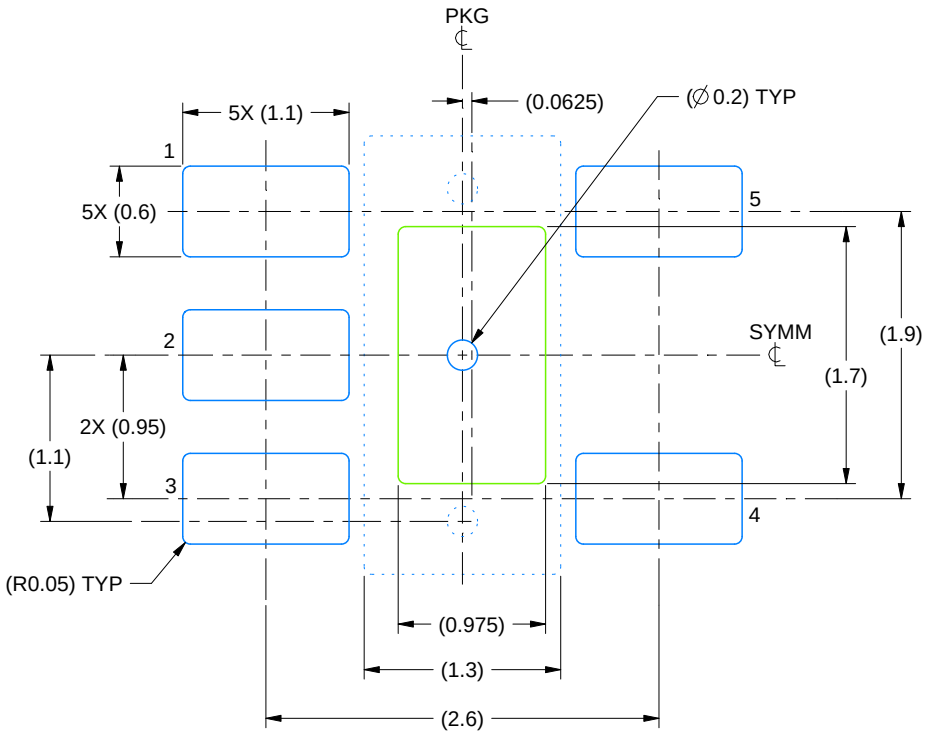
SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

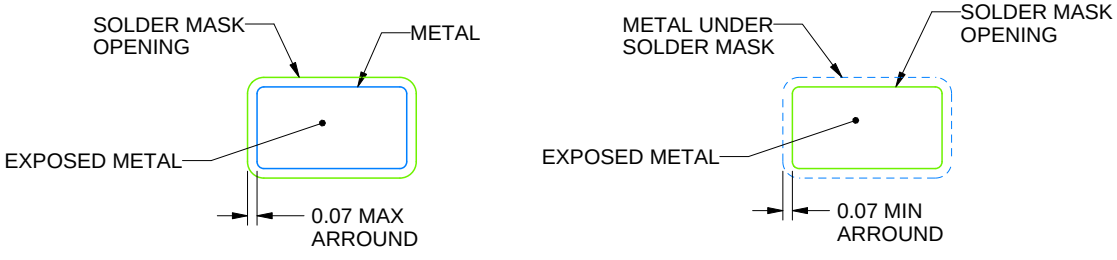


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK DEFINED (PREFERRED)

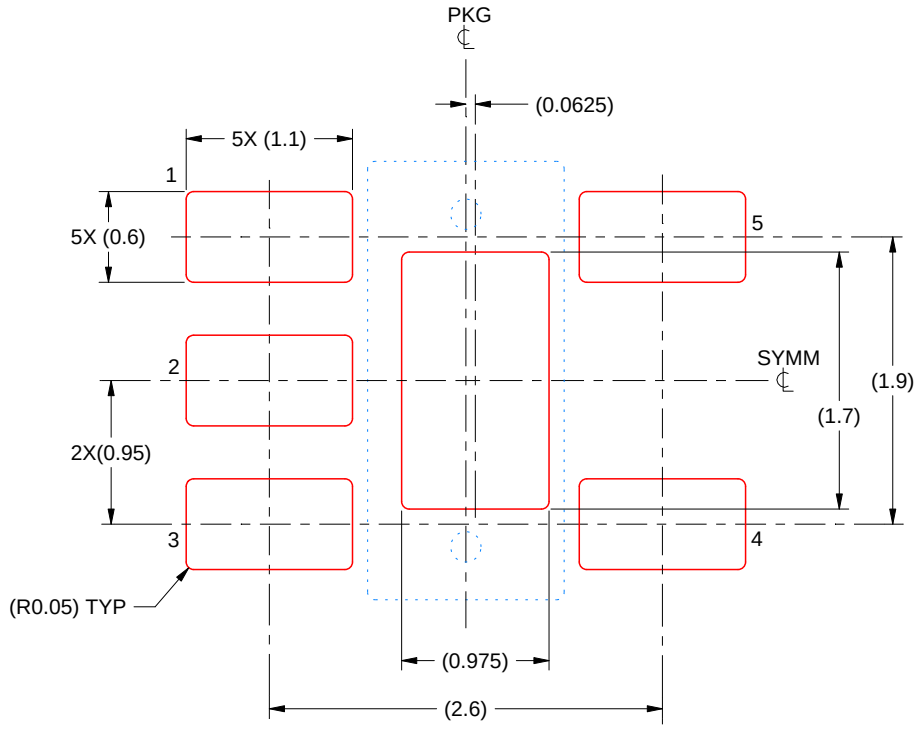
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4228946/A 08/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:20X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.100	1.09 X 1.90
0.125	0.975 X 1.700 (SHOWN)
0.150	0.89 X 1.55
0.175	0.82 X 1.44

4228946/A 08/2022

NOTES: (continued)

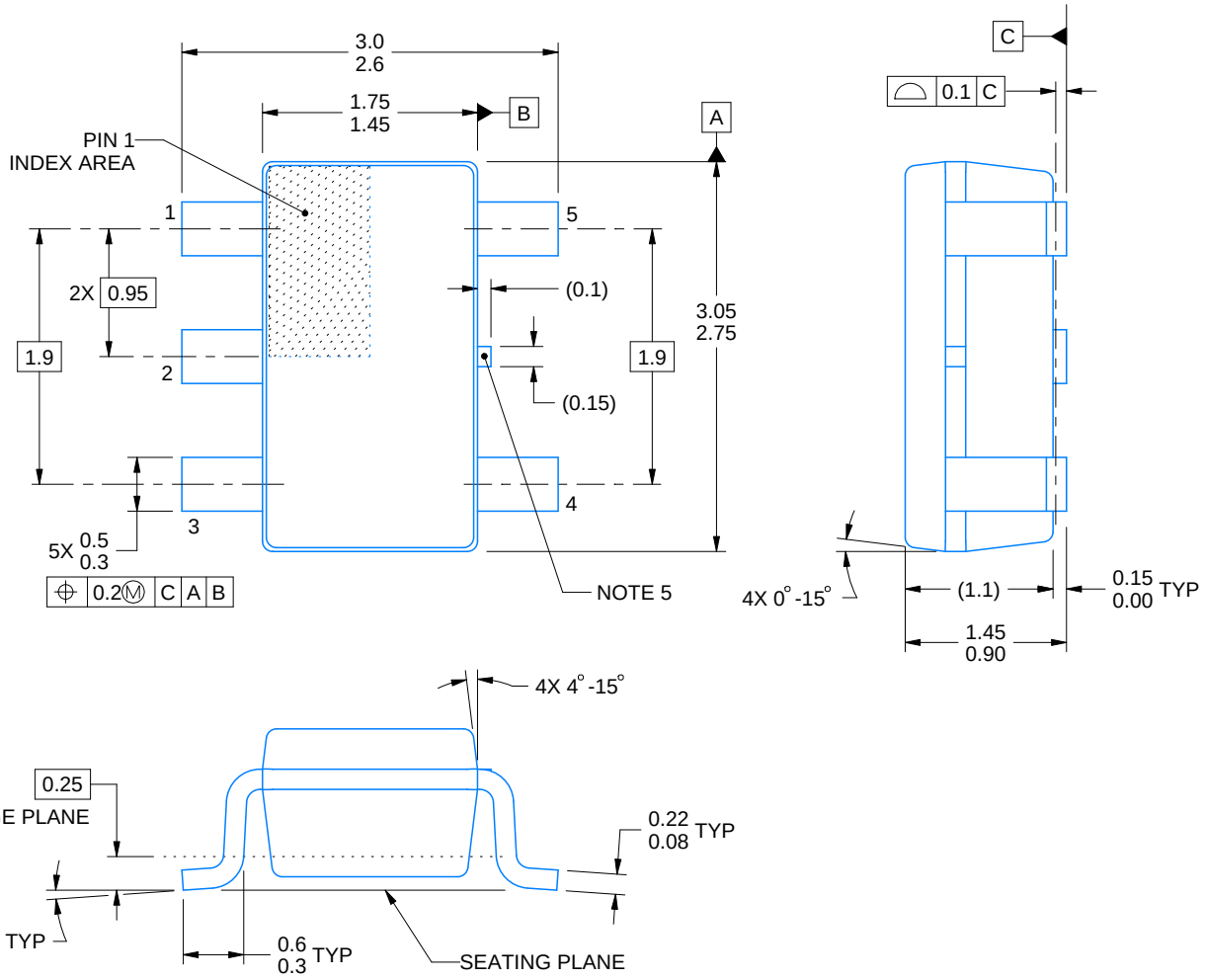
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

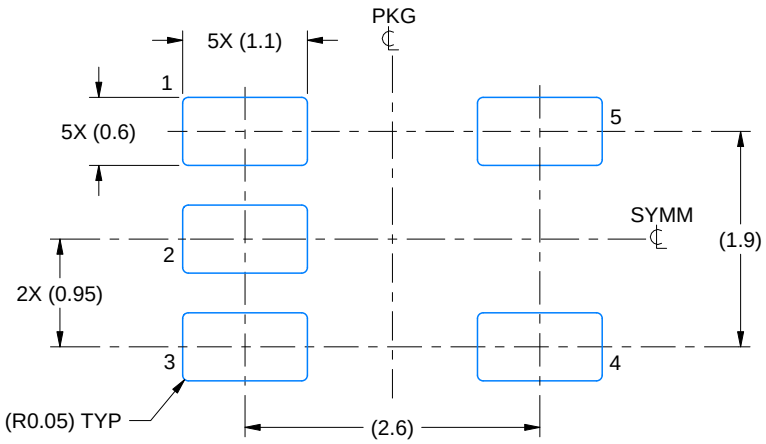
SMALL OUTLINE TRANSISTOR



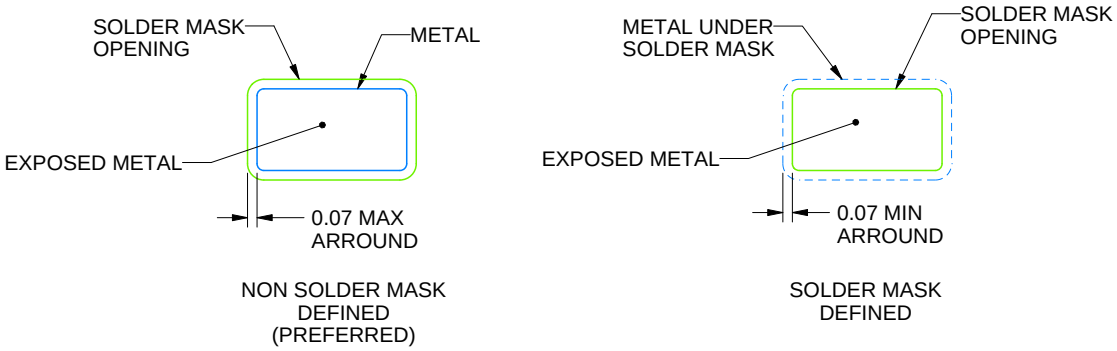
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

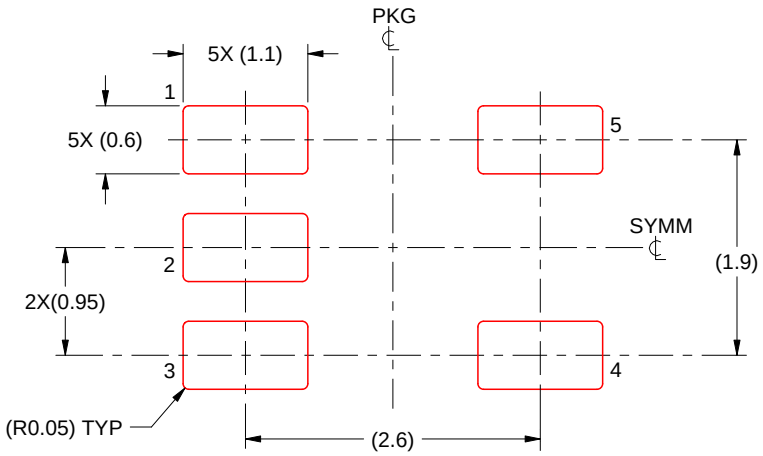


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

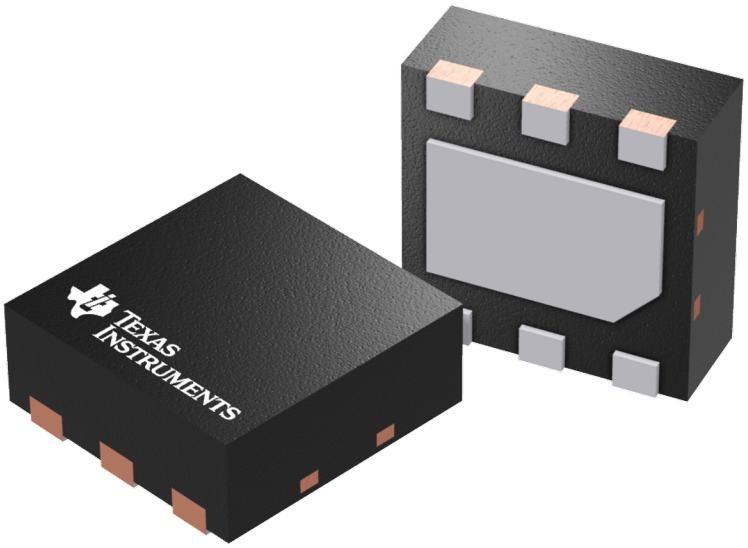
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



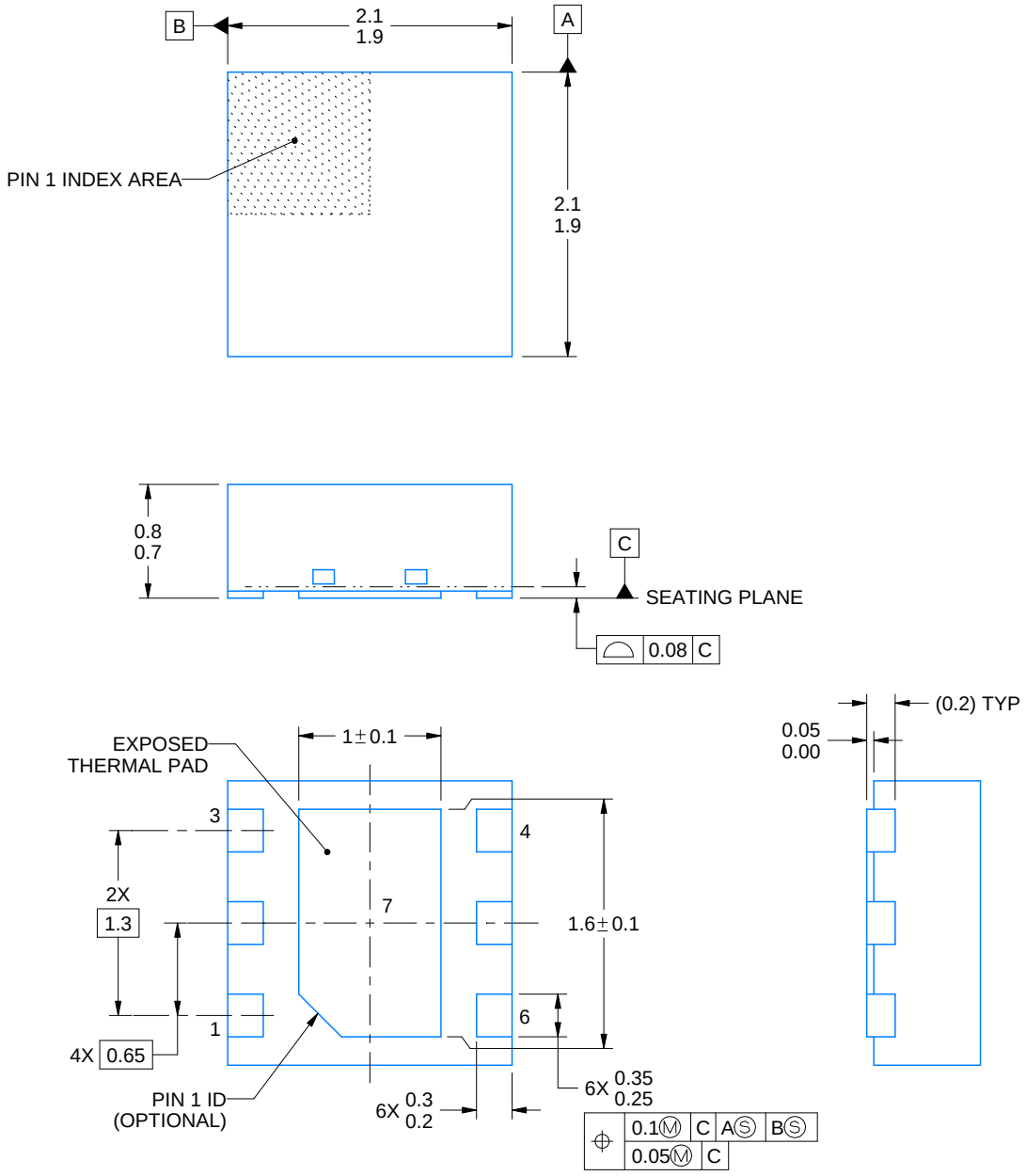
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

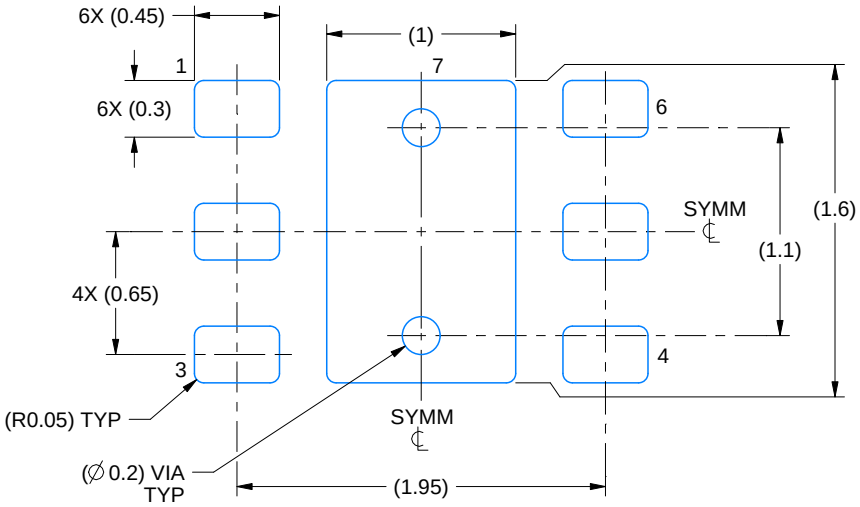
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

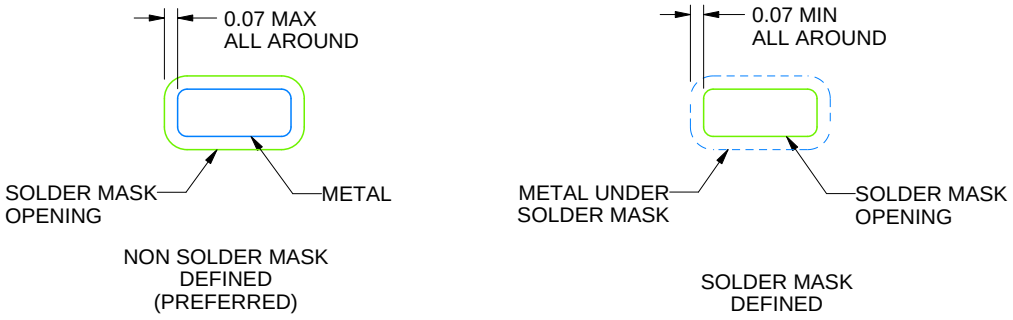


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

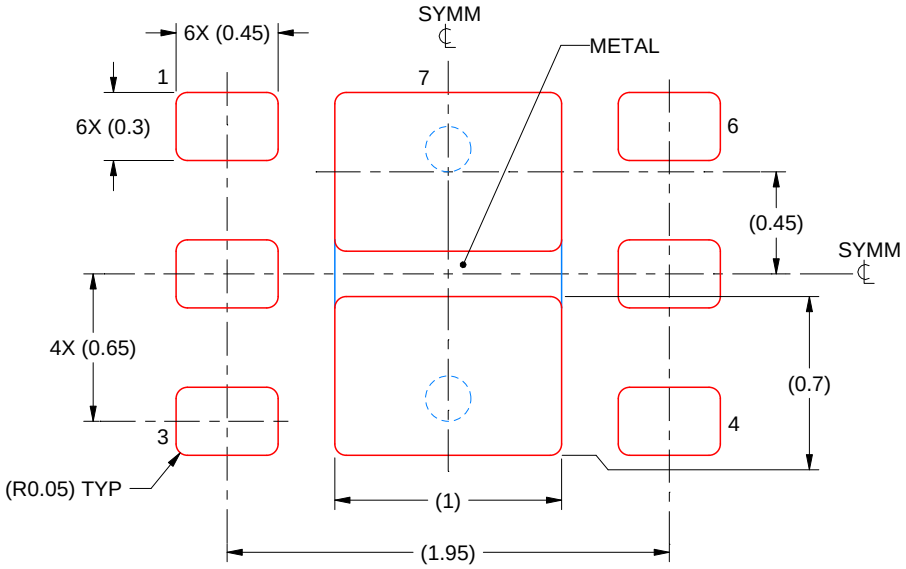
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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