



### DESCRIPTION

The MP5496 is a complete power management solution that integrates four high-efficiency, step-down DC/DC converters, five low-dropout (LDO) regulators, and a flexible logic interface.

A DC/DC converter with constant-on-time (COT) control provides fast transient response. The default 1.5MHz fixed switching frequency during continuous conduction mode (CCM) greatly reduces the external inductor and capacitor values. Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), and thermal shutdown.

The output voltage is adjustable through the I<sup>2</sup>C interface, or can be preset by the one-time programmable (OTP) function. The start-up and shutdown sequences can be configured via the OTP.

By using the I<sup>2</sup>C or OTP, the MP5496 can be utilized to configure the buck and LDO output voltages, mode, buck 1 and buck 3 current limits, and the enable function of all the buck converters and LDOs (ENBUCK/LDO).

When using only the I<sup>2</sup>C interface, the MP5496 allows users to configure the buck 2 and buck 4 current limits, slew rate (DVS slew rate), discharge (DISCHG), system enable (SYSEN), and software reset (SFRST). Status and ID2 registers can also be read via the I<sup>2</sup>C.

Additional features, such as AUTOON, frequency, power-on delay, RST delay, push-button time, LDORTC output voltage, OTP version, and the I<sup>2</sup>C slave address can only be configured via the OTP.

The MP5496 requires a minimal number of external components, and is available in a space-saving QFN-28 (4mmx4mm) package.

### FEATURES

#### Four High-Efficiency Step-Down Converters

- Buck 1: 4.5A DC/DC Converter
- Buck 2: 2.5A DC/DC Converter
- Buck 3: 4A DC/DC Converter
- Buck 4: 2A DC/DC Converter
- 0.6V to 2.1875V/12.5mV Step V<sub>OUT</sub> Range
- 2.8V to 5.5V Operating Input Range
- Adjustable Switching Frequency
- Configurable Forced PWM, Auto-PFM/PWM Mode
- Hiccup Over-Current Protection (OCP)

#### Five Low-Dropout Regulators

- One RTC-Dedicated LDO
- Four Low-Noise LDOs
- Two Separate Input Power Supplies
- 100mV Dropout at 300mA Load

#### System

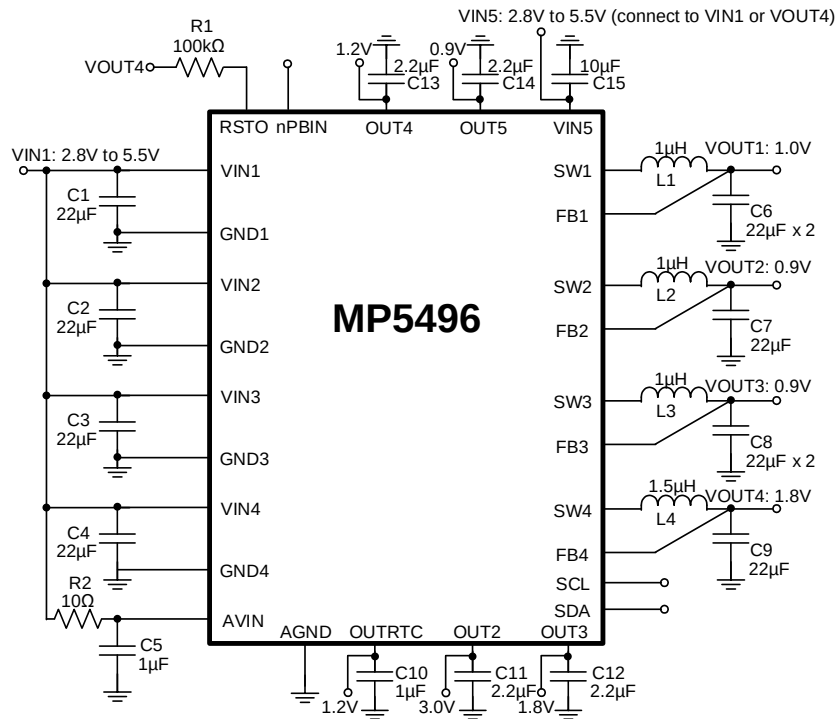
- I<sup>2</sup>C Bus and OTP
- Power-On/Off Button
- Power-On Reset Output
- Flexible Power-On/Off Sequencing via OTP
- Flexible DC/DC, LDO On/Off via OTP

### APPLICATIONS

- Cable Modems, Set-Top Boxes
- Televisions
- Wi-Fi Routers/Access Points
- PoS Machines
- SSDs
- IP Cameras

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## TYPICAL APPLICATION



**OTP E-Fuse Selected Table by Default (MP5496GR-0001)**

| OTP Items                      | Buck 1    | Buck 2 | Buck 3 | Buck 4 | LDORTC    | LDO2   | LDO3  | LDO4  | LDO5   |
|--------------------------------|-----------|--------|--------|--------|-----------|--------|-------|-------|--------|
| Output voltage                 | 1.0V      | 0.9V   | 0.9V   | 1.8V   | 1.2V      | 3V     | 1.8V  | 1.2V  | 0.9V   |
| Initial on/off                 | On        | On     | On     | On     | On        | On     | Off   | On    | On     |
| Mode                           | FPWM      | FPWM   | FPWM   | FPWM   | N/A       |        |       |       |        |
| Start-up delay/time slot #     | 0ms/0     | 4ms/2  | 2ms/1  | 6ms/3  | Always on | 12ms/6 | 2ms/1 | 8ms/4 | 10ms/5 |
| Automatic start-up             | Yes       |        |        |        |           |        |       |       |        |
| Switching frequency            | 1.5MHz    |        |        |        |           |        |       |       |        |
| Push-button timer              | 2 seconds |        |        |        |           |        |       |       |        |
| RSTO delay                     | 100ms     |        |        |        |           |        |       |       |        |
| Buck 1 peak current limit      | 6.8A      |        |        |        |           |        |       |       |        |
| Buck 3 peak current limit      | 5.6A      |        |        |        |           |        |       |       |        |
| I <sup>2</sup> C slave address | 0x69      |        |        |        |           |        |       |       |        |
| OTP version                    | 0004      |        |        |        |           |        |       |       |        |

**Other Parameter Information for the MP5496GR-0001**

|                       | Buck 1 | Buck 2 | Buck 3 | Buck 4 | LDORTC | LDO2 | LDO3 | LDO4 | LDO5 |
|-----------------------|--------|--------|--------|--------|--------|------|------|------|------|
| Minimum input voltage | 3V     |        |        |        |        |      |      |      |      |
| Typical input voltage | 3.3V   |        |        |        |        |      |      |      |      |
| Maximum input voltage | 3.6V   |        |        |        |        |      |      |      |      |

## ORDERING INFORMATION

| Part Number*    | Package          | Top Marking | MSL Rating |
|-----------------|------------------|-------------|------------|
| MP5496GR-xxxx** | QFN-28 (4mmx4mm) | See Below   | 1          |
| MP5496GR-0001   | QFN-28 (4mmx4mm) | See Below   |            |
| EVKT-MP5496     | Evaluation kit   | N/A         |            |

\* For Tape & Reel, add suffix –Z (e.g. MP5496GR-XXXX–Z).

\*\* “xxxx” is the configuration code identifier for the register setting stored in the OTP. The default number is “0001”. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0001” code. MP5496GR-0001 is the default version.

## TOP MARKING

**MPSYWW**  
**MP5496**  
**LLLLLL**

MPS: MPS prefix  
Y: Year code  
WW: Week code  
MP5496: Part number  
LLLLLL: Lot number

## EVKT-MP5496 EVALUATION KIT

EVKT-MP5496 kit contents (items below can be ordered separately):

| # | Part Number        | Item                                                                                                 | Quantity |
|---|--------------------|------------------------------------------------------------------------------------------------------|----------|
| 1 | EV5496-R-00B       | MP5496GR-CCCC evaluation board                                                                       | 1        |
| 2 | EVKT-USBI2C-02-BAG | Includes USB to I <sup>2</sup> C Communication Interface device, one USB cable, and one ribbon cable | 1        |
| 3 | MP5496GR-CCCC      | IC with default configurations                                                                       | 2        |

Order directly from [MonolithicPower.com](http://MonolithicPower.com) or our distributors.

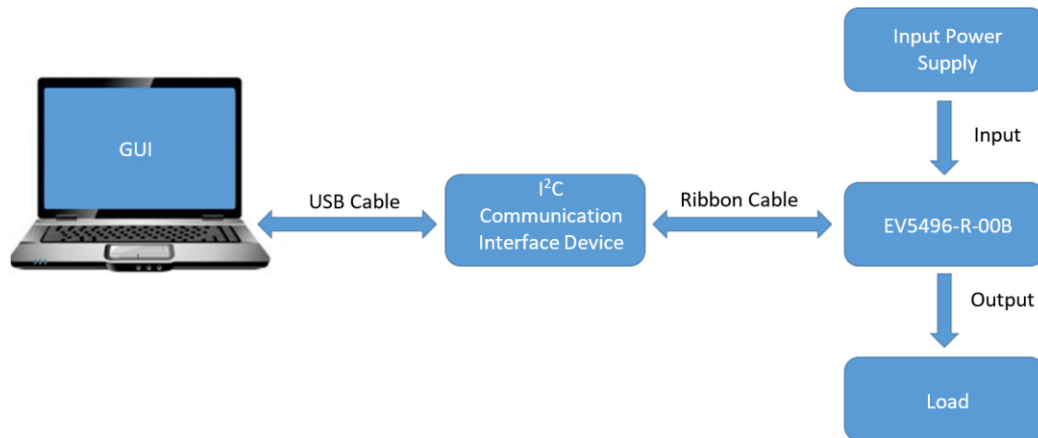
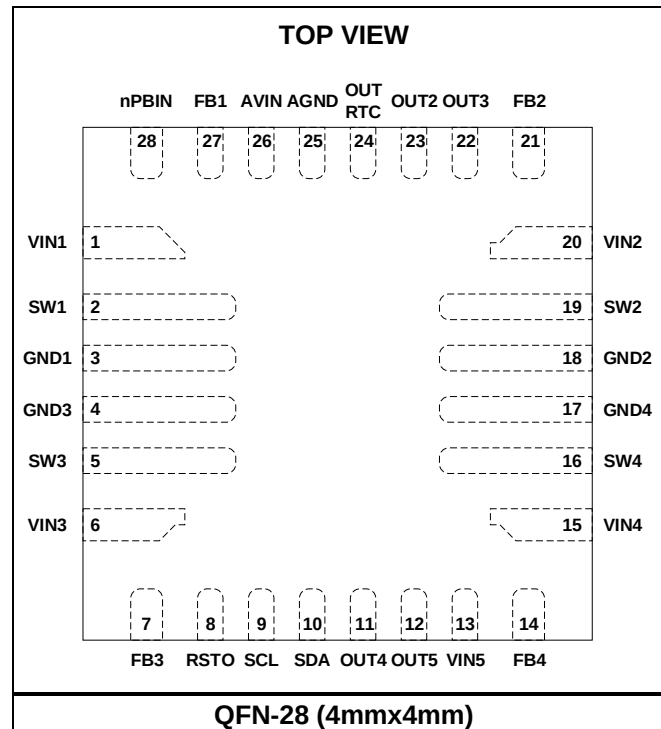


Figure 1: EVKT-MP5496 Evaluation Kit Set-Up

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name   | Description                                                                                                                                                                                                                                                          |
|-------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | VIN1   | <b>Buck 1 supply voltage input.</b> The MP5496 operates from a 2.8V to 5.5V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN1 using a wide PCB trace. VIN1, VIN2, VIN3, VIN4, and AVIN must be connected to the same bus voltage. |
| 2     | SW1    | <b>Buck 1 switch output.</b> Connect SW1 using a wide PCB trace.                                                                                                                                                                                                     |
| 3     | GND1   | <b>Buck 1 power ground.</b> GND1 requires special consideration when designing the PCB layout. Connect GND1 to GND with copper traces and vias.                                                                                                                      |
| 4     | GND3   | <b>Buck 3 power ground.</b> GND3 requires special consideration when designing the PCB layout. Connect GND3 to GND with copper traces and vias.                                                                                                                      |
| 5     | SW3    | <b>Buck 3 switch output.</b> Connect SW3 using a wide PCB trace.                                                                                                                                                                                                     |
| 6     | VIN3   | <b>Buck 3 supply voltage input.</b> The MP5496 operates from a 2.8V to 5.5V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN3 using a wide PCB trace.                                                                             |
| 7     | FB3    | <b>Buck 3 feedback.</b> Connect the output of buck 3 directly to FB3.                                                                                                                                                                                                |
| 8     | RSTO   | <b>PMIC to CPU output reset.</b> Once the buck 4 output is ready, the RSTO goes high after a delay. RSTO is an open-drain output that requires an external pull-up resistor.                                                                                         |
| 9     | SCL    | <b>I<sup>2</sup>C clock signal input.</b> Use an external resistor to pull SCL up to AVIN if I <sup>2</sup> C functionality is not used.                                                                                                                             |
| 10    | SDA    | <b>I<sup>2</sup>C data.</b> Use an external resistor to pull SDA up to AVIN if I <sup>2</sup> C functionality is not used.                                                                                                                                           |
| 11    | OUT4   | <b>LDO4 output.</b> LDO4 is powered by VIN5.                                                                                                                                                                                                                         |
| 12    | OUT5   | <b>LDO5 output.</b> LDO5 is powered by VIN5.                                                                                                                                                                                                                         |
| 13    | VIN5   | <b>LDO4 and LDO5 power input.</b>                                                                                                                                                                                                                                    |
| 14    | FB4    | <b>Buck 4 feedback.</b> Connect the output of buck 4 directly to FB4.                                                                                                                                                                                                |
| 15    | VIN4   | <b>Buck 4 supply voltage input.</b> The MP5496 operates from a 2.8V to 5.5V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN4 using a wide PCB trace.                                                                             |
| 16    | SW4    | <b>Buck 4 switch output.</b> Connect SW4 using a wide PCB trace.                                                                                                                                                                                                     |
| 17    | GND4   | <b>Buck 4 power ground.</b> GND4 requires special consideration when designing the PCB layout. Connect GND4 to GND with copper traces and vias.                                                                                                                      |
| 18    | GND2   | <b>Buck 2 power ground.</b> GND2 requires special consideration when designing the PCB layout. Connect GND2 to GND with copper traces and vias.                                                                                                                      |
| 19    | SW2    | <b>Buck 2 switch output.</b> Connect SW2 using a wide PCB trace.                                                                                                                                                                                                     |
| 20    | VIN2   | <b>Supply voltage input for buck 2, LDORTC, LDO2, and LDO3.</b> The MP5496 operates from a 2.8V to 5.5V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN2 using a wide PCB trace.                                                 |
| 21    | FB2    | <b>Buck 2 feedback.</b> Connect the output of buck 2 directly to FB2.                                                                                                                                                                                                |
| 22    | OUT3   | <b>LDO 3 output.</b> LDO 3 is powered by VIN2.                                                                                                                                                                                                                       |
| 23    | OUT2   | <b>LDO 2 output.</b> LDO 2 is powered by VIN2.                                                                                                                                                                                                                       |
| 24    | OUTRTC | <b>RTC LDO output.</b> This LDO is powered by VIN2. Set a sufficient output voltage to achieve a lower voltage gap between VIN2 and OUTRTC.                                                                                                                          |
| 25    | AGND   | <b>Analog ground.</b> Connect AGND to power ground.                                                                                                                                                                                                                  |
| 26    | AVIN   | <b>Power supply input for logic circuitry.</b> Bypass AVIN with a 0.1μF to 1μF ceramic capacitor to AGND. Connect AVIN to the system input.                                                                                                                          |
| 27    | FB1    | <b>Buck 1 feedback.</b> Connect the output of buck 1 directly to FB1.                                                                                                                                                                                                |
| 28    | nPBIN  | <b>Push-button input.</b> nPBIN is a logic input pin that can start up or shut down the device. A logic low over a preset deglitch time must be applied to nPBIN. nPBIN has a weak internal pull-up current.                                                         |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                     |                                                                   |
|---------------------------------------------------------------------|-------------------------------------------------------------------|
| VIN1, VIN2, VIN3, VIN4, VIN5, AVIN.....                             | 0.3V to 6.25V                                                     |
| V <sub>SWx</sub> .....                                              | -0.6V (-5V for <10ns) to<br>V <sub>IN</sub> + 0.3V (7V for <10ns) |
| All other pins .....                                                | -0.3V to +6.25V                                                   |
| Continuous power dissipation (T <sub>A</sub> = 25°C) <sup>(2)</sup> | 2.84W                                                             |
| Junction temperature .....                                          | 150°C                                                             |
| Lead temperature .....                                              | 260°C                                                             |
| Storage temperature .....                                           | -65°C to +150°C                                                   |

## ESD Ratings

|                                 |        |
|---------------------------------|--------|
| Human body model (HBM) .....    | ±2000V |
| Charged device model (CDM)..... | ±750V  |

## Recommended Operating Conditions <sup>(3)</sup>

|                                               |                 |
|-----------------------------------------------|-----------------|
| Step-down regulator (V <sub>IN</sub> ) .....  | 2.8V to 5.5V    |
| Step-down regulator (V <sub>OUT</sub> ) ..... | 0.6V to 2.18V   |
| LDO regulator (V <sub>OUTL</sub> ) .....      | 0.8V to 3.9V    |
| Operating junction temp (T <sub>J</sub> ) ... | -40°C to +125°C |

## Thermal Resistance

 $\theta_{JA}$      $\theta_{JC}$ 

QFN-28 (4mmx4mm)

JESD51-7 <sup>(4)</sup> ..... 44..... 9 .... °C/W

### Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature, T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation may produce an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

VIN1 = VIN2 = VIN3 = VIN4 = VIN5 = AVIN = 5V, T<sub>J</sub> = -40°C to 125°C <sup>(5)</sup>, unless otherwise noted.

| Parameter                                          | Symbol                | Condition                                                   | Min    | Typ  | Max    | Units |
|----------------------------------------------------|-----------------------|-------------------------------------------------------------|--------|------|--------|-------|
| Supply current (no switching)                      | I <sub>IN</sub>       | No switching, feedback is high, T <sub>J</sub> = 25°C       |        | 420  | 500    | μA    |
| Default oscillation frequency                      | f <sub>SW</sub>       |                                                             | 1.2    | 1.5  | 1.8    | MHz   |
| Thermal shutdown entry threshold <sup>(6)</sup>    | T <sub>OTP_R</sub>    |                                                             | 145    | 153  | 162    | °C    |
| Thermal shutdown recovery threshold <sup>(6)</sup> | T <sub>HYS</sub>      |                                                             | 121    | 130  | 139    | °C    |
| <b>Step-Down Regulator</b>                         |                       |                                                             |        |      |        |       |
| AVIN UVLO rising                                   | V <sub>AIN1_R</sub>   |                                                             | 2.4    | 2.55 | 2.7    | V     |
| AVIN UVLO hysteresis                               | V <sub>AIN1_HYS</sub> |                                                             |        | 300  |        | mV    |
| VIN1 UVLO rising                                   | V <sub>IN1_R</sub>    |                                                             |        | 2.45 |        | V     |
| VIN1 UVLO hysteresis                               | V <sub>IN1_HYS</sub>  |                                                             |        | 300  |        | mV    |
| VIN2 UVLO rising <sup>(7)</sup>                    | V <sub>IN2_R</sub>    |                                                             |        | 2.45 |        | V     |
| VIN2 UVLO hysteresis <sup>(7)</sup>                | V <sub>IN2_HYS</sub>  |                                                             |        | 300  |        | mV    |
| VIN3 UVLO rising                                   | V <sub>IN3_R</sub>    |                                                             |        | 2.45 |        | V     |
| VIN3 UVLO hysteresis                               | V <sub>IN3_HYS</sub>  |                                                             |        | 300  |        | mV    |
| VIN5 UVLO rising                                   | V <sub>IN5_R</sub>    |                                                             |        | 2.45 |        | V     |
| VIN5 UVLO hysteresis                               | V <sub>IN5_HYS</sub>  |                                                             |        | 300  |        | mV    |
| Feedback voltage accuracy                          | V <sub>FB1</sub>      | Default output of buck 1                                    | 0.985  | 1    | 1.015  | V     |
|                                                    | V <sub>FB2</sub>      | Default output of buck 2                                    | 0.8865 | 0.9  | 0.9135 | V     |
|                                                    | V <sub>FB3</sub>      | Default output of buck 3                                    | 0.8865 | 0.9  | 0.9135 | V     |
|                                                    | V <sub>FB4</sub>      | Default output of buck 4                                    | 1.7730 | 1.8  | 1.8270 | V     |
| Maximum duty cycle                                 | D <sub>MAX</sub>      | CH2 and CH4 only                                            |        | 100  |        | %     |
| <b>Buck 1, Buck 3 (4.5A/4A)</b>                    |                       |                                                             |        |      |        |       |
| HS switch on resistance                            | HS <sub>RDS-ON1</sub> | 500mA, T <sub>J</sub> = 25°C                                | 10     | 30   | 50     | mΩ    |
|                                                    | HS <sub>RDS-ON3</sub> |                                                             |        |      |        |       |
|                                                    | HS <sub>RDS-ON1</sub> | 500mA, T <sub>J</sub> = -40°C to +125°C                     | 10     | 30   | 50     | mΩ    |
|                                                    | HS <sub>RDS-ON3</sub> |                                                             |        |      |        |       |
| LS switch on resistance                            | LS <sub>RDS-ON1</sub> | 500mA, T <sub>J</sub> = 25°C                                |        | 12   | 20     | mΩ    |
|                                                    | LS <sub>RDS-ON3</sub> |                                                             |        |      |        |       |
|                                                    | LS <sub>RDS-ON1</sub> | 500mA, T <sub>J</sub> = -40°C to +125°C                     |        | 12   | 20     | mΩ    |
|                                                    | LS <sub>RDS-ON3</sub> |                                                             |        |      |        |       |
| Switch leakage 1                                   | HS <sub>WILK1</sub>   | EN = 0V, VIN = 5.5V, T <sub>J</sub> = 25°C, SW = 0V or 5.5V |        | 0    | 1      | μA    |
|                                                    | HS <sub>WILK3</sub>   |                                                             |        |      |        |       |
| Switch leakage 2                                   | LS <sub>WILK1</sub>   | EN = 0V, VIN = 5.5V, T <sub>J</sub> = 25°C, SW = 0V or 5.5V |        | 0    | 1      | μA    |
|                                                    | LS <sub>WILK3</sub>   |                                                             |        |      |        |       |
| High-side current limit                            | I <sub>LIMIT1</sub>   | Under 20% duty cycle, T <sub>J</sub> = 25°C                 | 5.5    | 6.8  | 8.3    | A     |
|                                                    | I <sub>LIMIT3</sub>   |                                                             | 4.5    | 5.6  | 7      | A     |

**ELECTRICAL CHARACTERISTICS (continued)**VIN1 = VIN2 = VIN3 = VIN4 = VIN5 = AVIN = 5V, T<sub>J</sub> = -40°C to +125°C <sup>(5)</sup>, unless otherwise noted.

| Parameter                       | Symbol                | Condition                                                                    | Min   | Typ | Max   | Units |
|---------------------------------|-----------------------|------------------------------------------------------------------------------|-------|-----|-------|-------|
| Minimum on time <sup>(8)</sup>  | t <sub>ON_MIN1</sub>  |                                                                              |       | 40  |       | ns    |
|                                 | t <sub>ON_MIN3</sub>  |                                                                              |       | 33  |       | ns    |
| Minimum off time <sup>(8)</sup> | t <sub>OFF_MIN1</sub> |                                                                              |       | 120 |       | ns    |
|                                 | t <sub>OFF_MIN3</sub> |                                                                              |       | 120 |       | ns    |
| Output discharge resistance     | R <sub>O_DIS1</sub>   |                                                                              |       | 7   |       | Ω     |
| Soft-start time                 | t <sub>SS_B1</sub>    | V <sub>OUT</sub> = 10% to 90%                                                |       | 450 |       | μs    |
|                                 | t <sub>SS_B3</sub>    | V <sub>OUT</sub> = 10% to 90%                                                |       | 450 |       | μs    |
| <b>Buck 2, Buck 4 (2.5A/2A)</b> |                       |                                                                              |       |     |       |       |
| HS switch on resistance         | HS <sub>RDS-ON2</sub> | 500mA, T <sub>J</sub> = 25°C                                                 | 20    | 50  | 80    | mΩ    |
|                                 | HS <sub>RDS-ON4</sub> |                                                                              |       |     |       |       |
|                                 | HS <sub>RDS-ON2</sub> | 500mA, T <sub>J</sub> = -40°C to 125°C                                       | 20    | 50  | 80    | mΩ    |
|                                 | HS <sub>RDS-ON4</sub> |                                                                              |       |     |       |       |
| LS switch on resistance         | LS <sub>RDS-ON2</sub> | 500mA, T <sub>J</sub> = 25°C                                                 |       | 65  | 105   | mΩ    |
|                                 | LS <sub>RDS-ON4</sub> |                                                                              |       |     |       |       |
|                                 | LS <sub>RDS-ON2</sub> | 500mA, T <sub>J</sub> = -40°C to 125°C                                       |       | 65  | 105   | mΩ    |
|                                 | LS <sub>RDS-ON4</sub> |                                                                              |       |     |       |       |
| Switch leakage 3                | HS <sub>WILK2</sub>   | Shutdown, V <sub>IN</sub> = 5.5V,<br>SW = 0V or 5.5V, T <sub>A</sub> = 25°C  |       | 0   | 1     | μA    |
|                                 | HS <sub>WILK4</sub>   |                                                                              |       |     |       |       |
| Switch leakage 4                | LS <sub>WILK2</sub>   | Shutdown, V <sub>IN</sub> = 5.5V,<br>SW = 0V or 5.5V, T <sub>A</sub> = 25°C  |       | 0   | 1     | μA    |
|                                 | LS <sub>WILK4</sub>   |                                                                              |       |     |       |       |
| High-side current limit         | I <sub>LIMIT2</sub>   | Under 20% duty cycle, T <sub>J</sub> = 25°C                                  | 3     | 4.2 | 5.4   | A     |
|                                 | I <sub>LIMIT4</sub>   |                                                                              |       |     |       |       |
| Minimum on time <sup>(8)</sup>  | t <sub>ON_MIN2</sub>  |                                                                              |       | 32  |       | ns    |
|                                 | t <sub>ON_MIN4</sub>  |                                                                              |       | 32  |       | ns    |
| Minimum off time <sup>(8)</sup> | t <sub>OFF_MIN2</sub> |                                                                              |       | 100 |       | ns    |
|                                 | t <sub>OFF_MIN4</sub> |                                                                              |       | 100 |       | ns    |
| Output discharge resistance     | R <sub>O_DIS2</sub>   |                                                                              |       | 7   |       | Ω     |
| Soft-start time                 | t <sub>SS_B2</sub>    | V <sub>OUT</sub> = 10 to 90%                                                 |       | 450 |       | μs    |
|                                 | t <sub>SS_B4</sub>    | V <sub>OUT</sub> = 10 to 90%                                                 |       | 450 |       | μs    |
| <b>10mA RTC LDO</b>             |                       |                                                                              |       |     |       |       |
| Default output voltage          | V <sub>RTC_LDO</sub>  | I <sub>OUT</sub> = 10mA, power-on state                                      | 1.164 | 1.2 | 1.236 | V     |
| Ground current                  | I <sub>Q_RTC</sub>    | No load                                                                      |       | 6.5 |       | μA    |
| Dropout voltage <sup>(8)</sup>  | V <sub>DROP1</sub>    | V <sub>OUT</sub> = 3V, I <sub>OUT</sub> = 10mA                               |       | 100 |       | mV    |
| Current limit                   | I <sub>LIM_RTC</sub>  | V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> drops 33%,<br>T <sub>J</sub> = 25°C | 25    | 55  | 85    | mA    |
| Soft-start slew rate            | t <sub>SS_RTC</sub>   | V <sub>OUT</sub> = 10% to 90%, C <sub>OUT</sub> = 1μF                        |       | 35  |       | mV/μs |



# ELECTRICAL CHARACTERISTICS (continued)

VIN1 = VIN2 = VIN3 = VIN4 = VIN5 = AVIN = 5V, T<sub>J</sub> = -40°C to +125°C <sup>(5)</sup>, unless otherwise noted.

| Parameter                                                     | Symbol                 | Condition                                               | Min   | Typ  | Max   | Units            |
|---------------------------------------------------------------|------------------------|---------------------------------------------------------|-------|------|-------|------------------|
| <b>Low-Dropout (LDO) Regulator: LDO2 to LDO5</b>              |                        |                                                         |       |      |       |                  |
| Output voltage                                                | V <sub>LDO2</sub>      |                                                         | 2.940 | 3.00 | 3.060 | V                |
|                                                               | V <sub>LDO3</sub>      |                                                         | 1.764 | 1.80 | 1.836 | V                |
|                                                               | V <sub>LDO4</sub>      |                                                         | 1.176 | 1.20 | 1.224 | V                |
|                                                               | V <sub>LDO5</sub>      |                                                         | 0.882 | 0.90 | 0.918 | V                |
| PSRR <sup>(8)</sup>                                           | PSRR <sub>1k</sub>     | f <sub>sw</sub> = 1kHz, 100mA, V <sub>OUT</sub> = 1.8V  |       | 47   |       | dB               |
|                                                               | PSRR <sub>10k</sub>    | f <sub>sw</sub> = 10kHz, 100mA, V <sub>OUT</sub> = 1.8V |       | 51   |       | dB               |
| Dropout voltage                                               | V <sub>DROP1</sub>     | V <sub>OUT</sub> = 3V, I <sub>OUT</sub> = 300mA         |       | 100  |       | mV               |
| Current limit                                                 | I <sub>LIMIT_LDO</sub> | VIN = 3.3V, V <sub>OUT</sub> drops 33%                  | 320   | 430  | 640   | mA               |
| Output discharge resistance                                   | R <sub>O_DIS2</sub>    |                                                         |       | 7    |       | Ω                |
| Soft-start time                                               | t <sub>SS_B2</sub>     | V <sub>OUT</sub> = 10% to 90%, C <sub>OUT</sub> = 2.2μF |       | 70   |       | μs               |
| Line regulation                                               |                        | VIN2 = VIN5 = 2.8V to 5.5V                              |       | 0.3  |       | %/V              |
| Load regulation                                               |                        | VIN2 = VIN5 = 3.3V, I <sub>OUT</sub> from 10mA to 100mA |       | 0.5  |       | %                |
| <b>Logic Pins</b>                                             |                        |                                                         |       |      |       |                  |
| nPBIN pull-up current                                         | I <sub>PBIN</sub>      | Internal pull-up to AVIN                                | 5     | 9    | 13    | μA               |
| Push-button detection threshold                               | V <sub>PB</sub>        |                                                         | 500   | 700  | 900   | mV               |
| Manual reset threshold                                        | V <sub>MS</sub>        | nPBIN pulls low, T <sub>J</sub> = 25°C                  |       |      | 50    | mV               |
| RSTO rising threshold                                         | V <sub>RSTO_R</sub>    | Monitor buck 4's output                                 |       | 90%  |       | V <sub>FB4</sub> |
| RSTO falling threshold                                        | V <sub>RSTO_F</sub>    |                                                         |       | 80%  |       | V <sub>FB4</sub> |
| RSTO rising delay                                             | t <sub>RSTO</sub>      | Adjustable through I <sup>2</sup> C/OTP                 | 70    | 100  | 130   | ms               |
| <b>I<sup>2</sup>C Interface Specifications <sup>(9)</sup></b> |                        |                                                         |       |      |       |                  |
| Input logic high                                              | V <sub>IH</sub>        |                                                         | 1.4   |      |       | V                |
| Input logic low                                               | V <sub>IL</sub>        |                                                         |       |      | 0.4   | V                |
| Output voltage logic low                                      | V <sub>OUT_L</sub>     | RSTO pin sink 4mA                                       |       |      | 0.4   | V                |
| SCL clock frequency                                           | f <sub>SCL</sub>       |                                                         |       |      | 3.4   | MHz              |
| SCL high time                                                 | t <sub>HIGH</sub>      |                                                         | 60    |      |       | ns               |
| SCL low time                                                  | t <sub>LOW</sub>       |                                                         | 160   |      |       | ns               |
| Data set-up time                                              | t <sub>SUDAT</sub>     |                                                         | 10    |      |       | ns               |
| Data hold time                                                | t <sub>HDDAT</sub>     |                                                         |       | 70   |       | ns               |
| Set-up time for repeated start condition                      | t <sub>SUSTA</sub>     |                                                         | 160   |      |       | ns               |
| Hold time for repeated start condition                        | t <sub>HDSTA</sub>     |                                                         | 160   |      |       | ns               |
| Bus free time between a start and stop condition              | t <sub>BUF</sub>       |                                                         | 160   |      |       | ns               |
| Set-up time for stop condition                                | t <sub>SUSTO</sub>     |                                                         | 160   |      |       | ns               |

## ELECTRICAL CHARACTERISTICS (continued)

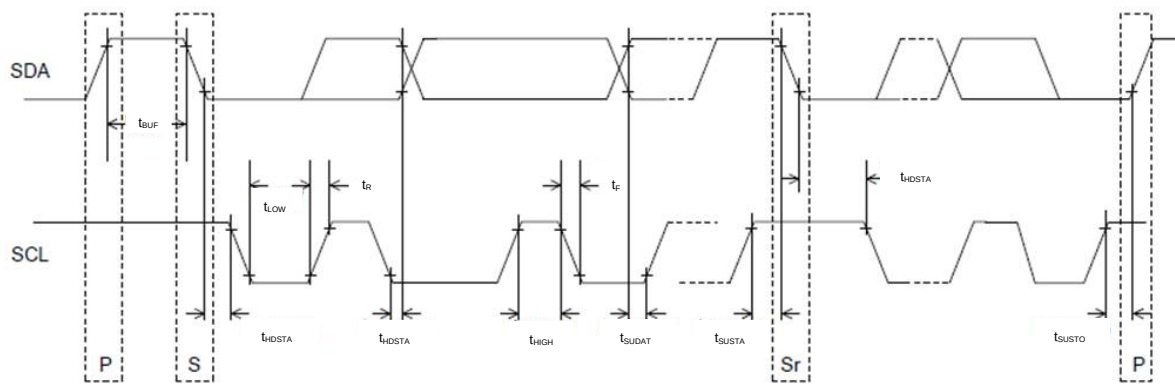
**VIN1 = VIN2 = VIN3 = VIN4 = VIN5 = AVIN = 5V, T<sub>J</sub> = -40°C to +125°C <sup>(5)</sup>, unless otherwise noted.**

| Parameter                         | Symbol    | Condition | Min | Typ | Max | Units |
|-----------------------------------|-----------|-----------|-----|-----|-----|-------|
| SCL and SDA rise time             | $t_R$     |           | 10  |     | 300 | ns    |
| SCL and SDA fall time             | $t_F$     |           | 10  |     | 300 | ns    |
| Pulse width of suppressed spike   | $t_{SP}$  |           | 0   |     | 50  | ns    |
| Capacitance bus for each bus line | $C_B$     |           |     |     | 400 | pF    |
| SCL low time                      | $t_{LOW}$ |           | 160 |     |     | ns    |

**Notes:**

- 5) Not tested in production. Guaranteed by over-temperature correlation.
- 6) Guaranteed by design.
- 7) VIN2 and VIN4 share the same UVLO threshold. It is recommended to connect VIN2 and VIN4 together in applications.
- 8) Guaranteed by engineering sample characterization.
- 9) See the I<sup>2</sup>C Timing Diagram below when reading the I<sup>2</sup>C interface specifications. It is recommended to begin operating the I<sup>2</sup>C after the power-on sequence is finished, or RSTO switches high.

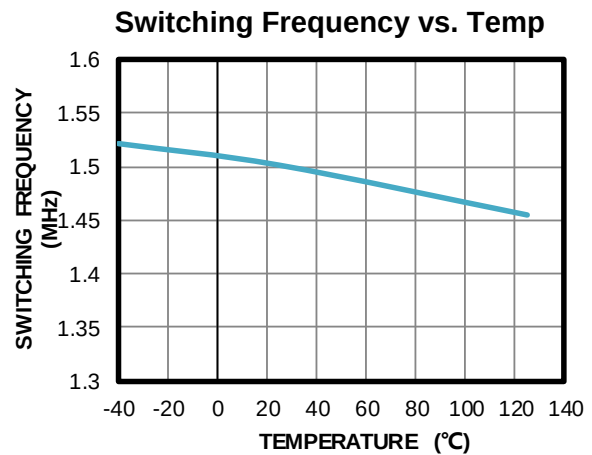
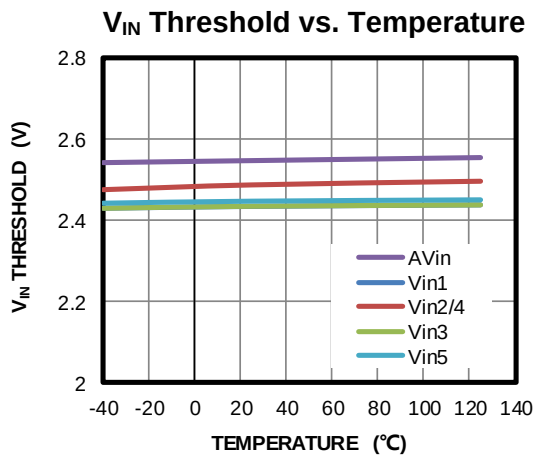
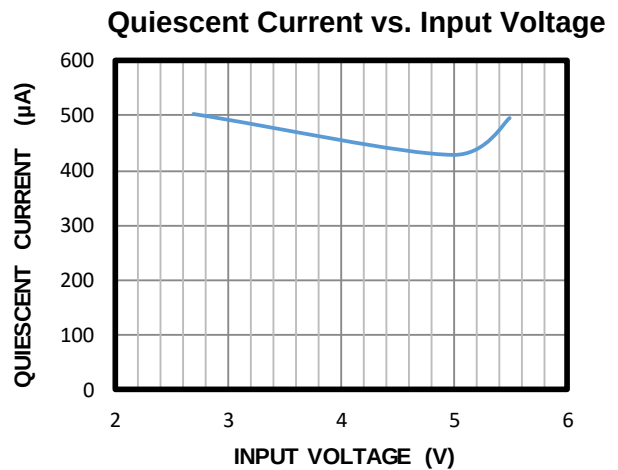
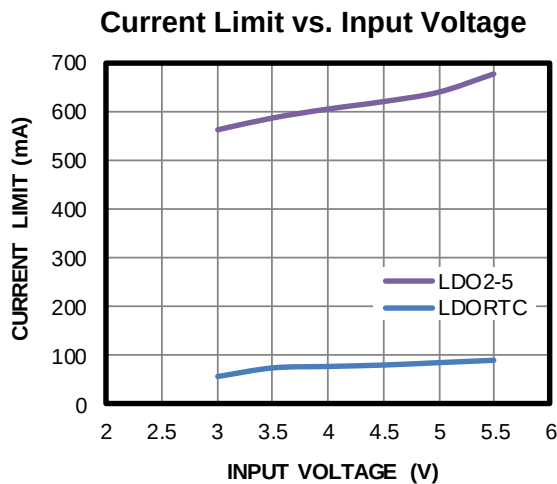
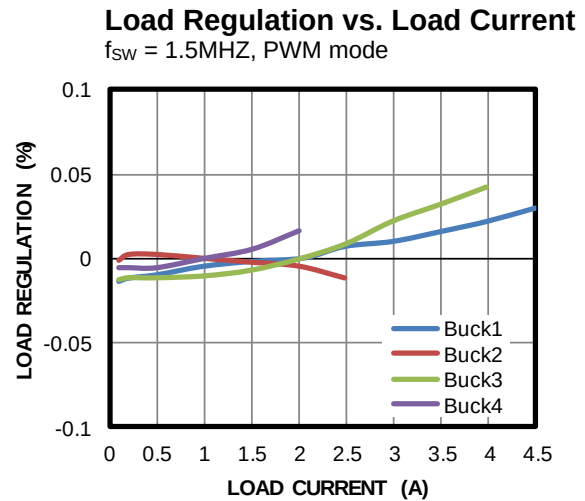
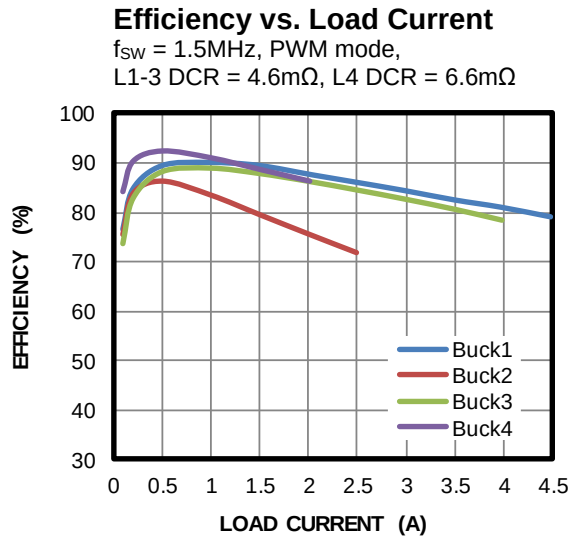
## I<sup>2</sup>C TIMING DIAGRAM



### Figure 2: I<sup>2</sup>C Timing Diagram

## TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board.  $V_{IN} = 3.3V$ ,  $T_A = 25^\circ C$ , tested using MP5496GR-0001 specified parts, unless otherwise noted.

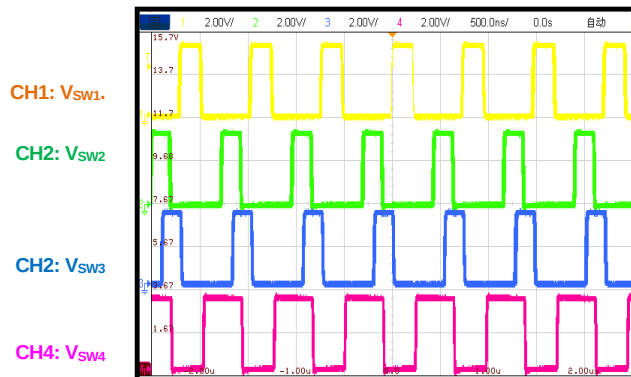


## TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.  $V_{IN} = 3.3V$ ,  $T_A = 25^\circ C$ , tested using MP5496GR-0001 specified parts, unless otherwise noted.

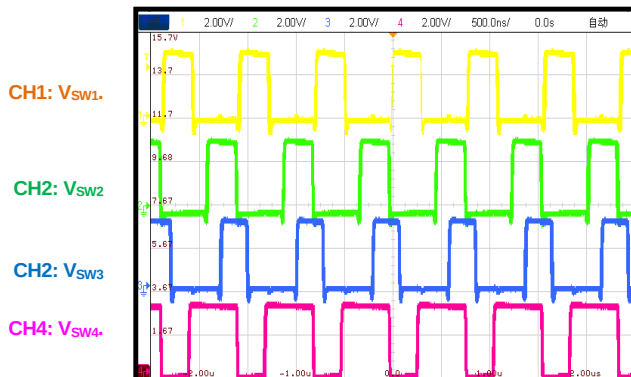
### Steady State

$V_{IN} = 3.3V$ , each channel buck with no load



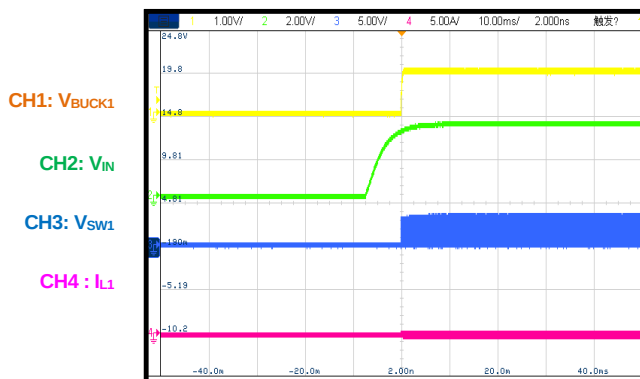
### Steady State

$V_{IN} = 3.3V$ , each channel buck with full load



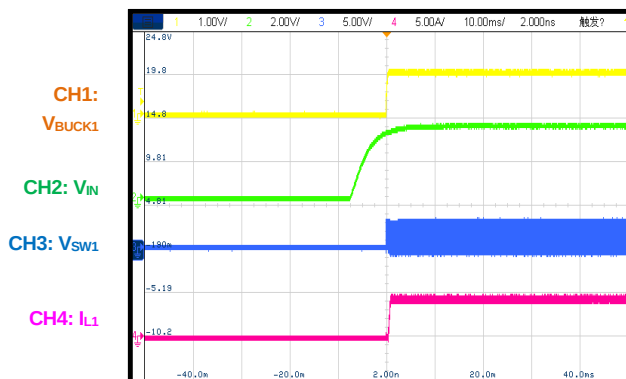
### Start-Up

$V_{IN} = 3.3V$ ,  $I_{BUCK1} = 0A$



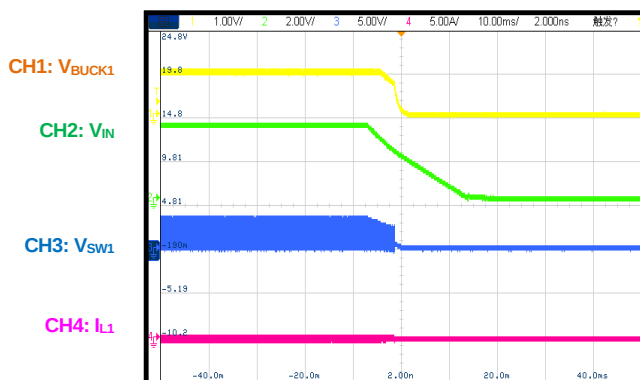
### Start-Up

$V_{IN} = 3.3V$ ,  $I_{BUCK1} = 4.5A$



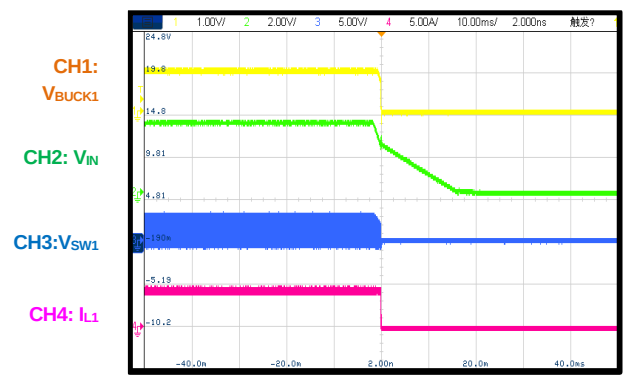
### Shutdown

$V_{IN} = 3.3V$ ,  $I_{BUCK1} = 0A$



### Shutdown

$V_{IN} = 3.3V$ ,  $I_{BUCK1} = 4.5A$

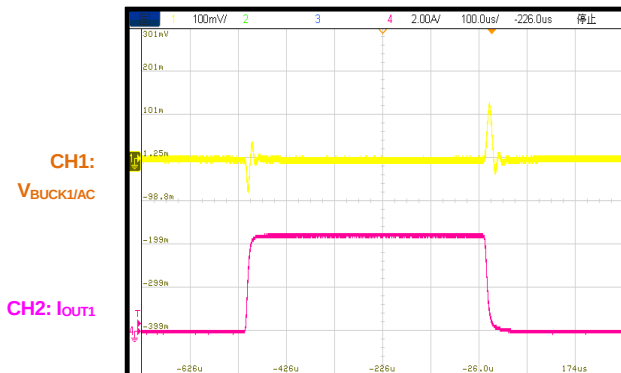


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 3.3V$ ,  $T_A = 25^\circ C$ , tested using MP5496GR-0001 specified parts, unless otherwise noted.

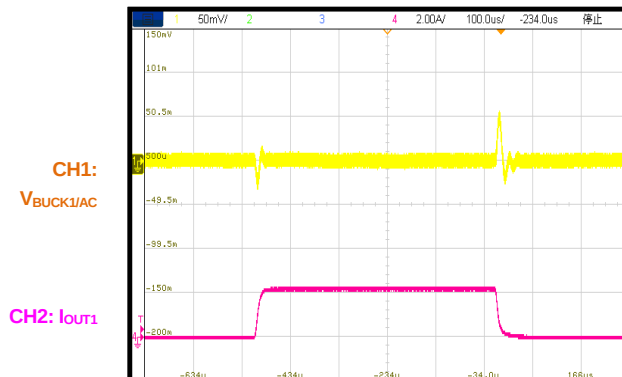
### Load Transient

$I_{OUT} = 0$  to 4.5A, 2.5A/ $\mu s$



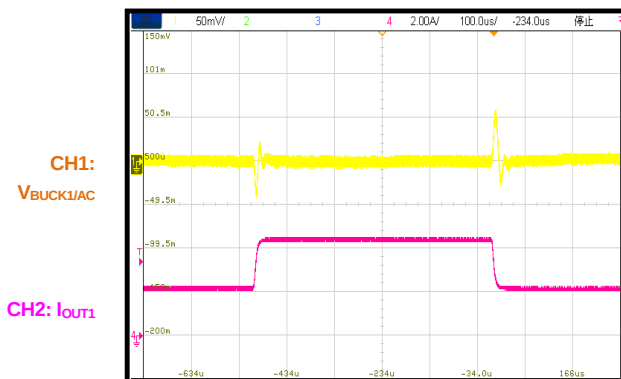
### Load Transient

$I_{OUT} = 0$  to 2A, 2.5A/ $\mu s$



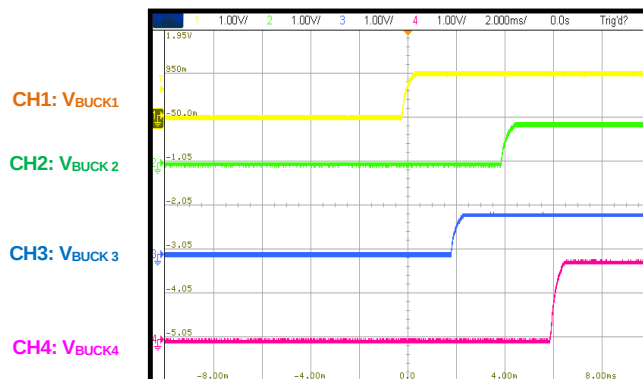
### Load Transient

$I_{OUT} = 2A$  to 4.5A, 2.5A/ $\mu s$



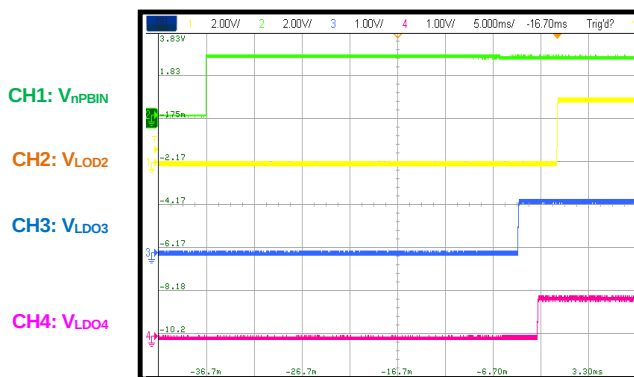
### nPBIN Start-Up

Each channel with no load



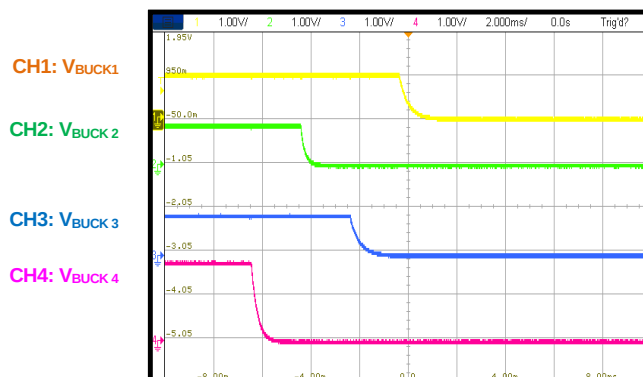
### nPBIN Start-Up

Each channel with no load



### nPBIN Shutdown

Each channel with no load

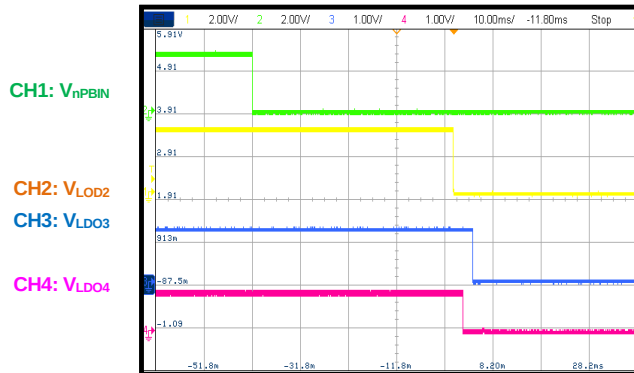


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Performance waveforms are tested on the evaluation board.  $V_{IN} = 3.3V$ ,  $T_A = 25^\circ C$ , tested using MP5496GR-0001 specified parts, unless otherwise noted.

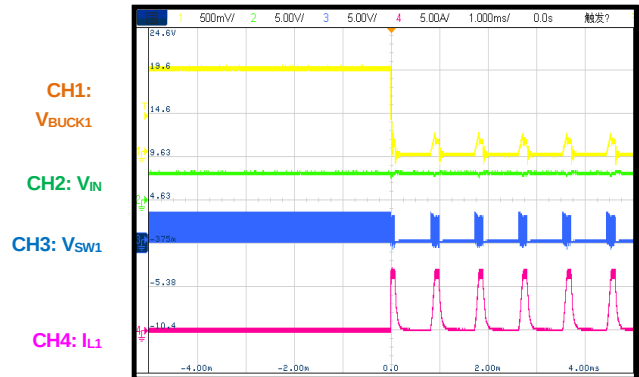
### nPBIN Shutdown

Each channel with no load



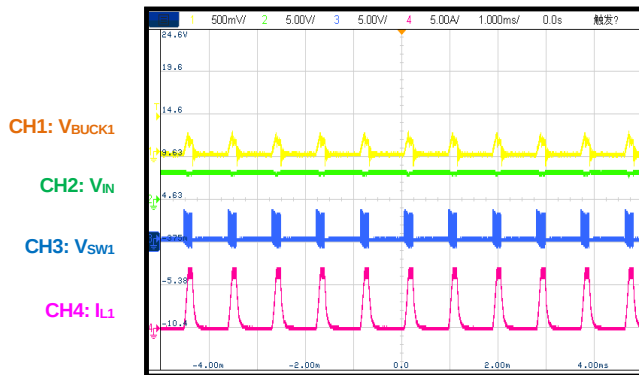
### SCP Entry

SCP entry, no load



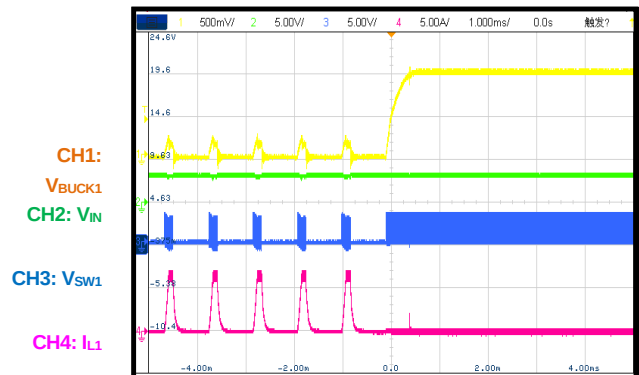
### SCP Steady State

SCP steady state, no load



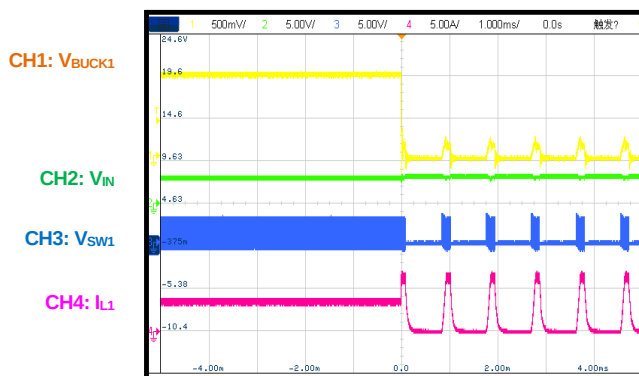
### SCP Recovery

SCP recovery, no load



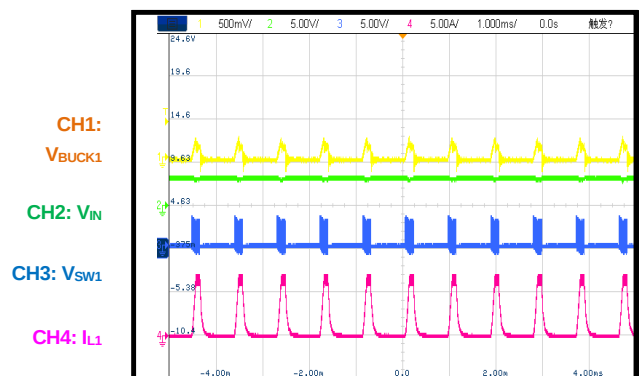
### SCP Entry

SCP entry, full load



### SCP Steady State

SCP steady state, full load

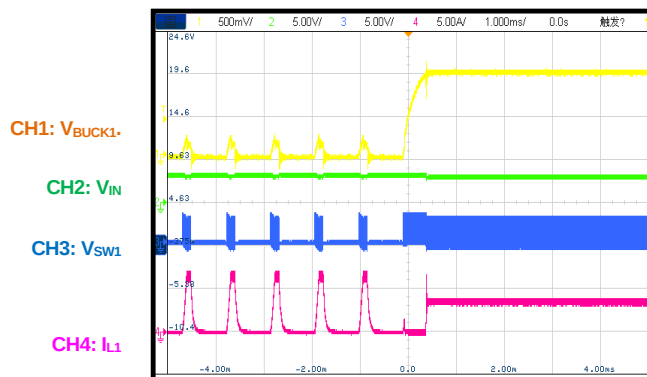


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 3.3V$ ,  $T_A = 25^{\circ}C$ , tested using MP5496GR-0001 specified parts, unless otherwise noted.

### SCP Recovery

SCP recovery, full load



## FUNCTIONAL BLOCK DIAGRAM

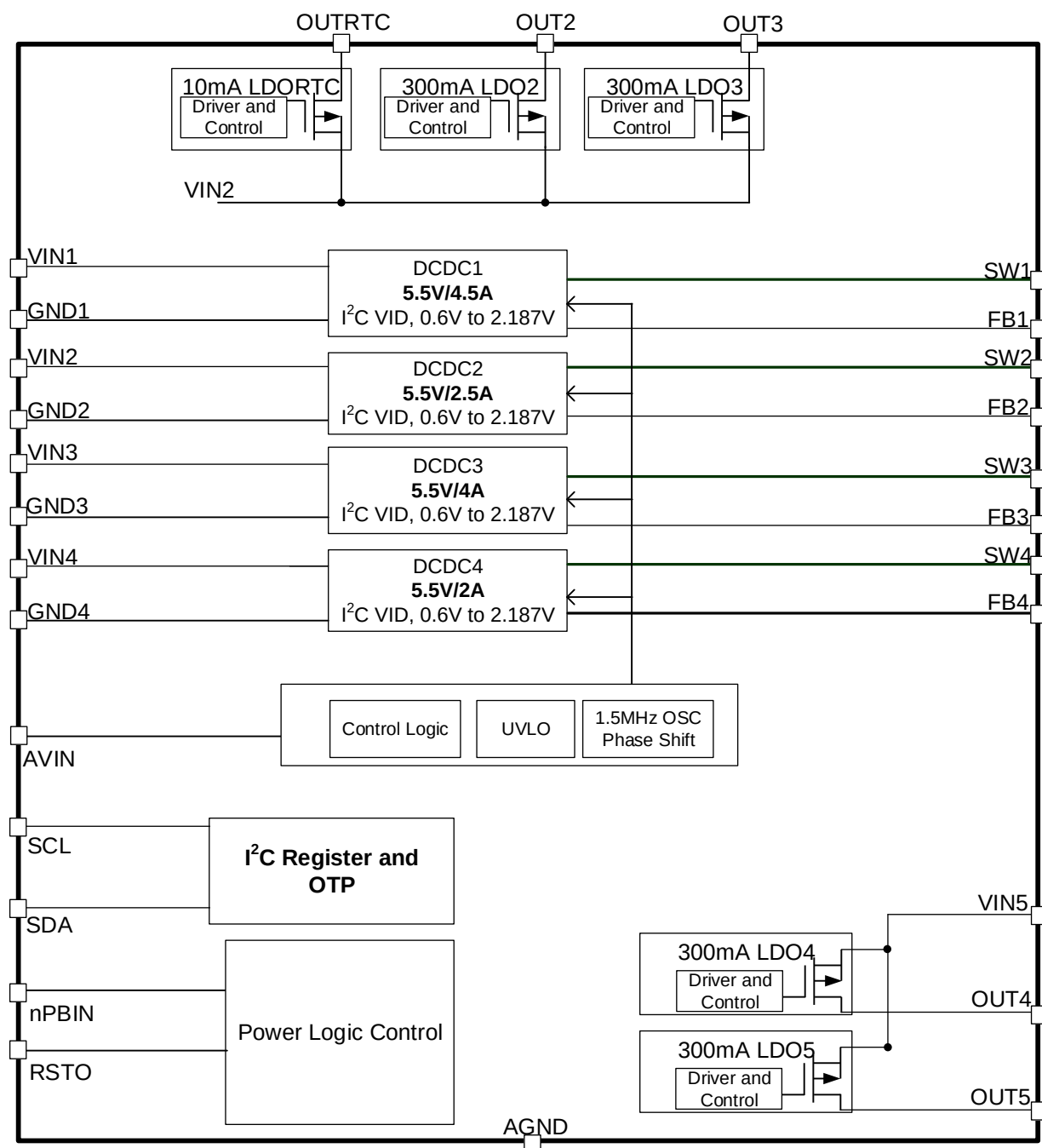


Figure 3: Functional Block Diagram



## OPERATION

The MP5496 provides a complete power management solution for many 5V systems, such as televisions, SSDs, and STBs. The MP5496 integrates four high-frequency, synchronous, rectified, step-down switch-mode converters and five low-dropout regulators. The MP5496 greatly reduces PCB space and the number of external components. The MP5496 can manage the power system for either a

single-cell Li-ion battery or a 5V regulated input voltage, allowing for greater flexibility of the system design.

The I<sup>2</sup>C interface and one-time programmable (OTP) memory interfaces provide an adjustable default output voltage and dynamic voltage scaling. The I<sup>2</sup>C also provides powerful logic functions. See the Register Map section starting on page 27 for more details.

## POWER CONTROL

### State Machine Diagram

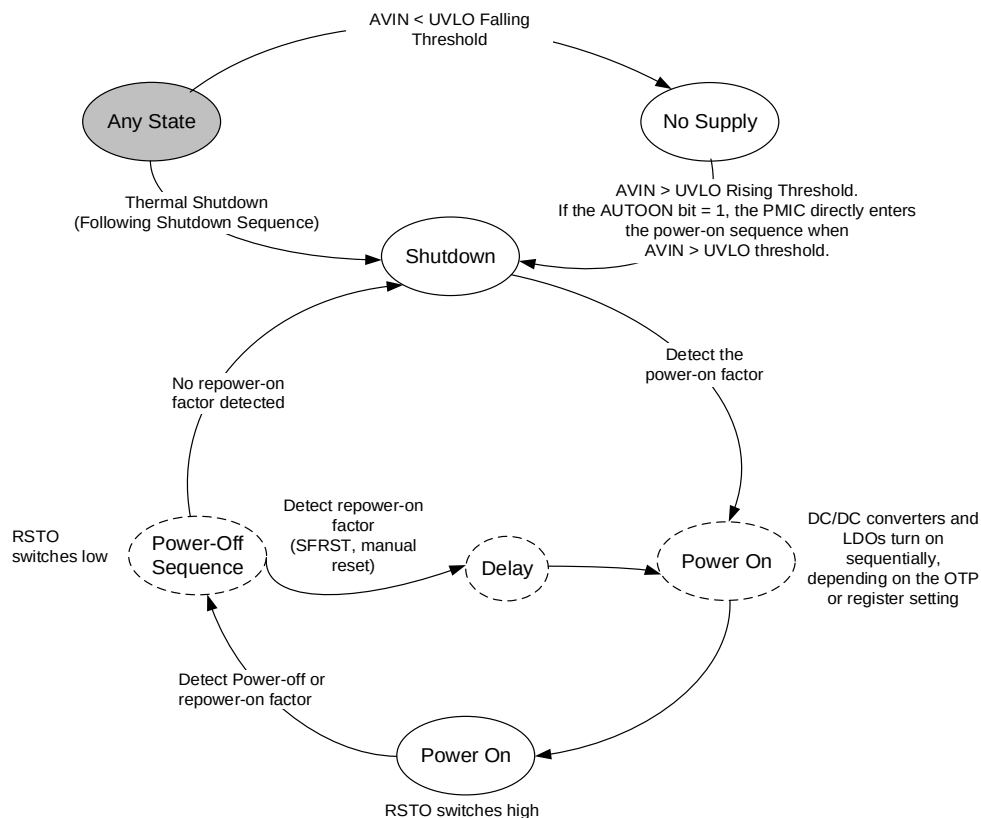


Figure 4: Power Control State Machine Diagram

### State Machine Description

Figure 4 shows the state machine, which has multiple features. These features are described below.

#### No Supply

The PMIC's input pin has an under-voltage lockout (UVLO) detection circuit. If the input voltage (AVIN) is below the UVLO rising threshold, the PMIC's functions are disabled.

#### Power Off

If AVIN exceeds its rising UVLO threshold and the AUTOON bit = 0, the PMIC first enters a power-off state. In this state, the PMIC always monitors the power-on factor. Once the power-on factor is detected, the device initiates the power-on sequence.

### Power-On Sequence

The DC/DC converters and LDO regulators turn on sequentially according to the preconfigured order via the OTP e-fuse.

### Power-On

The DC/DC converters and LDO regulators turn on. The RSTO output switches high. In this state, the PMIC always monitors the power-off or repower-on factors.

### Power-Off Sequence

The PMIC enters the power-off sequence if it detects the power-off or repower-on factors while in the power-on state. First RSTO switches low, and then the DC/DC converters and LDO regulators turn off sequentially in the reverse order of the power-on sequence. After the power-off sequence is completed, the repower-on condition (software control) is monitored. Then the PMIC enters the power-on sequence automatically after a delay timer.

### Shutdown Event

If the PMIC detects that the input voltage is below the UVLO falling threshold (the device enters a no supply state) or over-temperature protection is triggered (the device enters a power-off state), the PMIC switches to a no supply state or power-off state, regardless of the current state. <sup>(10)</sup>

#### Note:

10) If PMIC enters a power-off state due to over-temperature protection, LDORTC is off.

### Power-On Factors

The PMIC has three power-on factors, described below.

### SYSEN

SYSEN is one data bit in the I<sup>2</sup>C register. If the SYSEN bit is set to 1, the system changes from a power-off state and initiates the power-on sequence. Two methods can set SYSEN from 0 to 1. The first method is by setting the AUTOON bit to 1 via the OTP. With this method, the system auto-loads the AUTOON bit into SYSEN when the input voltage exceeds the UVLO threshold. The second method is by using the push button to initiate a power-on sequence.

### nPBIN On

nPBIN on includes two kinds of push-button events. If the nPBIN pin is pulled to logic low (but is not pulled to ground) and asserts low for longer than 2 seconds, the PMIC treats this as a power-on factor. If nPBIN is pulled to ground (below the manual reset threshold) in the power-off state, and asserts for longer than the maximum 30ms debounce time, the PMIC also treats this as a power-on factor. The SYSEN bit is set high if any of the nPBIN-initiated power-on events described above are detected.

### Thermal Recovery

If the MP5496 is in a power-off state because the die temperature has exceeded the thermal protection threshold, the PMIC enters a power-on sequence once the die's temperature decreases.

### Power-On Sequence

There are eight slots for power-on sequence timing (see Figure 5). All the DC/DC converters and LDO regulators (except RTCLDO) can be configured to time slots 0 through 7 by the OTP e-fuse. The delay time between each time slot is related to the default switching frequency of the MP5496 (see Table 1).

**Table 1: Slot Time Interval vs. Default Switching Frequency**

| Default Switching Frequency | Time Delay between Each Slot |
|-----------------------------|------------------------------|
| 1.0MHz                      | 3ms                          |
| 1.5MHz                      | 2ms                          |
| 2.0MHz                      | 1.5ms                        |
| 2.5MHz                      | 1.2ms                        |

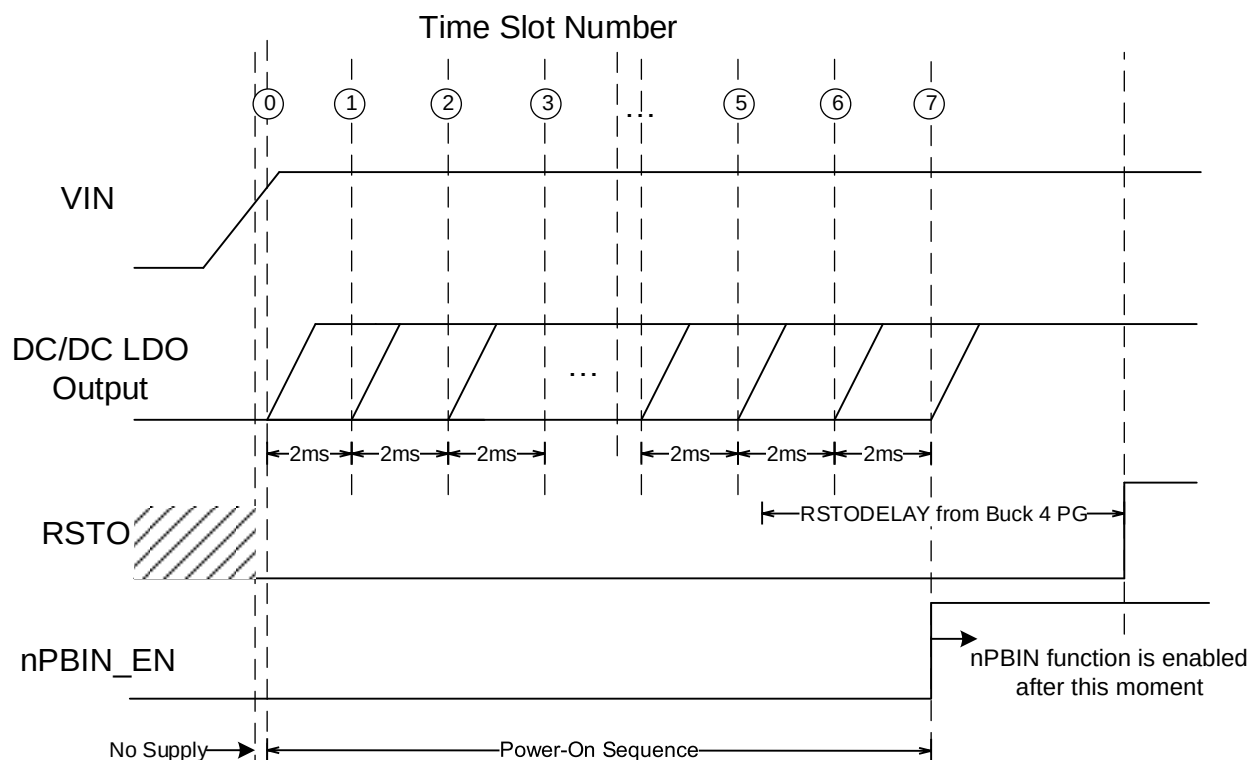


Figure 5: Power-On Sequence (AUTOON Bit is Set to 1)

### OUTRTC On

The OUTRTC LDO turns on if both VIN2 and AVIN exceed their respective UVLO rising thresholds, regardless of any other pin's status. OUTRTC turns off if either VIN2 or AVIN falls below its respective UVLO falling thresholds, or if thermal shutdown is triggered.

### Other Buck Regulators and LDOs On

The MP5496 provides a configurable power-on sequence. If the power-on sequence is fixed, the power-off sequence is reversed. See the OTP Register Description section on page 27 to determine which bits set the time slot number for each channel.

### Power-Off Factors

#### nPBIN Long Press

If nPBIN is pulled to logic low (but not pulled to ground) and asserts longer than 8 seconds, the PMIC enters the power-off sequence.

#### nPBIN Short Press

If nPBIN is pulled to GND (below the manual reset threshold) and lasts longer than the maximum 30ms debounce time, the PMIC enters the power-off sequence after an 8ms delay time (see Figure 8).

### SYSEN (Software-Initiated Shutdown)

The MP5496 supports a software-controlled shutdown through the I<sup>2</sup>C interface. SYSEN is one data bit in the I<sup>2</sup>C register. If the SYSEN bit is set to 0, the system enters a power-off sequence. To restart the PMIC, toggle the input power supply or use the nPBIN function (see the nPBIN Functions section on page 22 for more details).

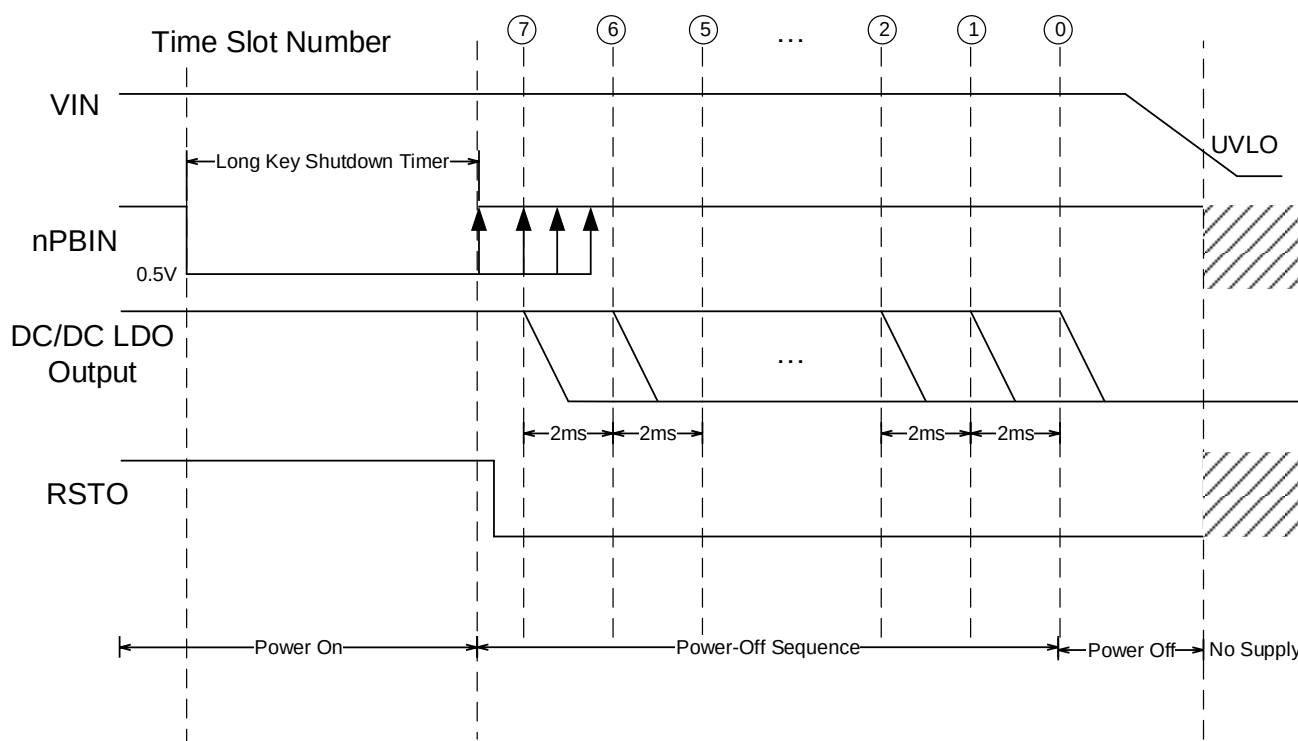


Figure 6: Power-Off Sequence via nPBIN Pin Press

### Power-Off Sequence

RSTO is pulled low before the DC/DC converter or LDO regulator turns off (see Figure 6). The DC/DC converter and LDO regulator power-off sequence is in the reverse order of the power-on sequence.

### Repower-On Factors

#### Manual Reset

To manually reset the device, pull the nPBIN pin to ground (below the manual reset threshold) for longer than the maximum 30ms debounce time. It is released after a set time (see Figure 8).

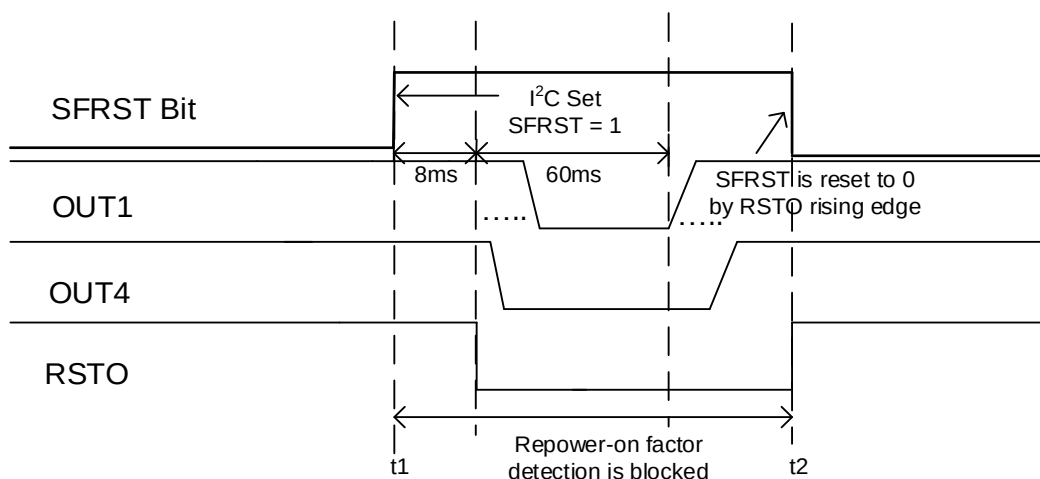
#### SFRST

Software reset. If the SFRST bit is set to 1 through the I<sup>2</sup>C interface, the system detects this as a repower-on factor.

### Repower-On Sequence (Software-Initiated Power Cycle)

The MP5496 supports a software-controlled power reset through the I<sup>2</sup>C interface or a manual reset push button.

When using the software-controlled method, the SFRST bit is set high. The MP5496 waits for 8ms and powers off the system, then powers on all of the power rails after a 60ms delay. The SFRST bit is automatically reset to 0 by the RSTO rising edge. After the SFRST bit is reset to 0, the software can control power cycle again. Repower-on factor detection is blocked during the repower-on period (t<sub>1</sub> to t<sub>2</sub>) (see Figure 7).

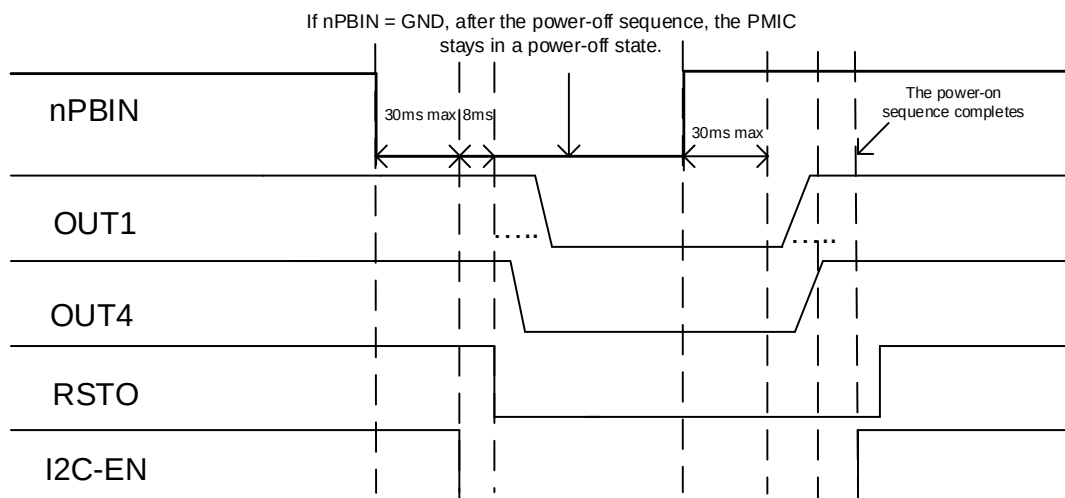


**Figure 7: Repower-On Sequence (Software Control)**

If the PMIC is working in a power-on state when using the manual reset control method, and the manual reset button is pressed down, the PMIC enters a power-off sequence. It enters this sequence after a maximum 30ms debounce time and 8ms of delay, then remains in the power-off state until the manual reset button is released. After a 30ms debounce time, the PMIC enters the power-on sequence again, and the manual reset function is also completed (see Figure 8).

### Shutdown Sequence

If the input voltage drops below the UVLO falling threshold, or the IC experiences an over-temperature condition, the PMIC immediately enters the shutdown sequence. All DC/DC converters and LDO regulators turn off at the same time (see Figure 9).



**Figure 8: Repower-On Sequence (Manual Reset Control)**

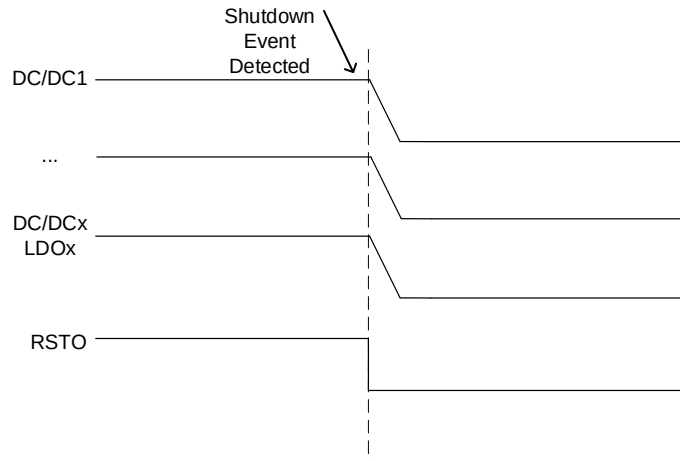


Figure 9: Shutdown Sequence

### HIGH-EFFICIENCY BUCK REGULATORS

Buck 1 to buck 4 are synchronous, step-down DC/DC converters with built-in under-voltage lockout (UVLO), soft start, compensation, and hiccup current limit protection. Fixed-frequency constant-on-time (COT) control provides fast transient response. The switching clock is phase-shifted from buck 1 to buck 4 during continuous conduction mode (CCM). Buck 2 and buck 4 support 100% duty cycle mode.

### Power Supply and Under-Voltage Lockout (UVLO)

VIN1 is the power supply for buck 1. VIN2 is the power supply for buck 2, LDORTC, LDO2, and LDO3. VIN3 is the power supply for buck 3. VIN4 is the supply for buck 4. VIN5 is the power supply for LDO4 and LDO5. AVIN is the power input for the biased internal logic blocks.

VIN1, VIN3, VIN5, and AVIN have their own under-voltage lockout (UVLO) thresholds with a proper hysteresis. VIN2 and VIN4 share the same UVLO threshold. If AVIN ramps up and exceeds the UVLO rising threshold, the nPBIN logic is enabled and ready to accept start-up and shutdown commands. LDORTC is active once VIN2 exceeds the rising threshold. Before the power key turns on, the input shutdown current is typically 15μA.

### Internal Soft Start (SS)

Soft start (SS) is implemented to prevent the PMIC output voltage from overshooting during start-up. When the PMIC starts up, the internal circuitry of each power rail generates a soft-start voltage that ramps up from 0V. The soft-start

period lasts until the voltage on the soft-start capacitor exceeds the reference voltage. At this point, the reference voltage takes over. For the four buck outputs, their soft-start times are fixed internally at 450μs. For the LDO2-5 outputs, their soft-start times are fixed internally at 70μs. For LDORTC, the soft-start slew rate is always 35mV/μs.

### Output Discharge

To discharge the energy of the output capacitor during a power-off sequence, there is an active discharge path from the DC/DC converters' and LDO regulators' output to ground. The discharge path turns on when the corresponding channel is disabled. The typical discharge resistance is 7Ω. The discharge function can be enabled or disabled through the I<sup>2</sup>C interface.

### SYSTEM CONTROL SIGNALS

#### nPBIN Functions

nPBIN is a multi-function pin that supports push-button detection and manual reset functions. There is an internal pull-up current to pull up nPBIN's voltage to AVIN. The MP5496 distinguishes between the push-button and manual reset functions by the different pull-low resistances. Connect nPBIN to ground for a manual reset function. Connect nPBIN to ground through a 34kΩ resistor to generate a push-button signal (see Figure 10).

A push-button event and manual reset event can both generate an interrupt signal, and set the corresponding interrupt bit high. See the Status 2 register on page 34 for details.

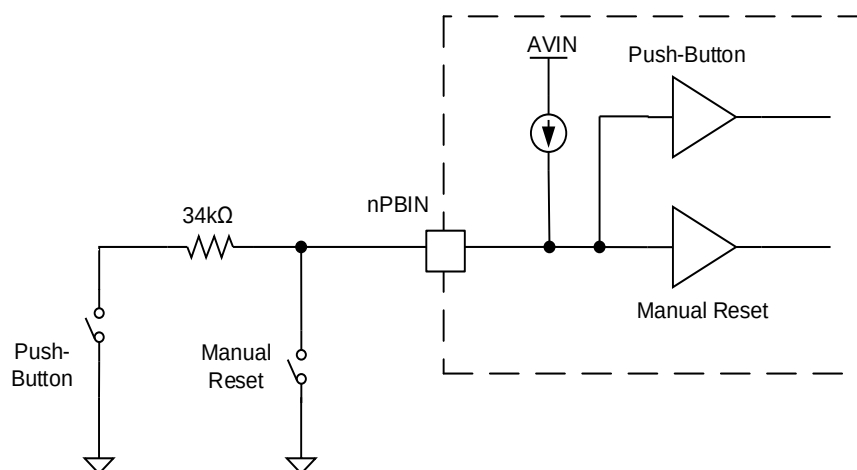


Figure 10: nPBIN Functional Block Diagram

### Push-Button Control

**Long Press 1/Start-Up:** If AVIN exceeds the UVLO threshold and the push button asserts low for longer than 2 seconds when the PMIC is in the power-off state, the power-on sequence

begins. The power-on sequence must be completed before the backside CPU can take over control. The power-on sequence must be complete when the RSTO signal switches high (see Figure 11).

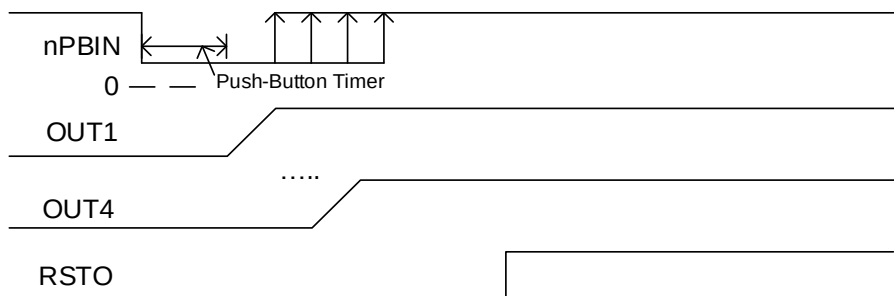


Figure 11: nPBIN Push-Button Long Press 1 (Start-Up)

**Long Press 2/Shutdown:** If the push button asserts low for more than 8 seconds during the power-on state, the power-off sequence begins. The MP5496 turns off all regulators and LDOs (excluding OUTRTC).

The power-off sequence turns off all components in the reverse order of start-up. If nPBIN is pulled low through a 34kΩ resistor at all times, the MP5496 remains in the power-off state (see Figure 12).

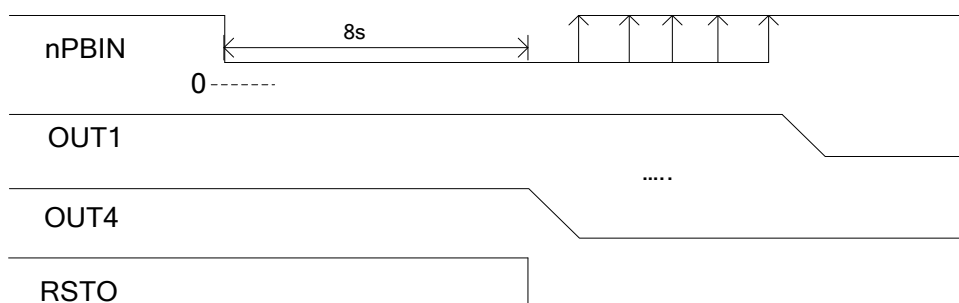


Figure 12: nPBIN Push Button Long Press 2 (Shutdown)



## Manual Reset Control

**Short Press and Release/Manual Reset:** If the PMIC is in a power-off state, a short press on nPBIN pulls the nPBIN voltage below the manual reset threshold with a maximum 30ms debounce

time, and then the PMIC begins the power-on sequence. When the PMIC is powered on, a short press drops the nPBIN voltage below the manual reset threshold with a maximum 30ms debounce time, and triggers the manual reset function (see Figure 13).

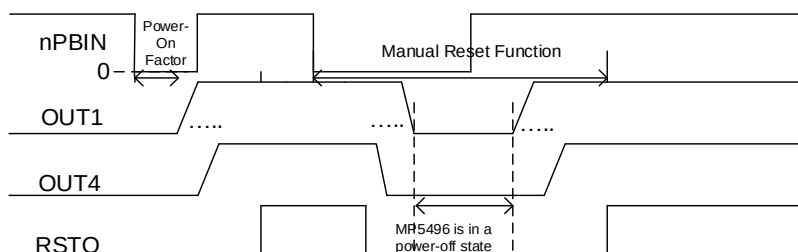


Figure 13: nPBIN Push Button Short Press to Ground

If the manual reset function is triggered, the PMIC turns off and remains off until the manual reset button is released. The PMIC enters the power-on state again after a maximum 30ms debounce time.

## Automatic Turn-On

If the AUTOON bit in the OTP configuration table is set high, the system changes the default value of SYSEN to 1. The PMIC enters the power-on sequence automatically once the input voltage (AVIN) exceeds its under-voltage lockout (UVLO) threshold. The system can start up automatically without the push button being pressed. After start-up, the push button can still support the manual power-on and power-off control. SYSEN can be read or written by the I<sup>2</sup>C.

## RSTO (Reset Output)

When buck 4's output voltage is ready ( $V_{FB}$  exceeds 90% of  $V_{REF}$ ), RSTO outputs high to enable the processor after an RSTO delay time. RSTO is an open-drain structure with an external pull-up resistor. RSTO is pulled low when buck

4's output is below 80% of the nominal value, or when the system detects a power-off factor, shutdown factor, or repower-on factor.

## Thermal Warning and Shutdown

Thermal warning and shutdown prevent the part from operating at exceedingly high temperatures. If the silicon die temperature exceeds 120°C, the MP5496 sets the OTWARNING bit to 1.

If the die temperature exceeds 153°C, the MP5496 sets the OTEMP bit to 1. Meanwhile, the system enters the shutdown sequence. When the temperature recovers to 130°C, the regulator enters the power-on sequence again.

## I<sup>2</sup>C Timing Graph

The I<sup>2</sup>C interface of the PMIC is powered by an internal, fixed, 2V power supply. When VIN exceeds its UVLO threshold during VIN start-up, this 2V power supply is ready after a 0.5ms delay. After another 5ms of delay time, the I<sup>2</sup>C is available (see Figure 14).

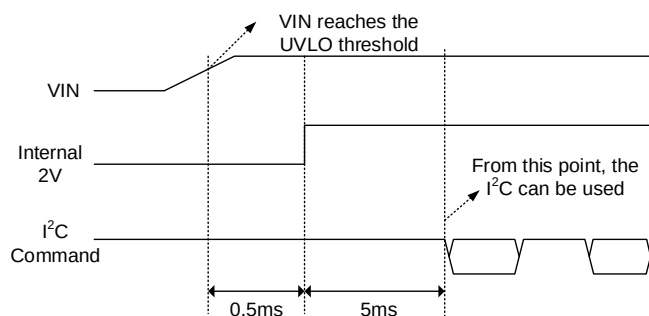


Figure 14: I<sup>2</sup>C Timing Graph



## I<sup>2</sup>C INTERFACE

### I<sup>2</sup>C Serial Interface Description

The I<sup>2</sup>C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. A master device connected to the line generates the SCL signal and device address, and arranges the communication sequence.

The MP5496 interface is an I<sup>2</sup>C slave that supports both fast mode (400kHz) and high-speed mode (3.4MHz). The I<sup>2</sup>C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I<sup>2</sup>C interface instantaneously. When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 or 1 to indicate a write or read operation, respectively.

### Start and Stop Conditions

Start (S) and stop (P) conditions are signaled by the master device, which signifies the beginning and end of the I<sup>2</sup>C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 15).

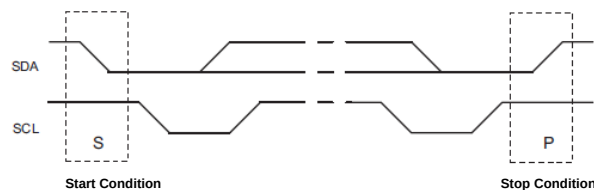


Figure 15: Start and Stop Conditions

The master generates the SCL clocks, then transmits the device address and the read/write direction bit (R/W) on the SDA line.

### Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

### I<sup>2</sup>C Update Sequence

The MP5496 requires a start condition, valid I<sup>2</sup>C address, register address byte, and a data byte for a single data update. The MP5496 acknowledges each byte that has been received by pulling the SDA line low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the MP5496. The MP5496 performs an update on the falling edge of the LSB byte. Figure 16, Figure 17, and Figure 18 show examples of I<sup>2</sup>C write and read sequences.

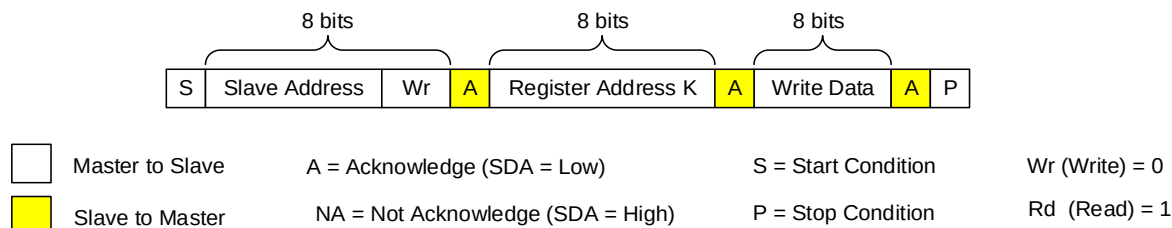


Figure 16: I<sup>2</sup>C Write Example (Write Single Register)

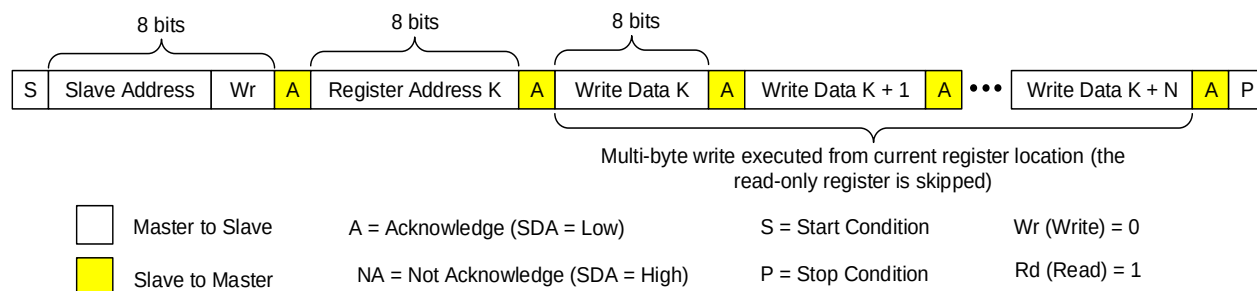
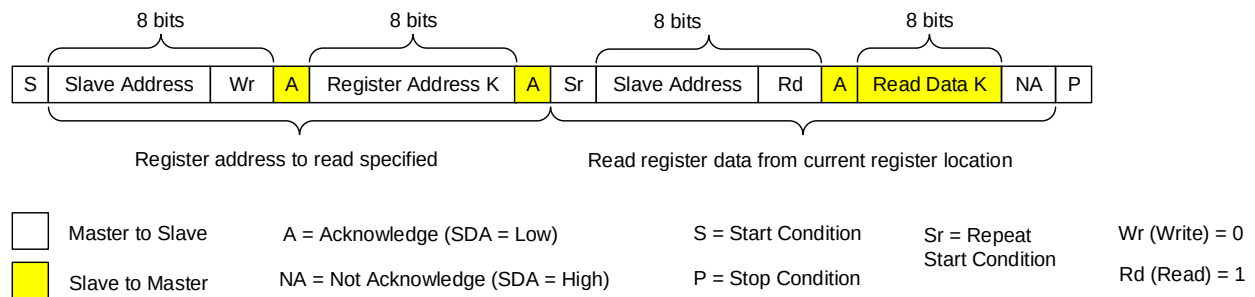


Figure 17: I<sup>2</sup>C Write Example (Write Multi-Register)



**Figure 18: I<sup>2</sup>C Read Example (Read Single Register)**

## OTP REGISTER DESCRIPTION

**OTP E-Fuse Configuration Table**

| #  | NAME  | D7        | D6                                                   | D5              | D4              | D3  | D2                                        | D1                 | D0 |
|----|-------|-----------|------------------------------------------------------|-----------------|-----------------|-----|-------------------------------------------|--------------------|----|
| 00 | CTL1  | AUTOON    | FREQUENCY                                            |                 | PUSHBUTTONTIMER |     |                                           | RSTODELAY          |    |
| 01 | CTL2  | ILIMBUCK1 |                                                      | ILIMBUCK3       |                 | N/A | PWRONDELAYBUCK1                           |                    |    |
| 02 | CTL3  | MODEBUCK1 | N/A                                                  | PWRONDELAYBUCK2 |                 |     | PWRONDELAYBUCK3                           |                    |    |
| 03 | CTL4  | MODEBUCK2 | N/A                                                  | PWRONDELAYBUCK4 |                 |     | PWRONDELAYLDO2                            |                    |    |
| 04 | CTL5  | MODEBUCK3 | N/A                                                  | PWRONDELAYLDO3  |                 |     | PWRONDELAYLDO4                            |                    |    |
| 05 | CTL6  | MODEBUCK4 | N/A                                                  | PWRONDELAYLDO5  |                 |     | N/A                                       |                    |    |
| 06 | VSET1 | ENBUCK1   | Buck 1 V <sub>OUT</sub> Set: 0.6V to 2.1V/100mV step |                 |                 |     | I <sup>2</sup> C SLAVE ADDRESS A3, A2, A1 |                    |    |
| 07 | VSET2 | ENBUCK2   | Buck 2 V <sub>OUT</sub> Set: 0.6V to 2.1/50mV step   |                 |                 |     |                                           | N/A                |    |
| 08 | VSET3 | ENBUCK3   | Buck 3 V <sub>OUT</sub> Set: 0.6V to 2.1V/100mV step |                 |                 |     | N/A                                       |                    |    |
| 09 | VSET4 | ENBUCK4   | Buck 4 V <sub>OUT</sub> Set: 0.6V to 2.1V/50mV step  |                 |                 |     |                                           | N/A                |    |
| 10 | VSET5 | RESERVED  | LDORTC V <sub>OUT</sub> Set: 0.8V to 3.9V/100mV step |                 |                 |     |                                           | N/A                |    |
| 11 | VSET6 | ENLDO2    | LDO2 V <sub>OUT</sub> Set: 0.8V to 3.9V/100mV step   |                 |                 |     |                                           | N/A                |    |
| 12 | VSET7 | ENLDO3    | LDO3 V <sub>OUT</sub> Set: 0.8V to 3.9V/100mV step   |                 |                 |     |                                           | N/A                |    |
| 13 | VSET8 | ENLDO4    | LDO4 V <sub>OUT</sub> Set: 0.8V to 3.9V/100mV step   |                 |                 |     |                                           | OTP version D1, D0 |    |
| 14 | VSET9 | ENLDO5    | LDO5 V <sub>OUT</sub> Set: 0.8V to 3.9V/100mV step   |                 |                 |     |                                           | OTP version D3, D2 |    |

**OTP E-Fuse Selected Table by Default (MP5496GR-0001)**

| OTP Items                      | Buck 1    | Buck 2 | Buck 3 | Buck 4 | LDORTC    | LDO2   | LDO3 | LDO4  | LDO5   |
|--------------------------------|-----------|--------|--------|--------|-----------|--------|------|-------|--------|
| Output voltage                 | 1.0V      | 0.9V   | 0.9V   | 1.8V   | 1.2V      | 3V     | 1.8V | 1.2V  | 0.9V   |
| Initial on/off                 | On        | On     | On     | On     | On        | On     | Off  | On    | On     |
| Mode                           | FPWM      | FPWM   | FPWM   | FPWM   | N/A       |        |      |       |        |
| Power-on delay/time slot #     | 0ms/0     | 4ms/2  | 2ms/1  | 6ms/3  | Always on | 12ms/6 | N/A  | 8ms/4 | 10ms/5 |
| Automatic turn-on              | Yes       |        |        |        |           |        |      |       |        |
| Switching frequency            | 1.5MHz    |        |        |        |           |        |      |       |        |
| Push-button timer              | 2 seconds |        |        |        |           |        |      |       |        |
| RSTO delay                     | 100ms     |        |        |        |           |        |      |       |        |
| Buck 1 peak current limit      | 6.8A      |        |        |        |           |        |      |       |        |
| Buck 3 peak current limit      | 5.6A      |        |        |        |           |        |      |       |        |
| I <sup>2</sup> C slave address | 0x69      |        |        |        |           |        |      |       |        |
| OTP version                    | 0004      |        |        |        |           |        |      |       |        |

**Other Parameter Information for the MP5496GR-0001**

|                       | Buck 1 | Buck 2 | Buck 3 | Buck 4 | LDORTC | LDO2 | LDO3 | LDO4 | LDO5 |
|-----------------------|--------|--------|--------|--------|--------|------|------|------|------|
| Minimum input voltage | 3V     |        |        |        |        |      |      |      |      |
| Typical input voltage | 3.3V   |        |        |        |        |      |      |      |      |
| Maximum input voltage | 3.6V   |        |        |        |        |      |      |      |      |

## OTP REGISTERS

| Bits   | Name                                                                                                                                                                                                                         | Default                  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                          |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|------------------------|--------------------------|------------------------|--------------------------|-----|-------|-------|--------|------|-----|-------|-------|-------|------|-----|-------|------|--------|------|-----|------|------|-------|------|-----|-------|------|--------|------|-----|------|----|-------|------|-----|-------|------|--------|------|-----|----|----|----|------|
| D[7]   | AUTOON                                                                                                                                                                                                                       | 1                        | System automatic turn-on bit. If AUTOON is set high, the system enters the power-on sequence when AVIN exceeds the UVLO rising threshold. Then the push button (nPBIN) does not have to be pressed. The AUTOON bit information is loaded into the SYSEN register after AVIN reaches the UVLO rising threshold.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                          |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| D[6:5] | FREQUENCY                                                                                                                                                                                                                    | 01                       | Switching frequency selection bit.<br>00: f <sub>sw</sub> = 1MHz<br>01: f <sub>sw</sub> = 1.5MHz<br>10: f <sub>sw</sub> = 2MHz<br>11: f <sub>sw</sub> = 2.5MHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                          |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| D[4:2] | PUSHBUTTON<br>TIMER                                                                                                                                                                                                          | 011                      | <div>This bit sets the push-button long press 1 power-on deglitch timer.</div> <table><tr><th></th><th>f<sub>sw</sub> = 1MHz</th><th>f<sub>sw</sub> = 1.5MHz</th><th>f<sub>sw</sub> = 2MHz</th><th>f<sub>sw</sub> = 2.5MHz</th></tr><tr><td>000</td><td>0.75s</td><td>0.5s</td><td>0.375s</td><td>0.3s</td></tr><tr><td>001</td><td>1.5s</td><td>1s</td><td>0.75s</td><td>0.6s</td></tr><tr><td>010</td><td>2.25s</td><td>1.5s</td><td>1.225s</td><td>0.9s</td></tr><tr><td>011</td><td>3s</td><td>2s</td><td>1.5s</td><td>1.2s</td></tr><tr><td>100</td><td>3.75s</td><td>2.5s</td><td>1.875s</td><td>1.5s</td></tr><tr><td>101</td><td>4.5s</td><td>3s</td><td>2.25s</td><td>1.8s</td></tr><tr><td>110</td><td>5.25s</td><td>3.5s</td><td>2.625s</td><td>2.1s</td></tr><tr><td>111</td><td>6s</td><td>4s</td><td>3s</td><td>2.4s</td></tr></table> <div>There is no corresponding data in the I<sup>2</sup>C register table for these 3 bits.</div> |                          | f <sub>sw</sub> = 1MHz | f <sub>sw</sub> = 1.5MHz | f <sub>sw</sub> = 2MHz | f <sub>sw</sub> = 2.5MHz | 000 | 0.75s | 0.5s  | 0.375s | 0.3s | 001 | 1.5s  | 1s    | 0.75s | 0.6s | 010 | 2.25s | 1.5s | 1.225s | 0.9s | 011 | 3s   | 2s   | 1.5s  | 1.2s | 100 | 3.75s | 2.5s | 1.875s | 1.5s | 101 | 4.5s | 3s | 2.25s | 1.8s | 110 | 5.25s | 3.5s | 2.625s | 2.1s | 111 | 6s | 4s | 3s | 2.4s |
|        | f <sub>sw</sub> = 1MHz                                                                                                                                                                                                       | f <sub>sw</sub> = 1.5MHz | f <sub>sw</sub> = 2MHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | f <sub>sw</sub> = 2.5MHz |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 000    | 0.75s                                                                                                                                                                                                                        | 0.5s                     | 0.375s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0.3s                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 001    | 1.5s                                                                                                                                                                                                                         | 1s                       | 0.75s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0.6s                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 010    | 2.25s                                                                                                                                                                                                                        | 1.5s                     | 1.225s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0.9s                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 011    | 3s                                                                                                                                                                                                                           | 2s                       | 1.5s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 1.2s                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 100    | 3.75s                                                                                                                                                                                                                        | 2.5s                     | 1.875s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1.5s                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 101    | 4.5s                                                                                                                                                                                                                         | 3s                       | 2.25s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 1.8s                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 110    | 5.25s                                                                                                                                                                                                                        | 3.5s                     | 2.625s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 2.1s                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 111    | 6s                                                                                                                                                                                                                           | 4s                       | 3s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 2.4s                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| D[1:0] | RSTODELAY                                                                                                                                                                                                                    | 01                       | <div>This bit sets the reset output delay.</div> <table><tr><th></th><th>f<sub>sw</sub> = 1MHz</th><th>f<sub>sw</sub> = 1.5MHz</th><th>f<sub>sw</sub> = 2MHz</th><th>f<sub>sw</sub> = 2.5MHz</th></tr><tr><td>00</td><td>210ms</td><td>140ms</td><td>105ms</td><td>84ms</td></tr><tr><td>01</td><td>150ms</td><td>100ms</td><td>75ms</td><td>60ms</td></tr><tr><td>10</td><td>75ms</td><td>50ms</td><td>37.5ms</td><td>30ms</td></tr><tr><td>11</td><td>15ms</td><td>10ms</td><td>7.5ms</td><td>6ms</td></tr></table> <div>There is no corresponding data in the I<sup>2</sup>C register table for these 3 bits.</div>                                                                                                                                                                                                                                                                                                                                |                          | f <sub>sw</sub> = 1MHz | f <sub>sw</sub> = 1.5MHz | f <sub>sw</sub> = 2MHz | f <sub>sw</sub> = 2.5MHz | 00  | 210ms | 140ms | 105ms  | 84ms | 01  | 150ms | 100ms | 75ms  | 60ms | 10  | 75ms  | 50ms | 37.5ms | 30ms | 11  | 15ms | 10ms | 7.5ms | 6ms  |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
|        | f <sub>sw</sub> = 1MHz                                                                                                                                                                                                       | f <sub>sw</sub> = 1.5MHz | f <sub>sw</sub> = 2MHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | f <sub>sw</sub> = 2.5MHz |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 00     | 210ms                                                                                                                                                                                                                        | 140ms                    | 105ms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 84ms                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 01     | 150ms                                                                                                                                                                                                                        | 100ms                    | 75ms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 60ms                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 10     | 75ms                                                                                                                                                                                                                         | 50ms                     | 37.5ms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 30ms                     |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 11     | 15ms                                                                                                                                                                                                                         | 10ms                     | 7.5ms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 6ms                      |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |
| 3 bits | PWRONDELAY<br>BUCK1<br>PWRONDELAY<br>BUCK2<br>PWRONDELAY<br>BUCK3<br>PWRONDELAY<br>BUCK4<br>PWRONDELAY<br>LDO2<br>PWRONDELAY<br>LDO2<br>PWRONDELAY<br>LDO3<br>PWRONDELAY<br>LDO4<br>PWRONDELAY<br>LDO5<br>PWRONDELAY<br>LDO6 | N/A                      | <div>Delay time from when SYSEN goes high to when the bucks/LDOs begin to switch.</div> <div>000: 0ms (time slot 0)<br/>001: 2ms (time slot 1)<br/>010: 4ms (time slot 2)<br/>011: 6ms (time slot 3)<br/>100: 8ms (time slot 4)<br/>101: 10ms (time slot 5)<br/>110: 12ms (time slot 6)<br/>111: 14ms (time slot 7)</div> <div>The delay time between neighboring slots are related to the PMIC default switching frequency. See the operation section on page 18 for details. There is no corresponding data in the I<sup>2</sup>C register table for these 3 bits.</div>                                                                                                                                                                                                                                                                                                                                                                            |                          |                        |                          |                        |                          |     |       |       |        |      |     |       |       |       |      |     |       |      |        |      |     |      |      |       |      |     |       |      |        |      |     |      |    |       |      |     |       |      |        |      |     |    |    |    |      |

| Bits   | Name                                                             | Default                    | Description                                                                                                                                                                                                                                                                  |
|--------|------------------------------------------------------------------|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 bit  | MODE<br>BUCK1<br>MODE<br>BUCK2<br>MODE<br>BUCK3<br>MODE<br>BUCK4 | N/A                        | Selects the mode (auto-PFM/PWM mode or forced PWM mode).<br><br>0: Auto-PFM/PWM mode<br>1: Forced PWM mode (default for buck 1, buck 2, buck 3, and buck 4)<br><br>These bits are loaded into the I <sup>2</sup> C MODEBUCKx registers when VIN1 exceeds its UVLO threshold. |
| 2 bits | ILIMBUCK1<br>ILIMBUCK3                                           | 11 (Buck 1)<br>10 (Buck 3) | Programs the current limit threshold of the buck regulator:<br><br>00: 3.8A typical high-side peak current limit<br>01: 4.6A typical high-side peak current limit<br>10: 5.6A typical high-side peak current limit<br>11: 6.8A typical high-side peak current limit          |
| 3 bits | I2C SLAVE<br>ADDRESS<br>A3, A2, A1                               | 001                        | Sets the A1, A2, and A3 bits of the slave's I <sup>2</sup> C address. See the I <sup>2</sup> C Bus Slave Address section on page 30 for more details.                                                                                                                        |

## I<sup>2</sup>C REGISTER MAP

| Add (Hex) | Name     | R/W | D7            | D6                                                     | D5           | D4          | D3          | D2           | D1           | D0           |
|-----------|----------|-----|---------------|--------------------------------------------------------|--------------|-------------|-------------|--------------|--------------|--------------|
| 00        | CTL0     | R/W | SYSEN         | SFRST                                                  | RESERVED     |             |             |              | RESERVED     | RESERVED     |
| 01        | CTL1     | R/W | RESERVED      | MODE BUCK1                                             | MODE BUCK2   | MODE BUCK3  | MODE BUCK4  | DISCHG BUCK3 | DISCHG BUCK2 | DISCHG BUCK1 |
| 02        | CTL2     | R/W | DVS SLEW RATE |                                                        | DISCHG BUCK4 | DISCHG LDO2 | DISCHG LDO3 | DISCHG LDO4  | DISCHG LDO5  | RESERVED     |
| 03        | ILIMIT   | R/W | ILIMBUCK1     |                                                        | ILIMBUCK3    |             | ILIMBUCK2   |              | ILIMBUCK4    |              |
| 04        | VSET1    | R/W | ENBUCK1       | Buck 1 output voltage set: 0.6V to 2.1875V/12.5mV step |              |             |             |              |              |              |
| 05        | VSET2    | R/W | ENBUCK2       | Buck 2 output voltage set: 0.6V to 2.1875V/12.5mV step |              |             |             |              |              |              |
| 06        | VSET3    | R/W | ENBUCK3       | Buck 3 output voltage set: 0.6V to 2.1875V/12.5mV step |              |             |             |              |              |              |
| 07        | VSET4    | R/W | ENBUCK4       | Buck 4 output voltage set: 0.6V to 2.1875V/12.5mV step |              |             |             |              |              |              |
| 08        | VSET5    | R/W | ENLDO2        | LDO2 output voltage set: 0.8V to 3.975V/25mV step      |              |             |             |              |              |              |
| 09        | VSET6    | R/W | ENLDO3        | LDO3 output voltage set: 0.8V to 3.975V/25mV step      |              |             |             |              |              |              |
| 0A        | VSET7    | R/W | ENLDO4        | LDO4 output voltage set: 0.8V to 3.975V/25mV step      |              |             |             |              |              |              |
| 0B        | VSET8    | R/W | ENLDO5        | LDO5 output voltage set: 0.8V to 3.975V/25mV step      |              |             |             |              |              |              |
| 0C        | RESERVED |     |               |                                                        |              |             |             |              |              |              |
| 0D        | Status1  | R   | PGLDO4        | PGLDO3                                                 | PGLDO2       | PGRTC       | PG4         | PG3          | PG2          | PG1          |
| 0E        | Status2  | R   | KEYON         | KEYOFF                                                 | MREST        | SHORTKEY ON | SFRST_ON    | RESERVED     | RESERVED     | PGLDO5       |
| 0F        | Status3  | R   | OT WARNING    | OTEMPP                                                 | RESERVE D    | RESERVED    | RESERVED    | RESERVED     | RESERVED     | RESERVED     |
| 10        | RESERVED |     |               |                                                        |              |             |             |              |              |              |
| 11        | ID2      | R   | VENDOR ID     |                                                        |              |             | OTP VERSION |              |              |              |

## REGISTER DESCRIPTION

### I<sup>2</sup>C Bus Slave Address <sup>(11)</sup>

The slave address is 7 bits followed by an 8th data direction bit (read or write). The A3, A2, and A1 bits can be configured via the OTP e-fuse.

|               | A7 | A6 | A5 | A4 | A3                | A2                | A1                |
|---------------|----|----|----|----|-------------------|-------------------|-------------------|
| Setting Value | 1  | 1  | 0  | 1  | 0 <sup>(12)</sup> | 0 <sup>(12)</sup> | 1 <sup>(12)</sup> |

#### Notes:

11) By default, the slave address is 0x69, A[7:1] = 1101 001.

12) This bit is configurable via the OTP e-fuse.

## I<sup>2</sup>C REGISTERS

### Reg 00: CTL0

| Bits | Name  | Default              | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Reset Condition                                                                                 |
|------|-------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|
| D[7] | SYSEN | BY OTP<br>AUTO<br>ON | System enable on/off bit. If the MP5496 detects a power-on event, this bit is set to 1. Then the power-on sequence starts. The DC/DC converters and LDO regulators turn on sequentially according to their enable bits (e.g. ENBUCK1 = 1) and power-on delay (POWERONDELAYBUCK1) settings.<br><br>Set this bit from 1 to 0 to trigger a power-off sequence. Other I <sup>2</sup> C registers are not reset when the I <sup>2</sup> C sets SYSEN from 1 to 0. The MP5496 is enabled again until the push button is long-pressed or a manual reset is asserted for more than 30ms of the maximum debounce time. | AVIN < UVLO                                                                                     |
| D[6] | SFRST | 0                    | Software reset. Once the SFRST bit is set high, the MP5496 waits for 8ms, then restarts all of the power rails. When the RSTO signal switches from low to high, the MP5496 resets SFRST and sets it to 0.                                                                                                                                                                                                                                                                                                                                                                                                     | <ul style="list-style-type: none"> <li>AVIN &lt; UVLO</li> <li>RSTO from low to high</li> </ul> |

### Reg 01: CTL1

| Bits   | Name                                                             | Default | Description                                                                                         | Reset Condition                                                                                                             |
|--------|------------------------------------------------------------------|---------|-----------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| D[6:3] | MODE<br>BUCK1<br>MODE<br>BUCK2<br>MODE<br>BUCK3<br>MODE<br>BUCK4 | BY OTP  | PFM/PWM mode or forced PWM mode.<br><br>0: Auto-PFM/PWM<br>1: Forced PWM mode                       | <ul style="list-style-type: none"> <li>AVIN &lt; UVLO</li> <li>SFRST</li> <li>Manual reset</li> <li>Long press 2</li> </ul> |
| D[2:0] | Regulator<br>Discharge                                           | 1       | Output discharge enable bit. The output discharge function is active during the power-off sequence. |                                                                                                                             |

### Reg 02: CTL2

| Bits   | Name                   | Default | Description                                                                                                                           | Reset Condition                                                                                                             |
|--------|------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| D[7:6] | DVS SLEW<br>RATE       | 01      | Voltage scaling slew rate for the buck 1 to buck 4 converters.<br><br>00: 32mV/μs<br>01: 16mV/μs<br>10: 8mV/μs<br>11: 4mV/μs          | <ul style="list-style-type: none"> <li>AVIN &lt; UVLO</li> <li>SFRST</li> <li>Manual reset</li> <li>Long press 2</li> </ul> |
| D[5:0] | Regulator<br>Discharge | 1       | Output discharge enable bit. The output discharge function is active during the power-off sequence and remains active after shutdown. |                                                                                                                             |

### Reg 03: ILIMIT

| Bits             | Name                   | Default | Description                                                                                                                                                                                                                                                 | Reset Condition                                                                                                                     |
|------------------|------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| D[7:6]<br>D[5:4] | ILIMBUCK1<br>ILIMBUCK3 | BY OTP  | Sets the current-limit threshold of the buck regulator.<br>00: 3.8A typical high-side peak current limit<br>01: 4.6A typical high-side peak current limit<br>10: 5.6A typical high-side peak current limit<br>11: 6.8A typical high-side peak current limit | <ul style="list-style-type: none"> <li>• AVIN &lt; UVLO</li> <li>• SFRST</li> <li>• Manual reset</li> <li>• Long press 2</li> </ul> |
| D[3:2]<br>D[1:0] | ILIMBUCK2<br>ILIMBUCK4 | 10      | Sets the current-limit threshold of the buck regulator.<br>00: 2.2A typical high-side peak current limit<br>01: 3.2A typical high-side peak current limit<br>10: 4.2A typical high-side peak current limit<br>11: 5.2A typical high-side peak current limit |                                                                                                                                     |

### Reg 04 to Reg 0B: VOUTSET and EN

| Bits   | Name                                                                             | Default | Description                                                                                                                                                 | Reset Condition                                                                                                                     |
|--------|----------------------------------------------------------------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| D[7]   | ENBUCK1<br>ENBUCK2<br>ENBUCK3<br>ENBUCK4<br>ENLDO2<br>ENLDO3<br>ENLDO4<br>ENLDO5 | BY OTP  | Enable bit for buck regulators and LDOs. The default value is 1, but the default SYSEN is set to 0. Regulators are enabled when both ENx = 1 and SYSEN = 1. | <ul style="list-style-type: none"> <li>• AVIN &lt; UVLO</li> <li>• SFRST</li> <li>• Manual reset</li> <li>• Long press 2</li> </ul> |
| D[6:0] | BUCK1 VOUTSET<br>BUCK2 VOUTSET<br>BUCK3 VOUTSET<br>BUCK4 VOUTSET                 | BY OTP  | Sets the output voltage from 0.6V to 2.1875V with 12.5mV steps (see Table 2).                                                                               |                                                                                                                                     |

**Table 2: Output Voltage Chart for Buck 1, Buck 2, Buck 3, and Buck 4**

| D[6:0]  | V <sub>OUT</sub> (V) | D[6:0]  | V <sub>OUT</sub> (V) | D[6:0]  | V <sub>OUT</sub> (V) | D[6:0]  | V <sub>OUT</sub> (V) |
|---------|----------------------|---------|----------------------|---------|----------------------|---------|----------------------|
| 0000000 | 0.6000               | 0100000 | 1.0000               | 1000000 | 1.4000               | 1100000 | 1.8000               |
| 0000001 | 0.6125               | 0100001 | 1.0125               | 1000001 | 1.4125               | 1100001 | 1.8125               |
| 0000010 | 0.6250               | 0100010 | 1.0250               | 1000010 | 1.4250               | 1100010 | 1.8250               |
| 0000011 | 0.6375               | 0100011 | 1.0375               | 1000011 | 1.4375               | 1100011 | 1.8375               |
| 0000100 | 0.6500               | 0100100 | 1.0500               | 1000100 | 1.4500               | 1100100 | 1.8500               |
| 0000101 | 0.6625               | 0100101 | 1.0625               | 1000101 | 1.4625               | 1100101 | 1.8625               |
| 0000110 | 0.6750               | 0100110 | 1.0750               | 1000110 | 1.4750               | 1100110 | 1.8750               |
| 0000111 | 0.6875               | 0100111 | 1.0875               | 1000111 | 1.4875               | 1100111 | 1.8875               |
| 0001000 | 0.7000               | 0101000 | 1.1000               | 1001000 | 1.5000               | 1101000 | 1.9000               |
| 0001001 | 0.7125               | 0101001 | 1.1125               | 1001001 | 1.5125               | 1101001 | 1.9125               |
| 0001010 | 0.7250               | 0101010 | 1.1250               | 1001010 | 1.5250               | 1101010 | 1.9250               |
| 0001011 | 0.7375               | 0101011 | 1.1375               | 1001011 | 1.5375               | 1101011 | 1.9375               |
| 0001100 | 0.7500               | 0101100 | 1.1500               | 1001100 | 1.5500               | 1101100 | 1.9500               |
| 0001101 | 0.7625               | 0101101 | 1.1625               | 1001101 | 1.5625               | 1101101 | 1.9625               |
| 0001110 | 0.7750               | 0101110 | 1.1750               | 1001110 | 1.5750               | 1101110 | 1.9750               |
| 0001111 | 0.7875               | 0101111 | 1.1875               | 1001111 | 1.5875               | 1101111 | 1.9875               |
| 0010000 | 0.8000               | 0110000 | 1.2000               | 1010000 | 1.6000               | 1110000 | 2.0000               |
| 0010001 | 0.8125               | 0110001 | 1.2125               | 1010001 | 1.6125               | 1110001 | 2.0125               |
| 0010010 | 0.8250               | 0110010 | 1.2250               | 1010010 | 1.6250               | 1110010 | 2.0250               |
| 0010011 | 0.8375               | 0110011 | 1.2375               | 1010011 | 1.6375               | 1110011 | 2.0375               |



|         |        |         |        |         |        |         |        |
|---------|--------|---------|--------|---------|--------|---------|--------|
| 0010100 | 0.8500 | 0110100 | 1.2500 | 1010100 | 1.6500 | 1110100 | 2.0500 |
| 0010101 | 0.8625 | 0110101 | 1.2625 | 1010101 | 1.6625 | 1110101 | 2.0625 |
| 0010110 | 0.8750 | 0110110 | 1.2750 | 1010110 | 1.6750 | 1110110 | 2.0750 |
| 0010111 | 0.8875 | 0110111 | 1.2875 | 1010111 | 1.6875 | 1110111 | 2.0875 |
| 0011000 | 0.9000 | 0111000 | 1.3000 | 1011000 | 1.7000 | 1111000 | 2.1000 |
| 0011001 | 0.9125 | 0111001 | 1.3125 | 1011001 | 1.7125 | 1111001 | 2.1125 |
| 0011010 | 0.9250 | 0111010 | 1.3250 | 1011010 | 1.7250 | 1111010 | 2.1250 |

Table 2: Output Voltage Chart for Buck 1, Buck 2, Buck 3, and Buck 4 (continued)

| D[6:0]  | V <sub>OUT</sub> (V) | D[6:0]  | V <sub>OUT</sub> (V) | D[6:0]  | V <sub>OUT</sub> (V) | D[6:0]  | V <sub>OUT</sub> (V) |
|---------|----------------------|---------|----------------------|---------|----------------------|---------|----------------------|
| 0011011 | 0.9375               | 0111011 | 1.3375               | 1011011 | 1.7375               | 1111011 | 2.1375               |
| 0011100 | 0.9500               | 0111100 | 1.3500               | 1011100 | 1.7500               | 1111100 | 2.1500               |
| 0011101 | 0.9625               | 0111101 | 1.3625               | 1011101 | 1.7625               | 1111101 | 2.1625               |
| 0011110 | 0.9750               | 0111110 | 1.3750               | 1011110 | 1.7750               | 1111110 | 2.1750               |
| 0011111 | 0.9875               | 0111111 | 1.3875               | 1011111 | 1.7875               | 1111111 | 2.1875               |

### LDO Regulator Output Voltage Set

| Bits   | Name        | Default | Description                                                                | Reset Condition                                                                                                                     |
|--------|-------------|---------|----------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| D[6:0] | LDOVOUT SET | BY OTP  | Sets the output voltage from 0.8V to 3.975V with 25mV steps (see Table 3). | <ul style="list-style-type: none"> <li>• AVIN &lt; UVLO</li> <li>• SFRST</li> <li>• Manual reset</li> <li>• Long press 2</li> </ul> |

Table 3: Output Voltage Chart of all LDOs

| D[6:0]  | V <sub>OUT</sub> (V) | D[6:0]  | V <sub>OUT</sub> (V) | D[6:0]  | V <sub>OUT</sub> (V) | D[6:0]  | V <sub>OUT</sub> (V) |
|---------|----------------------|---------|----------------------|---------|----------------------|---------|----------------------|
| 0000000 | 0.800                | 0100000 | 1.600                | 1000000 | 2.400                | 1100000 | 3.200                |
| 0000001 | 0.825                | 0100001 | 1.625                | 1000001 | 2.425                | 1100001 | 3.225                |
| 0000010 | 0.850                | 0100010 | 1.650                | 1000010 | 2.450                | 1100010 | 3.250                |
| 0000011 | 0.875                | 0100011 | 1.675                | 1000011 | 2.475                | 1100011 | 3.275                |
| 0000100 | 0.900                | 0100100 | 1.700                | 1000100 | 2.500                | 1100100 | 3.300                |
| 0000101 | 0.925                | 0100101 | 1.725                | 1000101 | 2.525                | 1100101 | 3.325                |
| 0000110 | 0.950                | 0100110 | 1.750                | 1000110 | 2.550                | 1100110 | 3.350                |
| 0000111 | 0.975                | 0100111 | 1.775                | 1000111 | 2.575                | 1100111 | 3.375                |
| 0001000 | 1.000                | 0101000 | 1.800                | 1001000 | 2.600                | 1101000 | 3.400                |
| 0001001 | 1.025                | 0101001 | 1.825                | 1001001 | 2.625                | 1101001 | 3.425                |
| 0001010 | 1.050                | 0101010 | 1.850                | 1001010 | 2.650                | 1101010 | 3.450                |
| 0001011 | 1.075                | 0101011 | 1.875                | 1001011 | 2.675                | 1101011 | 3.475                |
| 0001100 | 1.100                | 0101100 | 1.900                | 1001100 | 2.700                | 1101100 | 3.500                |
| 0001101 | 1.125                | 0101101 | 1.925                | 1001101 | 2.725                | 1101101 | 3.525                |
| 0001110 | 1.150                | 0101110 | 1.950                | 1001110 | 2.750                | 1101110 | 3.550                |
| 0001111 | 1.175                | 0101111 | 1.975                | 1001111 | 2.775                | 1101111 | 3.575                |
| 0010000 | 1.200                | 0110000 | 2.000                | 1010000 | 2.800                | 1110000 | 3.600                |
| 0010001 | 1.225                | 0110001 | 2.025                | 1010001 | 2.825                | 1110001 | 3.625                |
| 0010010 | 1.250                | 0110010 | 2.050                | 1010010 | 2.850                | 1110010 | 3.650                |
| 0010011 | 1.275                | 0110011 | 2.075                | 1010011 | 2.875                | 1110011 | 3.675                |
| 0010100 | 1.300                | 0110100 | 2.100                | 1010100 | 2.900                | 1110100 | 3.700                |
| 0010101 | 1.325                | 0110101 | 2.125                | 1010101 | 2.925                | 1110101 | 3.725                |
| 0010110 | 1.350                | 0110110 | 2.150                | 1010110 | 2.950                | 1110110 | 3.750                |
| 0010111 | 1.375                | 0110111 | 2.175                | 1010111 | 2.975                | 1110111 | 3.775                |
| 0011000 | 1.400                | 0111000 | 2.200                | 1011000 | 3.000                | 1111000 | 3.800                |
| 0011001 | 1.425                | 0111001 | 2.225                | 1011001 | 3.025                | 1111001 | 3.825                |
| 0011010 | 1.450                | 0111010 | 2.250                | 1011010 | 3.050                | 1111010 | 3.850                |
| 0011011 | 1.475                | 0111011 | 2.275                | 1011011 | 3.075                | 1111011 | 3.875                |
| 0011100 | 1.500                | 0111100 | 2.300                | 1011100 | 3.100                | 1111100 | 3.900                |
| 0011101 | 1.525                | 0111101 | 2.325                | 1011101 | 3.125                | 1111101 | 3.925                |
| 0011110 | 1.550                | 0111110 | 2.350                | 1011110 | 3.150                | 1111110 | 3.950                |
| 0011111 | 1.575                | 0111111 | 2.375                | 1011111 | 3.175                | 1111111 | 3.975                |

### Reg 0D: Status 1

Status registers are non-latch. This register automatically updates according to its real-time status.

| Bits   | Name                                                               | Description                                                                                                                                                                                                                                                                                                         | Reset Condition                                                                                                                     |
|--------|--------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| D[7:0] | PG1<br>PG2<br>PG3<br>PG4<br>PGLDO2<br>PGLDO3<br>PGLDO4<br>PGLDORTC | Power good indicator for the bucks and LDOs. PG = 1 when the output voltage exceeds 90% of the reference voltage. PG = 0 when the output voltage is below 80% of the reference voltage.<br><br>During the I <sup>2</sup> C-controlled dynamic voltage scaling, the PG deglitch timer blanks the possible PG glitch. | <ul style="list-style-type: none"> <li>• AVIN &lt; UVLO</li> <li>• SFRST</li> <li>• Manual reset</li> <li>• Long press 2</li> </ul> |

### Reg 0E: Status 2

| Bits | Name       | Description                                                                                                                                                 | Reset Condition                                                                                                                     |
|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| D[7] | KEYON      | A push-button power-on event (long press 1) is detected.                                                                                                    | These bits are latched once they are triggered. The bit can be cleared by a read action to the status register.<br><br>AVIN < UVLO  |
| D[6] | KEYOFF     | A push-button power-off event (long press 2) is detected.                                                                                                   |                                                                                                                                     |
| D[5] | MREST      | A manual reset event is detected.                                                                                                                           |                                                                                                                                     |
| D[4] | SHORTKEYON | If the MP5496 is in a power-off state, nPBIN is pulled to ground and lasts longer than the maximum 30ms debounce time. Then the SHORTKEYON bit is set high. |                                                                                                                                     |
| D[3] | SFRST_ON   | A software reset event is detected. When the SFRST bit is set high, the SFRST_ON bit goes high, and the high state is latched.                              |                                                                                                                                     |
| D[0] | PGLDO5     | Power good indicator for LDO5. Non-latch bits.                                                                                                              | <ul style="list-style-type: none"> <li>• AVIN &lt; UVLO</li> <li>• SFRST</li> <li>• Manual reset</li> <li>• Long press 2</li> </ul> |

### Reg 0F: Status 3

| Bits | Name      | Description                                                                                    | Reset Condition                                                                                                     |
|------|-----------|------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|
| D[7] | OTWARNING | Die temperature early warning bit. If the bit is high, the die temperature has exceeded 120°C. | This bit is latched once it is triggered. It is cleared by a read action to the status register.<br><br>AVIN < UVLO |
| D[6] | OTEMPP    | Over-temperature indication. If the bit is high, the IC is in thermal shutdown.                |                                                                                                                     |

### Reg 11: ID2

| Bits   | Name        | Description |
|--------|-------------|-------------|
| D[7:4] | Vendor ID   | 1000.       |
| D[3:0] | OTP version | 0100.       |

## APPLICATION INFORMATION

### Selecting the Inductor

For most applications, use a 0.47μH to 2.2μH inductor with a DC current rating at least 25% greater than the maximum load current. For the highest efficiency, use an inductor with a DC resistance below 15mΩ. For most designs, the inductance value can be calculated with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where  $\Delta I_L$  is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be estimated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Use a larger inductor (<100mA) to improve efficiency under light-load conditions.

### Selecting the Step-Down Converter Input Capacitor

The step-down converter has discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use a 22μF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at  $V_{IN} = 2V_{OUT}$ , calculated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

### Selecting the Step-Down Converter Output Capacitor

The output capacitor for the step-down regulator maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (6)$$

Where  $L_1$  is the inductor value, and  $R_{ESR}$  is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation.

## Recommended External Components for DC/DC and LDO Converters

Table 4 lists recommended external components for the DC/DC converters and LDO regulators.

**Table 4: Recommended External Components**

| Component                    | Value    | Description                                           |
|------------------------------|----------|-------------------------------------------------------|
| VIN1 C <sub>IN</sub>         | 22μF     | 0805 size/10V ceramic capacitor                       |
| VIN2 C <sub>IN</sub>         | 22μF     | 0805 size/10V ceramic capacitor                       |
| VIN3 C <sub>IN</sub>         | 22μF     | 0805 size/10V ceramic capacitor                       |
| VIN4 C <sub>IN</sub>         | 22μF     | 0805 size/10V ceramic capacitor                       |
| VIN5 C <sub>IN</sub>         | 10μF     | 0805 size/10V ceramic capacitor                       |
| AVIN C <sub>IN</sub>         | 1μF      | 0603 size/10V ceramic capacitor                       |
| Buck 1 C <sub>OUT</sub>      | 22μF x 2 | 0805 size/10V ceramic capacitor                       |
| Buck 1 inductance            | 1μH      | I <sub>SAT</sub> > current limit                      |
| Buck 2 C <sub>OUT</sub>      | 22μF     | 0805 size/10V ceramic capacitor                       |
| Buck 2 inductance            | 1μH      | I <sub>SAT</sub> > current limit                      |
| Buck 3 C <sub>OUT</sub>      | 22μF x 2 | 0805 size/10V ceramic capacitor                       |
| Buck 3 inductance            | 1μH      | I <sub>SAT</sub> > current limit                      |
| Buck 4 C <sub>OUT</sub>      | 22μF     | 0805 size/10V ceramic capacitor                       |
| Buck 4 inductance            | 1.5μH    | I <sub>SAT</sub> > current limit                      |
| RTCLDO C <sub>OUT</sub>      | 1μF      | 0603 size/6.3V ceramic capacitor                      |
| LDO2 C <sub>OUT</sub>        | 2.2μF    | 0603 size/6.3V ceramic capacitor                      |
| LDO3 C <sub>OUT</sub>        | 2.2μF    | 0603 size/6.3V ceramic capacitor                      |
| LDO4 C <sub>OUT</sub>        | 2.2μF    | 0603 size/6.3V ceramic capacitor                      |
| LDO5 C <sub>OUT</sub>        | 2.2μF    | 0603 size/6.3V ceramic capacitor                      |
| RSTO pull-up resistor        | 100kΩ    | 0603 or 0402 size film resistor                       |
| nPBIN pull-low resistor      | 34kΩ     | Push-button function, 0603 or 0402 size film resistor |
| AVIN series resistor to VIN1 | 10Ω      | 0603 or 0402 size film resistor                       |

### PCB Layout Guidelines <sup>(13)</sup>

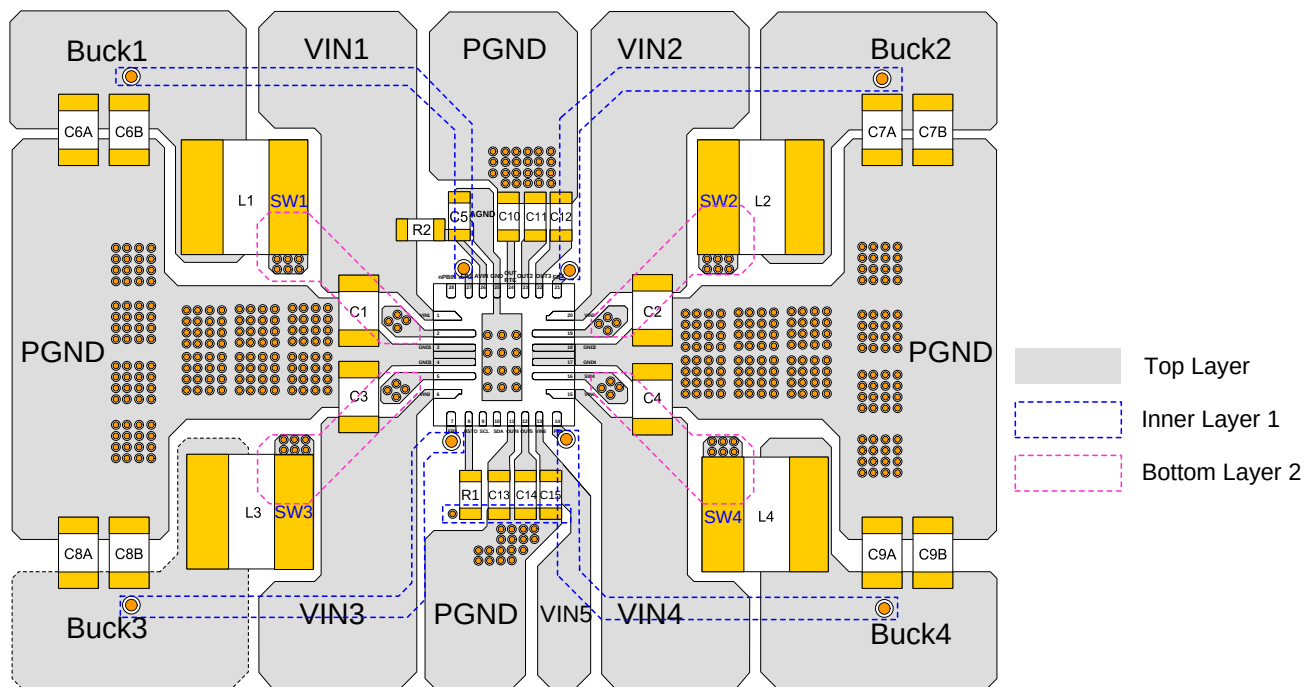
Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended for the best performance. For the best results, refer to Figure 14 and follow the guidelines below:

1. Connect the input ground to GND using the shortest and widest trace possible.
2. Connect the input capacitor to VIN using the shortest and widest trace possible.

3. Ensure that FB1, FB2, FB3, and FB4 are Kelvin-connected to the buck output capacitors. Do not directly connect FB to the inductor's output node.
4. Route SW away from sensitive analog areas, such as FB1 to FB4.

**Note:**

13) The recommended layout is based on Figure 20 on page 38.

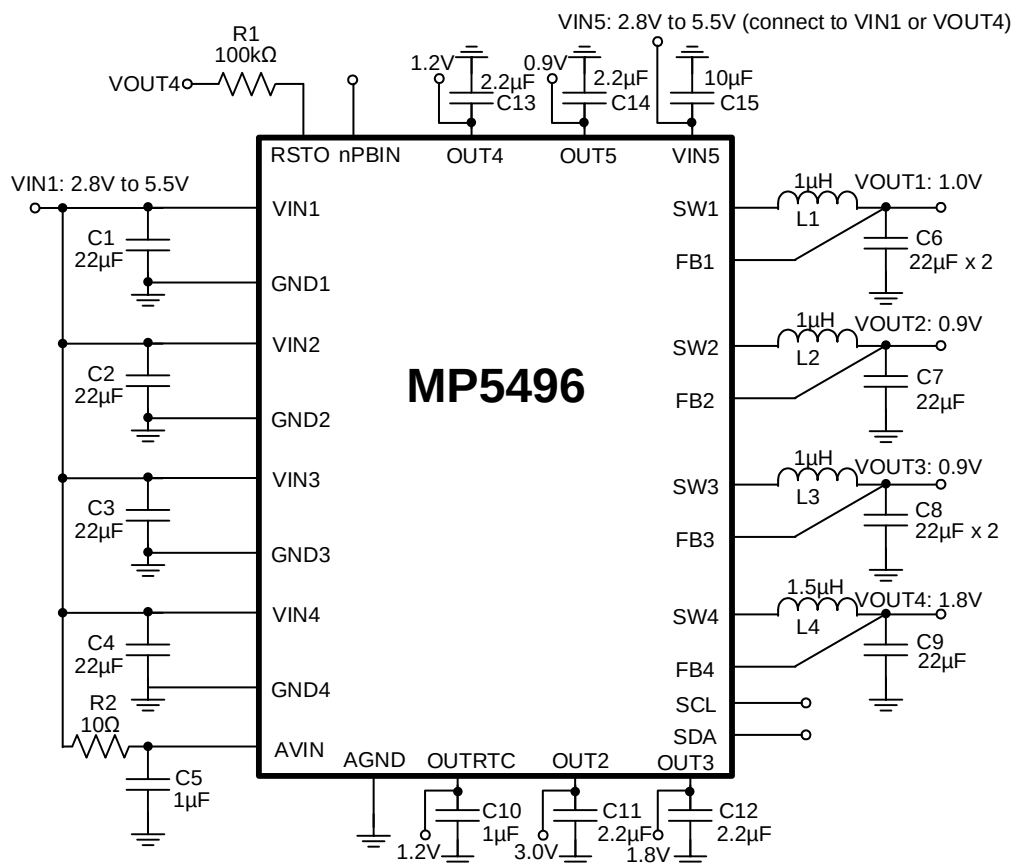


**Figure 19: Recommended Layout <sup>(14)</sup>**

**Note:**

14) It is recommended to separate Buck 1/3 and Buck 2/4's PGND on the top layer.

## TYPICAL APPLICATION CIRCUIT



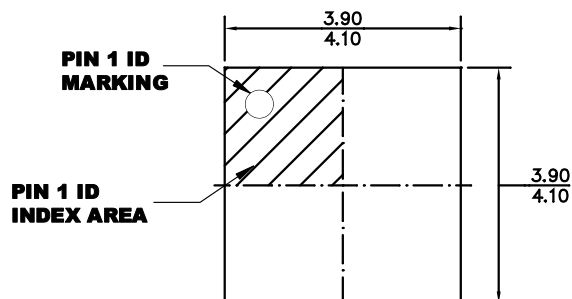
**Figure 20: Typical Application Circuit <sup>(15)</sup>**

**Note:**

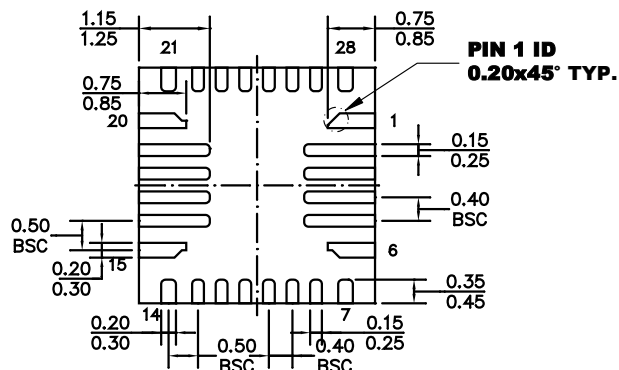
15) The minimum input voltage of VIN5 is equal to the maximum nominal output voltage of LDO4 and LDO5.

## PACKAGE INFORMATION

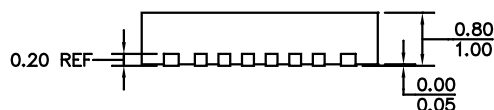
### QFN-28 (4mmx4mm)



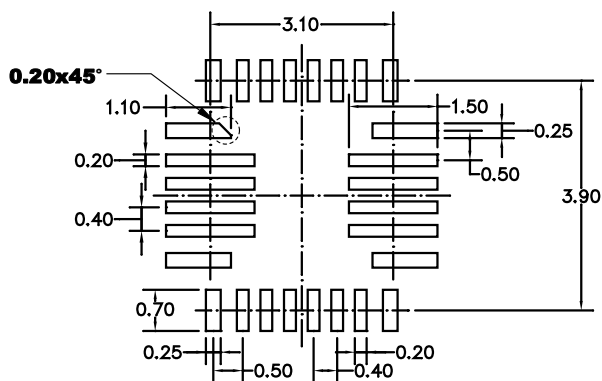
### TOP VIEW



### BOTTOM VIEW



### SIDE VIEW

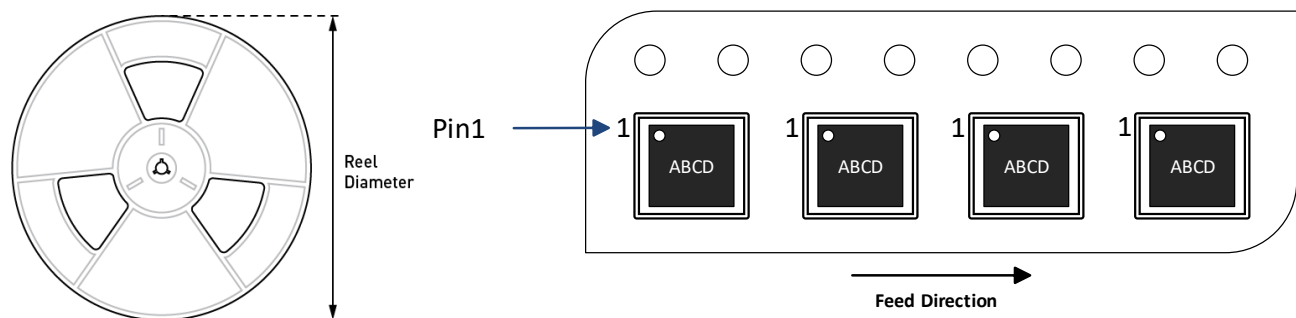


## RECOMMENDED LAND PATTERN

**NOTE:**

- 1) LAND PATTERNS OF PINS 1, 6, 15, AND 20 HAVE THE SAME LENGTH AND WIDTH.
- 2) LAND PATTERNS OF PINS 7, 14, 21, AND 28 HAVE THE SAME LENGTH AND WIDTH.
- 3) ALL DIMENSIONS ARE IN MILLIMETERS.
- 4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-220.
- 6) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



| Part Number     | Package Description | Quantity/ Reel | Quantity/ Tray | Quantity/ Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-----------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MP5496GR-0001-Z | QFN-28 (4mmx4mm)    | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                |



## Revision History

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 8/25/2020     | Initial Release | -             |

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