

# LP8733xx-Q1 Dual High-Current Buck Converter and Dual Linear Regulator

## 1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ambient operating temperature
- Input voltage: 2.8 V to 5.5 V
- Two high-efficiency step-down DC/DC converters:
  - Output voltage: 0.7 V to 3.36 V
  - Maximum output current 3 A per phase
  - Adding and shedding auto phase and force multi-phase operations in dual-phase configuration
  - Remote differential feedback voltage sensing in dual-phase configuration
  - Programmable output-voltage slew rate from  $0.5\text{ mV}/\mu\text{s}$  to  $10\text{ mV}/\mu\text{s}$
  - 2-MHz switching frequency
  - Spread-spectrum mode and phase interleaving for EMI reduction
- Two linear regulators:
  - Input voltage: 2.5 V to 5.5 V
  - Output voltage: 0.8 V to 3.3 V
  - Maximum output current 300 mA
- Configurable general-purpose output signals (GPO, GPO2)
- Interrupt function with programmable masking
- Programmable power-good signal (PGOOD)
- Output short-circuit and overload protection
- Overtemperature warning and protection
- Overvoltage protection (OVP) and undervoltage lockout (UVLO)
- 28-pin, 5-mm × 5-mm VQFN package with wettable flanks

## 2 Applications

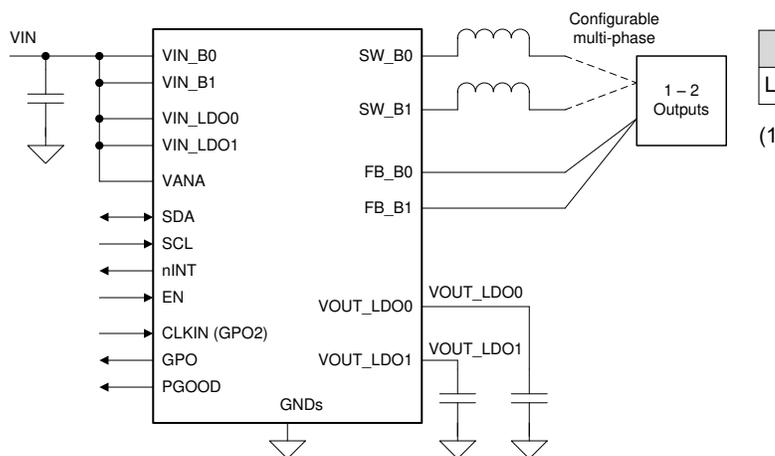
- Automotive head unit and cluster
- Automotive camera module
- Surround view system ECU
- Radar system ECU

## 3 Description

The LP8733xx-Q1 is designed to meet the power management requirements in automotive applications. The device has two step-down DC/DC converters (which can be configured as a single dual-phase regulator or two single-phase regulators), two linear regulators, and two general-purpose digital-output signals. The device is controlled by an I<sup>2</sup>C-compatible serial interface and by an enable signal.

The automatic PWM/PFM (AUTO mode) operation together with the automatic phase adding/shedding gives high efficiency over a wide output-current range. The LP8733xx-Q1 supports remote voltage sensing (differential in dual-phase configuration) to compensate IR drop between the regulator output and the point-of-load (POL), thus improving the accuracy of the output voltage. In addition, the switching clock can be forced to PWM mode and also synchronized to an external clock to minimize the disturbances.

The LP8733xx-Q1 device supports programmable start-up and shutdown delays and sequences including GPO signals synchronized to the enable signal. During start-up and voltage change, the device controls the output slew rate to minimize output voltage overshoot and the in-rush current.



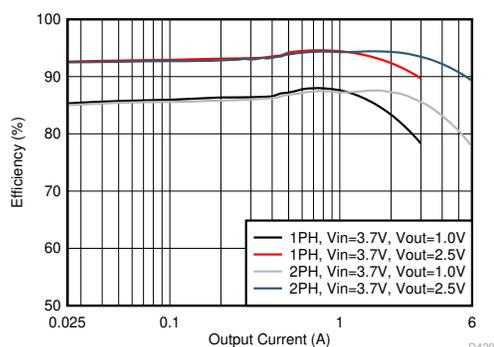
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Simplified Schematic

## Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP8733xx-Q1	VQFN (28)	5.00 mm × 5.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



DC/DC Efficiency vs Output Current (Dual-Phase)



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (June 2019) to Revision A (June 2021)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated the <i>LDO Output Capacitor Selection</i> section.....	64

## 5 Pin Configuration and Functions

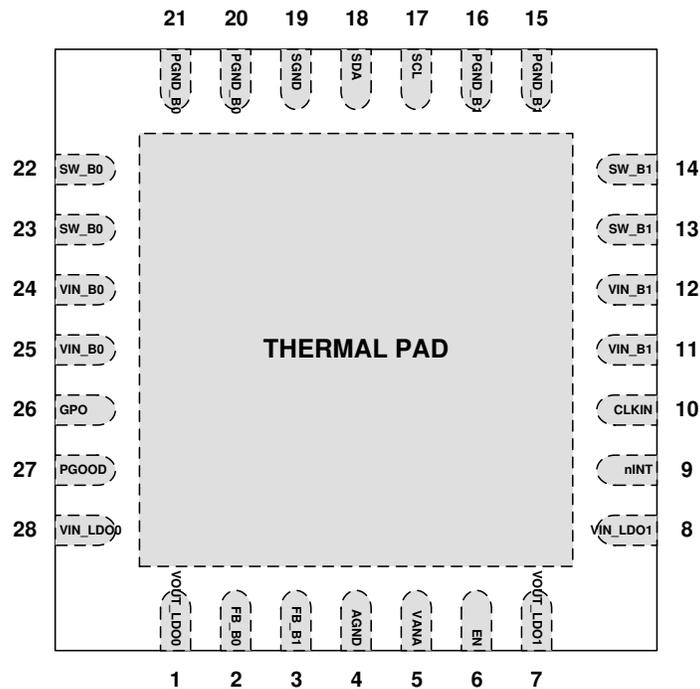


Figure 5-1. RHD Package 28-Pin VQFN With Thermal Pad Top View

Table 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NUMBER	NAME		
1	VOUT_LDO0	P/O	LDO0 output. If the LDO0 is not used, leave the pin floating.
2	FB_B0	A	Output voltage feedback (positive) for Buck 0.
3	FB_B1	A	Output voltage feedback (positive) for Buck 1 in two single-phase configuration and output ground feedback (negative) for Buck 0 in dual-phase configuration.
4	AGND	G	Ground.
5	VANA	P/I	Supply voltage for analog and digital blocks. Must be connected to same node with VIN_Bx.
6	EN	D/I	Programmable enable signal for regulators and GPOs. If the pin is not used, leave the pin floating.
7	VOUT_LDO1	P/O	LDO1 output. If LDO1 is not used, leave the pin floating.
8	VIN_LDO1	P/I	Power input for LDO1. If LDO1 is not used, connect the pin to VANA.
9	nINT	D/O	Open-drain interrupt output. Active LOW. If the pin is not used, connect the pin to ground.
10	CLKIN	D/I/O	External clock input. Alternative function is general-purpose digital output (GPO2). If the pin is not used, leave the pin floating.
11, 12	VIN_B1	P/I	Input for Buck 1. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
13, 14	SW_B1	P/O	Buck 1 switch node. If the Buck 1 is not used, leave the pin floating.
15, 16	PGND_B1	P/G	Power ground for Buck 1.
17	SCL	D/I	Serial interface clock input for I <sup>2</sup> C access. Connect a pullup resistor. If the I <sup>2</sup> C interface is not used, connect the pin to Ground.
18	SDA	D/I/O	Serial interface data input and output for I <sup>2</sup> C access. Connect a pullup resistor. If the I <sup>2</sup> C interface is not used, connect the pin to Ground.
19	SGND	G	Ground.
20, 21	PGND_B0	P/G	Power ground for Buck 0.
22, 23	SW_B0	P/O	Buck 0 switch node. If the Buck 0 is not used, leave the pin floating.

**Table 5-1. Pin Functions (continued)**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NUMBER	NAME		
24, 25	VIN_B0	P/I	Input for Buck 0. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
26	GPO	D/O	General-purpose digital output. If the pin is not used, leave the pin floating.
27	PGOOD	D/O	Power-good indication signal. If the pin is not used, leave the pin floating.
28	VIN_LDO0	P/I	Power input for LDO0. If the LDO0 is not used, connect the pin to VANA.
Thermal Pad	—	—	Connect to PCB ground plane using multiple vias for good thermal performance.

(1) A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, and O: Output Pin.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
VIN_Bx, VANA	Voltage on power connections (must use the same input supply)	-0.3	6	V
VIN_LDOx	Voltage on power connections	-0.3	6	V
SW_Bx	Voltage on buck switch nodes	-0.3	(VIN_Bx + 0.3 V) with 6-V maximum	V
FB_Bx	Voltage on buck voltage sense nodes	-0.3	(VANA + 0.3 V) with 6-V maximum	V
VOUT_LDOx	Voltage on LDO output	-0.3	(VIN_LDOx + 0.3 V) with 6-V maximum	V
SDA, SCL, nINT, EN	Voltage on logic pins (input or output pins)	-0.3	6	V
PGOOD, GPO, CLKIN (GPO2)	Voltage on logic pins (input or output pins)	-0.3	(VANA + 0.3 V) with 6-V maximum	V
T <sub>J-MAX</sub>	Junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	
Maximum lead temperature (soldering, 10 seconds)			260	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground.

### 6.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM)	±2000	V	
		Charged-device model (CDM)	All pins		±500
			Corner pins (1, 7, 8, 14, 15, 21, 22, 28)		±750

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
<b>INPUT VOLTAGE</b>				
VIN_Bx, VANA	Voltage on power connections (must use the same input supply)	2.8	5.5	V
VIN_LDOx	Voltage on LDO inputs	2.5	5.5	V
EN, nINT	Voltage on logic pins (input or output pins)	0	5.5	V
CLKIN	Voltage on logic pins (input pin)	0	VANA with 5.5-V maximum	V
PGOOD, GPO, GPO2	Voltage on logic pins (output pins)	0	VANA	V
SCL, SDA	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes	0	1.95	V
	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), and Fast+ (1 MHz) Modes	0	VANA with 3.6-V maximum	V
<b>TEMPERATURE</b>				
T <sub>J</sub>	Junction temperature	-40	140	°C
T <sub>A</sub>	Ambient temperature	-40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LP8733xx-Q1	UNIT
		RHD (VQFN)	
		28 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	36.7	°C/W
R <sub>θJCTop</sub>	Junction-to-case (top) thermal resistance	26.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	8.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	8.8	°C/W
R <sub>θJCbott</sub>	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 6.5 Electrical Characteristics

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>EXTERNAL COMPONENTS</b>						
C <sub>IN_BUCK</sub>	Input filtering capacitance for buck regulators	Effective capacitance, connected from VIN_Bx to PGND_Bx	1.9	10		μF
C <sub>OUT_BUCK</sub>	Output filtering capacitance for buck regulators	Effective capacitance per phase	10	22	500	μF
C <sub>POL_BUCK</sub>	Point-of-load (POL) capacitance for buck regulators	Optional POL capacitance		22		μF
C <sub>OUT_TOTAL_BUCK</sub>	Buck output capacitance, total (local and POL)	Total output capacitance per phase			500	μF
C <sub>IN_LDO</sub>	Input filtering capacitance for LDO regulators	Effective capacitance, connected from VIN_LDOx to AGND. C <sub>IN_LDO</sub> must be at least two times larger than C <sub>OUT_LDO</sub>	0.6	2.2		μF
C <sub>OUT_LDO</sub>	Output filtering capacitance for LDO regulators	Effective capacitance	0.4	1	2.7	μF
ESR <sub>C</sub>	Input and output capacitor ESR	[1-10] MHz		2	10	mΩ
L	Inductor	Inductance of the inductor		0.47		μH
			-30%		30%	
DCR <sub>L</sub>	Inductor DCR			25		mΩ
<b>BUCK REGULATORS</b>						
V <sub>(VIN_Bx)</sub> , V <sub>(VANA)</sub>	Input voltage range	VIN_Bx and VANA pins must be connected to the same supply line	2.8	3.7	5.5	V
V <sub>OUT_Bx</sub>	Output voltage	Programmable voltage range	0.7	1	3.36	V
		Step size, $0.7\text{ V} \leq V_{OUT} < 0.73\text{ V}$		10		mV
		Step size, $0.73\text{ V} \leq V_{OUT} < 1.4\text{ V}$		5		
		Step size, $1.4\text{ V} \leq V_{OUT} \leq 3.36\text{ V}$		20		
I <sub>OUT_Bx</sub>	Output current	Output current, single-phase output			3 <sup>(3)</sup>	A
		Output current, dual-phase output			6 <sup>(3)</sup>	
	Input and Output voltage difference	Minimum voltage between V <sub>(VIN_Bx)</sub> and V <sub>OUT</sub> to fulfill the electrical characteristics	0.8			V

## 6.5 Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT\_Bx\_DC}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature	Force PWM mode, $V_{OUT} < 1\text{ V}$	-20		20	mV
		Force PWM mode, $V_{OUT} \geq 1\text{ V}$	-2%		2%	
		PFM mode, $V_{OUT} < 1\text{ V}$ , the average output voltage level is increased by max. 20 mV	-20		40	mV
		PFM mode, $V_{OUT} \geq 1\text{ V}$ , the average output voltage level is increased by max. 20 mV	-2%		2% + 20 mV	
	Ripple voltage, single-phase output	PWM mode		10		mV <sub>p-p</sub>
		PFM mode, $I_{OUT} = 10\text{ mA}$		25		
	Ripple voltage, dual-phase output	PWM mode		5		mV <sub>p-p</sub>
		PFM mode, $I_{OUT} = 10\text{ mA}$		4		
$DC_{LNR}$	DC line regulation	$I_{OUT} = 1\text{ A}$		$\pm 0.05$		%/V
$DC_{LDR}$	DC load regulation in PWM mode	$V_{OUT\_Bx} = 1\text{ V}$ , $I_{OUT}$ from 0 to $I_{OUT(max)}$		0.3%		
$T_{LDSR}$	Transient load step response, single-phase output	$I_{OUT} = 0.1\text{ A to } 2\text{ A}$ , $T_R = T_F = 400\text{ ns}$ , PWM mode		$\pm 55$		mV
	Transient load step response, dual-phase output	$I_{OUT} = 0.1\text{ A to } 4\text{ A}$ , $T_R = T_F = 400\text{ ns}$ , PWM mode		$\pm 50$		mV
$T_{LNSR}$	Transient line response	$V_{(VIN\_Bx)}$ stepping $3\text{ V} \leftrightarrow 3.5\text{ V}$ , $T_R = T_F = 10\text{ }\mu\text{s}$ , $I_{OUT} = I_{OUT(max)}$		$\pm 10$		mV
$I_{LIM\ FWD}$	Forward current limit per phase (peak for every switching cycle)	Programmable range	1.5		4	A
		Step size		0.5		
		Accuracy, $V_{(VIN\_Bx)} \geq 3\text{ V}$ , $I_{LIM} = 4\text{ A}$	-5%	7.5%	20%	
		Accuracy, $2.8\text{ V} \leq V_{(VIN\_Bx)} < 3\text{ V}$ , $I_{LIM} = 4\text{ A}$	-20%	7.5%	20%	
$I_{LIM\ NEG}$	Negative current limit per phase		1.6	2.0	3.0	A
$R_{DS(ON)\ HS\ FET}$	On-resistance, high-side FET	Each phase, between $VIN\_Bx$ and $SW\_Bx$ pins ( $I = 1\text{ A}$ )		50	110	m $\Omega$
$R_{DS(ON)\ LS\ FET}$	On-resistance, low-side FET	Each phase, between $SW\_Bx$ and $PGND\_Bx$ pins ( $I = 1\text{ A}$ )		45	90	m $\Omega$
$f_{sw}$	Switching frequency	PWM mode	1.8	2	2.2	MHz
	Current balancing for dual-phase output	Current mismatch between phases, $I_{OUT} > 1\text{ mA}$			10%	
	Start-up time (soft start)	From $ENx$ to $V_{OUT\_Bx} = 0.35\text{ V}$ (slew-rate control begins)		120		$\mu\text{s}$
	Output voltage slew-rate <sup>(4)</sup>	$SLEW\_RATEx[2:0] = 010$ , $C_{OUT-TOTAL\_BUCK} < 80\text{ }\mu\text{F}$ per phase	-15%	10	15%	mV/ $\mu\text{s}$
$SLEW\_RATEx[2:0] = 011$ , $C_{OUT-TOTAL\_BUCK} < 130\text{ }\mu\text{F}$ per phase		7.5				
$SLEW\_RATEx[2:0] = 100$ , $C_{OUT-TOTAL\_BUCK} < 250\text{ }\mu\text{F}$ per phase		3.8				
$SLEW\_RATEx[2:0] = 101$ , $C_{OUT-TOTAL\_BUCK} < 500\text{ }\mu\text{F}$ per phase		1.9				
$SLEW\_RATEx[2:0] = 110$ , $C_{OUT-TOTAL\_BUCK} < 500\text{ }\mu\text{F}$ per phase		0.94				
$SLEW\_RATEx[2:0] = 111$ , $C_{OUT-TOTAL\_BUCK} < 500\text{ }\mu\text{F}$ per phase		0.47				

## 6.5 Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PFM-PWM}$	PFM-to-PWM - current threshold <sup>(5)</sup>			550		mA
$I_{PWM-PFM}$	PWM-to-PFM - current threshold <sup>(5)</sup>			290		mA
$I_{ADD}$	Phase adding level (dual-phase output)	From 1-phase to 2-phase		1000		mA
$I_{SHED}$	Phase shedding level (dual-phase output)	From 2-phase to 1-phase		650		mA
$R_{DIS\_Bx}$	Output pulldown resistance	Regulator disabled	150	250	350	$\Omega$
	Output voltage monitoring for PGOOD pin and for power-good Interrupt	$V_{(VIN\_Bx)}$ and $V_{(VANA)}$ fixed 3.7 V				
		Overvoltage threshold (compared to DC output voltage level, $V_{VOUT\_Bx\_DC}$ )	39	50	64	mV
		Undervoltage threshold (compared to DC output voltage level, $V_{VOUT\_Bx\_DC}$ )	-53	-40	-29	mV
		Deglitch time during operation and after voltage change	4		15	$\mu\text{s}$
	Gating time for PGOOD signal after regulator enable or voltage change	PGOOD_MODE = 0		800		$\mu\text{s}$
<b>LDO REGULATORS</b>						
$V_{IN\_LDOx}$	Input voltage range for LDO power inputs	$V_{IN\_LDOx}$ can be higher or lower than $V_{(VANA)}$	2.5	3.7	5.5	V
$V_{OUT\_LDOx}$	Output voltage	Programmable voltage range	0.8		3.3	V
		Step size		0.1		
$I_{OUT\_LDOx}$	Output current				300	mA
	Dropout voltage	$V_{(VIN\_LDOx)} - V_{(VOUT\_LDOx)}$ ; $I_{OUT} = I_{OUT(max)}$ ; Programmed output voltage is higher than $V_{(VIN\_LDOx)}$			200	mV
$V_{OUT\_LDO\_DC}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process, temperature	$V_{OUT} < 1\text{ V}$	-20		20	mV
		$V_{OUT} \geq 1\text{ V}$	-2%		2%	
$DC_{LNR}$	DC line regulation	$I_{OUT} = 1\text{ mA}$		0.1		%/V
$DC_{LDR}$	DC load regulation	$I_{OUT} = 1\text{ mA}$ to $I_{OUT(max)}$		0.8%		
$T_{LDSR}$	Transient load step response	$I_{OUT} = 1\text{ mA}$ to $300\text{ mA}$ , $T_R = T_F = 1\text{ }\mu\text{s}$		-50/+40		mV
$T_{LNSR}$	Transient line response	$V_{(VIN\_LDOx)}$ stepping 3 V $\leftrightarrow$ 3.5 V, $T_R = T_F = 10\text{ }\mu\text{s}$ , $I_{OUT} = I_{OUT(max)}$		$\pm 7$		mV
PSRR	Power supply ripple rejection	$f = 10\text{ kHz}$ , $I_{OUT} = I_{OUT(max)}$		53		dB
	Noise	$10\text{ Hz} < F < 100\text{ kHz}$ , $I_{OUT} = I_{OUT(max)}$		82		$\mu\text{V}_{rms}$
$I_{SHORT(LDOx)}$	LDO current limit	$V_{OUT} = 0\text{ V}$	400	500	600	mA
	Start-up time	From enable to valid output voltage		300		$\mu\text{s}$
	Slew rate during start-up			15		mV/ $\mu\text{s}$
$R_{DIS\_LDOx}$	Output pulldown resistance	Regulator disabled	150	250	350	$\Omega$

## 6.5 Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output voltage monitoring for PGOOD pin and for power-good interrupt	Overvoltage monitoring, voltage rising (compared to DC output voltage level, $V_{OUT\_LDO\_DC}$ )	106%	108%	110%	
		Overvoltage monitoring, hysteresis	3%	3.5%	4%	
		Undervoltage monitoring, voltage falling (compared to DC output voltage level, $V_{OUT\_LDO\_DC}$ )	90%	92%	94%	
		Undervoltage monitoring, hysteresis	3%	3.5%	4%	
		Deglintch time during operation and after voltage change	4		15	$\mu\text{s}$
	Gating time for PGOOD signal after regulator enable or voltage change	PGOOD_MODE = 0		800		$\mu\text{s}$
<b>EXTERNAL CLOCK AND PLL</b>						
$f_{EXT\_CLK}$	External input clock <sup>(6)</sup>	Nominal frequency	1		24	MHz
		Nominal frequency step size		1		
		Required accuracy from nominal frequency	-30%		10%	
	External clock detection	Delay for missing clock detection			1.8	$\mu\text{s}$
		Delay and debounce for clock detection			20	
	Clock change delay (internal to external)	Delay from valid clock detection to use of external clock		600		$\mu\text{s}$
	PLL output clock jitter	Cycle to cycle		300		ps, p-p
<b>PROTECTION FUNCTIONS</b>						
	Thermal warning	Temperature rising, TDIE_WARN_LEVEL = 0	115	125	135	$^{\circ}\text{C}$
		Temperature rising, TDIE_WARN_LEVEL = 1	127	137	147	
		Hysteresis		20		
	Thermal shutdown	Temperature rising	140	150	160	$^{\circ}\text{C}$
		Hysteresis		20		
$V_{ANA\_OVP}$	VANA overvoltage	Voltage rising	5.6	5.8	6.1	V
		Voltage falling	5.45	5.73	5.96	
		Hysteresis	40			
$V_{ANA\_UVLO}$	VANA undervoltage lockout	Voltage rising	2.51	2.63	2.75	V
		Voltage falling	2.5	2.6	2.7	
	Buck short-circuit detection	Threshold	280	360	440	mV
	LDO short-circuit detection	Threshold	190	300	450	mV
<b>LOAD CURRENT MEASUREMENT FOR BUCK REGULATORS</b>						
	Current measurement range	Maximum code			10.22	A
	Resolution	LSB		20		mA
	Measurement accuracy	$I_{OUT} > 1\text{ A}$ per phase		<10%		
	Measurement time	PFM mode (automatically changing to PWM mode for the measurement)		45		$\mu\text{s}$
		PWM mode		4		
<b>CURRENT CONSUMPTION</b>						

## 6.5 Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Standby current consumption, regulators disabled			9		$\mu\text{A}$
	Active current consumption, one buck regulator enabled in auto mode, internal RC oscillator, PGOOD monitoring enabled	Single-phase output: $I_{OUT\_Bx} = 0\text{ mA}$ , not switching		58		$\mu\text{A}$
	Active current consumption, two buck regulators enabled in auto mode, internal RC oscillator, PGOOD monitoring enabled	Single-phase output: $I_{OUT\_Bx} = 0\text{ mA}$ , not switching		100		$\mu\text{A}$
	Active current consumption, one buck regulator enabled in auto mode, internal RC oscillator, PGOOD monitoring enabled	Dual-phase output: $I_{OUT\_Bx} = 0\text{ mA}$ , not switching		72		$\mu\text{A}$
	Active current consumption during PWM operation, one buck regulator enabled	Single-phase output: $I_{OUT\_Bx} = 0\text{ mA}$		15		$\text{mA}$
	Active current consumption during PWM operation, two buck regulators enabled	Single-phase output: $I_{OUT\_Bx} = 0\text{ mA}$		30		$\text{mA}$
	Active current consumption during PWM operation, buck regulator enabled	Dual-phase output: $I_{OUT\_Bx} = 0\text{ mA}$		15		$\text{mA}$
	LDO regulator enabled	Additional current consumption per LDO, $I_{OUT\_LDOx} = 0\text{ mA}$		86		$\mu\text{A}$
	PLL and clock detector current consumption	$f_{EXT\_CLK} = 1\text{ MHz}$ , Additional current consumption when enabled		2		$\text{mA}$
<b>DIGITAL INPUT SIGNALS EN, SCL, SDA, CLKIN</b>						
$V_{IL}$	Input low level				0.4	V
$V_{IH}$	Input high level		1.2			
$V_{HYS}$	Hysteresis of Schmitt Trigger inputs		10	80	200	mV
	EN/CLKIN pulldown resistance	EN_PD/CLKIN_PD = 1		500		$\text{k}\Omega$
<b>DIGITAL OUTPUT SIGNALS nINT, SDA</b>						
$V_{OL}$	Output low level	nINT: $I_{SOURCE} = 2\text{ mA}$			0.4	V
		SDA: $I_{SOURCE} = 20\text{ mA}$			0.4	V
$R_P$	External pullup resistor for nINT	To VIO Supply		10		$\text{k}\Omega$
<b>DIGITAL OUTPUT SIGNALS PGOOD, GPO, GPO2</b>						
$V_{OL}$	Output low level	$I_{SOURCE} = 2\text{ mA}$			0.4	V
$V_{OH}$	Output high level, configured to push-pull	$I_{SINK} = 2\text{ mA}$	$V_{VANA} - 0.4$		$V_{VANA}$	V

## 6.5 Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq +140^{\circ}\text{C}$ , specified  $V_{VANA}$ ,  $V_{VIN\_Bx}$ ,  $V_{VIN\_LDOx}$ ,  $V_{VOUT\_Bx}$ ,  $V_{VOUT\_LDOx}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{VANA} = V_{VIN\_Bx} = V_{VIN\_LDOx} = 3.7\text{ V}$ , and  $V_{OUT} = 1\text{ V}$ , unless otherwise noted<sup>(1) (2)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PU}$	Supply voltage for external pullup resistor, configured to open-drain				$V_{VANA}$	V
$R_{PU}$	External pullup resistor, configured to open-drain			10		k $\Omega$
<b>ALL DIGITAL INPUTS</b>						
$I_{LEAK}$	Input current	All logic inputs over pin voltage range	-1		1	$\mu\text{A}$

- (1) All voltage values are with respect to network ground.
- (2) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers are not verified, but do represent the most likely norm.
- (3) The maximum output current can be limited by the forward current limit  $I_{LIM\_FWD}$ . The power dissipation inside the die increases the junction temperature and limits the maximum current depending of the length of the current pulse, efficiency, board and ambient temperature.
- (4) The slew-rate can be limited by the current limit (forward or negative current limit), output capacitance and load current.
- (5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependent on the output voltage, input voltage and the inductor current level.
- (6) The external clock frequency must be selected so that buck switching frequency is above 1.7 MHz.

## 6.6 I<sup>2</sup>C Serial Bus Timing Parameters

These specifications are ensured by design. Unless otherwise noted,  $V_{IN\_BX} = 3.7\text{ V}$  (see <sup>(1)</sup>). See [Figure 6-1](#) for details about the I<sup>2</sup>C-Compatible Timing diagram.

			MIN	MAX	UNIT
f <sub>SCL</sub>	Serial clock frequency	Standard mode		100	kHz
		Fast mode		400	
		Fast mode+		1	MHz
		High-speed mode, C <sub>b</sub> = 100 pF		3.4	
		High-speed mode, C <sub>b</sub> = 400 pF		1.7	
t <sub>LOW</sub>	SCL low time	Standard mode	4.7		μs
		Fast mode	1.3		
		Fast mode+	0.5		
		High-speed mode, C <sub>b</sub> = 100 pF	0.16		
		High-speed mode, C <sub>b</sub> = 400 pF	0.32		
t <sub>HIGH</sub>	SCL high time	Standard mode	4		μs
		Fast mode	0.6		
		Fast mode+	0.26		
		High-speed mode, C <sub>b</sub> = 100 pF	0.06		
		High-speed mode, C <sub>b</sub> = 400 pF	0.12		
t <sub>SU,DAT</sub>	Data setup time	Standard mode	250		ns
		Fast mode	100		
		Fast mode+	50		
		High-speed mode	10		
t <sub>HD,DAT</sub>	Data hold time	Standard mode	10	3450	ns
		Fast mode	10	900	
		Fast mode+	10		
		High-speed mode, C <sub>b</sub> = 100 pF	10	70	
		High-speed mode, C <sub>b</sub> = 400 pF	10	150	
t <sub>SU,STA</sub>	Setup time for a start or a repeated start condition	Standard mode	4.7		μs
		Fast mode	0.6		
		Fast mode+	0.26		
		High-speed mode	0.16		
t <sub>HD,STA</sub>	Hold time for a start or a repeated start condition	Standard mode	4		μs
		Fast mode	0.6		
		Fast mode+	0.26		
		High-speed mode	0.16		
t <sub>BUF</sub>	Bus free time between a stop and start condition	Standard mode	4.7		μs
		Fast mode	1.3		
		Fast mode +	0.5		
t <sub>SU,STO</sub>	Setup time for a stop condition	Standard mode	4		μs
		Fast mode	0.6		
		Fast mode+	0.26		
		High-speed mode	0.16		

## 6.6 I<sup>2</sup>C Serial Bus Timing Parameters (continued)

These specifications are ensured by design. Unless otherwise noted,  $V_{IN\_Bx} = 3.7\text{ V}$  (see (1)). See Figure 6-1 for details about the I<sup>2</sup>C-Compatible Timing diagram.

			MIN	MAX	UNIT
$t_{rDA}$	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	20	300	
		Fast mode+		120	
		High-speed mode, $C_b = 100\text{ pF}$	10	80	
		High-speed mode, $C_b = 400\text{ pF}$	20	160	
$t_{fDA}$	Fall time of SDA signal	Standard mode		300	ns
		Fast mode	$20 \times (V_{DD} / 5.5\text{ V})$	300	
		Fast mode+	$20 \times (V_{DD} / 5.5\text{ V})$	120	
		High-speed mode, $C_b = 100\text{ pF}$	10	80	
		High-speed mode, $C_b = 400\text{ pF}$	30	160	
$t_{rCL}$	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	20	300	
		Fast mode+		120	
		High-speed mode, $C_b = 100\text{ pF}$	10	40	
		High-speed mode, $C_b = 400\text{ pF}$	20	80	
$t_{rCL1}$	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	High-speed mode, $C_b = 100\text{ pF}$	10	80	ns
		High-speed mode, $C_b = 400\text{ pF}$	20	160	
$t_{fCL}$	Fall time of a SCL signal	Standard mode		300	ns
		Fast mode	$20 \times (V_{DD} / 5.5\text{ V})$	300	
		Fast mode+	$20 \times (V_{DD} / 5.5\text{ V})$	120	
		High-speed mode, $C_b = 10 - 100\text{ pF}$	10	40	
		High-speed mode, $C_b = 400\text{ pF}$	20	80	
$C_b$	Capacitive load for each bus line (SCL and SDA)			400	pF
$t_{SP}$	Pulse width of spike suppressed (SCL and SDA spikes that are less than the indicated width are suppressed)	Standard mode, fast mode, and fast mode+		50	ns
		High-speed mode		10	

(1)  $C_b$  refers to the capacitance of one bus line.

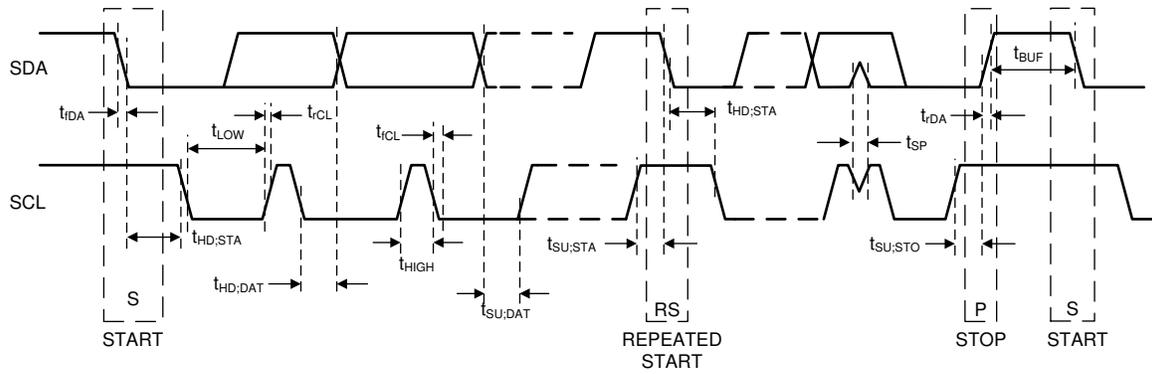
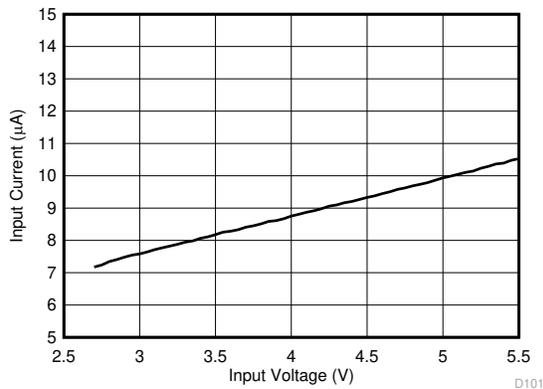


Figure 6-1. I<sup>2</sup>C-Compatible Timing

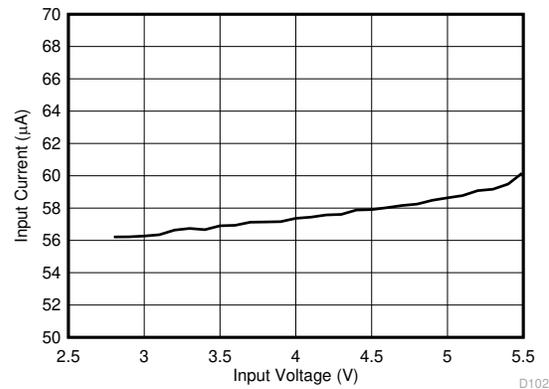
## 6.7 Typical Characteristics

Unless otherwise specified:  $V_{(VIN\_Bx)} = V_{(VIN\_LDOx)} = V_{(VANA)} = 3.7\text{ V}$ ,  $V_{OUT\_Bx} = 1\text{ V}$ ,  $V_{OUT\_LDO} = 1\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $L = 0.47\text{ }\mu\text{H}$  (TOKO DFE252012PD-R47M),  $C_{OUT\_BUCK} = 22\text{ }\mu\text{F / phase}$ ,  $C_{POL\_BUCK} = 22\text{ }\mu\text{F}$ , and  $C_{OUT\_LDO} = 1\text{ }\mu\text{F}$ .



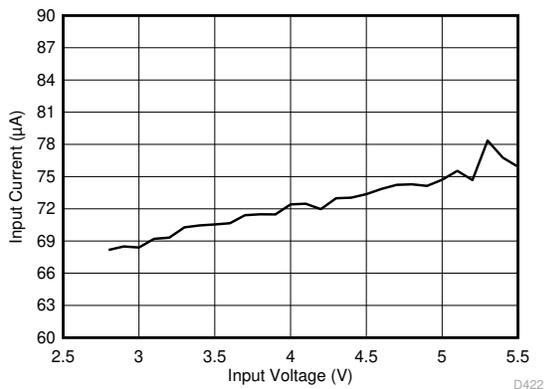
Regulators disabled

**Figure 6-2. Standby Current Consumption vs Input Voltage**



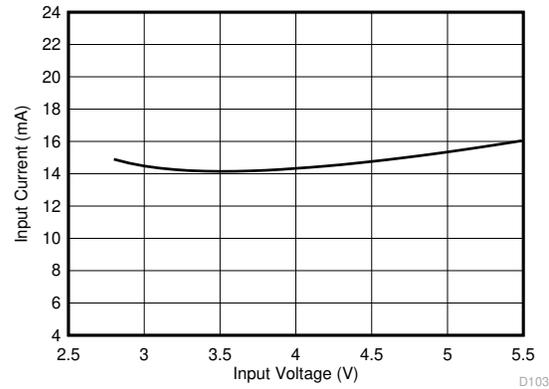
$V_{OUT\_Bx} = 1\text{ V}$  Load = 0 mA

**Figure 6-3. Active State Current Consumption vs Input Voltage, One Buck Regulator Enabled in PFM Mode (single-phase)**



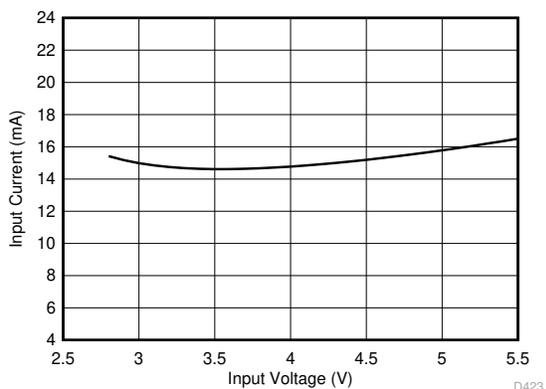
$V_{OUT\_Bx} = 1\text{ V}$  Load = 0 mA

**Figure 6-4. Active State Current Consumption vs Input Voltage, Regulator Enabled in PFM Mode (dual-phase)**



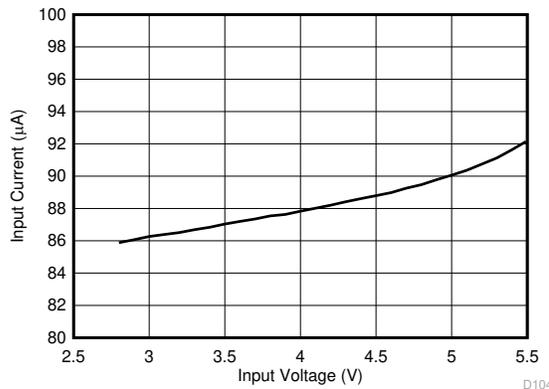
$V_{OUT\_Bx} = 1\text{ V}$  Load = 0 mA

**Figure 6-5. Active State Current Consumption vs Input Voltage, One Buck Regulator Enabled in Forced PWM Mode (single-phase)**



$V_{OUT\_Bx} = 1\text{ V}$  Load = 0 mA

**Figure 6-6. Active State Current Consumption vs Input Voltage, Regulator Enabled in Forced PWM Mode (dual-phase)**



$V_{OUT\_LDOx} = 1\text{ V}$  Load = 0 mA

**Figure 6-7. Active State Current Consumption vs Input Voltage, One LDO Regulator Enabled**

## 7 Detailed Description

### 7.1 Overview

The LP8733xx-Q1 is a high-efficiency, high-performance flexible power supply device with two step-down DC/DC converter cores (Buck0 and Buck1) and two low-dropout (LDO) linear regulators (LDO0 and LDO1) for automotive applications. The cores can be configured for a two single-phase output and dual-phase single output configuration. [Table 7-1](#) lists the output characteristics of the regulators.

**Table 7-1. Supply Specification**

SUPPLY	OUTPUT		
	V <sub>OUT</sub> RANGE (V)	RESOLUTION (mV)	I <sub>MAX</sub> MAXIMUM OUTPUT CURRENT (mA)
Buck0 (single-phase)	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3000
Buck1 (single-phase)	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3000
Buck0 and Buck1 (dual-phase)	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	6000
LDO0	0.8 to 3.3	100	300
LDO1	0.8 to 3.3	100	300

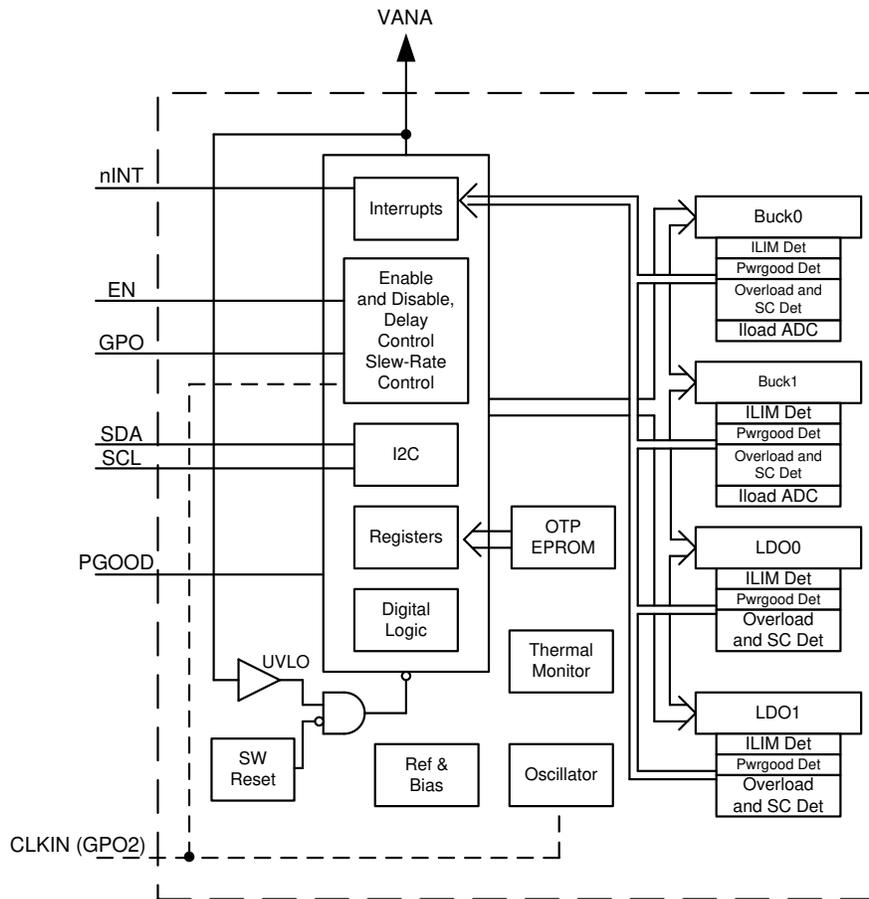
The LP8733xx-Q1 also supports switching clock synchronization to an external clock (CLKIN pin). The nominal frequency of the external clock can be from 1 MHz to 24 MHz with 1-MHz steps.

Additional features include:

- Soft-start
- Input voltage protection:
  - Undervoltage lockout
  - Overvoltage protection
- Output voltage monitoring and protection:
  - Overvoltage monitoring
  - Undervoltage monitoring
  - Overload protection
- Thermal warning
- Thermal shutdown

The LP8733xx-Q1 has one dedicated general purpose digital output (GPO) signal. The CLKIN pin can be programmed as a second GPO signal (GPO2), if the external clock is not needed. The output type (open-drain or push-pull) is programmable for the GPOs.

## 7.2 Functional Block Diagram



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## 7.3 Feature Description

### 7.3.1 DC/DC Converters

#### 7.3.1.1 Overview

The LP8733xx-Q1 includes two step-down DC/DC converter cores. The cores are designed for flexibility; most of the functions are programmable, thus giving a possibility to optimize the regulator operation for each application. The cores can be configured either for a dual-phase single output configuration or for a single-phase dual output configuration. The buck regulators deliver 0.7-V to 3.36-V regulated voltage rails from a 2.8-V to 5.5-V supply voltage.

The LP8733xx-Q1 has the following features:

- DVS support with programmable slew rate
- Automatic mode control based on the loading (PFM or PWM mode)
- Forced PWM mode option
- Optional external clock input to minimize crosstalk
- Optional spread-spectrum technique to reduce EMI
- Phase control for optimized EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Power Good flag with maskable interrupt
- Power Good signal (PGOOD) with selectable sources

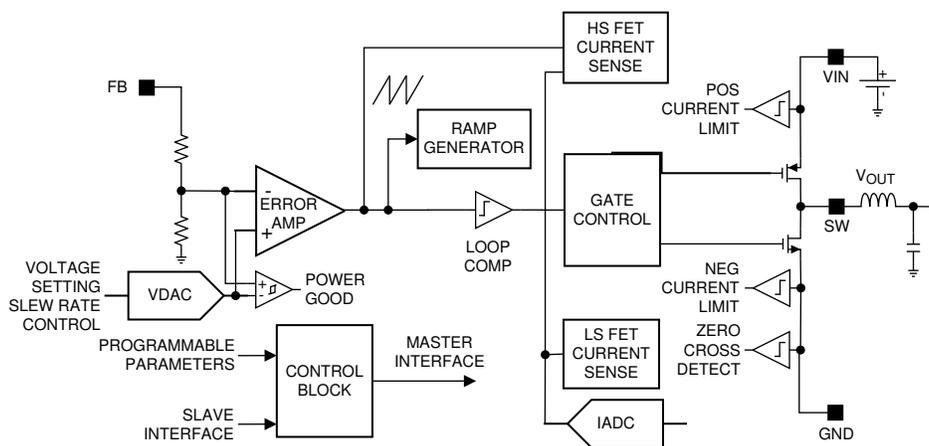
- Average output current sensing (for PFM entry, phase shedding and adding in dual-phase configuration, and load current measurement)
- Current balancing between the phases of the converter in dual-phase configuration
- Differential voltage sensing from point of the load in dual-phase configuration
- Dynamic phase shedding and adding, each output being phase shifted in dual-phase configuration

The following parameters can be programmed through the registers, the default values are set by OTP bits:

- Output voltage
- Forced PWM operation
- Forced dual-phase operation (forces also the PWM operation)
- Switch current limit
- Output voltage slew rate
- Enable and disable delays

There are two modes of operation for the buck converter, depending on the output current required: pulse-width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 600 mA or higher. When operating in PWM mode in dual-phase configuration the phases are automatically added and shedded based on the load current level. Lighter output current loads cause the converter to automatically switch into PFM mode for reduced current consumption when forced PWM mode is disabled. The forced PWM mode can be selected to maintain fixed switching frequency at all load current levels.

A block diagram of a single core is shown in [Figure 7-1](#).



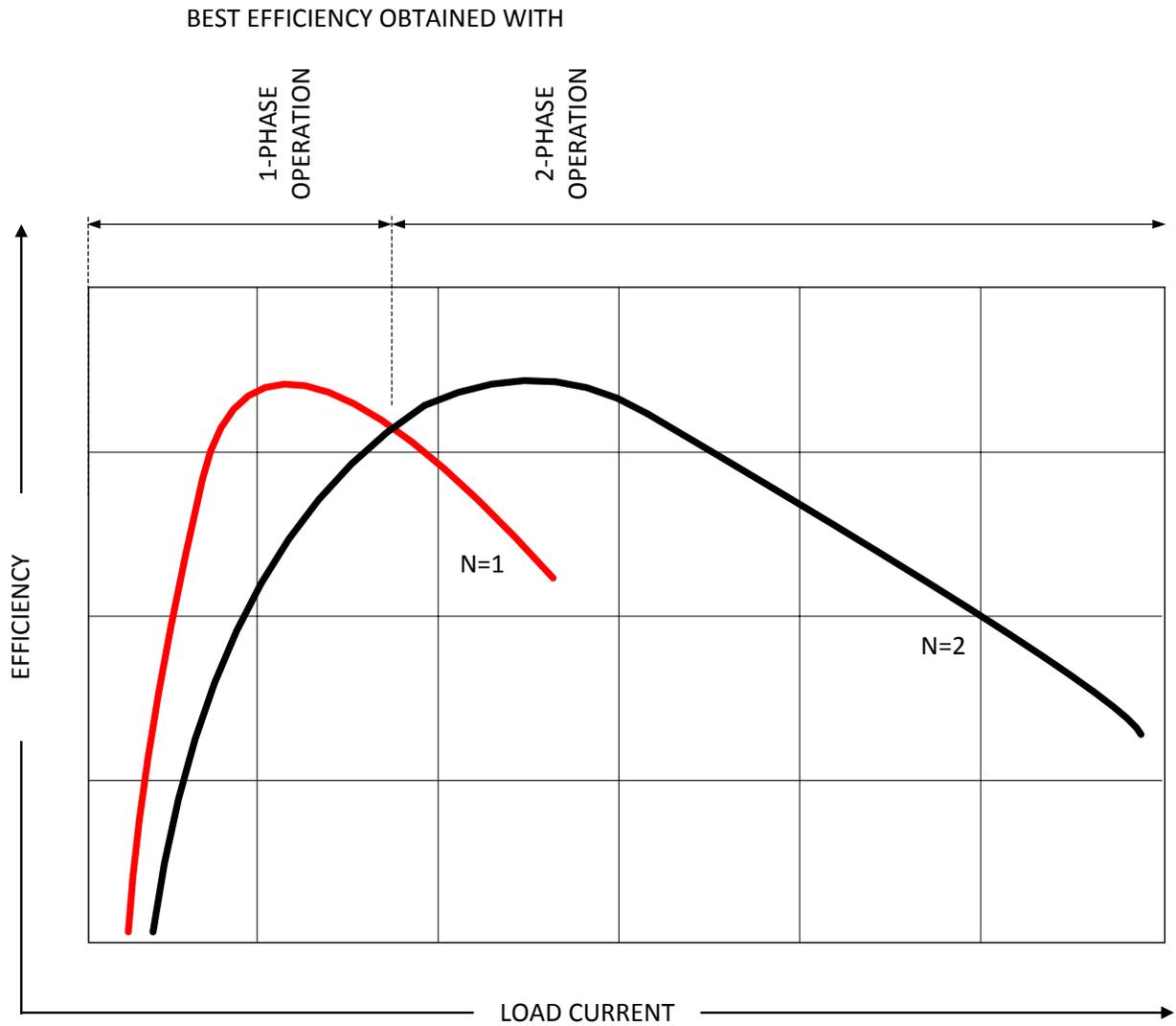
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**Figure 7-1. Detailed Block Diagram Showing One Core**

### 7.3.1.2 Dual-Phase Operation and Phase-Adding/Shedding

Under heavy load conditions, the dual-phase converter switches both channel 180° apart. As a result, the dual-phase converter has an effective ripple frequency two times greater than the switching frequency of a single phase. However, the parallel operation decreases the efficiency at light load conditions. In order to overcome this operational inefficiency, the LP8733xx-Q1 can change the number of active phases to optimize efficiency for the variations of the load. This is called phase adding and shedding. The concept is shown in [Figure 7-2](#).

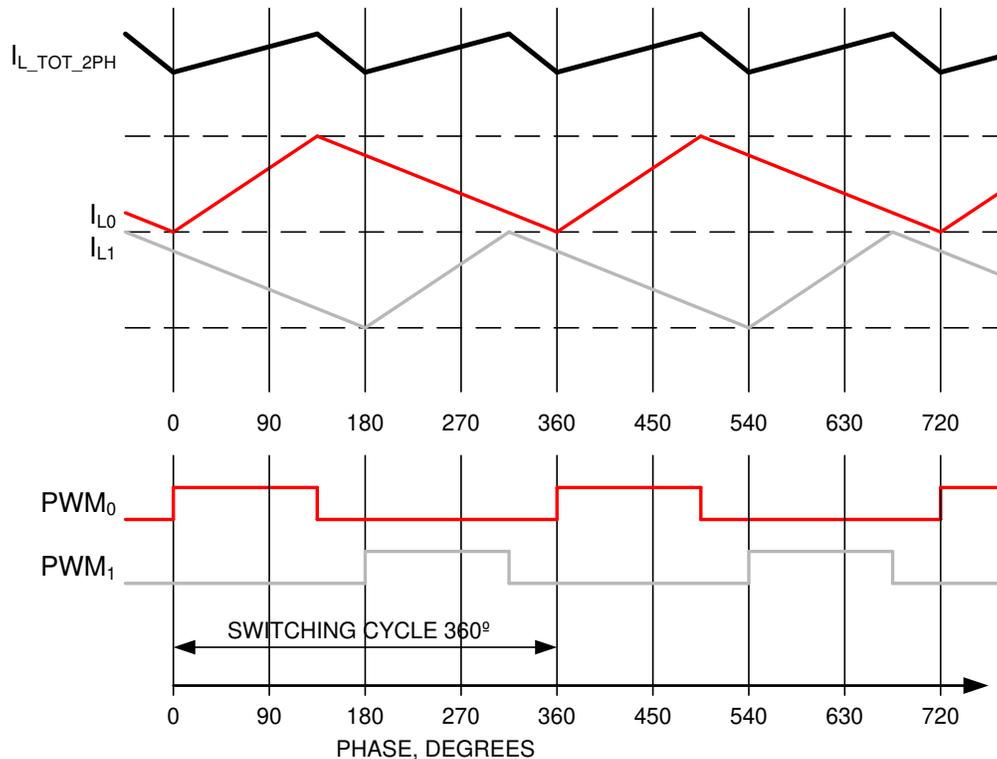
The converter can be forced to dual-phase operation by the BUCK0\_FPWM\_MP bit in the BUCK0\_CTRL\_1 register. If the regulator operates in forced dual-phase mode the forced PWM operation is automatically used. If the dual-phase operation is not forced, the number of phases are added and shedded automatically to follow the required output current.



**Figure 7-2. Multiphase Buck Converter Efficiency vs Number of Phases. All Converters in PWM mode. (UPDATE) <sup>1</sup>**

Interleaving switching action of the converters and channels in a 2-phase configuration is shown in [Figure 7-3](#).

<sup>1</sup> Graph is not in scale and is for illustrative purposes only.



**Figure 7-3. PWM Timings and Inductor Current Waveforms in 2-phase Configuration. (UPDATE) <sup>2</sup>**

### 7.3.1.3 Transition Between PWM and PFM Modes

The PWM mode operation with phase-adding and shedding optimizes efficiency at mid to full load at the expense of light-load efficiency. The LP8733xx-Q1 converter operates in the PWM mode at load current of about 600 mA or higher. At lighter load current levels the device automatically switches into the PFM mode for reduced current consumption when forced PWM mode is disabled (AUTO mode operation). By combining the PFM and the PWM modes, a high efficiency is achieved over a wide output-load current range.

### 7.3.1.4 Dual-Phase Switcher Configurations

The LP8733xx-Q1 device supports the following regulator configurations:

- Single dual-phase configuration, Buck0 is master (Buck0 and Buck1)
- Two single-phase configuration (Buck0 and Buck1)

In the dual-phase configuration the control of the dual-phase regulator settings is done using the control registers of the master buck. The following slave registers are ignored:

- The BUCK1\_CTRL\_1 (except the EN\_RDIS1 bit)
- The BUCK1\_CTRL\_2 (except the ILIM1[2:0] bits)
- The BUCK1\_VOUT
- The BUCK1\_DELAY
- The Interrupt bits related to the slave buck (except the BUCK1\_ILIM\_INT)

### 7.3.1.5 Buck Converter Load Current Measurement

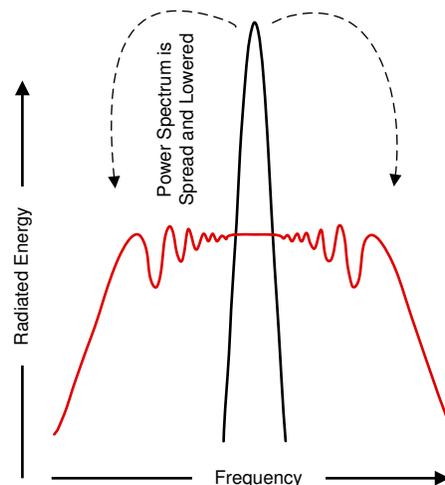
The buck load current can be monitored through I<sup>2</sup>C registers. The monitored buck converter is selected with the LOAD\_CURRENT\_BUCK\_SELECT bit in the SEL\_I\_LOAD register. A write to this selection register starts a current measurement sequence. The regulator is automatically forced to the PWM mode for the measurement period. The measurement sequence is 50  $\mu$ s long, maximum.

<sup>2</sup> Graph is not in scale and is for illustrative purposes only.

The LP8733xx-Q1 device can be configured to give out an interrupt (the I\_MEAS\_INT bit in the INT\_TOP\_1 register) after the load current measurement sequence is finished. The load current measurement interrupt can be masked with the I\_MEAS\_MASK bit (TOP\_MASK\_1 register). The measurement result can be read from the registers I\_LOAD\_1 and I\_LOAD\_2. The register I\_LOAD\_1 bits BUCK\_LOAD\_CURRENT[7:0] gives out the LSB bits, and the register I\_LOAD\_2 bit BUCK\_LOAD\_CURRENT[8] gives out the MSB bit. The measurement result BUCK\_LOAD\_CURRENT[8:0] LSB is 20 mA, and the maximum code value of the measurement corresponds to 10.22 A. In dual-phase configuration, the measured current is the total value of the master and slave phases.

### 7.3.1.6 Spread-Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP8733xx-Q1 has a register-selectable spread-spectrum mode which minimizes the need for output filters, ferrite beads, or chokes. In spread spectrum mode, the switching frequency varies around the center frequency, reducing the EMI emissions radiated by the converter and associated passive components and PCB traces (see [Figure 7-4](#)). Spread-spectrum mode is only available when an internal RC oscillator is used (EN\_PLL bit is 0 in PLL\_CTRL register), it is enabled with the EN\_SPREAD\_SPEC bit in the CONFIG register, and it affects both buck cores.



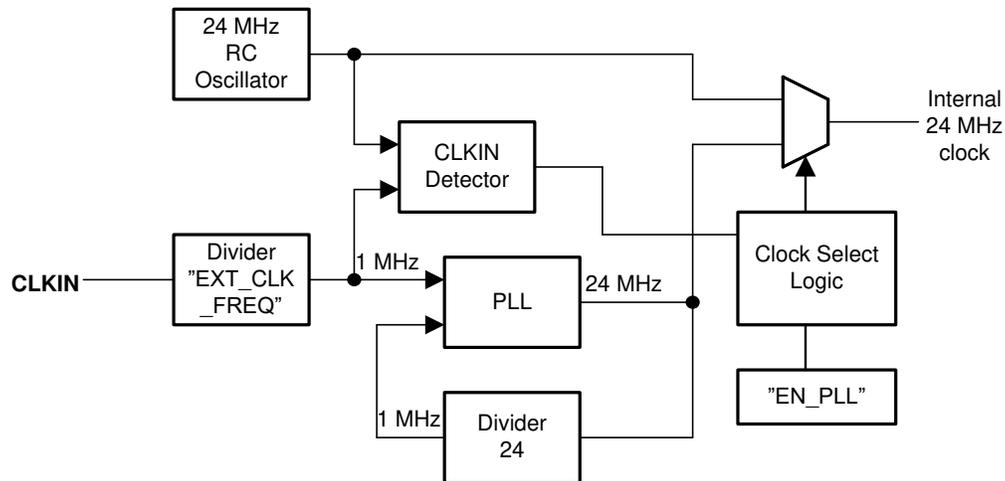
Where a fixed frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP8733xx-Q1 spreads that energy over a large bandwidth.

**Figure 7-4. Spread-Spectrum Modulation**

### 7.3.2 Sync Clock Functionality

The LP8733xx-Q1 device contains a CLKIN input to synchronize the switching clock of the buck regulators with the external clock. The block diagram of the clocking and PLL module is shown in [Figure 7-5](#). Depending on the EN\_PLL bit in the PLL\_CTRL register and the external clock availability, the external clock is selected and interrupt is generated as shown in [Table 7-2](#). The interrupt can be masked with the SYNC\_CLK\_MASK bit in the TOP\_MASK\_1 register. The nominal frequency of the external input clock is set by the EXT\_CLK\_FREQ[4:0] bits in the PLL\_CTRL register, and it can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–30%/+10%) of the selected frequency for valid clock detection.

The SYNC\_CLK\_INT interrupt in the INT\_TOP\_1 register is also generated in cases where the external clock is expected but is not available. These cases occur when EN\_PLL is 1 during start-up (read OTP-to-standby transition) and during Buck regulator enable (standby-to-active transition).



**Figure 7-5. Clock and PLL Module**

**Table 7-2. PLL Operation**

DEVICE OPERATION MODE	EN_PLL	PLL AND CLOCK DETECTOR STATE	INTERRUPT FOR EXTERNAL CLOCK	CLOCK
STANDBY	0	Disabled	No	Internal RC
ACTIVE	0	Disabled	No	Internal RC
STANDBY	1	Enabled	When external clock appears or disappears	Automatic change to external clock when available
ACTIVE	1	Enabled	When external clock appears or disappears	Automatic change to external clock when available

### 7.3.3 Low-Dropout Linear Regulators (LDOs)

The LP8733xx-Q1 device includes two identical linear regulators, LDO0 and LDO1, which target analog loads with low noise requirements. The LDO regulators deliver 0.8-V to 3.3-V regulated voltage rails from a 2.5-V to 5.5-V input voltage. Both regulators have dedicated inputs which can be higher or lower than the device system voltage  $V_{(VANA)}$  to minimize the power dissipation.

### 7.3.4 Power-Up

The power-up sequence for the LP8733xx-Q1 is as follows:

- The VANA and VIN\_Bx reach minimum recommended levels ( $V_{VANA} > VANA_{UVLO}$ ). This initiates power-on-reset (POR), OTP reading, and enables the system I/O interface. The I<sup>2</sup>C host should allow at least 1.2 ms before writing or reading data to the LP8733xx-Q1.
- The device enters standby mode.
- The host can change the default register setting by I<sup>2</sup>C if needed.
- The regulators can be enabled and disabled.
- The GPO signals can be controlled by the EN pin and the I<sup>2</sup>C interface.

Transitions between the operating modes are shown in [Section 7.4.1](#).

## 7.3.5 Regulator Control

### 7.3.5.1 Enabling and Disabling Regulators

The regulators can be enabled when the device is in STANDBY or ACTIVE state. There are two ways to enable and disable the buck regulators:

- Using the BUCKx\_EN bit in the BUCKx\_CTRL\_1 register (the BUCKx\_EN\_PIN\_CTRL bit is 0 in the BUCKx\_CTRL\_1 register).
- Using the EN control pin (the BUCKx\_EN bit *and* the BUCKx\_EN\_PIN\_CTRL bit is 1).

Similarly, there are two ways to enable and disable the LDO regulators:

- Using the LDOx\_EN bit in the LDOx\_CTRL register (the LDOx\_EN\_PIN\_CTRL bit is 0 in the LDOx\_CTRL register).
- Using the EN control pin (the LDOx\_EN bit is 1 *and* the LDOx\_EN\_PIN\_CTRL bit is 1).

If the EN control pin is used for enable and disable, then the following occurs:

- The delay from the control signal rising edge to start-up is set by the BUCKx\_STARTUP\_DELAY[3:0] bits in the BUCKx\_DELAY register and the LDOx\_STARTUP\_DELAY[3:0] bits in the LDOx\_DELAY register.
- The delay from the control signal falling edge to shutdown is set by the BUCKx\_SHUTDOWN\_DELAY[3:0] bits in the BUCKx\_DELAY register and the LDOx\_SHUTDOWN\_DELAY[3:0] bits in the LDOx\_DELAY register.

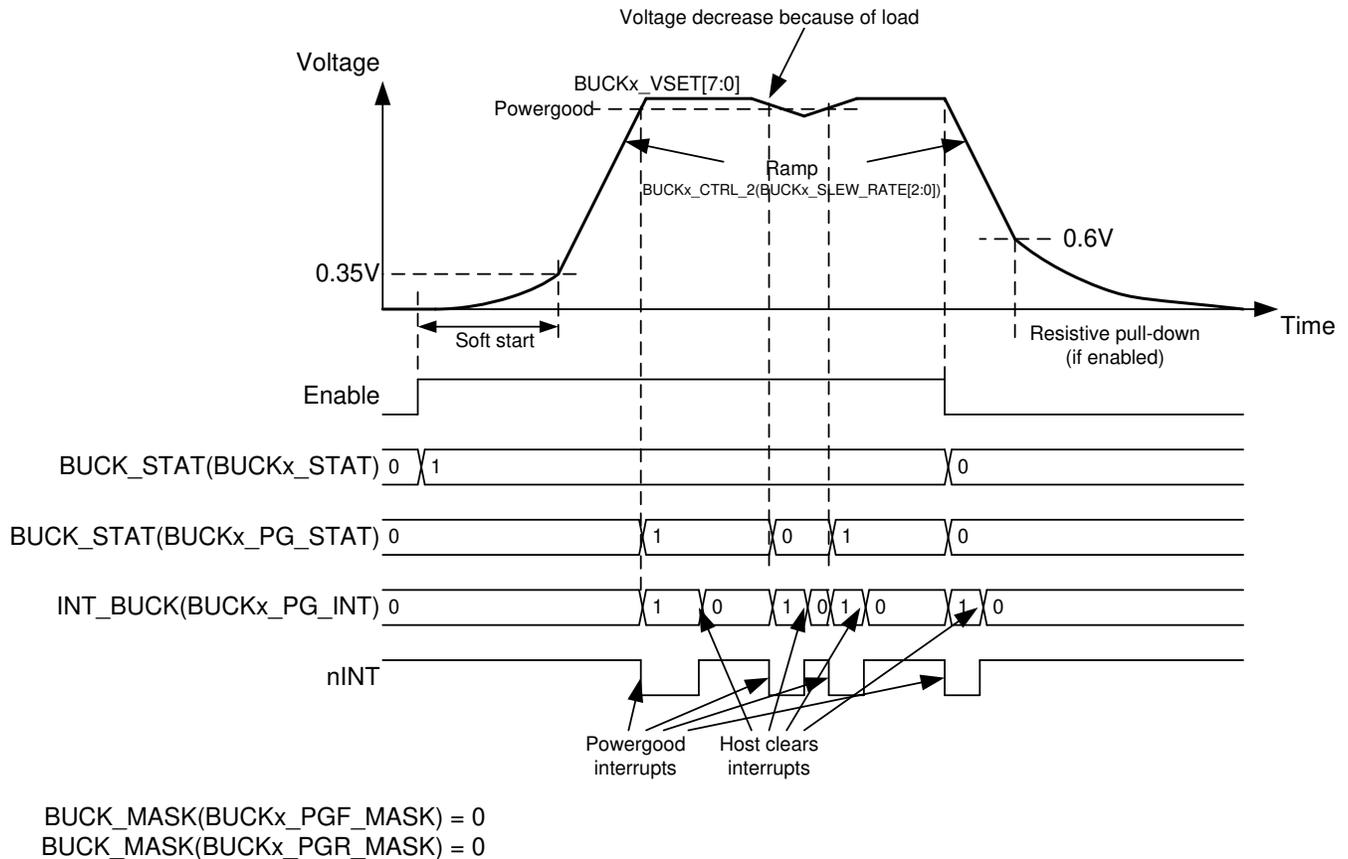
The delays are only valid for the EN signal transitions and not for control with I<sup>2</sup>C writings to the BUCKx\_EN and the LDOx\_EN bits.

The control of the regulator (with 0-ms delays) is shown in [Table 7-3](#). Dual-phase regulator is controlled with registers of the master phase.

**Table 7-3. Regulator Control**

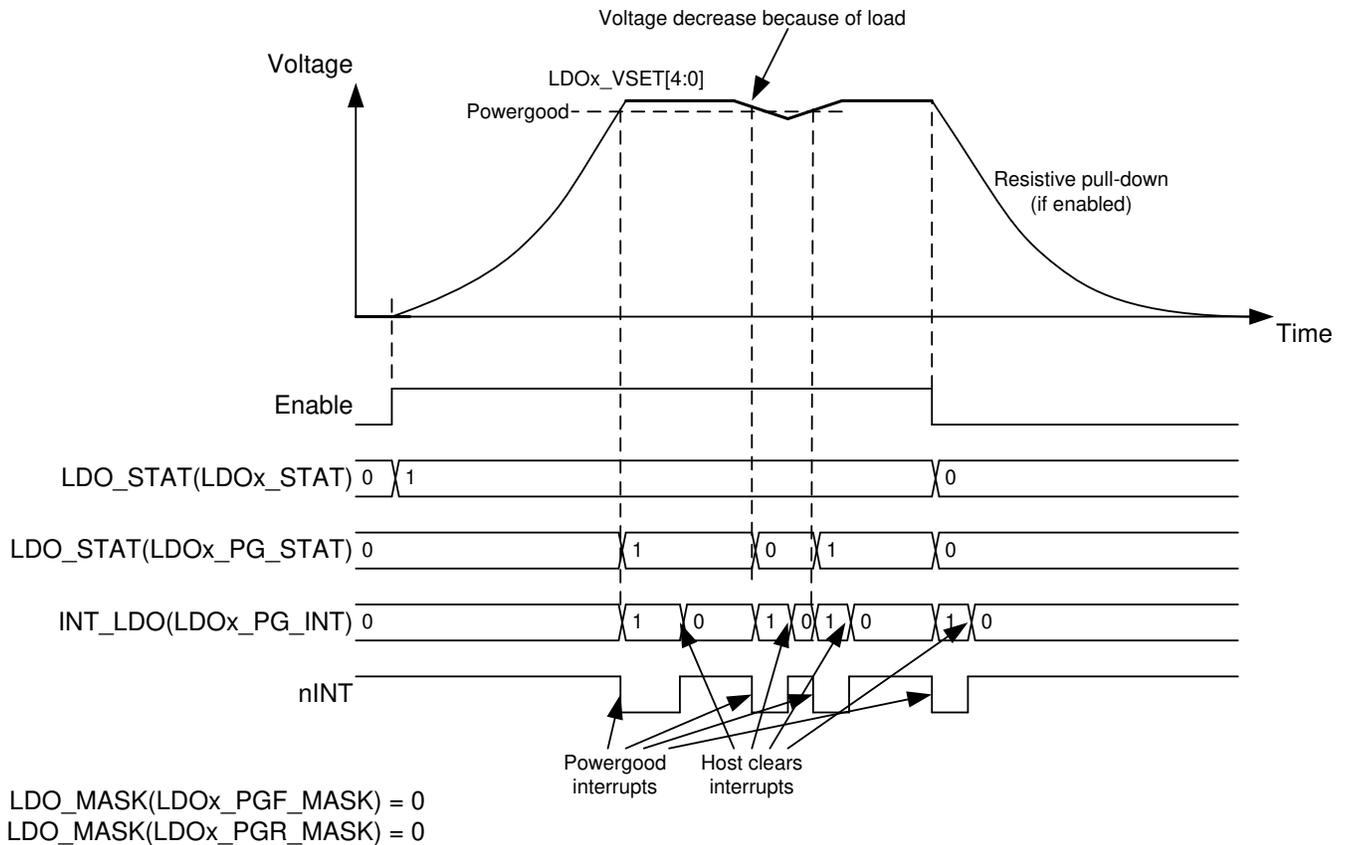
	BUCKx_EN AND LDOx_EN	BUCKx_EN_PIN_CTRL AND LDOx_EN_PIN_CTRL	EN PIN	BUCKx OUTPUT VOLTAGE AND LDOx OUTPUT VOLTAGE
Enable and disable control with the BUCKx_EN and the LDOx_EN bit	0	Don't Care	Don't Care	Disabled
	1	0	Don't Care	BUCKx_VSET[7:0] and LDOx_VSET[4:0]
Enable and disable control with the EN pin	1	1	Low	Disabled
	1	1	High	BUCKx_VSET[7:0] and LDOx_VSET[4:0]

The buck regulator is enabled by the EN pin or by I<sup>2</sup>C writing, as shown in [Figure 7-6](#). The soft-start circuit limits the in-rush current during start-up. When the output voltage rises to a 0.35-V level, the output voltage becomes slew-rate controlled. If there is a short circuit at the output, and the output voltage does not increase above the 0.35-V level in 1 ms or the output voltage drops below 0.35-V level during operation (for minimum of 1 ms), then the regulator is disabled, and the BUCKx\_SC\_INT interrupt in the INT\_BUCK register is set. When the output voltage reaches the the Power-Good threshold level, the BUCKx\_PG\_INT interrupt flag in the INT\_BUCK register is set. The Power-Good interrupt flag, when reaching the valid output voltage, can be masked using the BUCKx\_PGR\_MASK bit in the BUCK\_MASK register. The Power-Good interrupt flag can also be generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by the BUCKx\_PGF\_MASK bit in the BUCK\_MASK register. A BUCKx\_PG\_STAT bit in the BUCK\_STAT register always shows the validity of the output voltage; 1 means valid and 0 means invalid output voltage. A PGOOD\_WINDOW\_BUCK bit in the PGOOD\_CTRL\_1 register sets the detection method for the valid buck output voltage, either under-voltage detection, or under-voltage and over-voltage detection.



**Figure 7-6. Buck Regulator Enable and Disable**

The LDO regulator is enabled by the EN pin or by I<sup>2</sup>C writing, as shown in [Figure 7-7](#). The soft-start circuit limits the in-rush current during start-up. The output voltage increase rate is less than 100 mV/μsec during soft-start. If there is a short circuit at the output, and the output voltage does not increase above the 0.3-V level in 1 ms or the output voltage drops below 0.3-V level during operation (for minimum of 1 ms), then the regulator is disabled, and the LDOx\_SC\_INT interrupt in the INT\_LDO register is set. When the output voltage reaches the Power-Good threshold level, the LDOx\_PG\_INT interrupt flag in the INT\_LDO register is set. The Power-Good interrupt flag, when reaching valid output voltage, can be masked using the LDOx\_PGR\_MASK bit in the LDO\_MASK register. The Power-Good interrupt flag can also be generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by the LDOx\_PGF\_MASK bit in the LDO\_MASK register. A LDOx\_PG\_STAT bit in the LDO\_STAT register always shows the validity of the output voltage; 1 means valid, and 0 means invalid output voltage. A PGOOD\_WINDOW\_LDO bit in the PGOOD\_CTRL\_1 register sets the detection method for the valid LDO output voltage, either undervoltage detection or undervoltage and overvoltage detection.



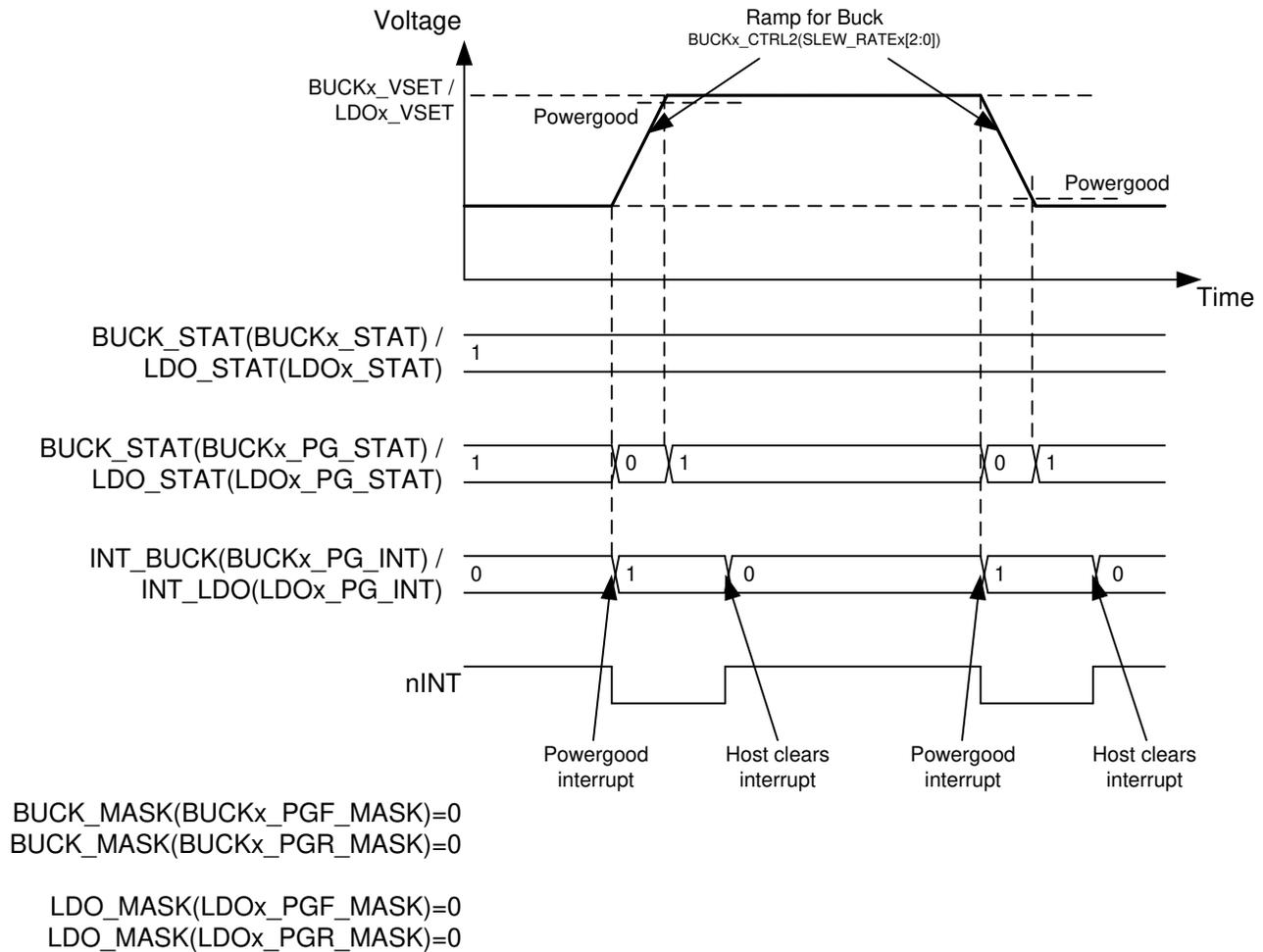
**Figure 7-7. LDO Regulator Enable and Disable**

The EN input pin has an integrated pulldown resistor. The pulldown resistor is controlled with the EN\_PD bit in the CONFIG register.

### 7.3.5.2 Changing Output Voltage

The output voltage of the regulator can be changed by writing to the BUCKx\_VOUT and LDOx\_VOUT register. The voltage change for the buck regulator is always slew-rate controlled, and the slew-rate is defined by the BUCKx\_SLEW\_RATE[2:0] bits in the BUCKx\_CTRL\_2 register. During voltage change, the forced PWM mode is used automatically. If the dual-phase operation is forced by the BUCK0\_FPWM\_MP bit in the BUCK0\_CTRL\_1 register, the regulator operates in dual-phase mode. If the dual-phase operation is not forced, the number of phases are added and shedded automatically to follow the required slew rate. When the programmed output voltage is achieved, the mode becomes the one defined by the load current, the BUCKx\_FPWM bit in the BUCKx\_CTRL\_1 register, and the BUCK0\_FPWM\_MP bit.

The voltage change and Power-Good interrupts are shown in [Figure 7-8](#).



**Figure 7-8. Regulator Output Voltage Change**

During an LDO voltage change, the internal reference for the Power-Good detection is also changed. For this reason when the output voltage is changing, toggling of the Power-Good signal may still indicate a valid output. This period takes less than 100  $\mu$ s and after that time the Power-Good gives correct value.

### 7.3.6 Enable and Disable Sequences

The LP8733xx-Q1 device supports start-up and shutdown sequencing with programmable delays for different regulator outputs using a single EN control signal. The Buck regulator is selected for delayed control with:

- The BUCKx\_EN = 1 in the BUCKx\_CTRL\_1 register
- The BUCKx\_EN\_PIN\_CTRL = 1 in the BUCKx\_CTRL\_1 register
- The BUCKx\_VSET[7:0] bits in the BUCKx\_VOUT register defines the voltage when the EN pin is high
- The delay from the rising edge of the EN pin to the regulator enable is set by the BUCKx\_STARTUP\_DELAY[3:0] bits in the BUCKx\_DELAY register.
- The delay from the falling edge of the EN pin to the regulator disable is set by the BUCKx\_SHUTDOWN\_DELAY[3:0] bits in the BUCKx\_DELAY register.

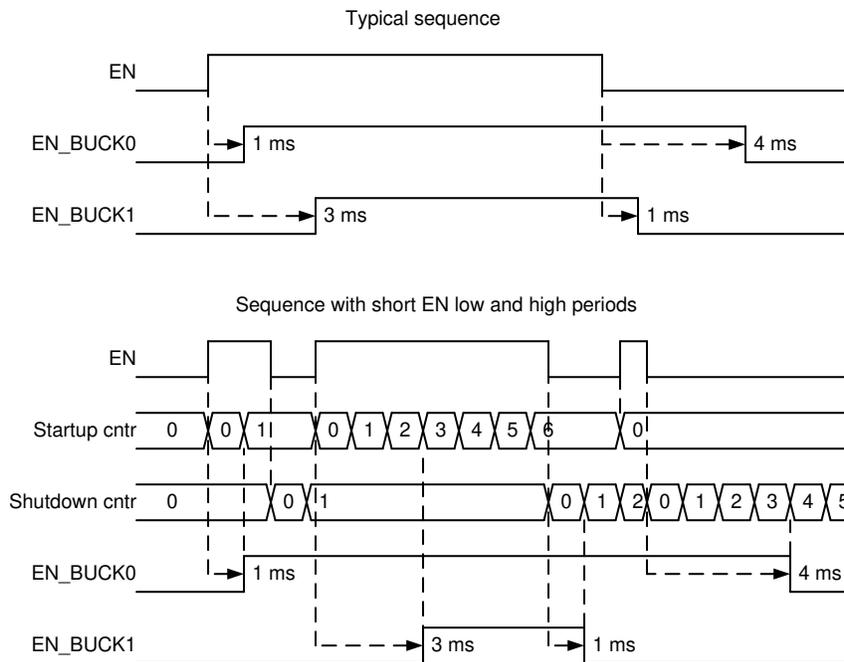
In the same way, the LDO regulator is selected for delayed control with:

- The LDOx\_EN = 1 in the LDOx\_CTRL register
- The LDOx\_EN\_PIN\_CTRL = 1 in the LDOx\_CTRL register
- The LDOx\_VSET[4:0] bits in the LDOx\_VOUT register defines the voltage when the EN pin is high
- The delay from the rising edge of the EN pin to the regulator enable is set by the LDOx\_STARTUP\_DELAY[3:0] bits in the LDOx\_DELAY register.
- The delay from the falling edge of the EN pin to the regulator disable is set by the LDOx\_SHUTDOWN\_DELAY[3:0] bits in the LDOx\_DELAY register.

The GPO and GPO2 digital output signals can be also controlled as a part of start-up and shutdown sequencing with the following settings:

- GPOx\_EN = 1 in GPO\_CTRL register
- GPOx\_EN\_PIN\_CTRL = 1 in GPO\_CTRL register
- The delay from the rising edge of the EN pin to the rising edge of the GPO or GPO2 signal is set by the GPOx\_STARTUP\_DELAY[3:0] bits in the GPOx\_DELAY register.
- The delay from the falling edge of the EN pin to the falling edge of the GPO or GPO2 signal is set by the GPOx\_SHUTDOWN\_DELAY[3:0] bits in the GPOx\_DELAY register.

An example of the start-up and shutdown sequences for the buck regulators are shown in [Figure 7-9](#). The start-up and shutdown delays for the Buck0 regulator are 1 ms and 4 ms, and for the Buck1 regulator the start-up and shutdown delays are 3 ms and 1 ms. The delay settings are only used for enable or disable control with the EN signal.



**Figure 7-9. Start-Up and Shutdown Sequencing**

### 7.3.7 Device Reset Scenarios

There are two reset methods implemented on the LP8733xx-Q1:

- Software reset with the SW\_RESET bit in the RESET register.
- Undervoltage lockout (UVLO) reset from the VANA supply.

An software reset occurs when 1 is written to the SW\_RESET bit. The bit is automatically cleared after writing. This event disables all the regulators immediately, drives the GPO or GPO2 signals low, resets all the register bits to the default values, and loads the OTP bits (see [Figure 7-15](#)). The I<sup>2</sup>C interface is not reset during a software reset.

If the VANA supply voltage falls below the UVLO threshold level, then all the regulators are disabled immediately, the GPO or GPO2 signals are driven low, and all the register bits are reset to the default values. When the VANA supply voltage transitions above the UVLO threshold level, an internal POR occurs. The OTP bits are loaded to the registers and a startup is initiated according to the register settings.

### 7.3.8 Diagnosis and Protection Features

The LP8733xx-Q1 is capable of providing four levels of protection features:

- Information of valid regulator output voltage, which sets the interrupt or PGOOD signal.
- Warnings for diagnosis, which sets the interrupt.
- Protection events, which are disabling the regulators.
- Faults, which are causing the device to shutdown.

The LP8733xx-Q1 sets the flag bits indicating what protection or warning conditions have occurred, and the nINT pin is pulled low. The nINT is released again after a clear of flags is complete. The nINT signal stays low until all the pending interrupts are cleared.

When a fault is detected or software requested reset, it is indicated by a RESET\_REG\_INT interrupt flag in the INT\_TOP\_2 register after next start-up. If the RESET\_REG\_MASK is set to masked in the OTP, then the interrupt is not generated. The mask bit change with I<sup>2</sup>C does not affect, because the RESET\_REG\_MASK bit is loaded from the OTP during reset sequence.

**Table 7-4. Summary of Interrupt Signals**

EVENT	DEVICE RESPONSE	INTERRUPT BIT	INTERRUPT MASK BIT	STATUS BIT	RECOVERY AND INTERRUPT CLEAR
Buck current limit triggered	No effect	BUCK_INT BUCKx_ILIM_INT	BUCKx_ILIM_MASK	BUCKx_ILIM_STAT	Write 1 to the BUCKx_ILIM_INT bit. Interrupt is not cleared if the current limit is active
LDO current limit triggered	No effect	LDO_INT LDOx_ILIM_INT	LDOx_ILIM_MASK	LDOx_ILIM_STAT	Write 1 to the LDOx_ILIM_INT bit Interrupt is not cleared if the current limit is active
Buck short circuit ( $V_{VOUT} < 0.35$ V at 1 ms after enable) or overload ( $V_{VOUT}$ decreasing below 0.35 V during operation, 1-ms debounce)	Regulator disable	BUCK_INT BUCKx_SC_INT	N/A	N/A	Write 1 to the BUCKx_SC_INT bit
LDO short circuit ( $V_{VOUT} < 0.3$ V at 1 ms after enable) or overload ( $V_{VOUT}$ decreasing below 0.3 V during operation, 1-ms debounce)	Regulator disable	LDO_INT LDOx_SC_INT	N/A	N/A	Write 1 to the LDOx_SC_INT bit
Thermal warning	No effect	TDIE_WARN_INT	TDIE_WARN_MASK	TDIE_WARN_STAT	Write 1 to the TDIE_WARN_INT bit Interrupt is not cleared if the temperature is above the thermal warning level
Thermal shutdown	All the regulators are disabled immediately, and the GPO and GPO2 are set to low	TDIE_SD_INT	N/A	TDIE_SD_STAT	Write 1 to the TDIE_SD_INT bit Interrupt is not cleared if the temperature is above the thermal shutdown level
VANA overvoltage ( $VANA_{OVP}$ )	All the regulators are disabled immediately, and the GPO and GPO2 are set to low	OVP_INT	N/A	OVP_STAT	Write 1 to the OVP_INT bit Interrupt is not cleared if the VANA voltage is above the $VANA_{OVP}$ level
Buck power good, output voltage becomes valid	No effect	BUCK_INT BUCKx_PG_INT	BUCKx_PGR_MASK	BUCKx_PG_STAT	Write 1 to the BUCKx_PG_INT bit
Buck power good, output voltage becomes invalid	No effect	BUCK_INT BUCKx_PG_INT	BUCKx_PGF_MASK	BUCKx_PG_STAT	Write 1 to the BUCKx_PG_INT bit
LDO Power good, output voltage becomes valid	No effect	LDO_INT LDOx_PG_INT	LDOx_PGR_MASK	LDOx_PG_STAT	Write 1 to the LDOx_PG_INT bit
LDO power good, output voltage becomes invalid	No effect	LDO_INT LDOx_PG_INT	LDOx_PGF_MASK	LDOx_PG_STAT	Write 1 to the LDOx_PG_INT bit
PGOOD pin changing from active to inactive state <sup>(1)</sup>	No effect	PGOOD_INT	PGOOD_MASK	PGOOD_STAT	Write 1 to the PGOOD_INT bit
External clock appears or disappears	No effect to regulators	SYNC_CLK_INT <sup>(2)</sup>	SYNC_CLK_MASK	SYNC_CLK_STAT	Write 1 to the SYNC_CLK_INT bit
Load current measurement is ready	No effect	I_MEAS_INT	I_MEAS_MASK	N/A	Write 1 to the I_MEAS_INT bit
Supply voltage $VANA_{UVLO}$ triggered (VANA falling)	Immediate shutdown and the registers reset to default values	N/A	N/A	N/A	N/A
Supply voltage $VANA_{UVLO}$ triggered (VANA rising)	Startup and the registers reset to default values and the OTP bits are loaded	RESET_REG_INT	RESET_REG_MASK	N/A	Write 1 to the RESET_REG_INT bit
Software requested reset	Immediate shutdown is followed by power up and the registers are reset to their default values	RESET_REG_INT	RESET_REG_MASK	N/A	Write 1 to the RESET_REG_INT bit

- (1) The PGOOD\_STAT bit is 1 when the PGOOD pin shows valid voltages. The PGOOD\_POL bit in the PGOOD\_CTRL\_1 register affects only the PGOOD pin polarity, not the Power Good and PGOOD\_INT interrupt polarity.
- (2) If the clock is not available when the clock detector is enabled, then an interrupt is generated during the clock-detector operation.

### 7.3.8.1 Power-Good Information (PGOOD pin)

In addition to the interrupt-based indication of the current limit and the Power-Good level, the LP8733xx-Q1 device supports monitoring with PGOOD signal:

- Regulator output voltage
- Input supply overvoltage
- Thermal warning
- Thermal shutdown

The regulator output voltage monitoring (not current limit monitoring) can be selected for the PGOOD indication. This selection is individual for both buck regulators (only master buck in dual-phase configuration) and LDO regulators, and is set by the EN\_PGOOD\_BUCKx bits in the PGOOD\_CTRL\_1 register and the EN\_PGOOD\_LDOx bits in the PGOOD\_CTRL\_1 register. When a regulator is disabled, the monitoring is automatically masked to prevent it forcing the PGOOD inactive. A thermal warning can also be selected for the PGOOD indication with the EN\_PGOOD\_TWARN bit in the PGOOD\_CTRL\_2 register. The monitoring from all the output rails, thermal warning (TDIE\_WARN\_STAT), input overvoltage interrupt (OVP\_INT), and thermal shutdown interrupt (TDIE\_SD\_INT) are combined, and the PGOOD pin is active only if all the selected sources shows a valid status.

The type of output voltage monitoring for the PGOOD signal is selected by the PGOOD\_WINDOW\_x bits in the PGOOD\_CTRL\_1 register. If the bit is 0, only undervoltage is monitored; if the bit is 1, both undervoltage and overvoltage are monitored.

The polarity and the output type (push-pull or open-drain) are selected by the PGOOD\_POL and PGOOD\_OD bits in the PGOOD\_CTRL\_1 register.

The PGOOD is only *active* and *asserted* when all enabled power resource output voltages are within specified tolerance for each requested and programmed output voltage.

The PGOOD is *inactive* and *de-asserted* if any enabled power resource output voltages is outside specified tolerance for each requested and programmed output voltage.

The device OTP setting selects either gated (or *unusual*) or continuous (or *invalid*) mode of operation.

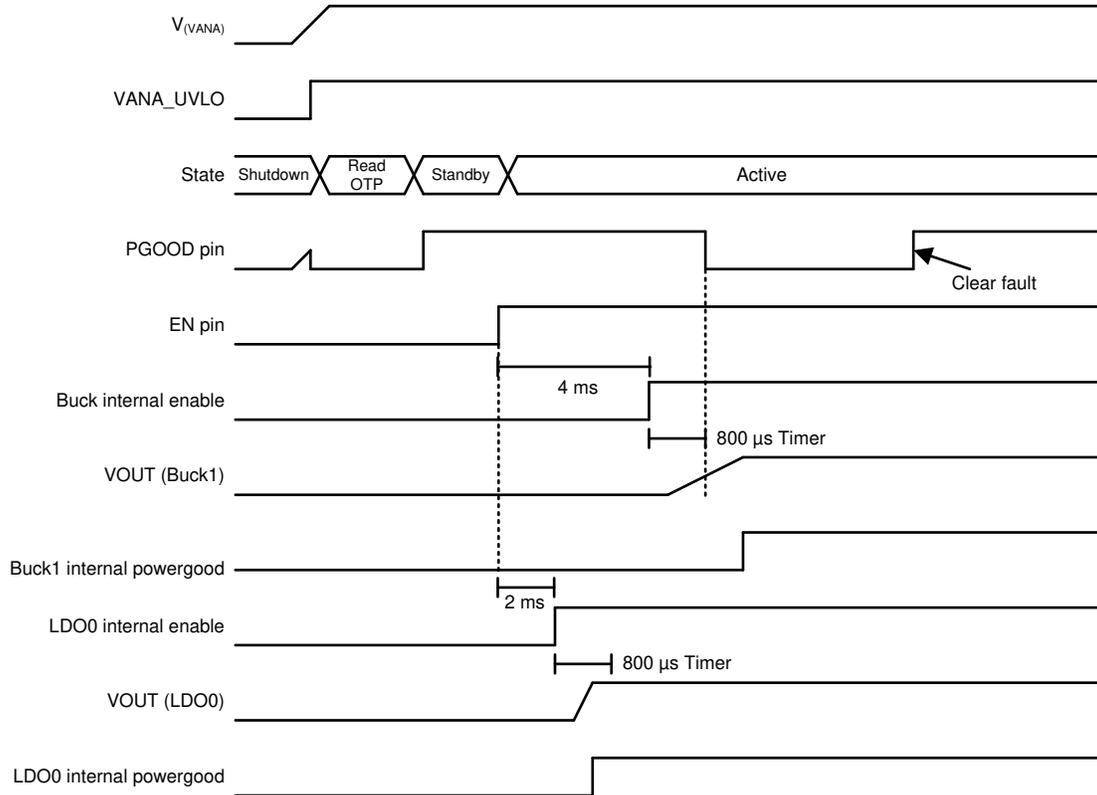
#### 7.3.8.1.1 PGOOD Pin Gated Mode

The gated (or *unusual*) mode of operation is selected by setting the PGOOD\_MODE bit to 0 in the PGOOD\_CTRL\_2 register.

For the gated mode of operation, the PGOOD behaves as follows:

- PGOOD is set to *active* or *asserted* state upon exiting the OTP configuration as an initial default state.
- PGOOD status is suspended or unchanged during an 800- $\mu$ s gated time period, thereby *gating-off* the status indication.
- During normal power-up sequencing and requested voltage changes, the PGOOD state is not changed during an 800- $\mu$ s gated time period. It typically remains *active* or *asserted* for normal conditions.
- During an *abnormal* power-up sequencing and requested voltage changes, the PGOOD status could change to *inactive* or *de-asserted* after an 800- $\mu$ s gated time period if any output voltage is outside of regulation range.
- Using the *gated mode of operation* could allow the PGOOD signal to initiate an immediate power shutdown sequence if the PGOOD signal is wired-OR with signal connected to the EN input. This type of circuit configuration provides a smart PORz function for processor that eliminates the need for additional components to generate PORz upon start-up and to monitor voltage levels of key voltage domains.

Each detected fault sets the correcting fault bit in the PG\_FAULT register to 1. The detected fault must be cleared to continue the PGOOD monitoring. The overvoltage and thermal shutdown are cleared by writing 1 to the OVP\_INT and TDIE\_SD\_INT interrupt bits in the INT\_TOP\_1 register. The regulator fault is cleared by writing 1 to the corresponding register bit in the PG\_FAULT register. The interrupts can also be cleared with the VANA UVLO by toggling the input supply. An example of the PGOOD pin operation in gated mode is shown in [Figure 7-10](#).



**Figure 7-10. PGOOD Pin Operation in Gated Mode**

#### 7.3.8.1.2 PGOOD Pin Continuous Mode

The continuous (or *invalid*) mode of operation is selected by setting the PGOOD\_MODE bit to 1 in the PGOOD\_CTRL\_2 register.

For the continuous mode of operation, PGOOD behaves as follows:

- PGOOD is set to *active* or *asserted* state upon exiting OTP configuration.
- PGOOD is set to *inactive* or *de-asserted* as soon as the regulator is enabled.
- PGOOD status begins indicating output voltage regulation status immediately and continuously.
- During power-up sequencing and requested voltage changes, PGOOD will toggle between *inactive* or *de-asserted* while output voltages are outside of regulation ranges and *active* or *asserted* when inside of regulation ranges.

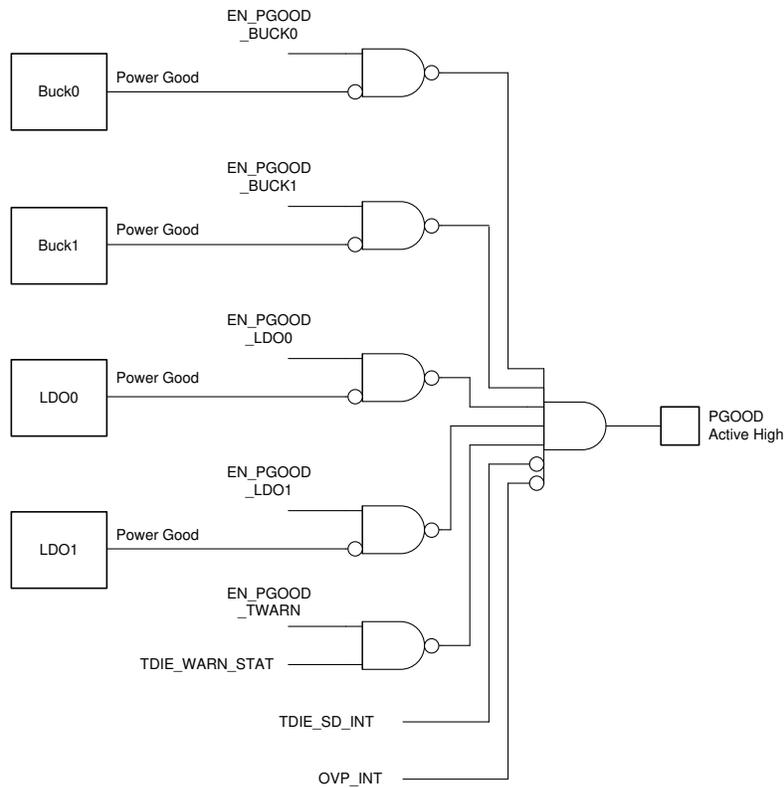
The PG\_FAULT register bits are latched, and maintain the fault information until the host clears the fault bit by writing 1 to the bit. The PGOOD signal also indicates a thermal shutdown and input overvoltage interrupts, which are cleared by clearing the interrupt bits.

When the regulator voltage is transitioning from one target voltage to another, the PGOOD signal becomes inactive.

#### 7.3.8.1.3 PGOOD Pin Inactive Mode

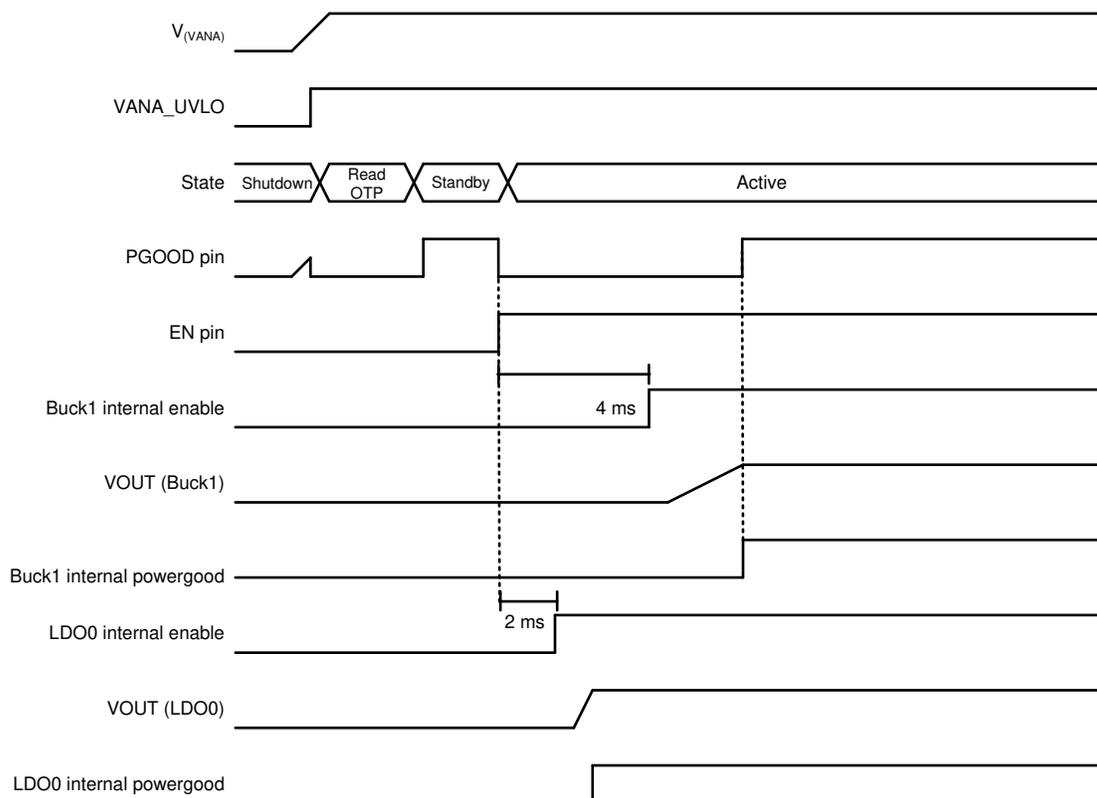
When the PGOOD signal becomes inactive, the source for the fault can be read from the PG\_FAULT register. If the invalid output voltage becomes valid again, then the PGOOD signal becomes active. Thus the PGOOD signal always shows if the monitored output voltages are valid. The block diagram for this operation is shown in [Figure 7-11](#) and an example of operation is shown in [Figure 7-12](#).

The PGOOD signal can also be configured so that it maintains an inactive state even when the monitored outputs are valid, but there are PG\_FAULT\_x bits in the PG\_FAULT register pending clearance. This type of operation is selected by setting the PGFAULT\_GATES\_PGOOD bit to 1 in the PGOOD\_CTRL\_2 register.



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**Figure 7-11. PGOOD Block Diagram (Continuous Mode)**

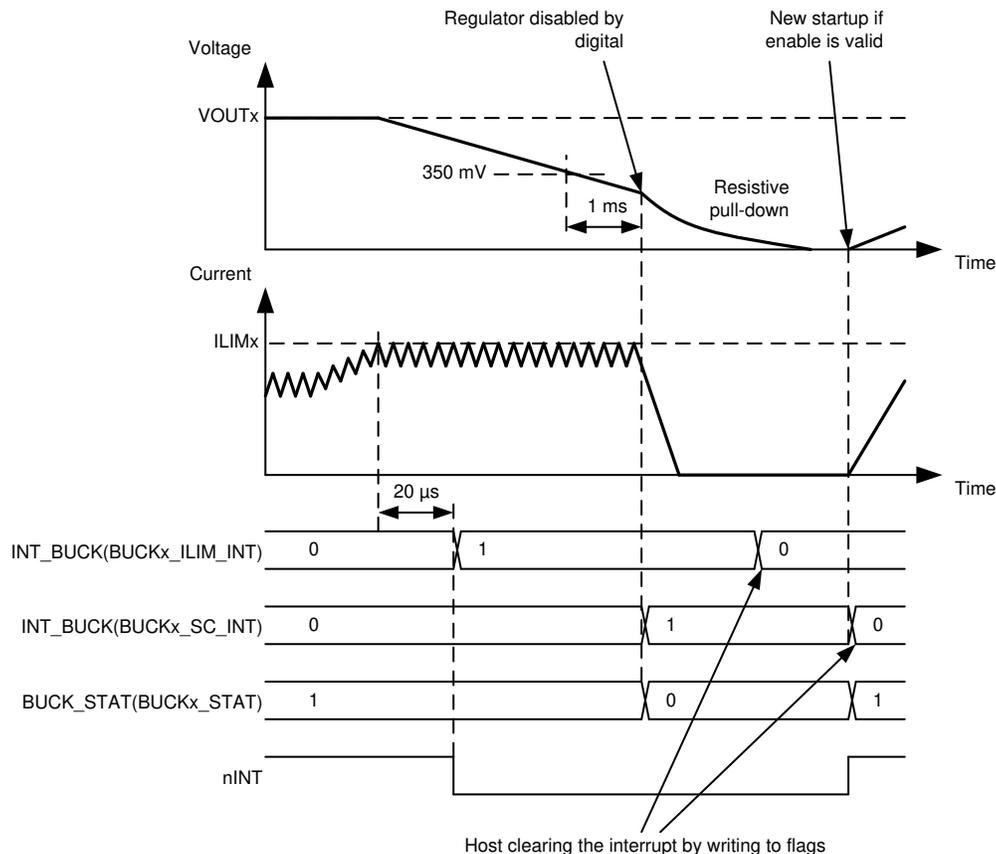


**Figure 7-12. PGOOD Pin Operation in Continuous Mode**

### 7.3.8.2 Warnings for Diagnosis (Interrupt)

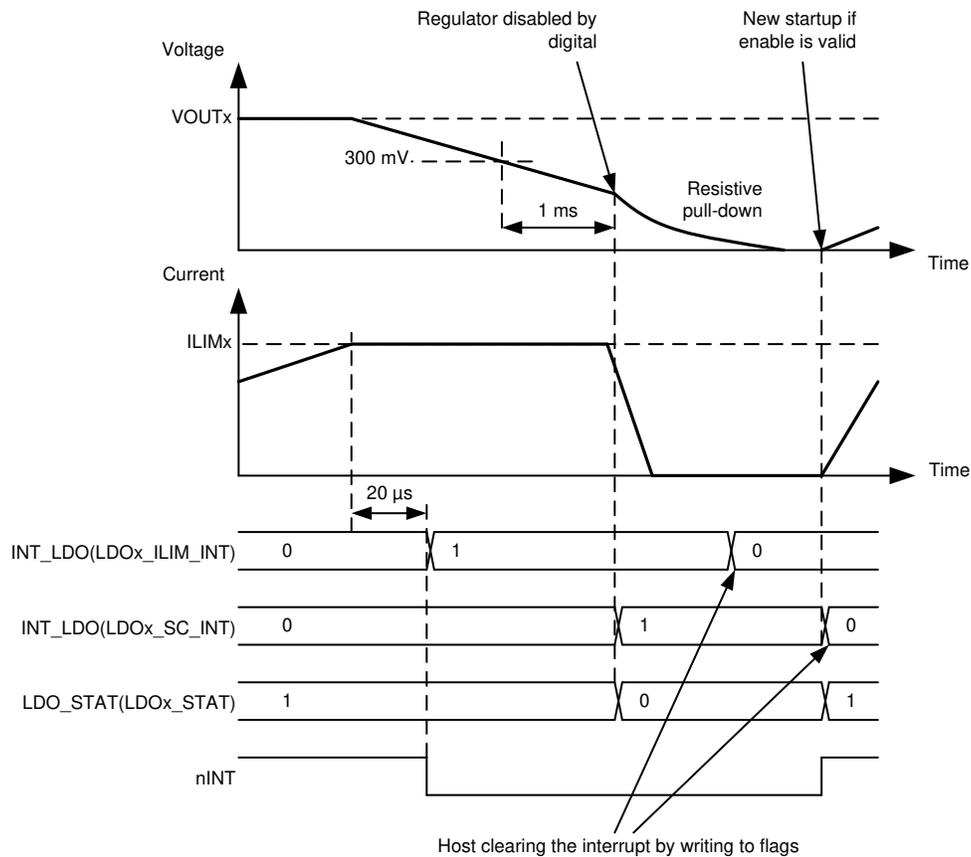
#### 7.3.8.2.1 Output Power Limit

The Buck regulators have programmable output peak current limits. The limits are individually programmed for both regulators with the BUCKx\_ILIM[2:0] bits in the BUCKx\_CTRL\_2 register. The current limit settings of master and slave regulators used for the same output voltage rail must be identical. If the load current is increased so that the current limit is triggered, then the regulator continues to regulate at the limit current level (peak current regulation). The voltage may decrease if the load current is higher than the limit current. If the current regulation continues for 20  $\mu$ s, then the LP8733xx-Q1 device sets the BUCKx\_ILIM\_INT bit in the INT\_BUCK register and pulls the nINT pin low. The host processor can read the BUCKx\_ILIM\_STAT bits in the BUCK\_STAT register to see if the regulator is still in peak current regulation mode, and the interrupt is cleared by writing 1 to the BUCKx\_ILIM\_INT bit. The current limit interrupt can be masked by setting the BUCKx\_ILIM\_MASK bit in the BUCK\_MASK register to 1. The Buck overload situation is shown in Figure 7-13.



**Figure 7-13. Buck Regulator Overload Situation**

The LDO regulators also include current limit circuitry. If the load current is increased so that the current limit is triggered, the regulator limits the output current to the threshold level. The voltage may decrease if the load current is higher than the current limit. If the current regulation continues for 20  $\mu$ s, the LP8733xx-Q1 device sets the LDOx\_ILIM\_INT bit in the INT\_LDO register and pulls the nINT pin low. The host processor can read the LDOx\_ILIM\_STAT bits in the LDO\_STAT register to see if the regulator is still in current regulation mode and the interrupt is cleared by writing 1 to the LDOx\_ILIM\_INT bit. The current limit interrupt can be masked by setting the LDOx\_ILIM\_MASK bit in the LDO\_MASK register to 1. The LDO overload situation is shown in Figure 7-14.



**Figure 7-14. LDO Regulator Overload Situation**

### 7.3.8.2.2 Thermal Warning

The LP8733xx-Q1 device includes a protection feature against overtemperature by setting an interrupt for the host processor. The threshold level of the thermal warning is selected with the TDIE\_WARN\_LEVEL bit in the CONFIG register.

If the LP8733xx-Q1 device temperature increases above the thermal warning level, then the device sets the TDIE\_WARN\_INT bit in the INT\_TOP\_1 register and pulls the nINT pin low. The status of the thermal warning can be read from the TDIE\_WARN\_STAT bit in the TOP\_STAT register, and the interrupt is cleared by writing 1 to the TDIE\_WARN\_INT bit. The thermal warning interrupt can be masked by setting the TDIE\_WARN\_MASK bit in the TOP\_MASK\_1 register to 1.

### 7.3.8.3 Protection (Regulator Disable)

If the regulator is disabled, because of protection or fault (short-circuit protection, overload protection, thermal shutdown, input overvoltage protection, or UVLO), then the output power FETs are set to high-impedance mode and the output pulldown resistor is enabled (if enabled with the BUCKx\_RDIS\_EN bit in the BUCKx\_CTRL\_1 register and the LDOx\_RDIS\_EN bit in the LDOx\_CTRL register). The turnoff time of the output voltage is defined by the output capacitance, load current, and resistance of the integrated pull-down resistor. The pull-down resistors are active as long as the VANA voltage is above approximately a 1.2-V level.

#### 7.3.8.3.1 Short-Circuit and Overload Protection

A short-circuit protection feature allows the LP8733xx-Q1 to protect itself and the external components against a short circuit at the output or against overload during start-up. For the buck and LDO regulators, the fault thresholds are about 350 mV (buck) and 300 mV (LDO). The protection is triggered and the regulator is disabled if the output voltage is below the threshold level (1 ms) after the regulator is enabled.

In a similar way, the overload situation is protected during normal operation. If the output voltage falls below 0.35 V and 0.3 V and remains below the threshold level for 1 ms, then the regulator is disabled.

In Buck regulator short-circuit and overload situations, the BUCKx\_SC\_INT bit in the INT\_BUCK register and the INT\_BUCKx bit in the INT\_TOP\_1 register are set to 1, the BUCKx\_STAT bit in BUCK\_STAT register is set to 0, and the nINT signal is pulled low. In LDO regulator short-circuit and overload situations, the LDOx\_SC\_INT bit in the INT\_LDO register and the INT\_LDOx bit in the INT\_TOP\_1 register are set to 1, the LDOx\_STAT bit in the LDO\_STAT register is set to 0, and the nINT signal is pulled low. The host processor clears the interrupt by writing 1 to the BUCKx\_SC\_INT or to the LDOx\_SC\_INT bit. Upon clearing the interrupt, the regulator makes a new start-up attempt if the regulator is in an enabled state.

#### 7.3.8.3.2 Overvoltage Protection

The LP8733xx-Q1 device monitors the input voltage from the VANA pin in standby and active operation modes. If the input voltage rises above the VANA<sub>OVP</sub> voltage level, the following occurs:

- All regulators are disabled immediately (without switching ramp or shutdown delays).
- The pull-down resistors discharge the output voltages, if the pull-down resistors are enabled (the BUCKx\_RDIS\_EN = 1 in the BUCKx\_CTRL\_1 register and the LDOx\_RDIS\_EN = 1 in the LDOx\_CTRL register).
- The GPOs are set to logic low level.
- The nINT signal is pulled low.
- The OVP\_INT bit in the INT\_TOP\_1 register is set to 1.
- The BUCKx\_STAT bit in the BUCK\_STAT register and the LDOx\_STAT bit in the LDO\_STAT register are set to 0.

The host processor clears the interrupt by writing 1 to the OVP\_INT bit. If the input voltage is above the overvoltage detection level, then the interrupt is not cleared. The host can read the status of the overvoltage from the OVP\_STAT bit in the TOP\_STAT register. The regulators cannot be enabled as long as the input voltage is above the overvoltage detection level or while the overvoltage interrupt is pending.

#### 7.3.8.3.3 Thermal Shutdown

The LP8733xx-Q1 has an overtemperature protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the regulators are disabled immediately (without switching ramp and shutdown delays), the TDIE\_SD\_INT bit in the INT\_TOP\_1 register is set to 1, the nINT signal is pulled low, and the device enters STANDBY. The nINT is cleared by writing 1 to the TDIE\_SD\_INT bit. If the temperature is above thermal shutdown level, then the interrupt is not cleared. The host can read the status of the thermal shutdown from the TDIE\_SD\_STAT bit in the TOP\_STAT register. The regulators cannot be enabled as long as the junction temperature is above the thermal shutdown level or while the thermal shutdown interrupt is pending.

### 7.3.8.4 Fault (Power Down)

#### 7.3.8.4.1 Undervoltage Lockout

When the input voltage falls below the  $V_{ANA_{UVLO}}$  at the VANA pin, the buck and LDO regulators are disabled immediately (without switching ramp and shutdown delays), the output capacitor is discharged using the pulldown resistor, and the LP8733xx-Q1 device enters SHUTDOWN. When the  $V_{(VANA)}$  voltage is above the  $V_{ANA_{UVLO}}$  threshold level, the device powers up to STANDBY state.

If the reset interrupt is unmasked by default (OTP bit for RESET\_REG\_MASK is 0 in TOP\_MASK\_2 register), then the RESET\_REG\_INT interrupt bit in the INT\_TOP\_2 register indicates that the device has been in SHUTDOWN. The host processor must clear the interrupt by writing 1 to the RESET\_REG\_INT bit. If the host processor reads the RESET\_REG\_INT interrupt bit after detecting an nINT low signal, then it detects that the input supply voltage has been below the  $V_{ANA_{UVLO}}$  level (or the host has requested reset with the SW\_RESET bit in the RESET register), and the registers are reset to default values.

### 7.3.9 Operation of the GPO Signals

The LP8733xx-Q1 device supports up to two general purpose output signals, GPO and GPO2. The GPO2 signal is multiplexed with the CLKIN signal. The selection between the CLKIN and GPO2 pin function is set with the CLKIN\_PIN\_SEL bit in the CONFIG register.

The GPO pins are configured with the following bits:

- The GPOx\_OD bit in The GPO\_CTRL register defines the type of the output, either push-pull with  $V_{(VANA)}$  level or open drain.

The logic level of the GPOx pin is set by the EN\_GPOx bit in the GPO\_CTRL register.

The control of the GPOs can be included to start-up and shutdown sequences. The GPO control for a sequence with an EN pin is selected by the GPOx\_EN\_PIN\_CTRL bit in the GPO\_CTRL register. For start-up and shutdown sequence control, see [Section 7.3.6](#).

### 7.3.10 Digital Signal Filtering

The digital signals have a debounce filtering. The signal or supply is sampled with a clock signal and a counter. This results as an accuracy of one clock period for the debounce window.

**Table 7-5. Digital Signal Filtering**

EVENT	SIGNAL/SUPPLY	RISING EDGE	FALLING EDGE
		LENGTH	LENGTH
Enable/disable for BUCKx, LDOx or GPOx	EN	3 $\mu$ s <sup>(1)</sup>	3 $\mu$ s <sup>(1)</sup>
VANA UVLO	VANA	3 $\mu$ s <sup>(1)</sup> (VANA voltage rising)	Immediate (VANA voltage falling)
VANA overvoltage	VANA	1 $\mu$ s (VANA voltage rising)	20 $\mu$ s (VANA voltage falling)
Thermal warning	TDIE_WARN_INT	20 $\mu$ s	20 $\mu$ s
Thermal shutdown	TDIE_SD_INT	20 $\mu$ s	20 $\mu$ s
Current limit	VOUtx_ILIM	20 $\mu$ s	20 $\mu$ s
Overload	FB_B0, FB_B1, VOUT_LDO0, VOUT_LDO1	1 ms	N/V
PGOOD pin and power-good interrupt	PGOOD / FB_B0, FB_B1, VOUT_LDO0, VOUT_LDO1	6 $\mu$ s	6 $\mu$ s

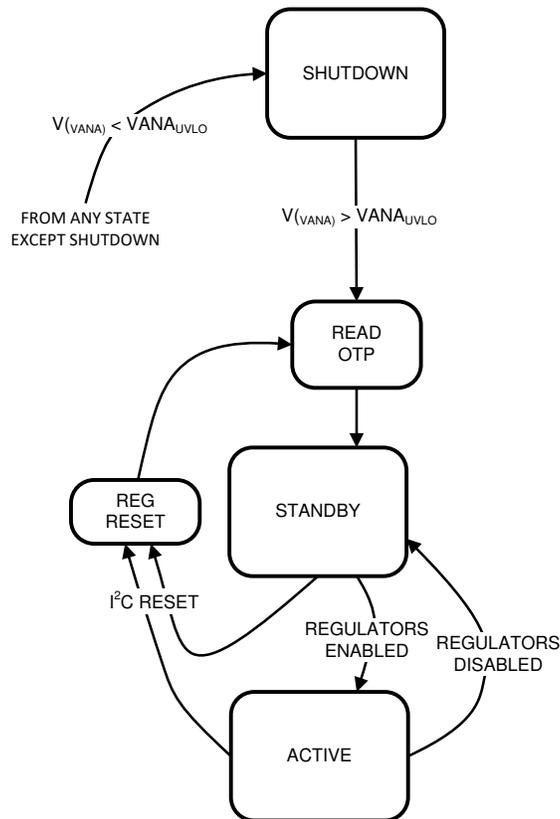
(1) No glitch filtering, only synchronization.

## 7.4 Device Functional Modes

### 7.4.1 Modes of Operation

- SHUTDOWN:** The  $V_{(VANA)}$  voltage is below  $VANA_{UVLO}$  threshold level. All switch, reference, control, and bias circuitry of the LP8733xx-Q1 device are turned off.
- READ OTP:** The main supply voltage  $V_{(VANA)}$  is above  $VANA_{UVLO}$  level. The regulators are disabled, and the reference and bias circuitry of the LP8733xx-Q1 are enabled. The OTP bits are loaded to registers.
- STANDBY:** The main supply voltage  $V_{(VANA)}$  is above  $VANA_{UVLO}$  level. The regulators are disabled, and the reference, control, and bias circuitry of the LP8733xx-Q1 are enabled. All registers can be read or written by the host processor through the system serial interface. The regulators can be enabled if needed.
- ACTIVE:** The main supply voltage  $V_{(VANA)}$  is above  $VANA_{UVLO}$  level. At least one regulator is enabled. All registers can be read or written by the host processor through the system serial interface.

The operating modes and transitions between the modes are shown in [Figure 7-15](#).



**Figure 7-15. Device Operation Modes**

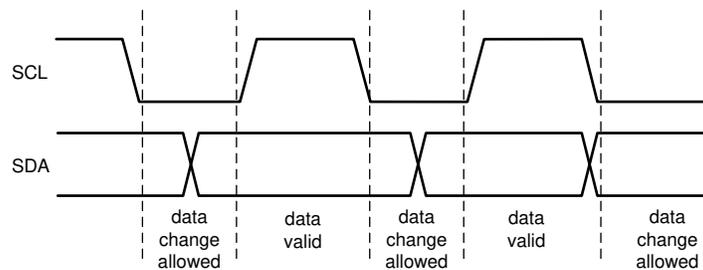
## 7.5 Programming

### 7.5.1 I<sup>2</sup>C-Compatible Interface

The I<sup>2</sup>C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the ICs connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address, and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed on the line and remain HIGH even when the bus is idle. The LP8733xx-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz).

#### 7.5.1.1 Data Validity

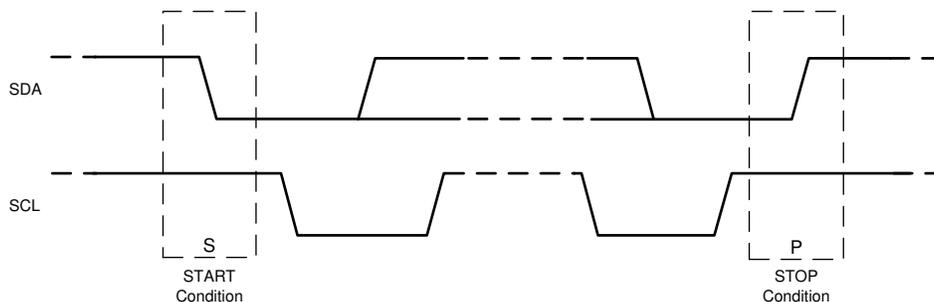
The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.



**Figure 7-16. Data Validity Diagram**

#### 7.5.1.2 Start and Stop Conditions

The LP8733xx-Q1 is controlled through an I<sup>2</sup>C-compatible interface. START and STOP conditions classify the beginning and end of the I<sup>2</sup>C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as an SDA transition from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates the START and STOP conditions.



**Figure 7-17. Start and Stop Sequences**

The I<sup>2</sup>C bus is considered busy after a START condition and free after a STOP condition. During data transmission, the I<sup>2</sup>C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. [Figure 7-18](#) shows the SDA and SCL signal timing for the I<sup>2</sup>C-compatible bus. See [Section 6.6](#) for the timing values.

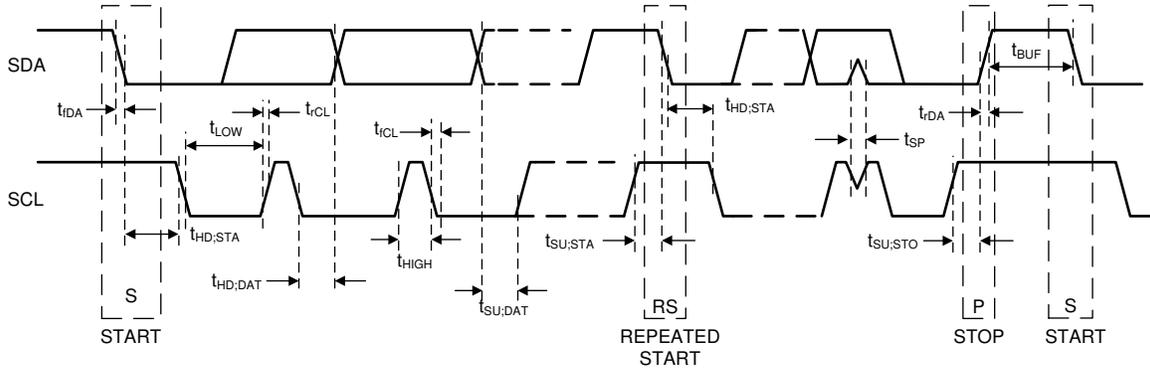


Figure 7-18. I<sup>2</sup>C-Compatible Timing

### 7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP8733xx-Q1 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP8733xx-Q1 generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

#### Note

If the  $V_{(VANA)}$  voltage is below the  $VANA_{UVLO}$  threshold level during I<sup>2</sup>C communication, the LP8733xx-Q1 device does not drive SDA line. The ACK signal and data transfer to the master is disabled at that time.

After the START condition, the bus master sends a chip address. This address is seven bits long, followed by an eighth bit, which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

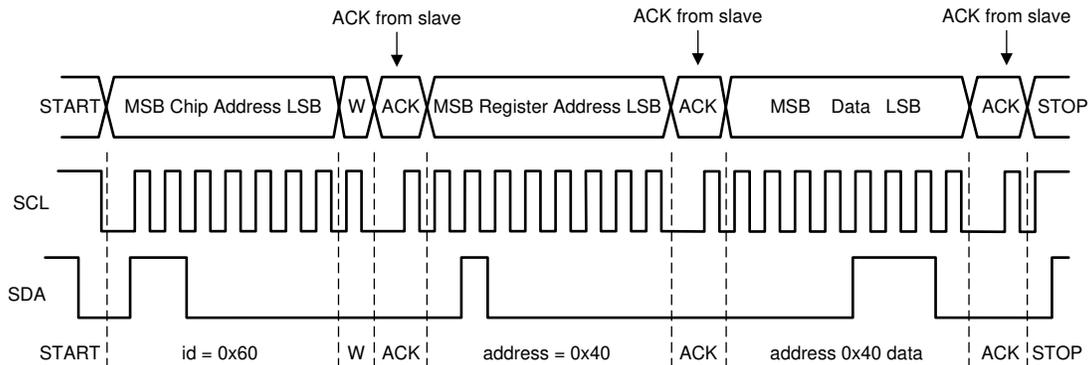
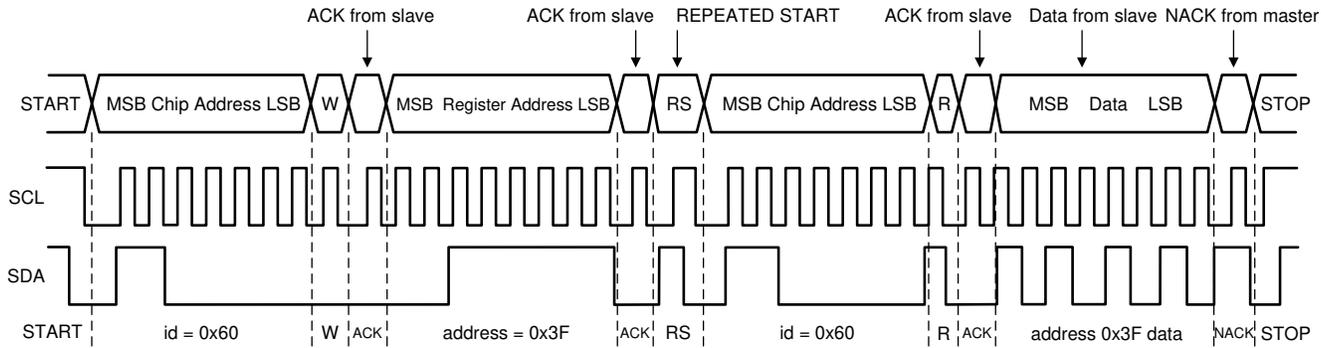


Figure 7-19. Write Cycle (w = write; SDA = 0). Example Device Address = 0x60

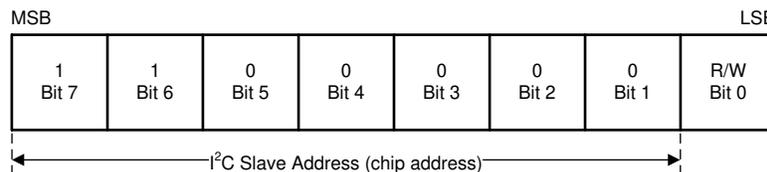


When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

**Figure 7-20. Read Cycle (r = read; SDA = 1). Example Device Address = 0x60**

### 7.5.1.4 I<sup>2</sup>C-Compatible Chip Address

After the START condition, the I<sup>2</sup>C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data is written. The third byte contains the data for the selected register.



Here in an example with device address of 1100000Bin = 60Hex.

**Figure 7-21. Device Address Example**

### 7.5.1.5 Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the LP8733xx-Q1, the internal address index counter is incremented by one and the next register is written. Table 7-6 shows writing sequence to two consecutive registers. The auto-increment feature does not work for read.

**Table 7-6. Auto-Increment Example**

MASTER ACTION	START	DEVICE ADDRESS = X	WRITE		REGISTER ADDRESS		DATA		DATA		STOP
LP8733xx-Q1				ACK		ACK		ACK		ACK	

## 7.6 Register Maps

### 7.6.1 Register Descriptions

The LP8733xx-Q1 is controlled by a set of registers through the I<sup>2</sup>C-compatible interface. The device registers addresses and abbreviations are listed in [Table 7-7](#). A more detailed description is given in the [Section 7.6.1.1](#) to [Section 7.6.1.39](#) sections.

#### Note

This register map describes the default values for bits that are not read from OTP memory. The orderable code and the default register bit values are defined in part-number specific Technical Reference Manuals.

**Table 7-7. Summary of LP8733xx-Q1 Control Registers**

Addr	Register	Read / Write	D7	D6	D5	D4	D3	D2	D1	D0	
0x00	DEV_REV	R	DEVICE_ID[1:0]		Reserved - do not use						
0x01	OTP_REV	R	OTP_ID[7:0]								
0x02	BUCK0_CTRL_1	R/W	Reserved - do not use			BUCK0_FP_WM_MP	BUCK0_FP_WM	BUCK0_RDIS_EN	BUCK0_EN_PIN_CTL	BUCK0_EN	
0x03	BUCK0_CTRL_2	R/W	Reserved - do not use		BUCK0_ILIM[2:0]		BUCK0_SLEW_RATE[2:0]				
0x04	BUCK1_CTRL_1	R/W	Reserved - do not use			BUCK1_FP_WM	BUCK1_RDIS_EN	BUCK1_EN_PIN_CTL	BUCK1_EN		
0x05	BUCK1_CTRL_2	R/W	Reserved - do not use		BUCK1_ILIM[2:0]		BUCK1_SLEW_RATE[2:0]				
0x06	BUCK0_VOUT	R/W	BUCK0_VSET[7:0]								
0x07	BUCK1_VOUT	R/W	BUCK1_VSET[7:0]								
0x08	LDO0_CTRL	R/W	Reserved - do not use					LDO0_RDIS_EN	LDO0_EN_PIN_CTL	LDO0_EN	
0x09	LDO1_CTRL	R/W	Reserved - do not use					LDO1_RDIS_EN	LDO1_EN_PIN_CTL	LDO1_EN	
0x0A	LDO0_VOUT	R/W	Reserved - do not use			LDO0_VSET[4:0]					
0x0B	LDO1_VOUT	R/W	Reserved - do not use			LDO1_VSET[4:0]					
0x0C	BUCK0_DELAY	R/W	BUCK0_SHUTDOWN_DELAY[3:0]				BUCK0_STARTUP_DELAY[3:0]				
0x0D	BUCK1_DELAY	R/W	BUCK1_SHUTDOWN_DELAY[3:0]				BUCK1_STARTUP_DELAY[3:0]				
0x0E	LDO0_DELAY	R/W	LDO0_SHUTDOWN_DELAY[3:0]				LDO0_STARTUP_DELAY[3:0]				
0x0F	LDO1_DELAY	R/W	LDO1_SHUTDOWN_DELAY[3:0]				LDO1_STARTUP_DELAY[3:0]				
0x10	GPO_DELAY	R/W	GPO_SHUTDOWN_DELAY[3:0]				GPO_STARTUP_DELAY[3:0]				
0x11	GPO2_DELAY	R/W	GPO2_SHUTDOWN_DELAY[3:0]				GPO2_STARTUP_DELAY[3:0]				
0x12	GPO_CTRL	R/W	Reserved - do not use	GPO2_OD	GPO2_EN_PIN_CTL	GPO2_EN	Reserved - do not use	GPO_OD	GPO_EN_PIN_CTL	GPO_EN	
0x13	CONFIG	R/W	Reserved - do not use	STARTUP_DELAY_SEL	SHUTDOWN_DELAY_SEL	CLKIN_PIN_SEL	CLKIN_PD	EN_PD	TDIE_WARN_LEVEL	EN_SPREAD_SPEC	
0x14	PLL_CTRL	R/W	Reserved - do not use	EN_PLL	Reserved - do not use	EXT_CLK_FREQ[4:0]					

**Table 7-7. Summary of LP8733xx-Q1 Control Registers (continued)**

Addr	Register	Read / Write	D7	D6	D5	D4	D3	D2	D1	D0	
0x15	PGOOD_CT RL_1	R/W	PGOOD_PO L	PGOOD_OD	PGOOD_WI NDOW_LDO	PGOOD_WI NDOW_BUC K	EN_PGOOD _LDO1	EN_PGOOD _LDO0	EN_PGOOD _BUCK1	EN_PGOOD _BUCK0	
0x16	PGOOD_CT RL_2	R/W	Reserved - do not use						EN_PGOOD _TWARN	PG_FAULT GATES_PG OOD	PGOOD_M ODE
0x17	PG_FAULT	R	Reserved - do not use				PG_FAULT_ LDO1	PG_FAULT_ LDO0	PG_FAULT_ BUCK1	PG_FAULT_ BUCK0	
0x18	RESET	R/W	Reserved - do not use								SW RESÉT
0x19	INT_TOP_1	R/W	PGOOD_ INT	INT_ LDO	INT_ BUCK	SYNC_ CLK_INT	TDIE_SD_ IN T	TDIE_ WARN_INT	OVP_INT	I_MEAS_ INT	
0x1A	INT_TOP_2	R/W	Reserved - do not use								RESET_ REG_INT
0x1B	INT_BUCK	R/W	Reserved - do not use	BUCK1_ PG_INT	BUCK1_ SC_INT	BUCK1_ ILIM_INT	Reserved - do not use	BUCK0_ PG_INT	BUCK0_ SC_INT	BUCK0_ ILIM_INT	
0x1C	INT_LDO	R/W	Reserved - do not use	LDO1_ PG_INT	LDO1_ SC_INT	LDO1_ ILIM_INT	Reserved - do not use	LDO0_ PG_INT	LDO0_ SC_INT	LDO0_ ILIM_INT	
0x1D	TOP_ STAT	R	PGOOD_ STAT	Reserved - do not use		SYNC_CLK _STAT	TDIE_SD _STAT	TDIE_ WARN_ STAT	OVP_ STAT	Reserved - do not use	
0x1E	BUCK_STAT	R	BUCK1_ STAT	BUCK1_ PG_STAT	Reserved - do not use	BUCK1_ ILIM_STAT	BUCK0_ STAT	BUCK0_ PG_STAT	Reserved - do not use	BUCK0_ ILIM_STAT	
0x1F	LDO_STAT	R	LDO1_ STAT	LDO1_ PG_STAT	Reserved - do not use	LDO1_ ILIM_STAT	LDO0_ STAT	LDO0_ PG_STAT	Reserved - do not use	LDO0_ ILIM_STAT	
0x20	TOP_ MASK_1	R/W	PGOOD_ INT_MASK	Reserved - do not use		SYNC_CLK _MASK	Reserved - do not use	TDIE_WARN _MASK	Reserved - do not use	I_MEAS_ MASK	
0x21	TOP_ MASK_2	R/W	Reserved - do not use								RESET_ REG_MASK
0x22	BUCK_MAS K	R/W	BUCK1_PG F_MASK	BUCK1_PG R_MASK	Reserved - do not use	BUCK1_ ILIM_ MASK	BUCK0_PG F_MASK	BUCK0_PG R_MASK	Reserved - do not use	BUCK0_ ILIM_ MASK	
0x23	LDO_MASK	R/W	LDO1_PGF_ MASK	LDO1_PGR _MASK	Reserved - do not use	LDO1_ ILIM_ MASK	LDO0_PGF_ MASK	LDO0_PGR _MASK	Reserved - do not use	LDO0_ ILIM_ MASK	
0x24	SEL_I_ LOAD	R/W	Reserved - do not use								LOAD_CUR RENT_ BUCK_SEL ECT
0x25	I_LOAD_2	R	Reserved - do not use								BUCK_LOA D_CURREN T[8]
0x26	I_LOAD_1	R	BUCK_LOAD_CURRENT[7:0]								

### 7.6.1.1 DEV\_REV

DEV\_REV is shown in [Table 7-9](#), Address: 0x00

**Table 7-8. DEV\_REV Register**

D7	D6	D5	D4	D3	D2	D1	D0
DEVICE_ID[1:0]			Reserved - do not use				

**Table 7-9. DEV\_REV Register Field Descriptions**

Bits	Field	Type	Default	Description
7:6	DEVICE_ID[1:0]	R	X	Device specific ID code.
5:0	Reserved - do not use	R	00 0010	

### 7.6.1.2 OTP\_REV

OTP\_REV is shown in [Table 7-11](#), Address: 0x01

**Table 7-10. OTP\_REV Register**

D7	D6	D5	D4	D3	D2	D1	D0
OTP_ID[7:0]							

**Table 7-11. OTP\_REV Register Field Descriptions**

Bits	Field	Type	Default	Description
7:0	OTP_ID[7:0]	R	X	Identification Code of the OTP EPROM Version.

### 7.6.1.3 BUCK0\_CTRL\_1

BUCK0\_CTRL\_1 is shown in [Table 7-13](#), Address: 0x02

**Table 7-12. BUCK0\_CTRL\_1 Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use			BUCK0_FPWM_MP	BUCK0_FPWM	BUCK0_RDIS_EN	BUCK0_EN_PI_CTRL	BUCK0_EN

**Table 7-13. BUCK0\_CTRL\_1 Register Field Descriptions**

Bits	Field	Type	Default	Description
7:5	Reserved - do not use	R/W	000	
4	BUCK0_FPWM_MP	R/W	X	Forces the Buck0 regulator to always operate in the multi-phase and forced PWM operation mode: 0 - Automatic phase adding and shedding. 1 - Forced to multi-phase operation, 2 phases in the 2-phase configuration.
3	BUCK0_FPWM	R/W	X	Buck0 mode selection: 0 - Automatic transitions between the PFM and PWM modes (AUTO mode). 1 - Forced to the PWM operation.
2	BUCK0_RDIS_EN	R/W	1	Enable output discharge resistor (R <sub>DIS_Bx</sub> ) when the Buck0 is disabled: 0 - Discharge resistor disabled. 1 - Discharge resistor enabled.
1	BUCK0_EN_PIN_CTRL	R/W	X	Enable control for the Buck0: 0 - only the BUCK0_EN bit controls the Buck0. 1 - BUCK0_EN bit <i>and</i> the EN pin control the Buck0.
0	BUCK0_EN	R/W	X	Enable the Buck0 regulator: 0 - Buck0 regulator is disabled. 1 - Buck0 regulator is enabled.

### 7.6.1.4 BUCK0\_CTRL\_2

 BUCK0\_CTRL\_2 is shown in [Table 7-15](#), Address: 0x03

**Table 7-14. BUCK0\_CTRL\_2 Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use		BUCK0_ILIM[2:0]			BUCK0_SLEW_RATE[2:0]		

**Table 7-15. BUCK0\_CTRL\_2 Register Field Descriptions**

Bits	Field	Type	Default	Description
7:6	Reserved - do not use	R/W	00	
5:3	BUCK0_ILIM[2:0]	R/W	X	Sets the switch current limit of Buck0. Can be programmed at any time during operation: 0x0 - 1.5 A 0x1 - 2.0 A 0x2 - 2.5 A 0x3 - 3.0 A 0x4 - 3.5 A 0x5 - 4.0 A 0x6 - Reserved - do not use. 0x7 - Reserved - do not use.
2:0	BUCK0_SLEW_RATE[2:0]	R/W	X	Sets the output voltage slew rate for Buck0 regulator (rising and falling edges): 0x0 - Reserved - do not use. 0x1 - Reserved - do not use. 0x2 - 10 mV/μs 0x3 - 7.5 mV/μs 0x4 - 3.8 mV/μs 0x5 - 1.9 mV/μs 0x6 - 0.94 mV/μs 0x7 - 0.47 mV/μs

### 7.6.1.5 BUCK1\_CTRL\_1

 BUCK1\_CTRL\_1 is shown in [Table 7-17](#), Address: 0x04

**Table 7-16. BUCK1\_CTRL\_1 Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use				BUCK1_FPWM	BUCK1_RDIS_EN	BUCK1_EN_PIN_CTRL	BUCK1_EN

**Table 7-17. BUCK1\_CTRL\_1 Register Field Descriptions**

Bits	Field	Type	Default	Description
7:4	Reserved - do not use	R/W	0000	
3	BUCK1_FPWM	R/W	X	Buck1 mode selection: 0 - Automatic transitions between the PFM and PWM modes (AUTO mode). 1 - Forced to PWM operation.
2	BUCK1_RDIS_EN	R/W	1	Enable output discharge resistor ( $R_{DIS\_BX}$ ) when the Buck1 is disabled: 0 - Discharge resistor is disabled. 1 - Discharge resistor is enabled.
1	BUCK1_EN_PIN_CTRL	R/W	X	Enable control for the Buck1: 0 - only the BUCK1_EN bit controls the Buck1 1 - BUCK1_EN bit <i>and</i> the EN pin control the Buck1.
0	BUCK1_EN	R/W	X	Enable the Buck1 regulator: 0 - Buck1 regulator is disabled. 1 - Buck1 regulator is enabled.

### 7.6.1.6 BUCK1\_CTRL\_2

BUCK1\_CTRL\_2 is shown in [Table 7-19](#), Address: 0x05

**Table 7-18. BUCK1\_CTRL\_2 Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use		BUCK1_ILIM[2:0]			BUCK1_SLEW_RATE[2:0]		

**Table 7-19. BUCK1\_CTRL\_2 Register Field Descriptions**

Bits	Field	Type	Default	Description
7:6	Reserved - do not use	R/W	00	
5:3	BUCK1_ILIM[2:0]	R/W	X	Sets the switch current limit of the Buck1. Can be programmed at any time during operation: 0x0 - 1.5 A 0x1 - 2.0 A 0x2 - 2.5 A 0x3 - 3.0 A 0x4 - 3.5 A 0x5 - 4.0 A 0x6 - Reserved - do not use. 0x7 - Reserved - do not use.
2:0	BUCK1_SLEW_RATE[2:0]	R/W	X	Sets the output voltage slew rate for the Buck1 regulator (rising and falling edges): 0x0 - Reserved - do not use. 0x1 - Reserved - do not use. 0x2 - 10 mV/μs 0x3 - 7.5 mV/μs 0x4 - 3.8 mV/μs 0x5 - 1.9 mV/μs 0x6 - 0.94 mV/μs 0x7 - 0.47 mV/μs

### 7.6.1.7 BUCK0\_VOUT

BUCK0\_VOUT is shown in [Table 7-21](#), Address: 0x06

**Table 7-20. BUCK0\_VOUT Register**

D7	D6	D5	D4	D3	D2	D1	D0
BUCK0_VSET[7:0]							

**Table 7-21. BUCK0\_VOUT Register Field Descriptions**

Bits	Field	Type	Default	Description
7:0	BUCK0_VSET[7:0]	R/W	X	Sets the output voltage of the Buck0 regulator: <i>Reserved; do not use.</i> 0x00 ... 0x13 0.7 V - 0.73 V, 10 mV steps 0x14 - 0.7V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V

### 7.6.1.8 BUCK1\_VOUT

BUCK1\_VOUT is shown in [Table 7-23](#), Address: 0x07

**Table 7-22. BUCK1\_VOUT Register**

D7	D6	D5	D4	D3	D2	D1	D0
BUCK1_VSET[7:0]							

**Table 7-23. BUCK1\_VOUT Register Field Descriptions**

Bits	Field	Type	Default	Description
7:0	BUCK1_VSET[7:0]	R/W	X	Sets the output voltage of the Buck0 regulator: <i>Reserved; do not use.</i> 0x00 ... 0x13 0.7 V - 0.73 V, 10 mV steps 0x14 - 0.7V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V

**7.6.1.9 LDO0\_CTRL**LDO0\_CTRL is shown in [Table 7-25](#), Address: 0x08**Table 7-24. LDO0\_CTRL Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use					LDO0_RDIS_EN	LDO0_EN_PIN_CTRL	LDO0_EN

**Table 7-25. LDO0\_CTRL Register Field Descriptions**

Bits	Field	Type	Default	Description
7:3	Reserved - do not use	R/W	0 0000	
2	LDO0_RDIS_EN	R/W	1	Enable output discharge resistor (R <sub>DIS_LDOx</sub> ) when the LDO0 is disabled: 0 - Discharge resistor is disabled. 1 - Discharge resistor is enabled.
1	LDO0_EN_PIN_CTRL	R/W	X	Enable control for the LDO0: 0 - only the LDO0_EN bit controls the LDO0. 1 - LDO0_EN bit <i>and</i> the EN pin control the LDO0.
0	LDO0_EN	R/W	X	Enable the LDO0 regulator: 0 - LDO0 regulator is disabled. 1 - LDO0 regulator is enabled.

**7.6.1.10 LDO1\_CTRL**LDO1\_CTRL is shown in [Table 7-27](#), Address: 0x09**Table 7-26. LDO1\_CTRL Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use					LDO1_RDIS_EN	LDO1_EN_PIN_CTRL	LDO1_EN

**Table 7-27. LDO1\_CTRL Register Field Descriptions**

Bits	Field	Type	Default	Description
7:3	Reserved - do not use	R/W	0 0000	

**Table 7-27. LDO1\_CTRL Register Field Descriptions (continued)**

Bits	Field	Type	Default	Description
2	LDO1_RDIS_EN	R/W	1	Enable output discharge resistor ( $R_{DIS\_LDOx}$ ) when the LDO1 is disabled: 0 - Discharge resistor is disabled. 1 - Discharge resistor is enabled.
1	LDO1_EN_PIN_CTRL	R/W	X	Enable control for the LDO1: 0 - only the LDO1_EN bit controls the LDO1. 1 - LDO1_EN bit <i>and</i> the EN pin control the LDO1.
0	LDO1_EN	R/W	X	Enable the LDO1 regulator: 0 - LDO1 regulator is disabled. 1 - LDO1 regulator is enabled.

### 7.6.1.11 LDO0\_VOUT

LDO0\_VOUT is shown in [Table 7-29](#), Address: 0x0A

**Table 7-28. LDO0\_VOUT Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use				LDO0_VSET[4:0]			

**Table 7-29. LDO0\_VOUT Register Field Descriptions**

Bits	Field	Type	Default	Description
7:5	Reserved - do not use	R/W	000	
4:0	LDO0_VSET[4:0]	R/W	X	Sets the output voltage of the LDO0 regulator: <i>0.8 V - 3.3 V, 100 mV steps</i> 0x00 - 0.8V ... 0x19 - 3.3 V <i>Reserved; do not use.</i> 0x1A ... 0x1F

### 7.6.1.12 LDO1\_VOUT

LDO1\_VOUT is shown in [Table 7-31](#), Address: 0x0B

**Table 7-30. LDO1\_VOUT Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use				LDO1_VSET[4:0]			

**Table 7-31. LDO1\_VOUT Register Field Descriptions**

Bits	Field	Type	Default	Description
7:5	Reserved - do not use	R/W	000	
4:0	LDO1_VSET[4:0]	R/W	X	Sets the output voltage of the LDO1 regulator: <i>0.8 V - 3.3 V, 100 mV steps</i> 0x00 - 0.8V ... 0x19 - 3.3 V <i>Reserved; do not use.</i> 0x1A ... 0x1F

### 7.6.1.13 BUCK0\_DELAY

BUCK0\_DELAY is shown in [Table 7-33](#), Address: 0x0C

**Table 7-32. BUCK0\_DELAY Register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

BUCK0_SHUTDOWN_DELAY[3:0]	BUCK0_STARTUP_DELAY[3:0]
---------------------------	--------------------------

**Table 7-33. BUCK0\_DELAY Register Field Descriptions**

Bits	Field	Type	Default	Description
7:4	BUCK0_SHUTDOWN_DELAY[3:0]	R/W	X	Shutdown delay of the Buck0 from the EN signal's falling edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.)
3:0	BUCK0_STARTUP_DELAY[3:0]	R/W	X	Startup delay of the Buck0 from the EN signal's rising edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.)

**7.6.1.14 BUCK1\_DELAY**

BUCK1\_DELAY is shown in [Table 7-35](#), Address: 0x0D

**Table 7-34. BUCK1\_DELAY Register**

D7	D6	D5	D4	D3	D2	D1	D0
BUCK1_SHUTDOWN_DELAY[3:0]				BUCK1_STARTUP_DELAY[3:0]			

**Table 7-35. BUCK1\_DELAY Register Field Descriptions**

Bits	Field	Type	Default	Description
7:4	BUCK1_SHUTDOWN_DELAY[3:0]	R/W	X	Shutdown delay of the Buck1 from the EN signal's falling edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.)
3:0	BUCK1_STARTUP_DELAY[3:0]	R/W	X	Startup delay of the Buck1 from the EN signal's rising edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.)

**7.6.1.15 LDO0\_DELAY**

LDO0\_DELAY is shown in [Table 7-37](#), Address: 0x0E

**Table 7-36. LDO0\_DELAY Register**

D7	D6	D5	D4	D3	D2	D1	D0
LDO0_SHUTDOWN_DELAY[3:0]				LDO0_STARTUP_DELAY[3:0]			

**Table 7-37. LDO0\_DELAY Register Field Descriptions**

Bits	Field	Type	Default	Description
7:4	LDO0_SHUTDOWN_DELAY[3:0]	R/W	X	Shutdown delay of the LDO0 from the EN signal's falling edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.)
3:0	LDO0_STARTUP_DELAY[3:0]	R/W	X	Startup delay of the LDO0 from the EN signal's rising edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.)

### 7.6.1.16 LDO1\_DELAY

LDO1\_DELAY is shown in [Table 7-39](#), Address: 0x0F

**Table 7-38. LDO1\_DELAY Register**

D7	D6	D5	D4	D3	D2	D1	D0
LDO1_SHUTDOWN_DELAY[3:0]				LDO1_STARTUP_DELAY[3:0]			

**Table 7-39. LDO1\_DELAY Register Field Descriptions**

Bits	Field	Type	Default	Description
7:4	LDO1_SHUTDOWN_DELAY[3:0]	R/W	X	Shutdown delay of the LDO1 from the EN signal's falling edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.)
3:0	LDO1_STARTUP_DELAY[3:0]	R/W	X	Startup delay of the LDO1 from the EN signal's rising edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.)

### 7.6.1.17 GPO\_DELAY

GPO\_DELAY is shown in [Table 7-41](#), Address: 0x10

**Table 7-40. GPO\_DELAY Register**

D7	D6	D5	D4	D3	D2	D1	D0
GPO_SHUTDOWN_DELAY[3:0]				GPO_STARTUP_DELAY[3:0]			

**Table 7-41. GPO\_DELAY Register Field Descriptions**

Bits	Field	Type	Default	Description
7:4	GPO_SHUTDOWN_DELAY[3:0]	R/W	X	Delay for the GPO falling edge from the EN signal's falling edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register)
3:0	GPO_STARTUP_DELAY[3:0]	R/W	X	Delay for the GPO rising edge from the EN signal's rising edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.)

### 7.6.1.18 GPO2\_DELAY

GPO2\_DELAY is shown in [Table 7-43](#), Address: 0x11

**Table 7-42. GPO2\_DELAY Register**

D7	D6	D5	D4	D3	D2	D1	D0
GPO2_SHUTDOWN_DELAY[3:0]				GPO2_STARTUP_DELAY[3:0]			

**Table 7-43. GPO2\_DELAY Register Field Descriptions**

Bits	Field	Type	Default	Description
7:4	GPO2_SHUTDOWN_DELAY[3:0]	R/W	X	Delay for the GPO2 falling edge from the EN signal's falling edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in the CONFIG register.)

**Table 7-43. GPO2\_DELAY Register Field Descriptions (continued)**

Bits	Field	Type	Default	Description
3:0	GPO2_STARTUP_DELAY[3:0]	R/W	X	Delay for the GPO2 rising edge from the EN signal's rising edge: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in the CONFIG register.)

**7.6.1.19 GPO\_CTRL**

GPO\_CTRL is shown in [Table 7-45](#), Address: 0x12

**Table 7-44. GPO\_CTRL Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use	GPO2_OD	GPO2_EN_PIN_CTRL	GPO2_EN	Reserved - do not use	GPO_OD	GPO_EN_PIN_CTRL	GPO_EN

**Table 7-45. GPO\_CTRL Register Field Descriptions**

Bits	Field	Type	Default	Description
7	Reserved - do not use	R	0	
6	GPO2_OD	R/W	X	GPO2 signal type when configured as the General Purpose Output (CLKIN pin): 0 - Push-pull output (VANA level) 1 - Open-drain output
5	GPO2_EN_PIN_CTRL	R/W	X	Control for the GPO2: 0 - Only the GPO2_EN bit controls the GPO2 1 - GPO2_EN bit <i>and</i> the EN pin control the GPO2.
4	GPO2_EN	R/W	X	Output level of the GPO2 signal (when configured as the General Purpose Output): 0 - Logic low level 1 - Logic high level
3	Reserved - do not use	R	0	
2	GPO_OD	R/W	X	GPO signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output
1	GPO_EN_PIN_CTRL	R/W	X	Control for the GPO: 0 - Only the GPO_EN bit controls the GPO 1 - GPO_EN bit <i>and</i> the EN pin control the GPO.
0	GPO_EN	R/W	X	Output level of the GPO signal: 0 - Logic low level 1 - Logic high level

**7.6.1.20 CONFIG**

CONFIG is shown in [Table 7-47](#), Address: 0x13

**Table 7-46. CONFIG Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use	STARTUP_DELAY_SEL	SHUTDOWN_DELAY_SEL	CLKIN_PIN_SEL	CLKIN_PD	EN2_PD	TDIE_WARN_LEVEL	EN_SPREAD_SPEC

**Table 7-47. CONFIG Register Field Descriptions**

Bits	Field	Type	Default	Description
7	Reserved - do not use	R/W	0	
6	STARTUP_DELAY_SEL	R/W	X	Startup delay range from the EN signals: 0 - 0 ms - 7.5 ms with 0.5 ms steps 1 - 0 ms - 15 ms with 1 ms steps

**Table 7-47. CONFIG Register Field Descriptions (continued)**

Bits	Field	Type	Default	Description
5	SHUTDOWN_DELAY_SEL	R/W	X	Shutdown delay range from the EN signals: 0 - 0 ms - 7.5 ms with 0.5 ms steps 1 - 0 ms - 15 ms with 1 ms steps
4	CLKIN_PIN_SEL	R/W	X	CLKIN pin function: 0 - GPO2 1 - CLKIN
3	CLKIN_PD	R/W	X	Selects the pull down resistor on the CLKIN input pin (valid also when selected as GPO2): 0 - Pull-down resistor is disabled. 1 - Pull-down resistor is enabled.
2	EN_PD	R/W	X	Selects the pull down resistor on the EN input pin. 0 - Pull-down resistor is disabled. 1 - Pull-down resistor is enabled.
1	TDIE_WARN_LEVEL	R/W	X	Thermal warning threshold level: 0 - 125°C 1 - 137°C
0	EN_SPREAD_SPEC	R/W	X	Enable spread spectrum feature: 0 - Disabled 1 - Enabled

### 7.6.1.21 PLL\_CTRL

PLL\_CTRL is shown in [Table 7-49](#), Address: 0x14

**Table 7-48. PLL\_CTRL Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use	EN_PLL	Reserved - do not use	EXT_CLK_FREQ[4:0]				

**Table 7-49. PLL\_CTRL Register Field Descriptions**

Bits	Field	Type	Default	Description
7	Reserved - do not use	R/W	0	
6	EN_PLL	R/W	X	Selection of the external clock and PLL operation: 0 - Forced to the internal RC oscillator. The PLL is disabled. 1 - PLL is enabled in the STANDBY and ACTIVE modes. Automatic external clock use when available, and interrupt is generated if the external clock appears or disappears.
5	Reserved - do not use	R/W	0	<i>This bit must be set to "0."</i>
4:0	EXT_CLK_FREQ[4:0]	R/W	X	Frequency of the external clock (CLKIN): 0x00 - 1 MHz 0x01 - 2 MHz 0x02 - 3 MHz ... 0x16 - 23 MHz 0x17 - 24 MHz 0x18...0x1F - Reserved - do not use See electrical specification for the input clock frequency tolerance.

### 7.6.1.22 PGOOD\_CTRL\_1

PGOOD\_CTRL\_1 is shown in [Table 7-51](#), Address: 0x15

**Table 7-50. PGOOD\_CTRL\_1 Register**

D7	D6	D5	D4	D3	D2	D1	D0
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PGOOD_POL	PGOOD_OD	PGOOD_WINDOW_LDO	PGOOD_WINDOW_BUCK	EN_PGOOD_LDO1	EN_PGOOD_LDO0	EN_PGOOD_BUCK1	EN_PGOOD_BUCK0
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**Table 7-51. PGOOD\_CTRL\_1 Register Field Descriptions**

Bits	Field	Type	Default	Description
7	PGOOD_POL	R/W	X	PGOOD signal polarity: 0 - PGOOD signal high when the monitored outputs are valid. 1 - PGOOD signal low when the monitored outputs are valid.
6	PGOOD_OD	R/W	X	PGOOD signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output
5	PGOOD_WINDOW_LDO	R/W	X	LDO Output voltage monitoring method for the PGOOD signal: 0 - Only undervoltage monitoring 1 - Overvoltage and undervoltage monitoring
4	PGOOD_WINDOW_BUCK	R/W	X	Buck Output voltage monitoring method for the PGOOD signal: 0 - Only undervoltage monitoring 1 - Overvoltage and undervoltage monitoring
3	EN_PGOOD_LDO1	R/W	X	PGOOD signal source control from LDO1: 0 - LDO1 is not monitored. 1 - LDO1 Power-Good threshold voltage is monitored.
2	EN_PGOOD_LDO0	R/W	X	PGOOD signal source control from theLDO0: 0 - LDO0 is not monitored. 1 - LDO0 Power-Good threshold voltage is monitored.
1	EN_PGOOD_BUCK1	R/W	X	PGOOD signal source control from the Buck1: 0 - Buck1 is not monitored. 1 - Buck1 Power-Good threshold voltage is monitored.
0	EN_PGOOD_BUCK0	R/W	X	PGOOD signal source control from the Buck0: 0 - Buck0 is not monitored. 1 - Buck0 Power-Good threshold voltage is monitored.

### 7.6.1.23 PGOOD\_CTRL\_2

 PGOOD\_CTRL\_2 is shown in [Table 7-53](#), Address: 0x16

**Table 7-52. PGOOD\_CTRL\_2 Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use					EN_PGOOD_TWARN	PG_FAULT_GATES_PGGOOD	PGOOD_MODE

**Table 7-53. PGOOD\_CTRL\_2 Register Field Descriptions**

Bits	Field	Type	Default	Description
7:3	Reserved - do not use	R/W	0 0000	
2	EN_PGOOD_TWARN	R/W	X	Thermal warning control for the PGOOD signal: 0 - Thermal warning is not monitored. 1 - PGOOD inactive if the thermal warning flag is active.
1	PG_FAULT_GATES_PGGOOD	R/W	X	Type of operation for the PGOOD signal: 0 - Indicates live status of monitored voltage outputs. 1 - Indicates status of the PG_FAULT register, inactive when at least one PG_FAULT_x bit is inactive.
0	PGOOD_MODE	R/W	X	Operating mode for the PGOOD signal: 0 - Gated mode 1 - Continuous mode

### 7.6.1.24 PG\_FAULT

 PG\_FAULT is shown in [Table 7-55](#), Address: 0x17

**Table 7-54. PG\_FAULT Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use				PG_FAULT_LD O1	PG_FAULT_LD O0	PG_FAULT_BU CK1	PG_FAULT_BU CK0

**Table 7-55. PG\_FAULT Register Field Descriptions**

Bits	Field	Type	Default	Description
7:4	Reserved - do not use	R/W	0000	
3	PG_FAULT_LDO1	R/W	0	Source for the PGOOD inactive signal: 0 - LDO1 has not set the PGOOD signal inactive. 1 - LDO1 is selected for the PGOOD signal and it has set the PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when the LDO1 output is valid.
2	PG_FAULT_LDO0	R/W	0	Source for PGOOD inactive signal: 0 - LDO0 has not set the PGOOD signal inactive. 1 - LDO0 is selected for the PGOOD signal and it has set the PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when the LDO0 output is valid.
1	PG_FAULT_BUCK1	R/W	0	Source for PGOOD inactive signal: 0 - Buck1 has not set PGOOD signal inactive. 1 - Buck1 is selected for the PGOOD signal and it has set the PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when the Buck1 output is valid.
0	PG_FAULT_BUCK0	R/W	0	Source for PGOOD inactive signal: 0 - Buck0 has not set PGOOD signal inactive. 1 - Buck0 is selected for the PGOOD signal and it has set the PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when the Buck0 output is valid.

#### 7.6.1.25 RESET

RESET is shown in [Table 7-57](#), Address: 0x18

**Table 7-56. RESET Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use						SW_RESET	

**Table 7-57. RESET Register Field Descriptions**

Bits	Field	Type	Default	Description
7:1	Reserved - do not use	R/W	000 0000	
0	SW_RESET	R/W	0	Software commanded reset. When written to 1, the registers will be reset to the default values, the OTP memory is read, and the I <sup>2</sup> C interface is reset. The bit is automatically cleared.

#### 7.6.1.26 INT\_TOP\_1

INT\_TOP\_1 is shown in [Table 7-59](#), Address: 0x19

**Table 7-58. INT\_TOP\_1 Register**

D7	D6	D5	D4	D3	D2	D1	D0
PGOOD_INT	LDO_INT	BUCK_INT	SYNC_CLK_IN T	TDIE_SD_INT	TDIE_WARN_I NT	OVP_INT	I_MEAS_INT

**Table 7-59. INT\_TOP\_1 Register Field Descriptions**

Bits	Field	Type	Default	Description
7	PGOOD_INT	R/W	0	Latched status bit indicating that the PGOOD pin has changed from active to inactive. Write 1 to clear interrupt.

**Table 7-59. INT\_TOP\_1 Register Field Descriptions (continued)**

Bits	Field	Type	Default	Description
6	LDO_INT	R	0	Interrupt indicating that the LDO1 and LDO0 have a pending interrupt. The reason for the interrupt is indicated in the INT_LDO register. This bit is cleared automatically when the INT_LDO register is cleared to 0x00.
5	BUCK_INT	R	0	Interrupt indicating that the Buck1 and Buck0 have a pending interrupt. The reason for the interrupt is indicated in the INT_BUCK register. This bit is cleared automatically when INT_BUCK register is cleared to 0x00.
4	SYNC_CLK_INT	R/W	0	Latched status bit indicating that the external clock has appeared or disappeared. Write 1 to clear interrupt.
3	TDIE_SD_INT	R/W	0	Latched status bit indicating that the die junction temperature has exceeded the thermal shutdown level. The regulators have been disabled if they were enabled and the GPO and GPO2 signals are driven low. The regulators cannot be enabled if this bit is active. The actual status of the thermal shutdown is indicated by the TDIE_SD_STAT bit in the TOP_STAT register. Write 1 to clear interrupt.
2	TDIE_WARN_INT	R/W	0	Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by the TDIE_WARN_STAT bit in the TOP_STAT register. Write 1 to clear interrupt.
1	OVP_INT	R/W	0	Latched status bit indicating that the input voltage has exceeded the over-voltage detection level. The regulators have been disabled if they were enabled and the GPO and GPO2 signals are driven low. The actual status of the over-voltage is indicated by the OVP_STAT bit in the TOP_STAT register. Write 1 to clear interrupt.
0	I_MEAS_INT	R/W	0	Latched status bit indicating that the load current measurement result is available in the I_LOAD_1 and I_LOAD_2 registers. Write 1 to clear interrupt.

**7.6.1.27 INT\_TOP\_2**

INT\_TOP\_2 is shown in [Table 7-61](#), Address: 0x1A

**Table 7-60. INT\_TOP\_2 Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use							RESET_REG_INT

**Table 7-61. INT\_TOP\_2 Register Field Descriptions**

Bits	Field	Type	Default	Description
7:1	Reserved - do not use	R/W	000 0000	
0	RESET_REG_INT	R/W	0	Latched status bit indicating that either VANA supply voltage has been below the undervoltage threshold level or the host has requested a reset using the SW_RESET bit in RESET register. The regulators have been disabled, the registers are reset to the default values, and the normal startup procedure is done. Write 1 to clear interrupt.

**7.6.1.28 INT\_BUCK**

INT\_BUCK is shown in [Table 7-63](#), Address: 0x1B

**Table 7-62. INT\_BUCK Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use	BUCK1_PG_INT	BUCK1_SC_INT	BUCK1_ILIM_INT	Reserved - do not use	BUCK0_PG_INT	BUCK0_SC_INT	BUCK0_ILIM_INT

**Table 7-63. INT\_BUCK Register Field Descriptions**

Bits	Field	Type	Default	Description
7	Reserved - do not use	R/W	0	
6	BUCK1_PG_INT	R/W	0	Latched status bit indicating that Buck1 Power-Good event has been detected. Write 1 to clear.
5	BUCK1_SC_INT	R/W	0	Latched status bit indicating that the Buck1 output voltage has been over 1 ms below the short-circuit threshold level. Write 1 to clear.
4	BUCK1_ILIM_INT	R/W	0	Latched status bit indicating that the Buck1 output current limit has been active. Write 1 to clear.
3	Reserved - do not use	R/W	0	
2	BUCK0_PG_INT	R/W	0	Latched status bit indicating that the Buck0 Power-Good event has been detected. Write 1 to clear.
1	BUCK0_SC_INT	R/W	0	Latched status bit indicating that the Buck0 output voltage has been over 1 ms below the short-circuit threshold level. Write 1 to clear.
0	BUCK0_ILIM_INT	R/W	0	Latched status bit indicating that the Buck0 output current limit has been active. Write 1 to clear.

#### 7.6.1.29 INT\_LDO

INT\_LDO is shown in [Table 7-65](#), Address: 0x1C

**Table 7-64. INT\_LDO Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use	LDO1_PG_INT	LDO1_SC_INT	LDO1_ILIM_INT	Reserved - do not use	LDO0_PG_INT	LDO0_SC_INT	LDO0_ILIM_INT

**Table 7-65. INT\_LDO Register Field Descriptions**

Bits	Field	Type	Default	Description
7	Reserved - do not use	R/W	0	
6	LDO1_PG_INT	R/W	0	Latched status bit indicating that the LDO1 Power-Good event has been detected. Write 1 to clear.
5	LDO1_SC_INT	R/W	0	Latched status bit indicating that the LDO1 output voltage has been over 1 ms below the short-circuit threshold level. Write 1 to clear.
4	LDO1_ILIM_INT	R/W	0	Latched status bit indicating that the LDO1 output current limit has been active. Write 1 to clear.
3	Reserved - do not use	R/W	0	
2	LDO0_PG_INT	R/W	0	Latched status bit indicating that the LDO0 Power-Good event has been detected. Write 1 to clear.
1	LDO0_SC_INT	R/W	0	Latched status bit indicating that the LDO0 output voltage has been over 1 ms below the short-circuit threshold level. Write 1 to clear.
0	LDO0_ILIM_INT	R/W	0	Latched status bit indicating that the LDO0 output current limit has been active. Write 1 to clear.

#### 7.6.1.30 TOP\_STAT

TOP\_STAT is shown in [Table 7-67](#), Address: 0x1D

**Table 7-66. TOP\_STAT Register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

PGOOD_STAT	Reserved - do not use	SYNC_CLK_STAT	TDIE_SD_STAT	TDIE_WARN_STAT	OVP_STAT	Reserved - do not use
------------	-----------------------	---------------	--------------	----------------	----------	-----------------------

**Table 7-67. TOP\_STAT Register Field Descriptions**

Bits	Field	Type	Default	Description
7	PGOOD_STAT	R	0	Status bit indicating the status of the PGOOD pin: 0 - PGOOD pin is inactive. 1 - PGOOD pin is active.
6:5	Reserved - do not use	R	00	
4	SYNC_CLK_STAT	R	0	Status bit indicating the status of the external clock (CLKIN): 0 - External clock frequency is valid. 1 - External clock frequency is not valid.
3	TDIE_SD_STAT	R	0	Status bit indicating the status of the thermal shutdown: 0 - Die temperature below the thermal shutdown level. 1 - Die temperature above the thermal shutdown level.
2	TDIE_WARN_STAT	R	0	Status bit indicating the status of thermal warning: 0 - Die temperature below the thermal warning level. 1 - Die temperature above the thermal warning level.
1	OVP_STAT	R	0	Status bit indicating the status of the input overvoltage monitoring: 0 - Input voltage is below overvoltage threshold level. 1 - Input voltage above overvoltage threshold level.
0	Reserved - do not use	R	0	

### 7.6.1.31 BUCK\_STAT

 BUCK\_STAT is shown in [Table 7-69](#), Address: 0x1E

**Table 7-68. BUCK\_STAT Register**

D7	D6	D5	D4	D3	D2	D1	D0
BUCK1_STAT	BUCK1_PG_STAT	Reserved - do not use	BUCK1_ILIM_STAT	BUCK0_STAT	BUCK0_PG_STAT	Reserved - do not use	BUCK0_ILIM_STAT

**Table 7-69. BUCK\_STAT Register Field Descriptions**

Bits	Field	Type	Default	Description
7	BUCK1_STAT	R	0	Status bit indicating the enable and disable status of the Buck1: 0 - Buck1 regulator is disabled. 1 - Buck1 regulator is enabled.
6	BUCK1_PG_STAT	R	0	Status bit indicating the Buck1 output voltage validity (raw status): 0 - Buck1 output voltage is valid. 1 - Buck1 output voltage is invalid.
5	Reserved - do not use	R	0	
4	BUCK1_ILIM_STAT	R	0	Status bit indicating the Buck1 current limit status (raw status): 0 - Buck1 output current is below the current limit level. 1 - Buck1 output current limit is active.
3	BUCK0_STAT	R	0	Status bit indicating the enable and disable status of the Buck0: 0 - Buck0 regulator is disabled. 1 - Buck0 regulator is enabled.
2	BUCK0_PG_STAT	R	0	Status bit indicating the Buck0 output voltage validity (raw status): 0 - Buck0 output voltage is valid. 1 - Buck0 output voltage is invalid.
1	Reserved - do not use	R	0	

**Table 7-69. BUCK\_STAT Register Field Descriptions (continued)**

Bits	Field	Type	Default	Description
0	BUCK0_ILIM_STAT	R	0	Status bit indicating the Buck0 current limit status (raw status): 0 - Buck0 output current is below the current limit level. 1 - Buck0 output current limit is active.

### 7.6.1.32 LDO\_STAT

LDO\_STAT is shown in [Table 7-71](#), Address: 0x1F

**Table 7-70. LDO\_STAT Register**

D7	D6	D5	D4	D3	D2	D1	D0
LDO1_STAT	LDO1_PG_STAT	Reserved - do not use	LDO1_ILIM_STAT	LDO0_STAT	LDO0_PG_STAT	Reserved - do not use	LDO0_ILIM_STAT

**Table 7-71. LDO\_STAT Register Field Descriptions**

Bits	Field	Type	Default	Description
7	LDO1_STAT	R	0	Status bit indicating the enable and disable status of the LDO1: 0 - LDO1 regulator is disabled. 1 - LDO1 regulator is enabled.
6	LDO1_PG_STAT	R	0	Status bit indicating the LDO1 output voltage validity (raw status): 0 - LDO1 output voltage is valid. 1 - LDO1 output voltage is invalid.
5	Reserved - do not use	R	0	
4	LDO1_ILIM_STAT	R	0	Status bit indicating the LDO1 current limit status (raw status): 0 - LDO1 output current is below the current limit level. 1 - LDO1 output current limit is active.
3	LDO0_STAT	R	0	Status bit indicating the enable and disable status of the LDO0: 0 - LDO0 regulator is disabled. 1 - LDO0 regulator is enabled.
2	LDO0_PG_STAT	R	0	Status bit indicating the LDO0 output voltage validity (raw status): 0 - LDO0 output voltage is valid. 1 - LDO0 output voltage is invalid.
1	Reserved - do not use	R	0	
0	LDO0_ILIM_STAT	R	0	Status bit indicating the LDO0 current limit status (raw status): 0 - LDO0 output current is below the current limit level. 1 - LDO0 output current limit is active.

### 7.6.1.33 TOP\_MASK\_1

TOP\_MASK\_1 is shown in [Table 7-73](#), Address: 0x20

**Table 7-72. TOP\_MASK\_1 Register**

D7	D6	D5	D4	D3	D2	D1	D0
PGOOD_INT_MASK	Reserved - do not use		SYNC_CLK_MASK	Reserved - do not use	TDIE_WARN_MASK	Reserved - do not use	I_LOAD_READY_MASK

**Table 7-73. TOP\_MASK\_1 Register Field Descriptions**

Bits	Field	Type	Default	Description
7	PGOOD_INT_MASK	R/W	X	Masking for Power-Good interrupt (PGOOD_INT in INT_TOP_1 register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the PGOOD_STAT status bit in the TOP_STAT register.
6:5	Reserved - do not use	R/W	00	

**Table 7-73. TOP\_MASK\_1 Register Field Descriptions (continued)**

Bits	Field	Type	Default	Description
4	SYNC_CLK_MASK	R/W	X	Masking for the external clock detection interrupt (SYNC_CLK_INT in INT_TOP_1 register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the SYNC_CLK_STAT status bit in the TOP_STAT register.
3	Reserved - do not use	R/W	0	
2	TDIE_WARN_MASK	R/W	X	Masking for the thermal warning interrupt (TDIE_WARN_INT in INT_TOP_1 register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the TDIE_WARN_STAT status bit in the TOP_STAT register.
1	Reserved - do not use	R/W	0	
0	I_MEAS_MASK	R/W	X	Masking for the load current measurement ready interrupt (MEAS_INT in INT_TOP_1 register): 0 - Interrupt is generated. 1 - Interrupt is not generated.

**7.6.1.34 TOP\_MASK\_2**

TOP\_MASK\_2 is shown in [Table 7-75](#), Address: 0x21

**Table 7-74. TOP\_MASK\_2 Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use							RESET_REG_MASK

**Table 7-75. TOP\_MASK\_2 Register Field Descriptions**

Bits	Field	Type	Default	Description
7:1	Reserved - do not use	R/W	000 0000	
0	RESET_REG_MASK	R/W	X	Masking for register reset interrupt (RESET_REG_INT in INT_TOP_2 register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This change of this bit by I <sup>2</sup> C writing has no effect because it will be read from OTP memory during reset.

**7.6.1.35 BUCK\_MASK**

BUCK\_MASK is shown in [Table 7-77](#), Address: 0x22

**Table 7-76. BUCK\_MASK Register**

D7	D6	D5	D4	D3	D2	D1	D0
BUCK1_PGF_MASK	BUCK1_PGR_MASK	Reserved - do not use	BUCK1_ILIM_MASK	BUCK0_PGF_MASK	BUCK0_PGR_MASK	Reserved - do not use	BUCK0_ILIM_MASK

**Table 7-77. BUCK\_MASK Register Field Descriptions**

Bits	Field	Type	Default	Description
7	BUCK1_PGF_MASK	R/W	X	Masking of the Power Good invalid detection for the Buck1 power good interrupt (BUCK1_PG_INT in INT_BUCK register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the BUCK1_PG_STAT status bit in the BUCK_STAT register.

**Table 7-77. BUCK\_MASK Register Field Descriptions (continued)**

Bits	Field	Type	Default	Description
6	BUCK1_PGR_MASK	R/W	X	Masking of the Power Good valid detection for the Buck1 Power Good interrupt (BUCK1_PG_INT in INT_BUCK register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the BUCK1_PG_STAT status bit in the BUCK_STAT register.
5	Reserved - do not use	R	0	
4	BUCK1_ILIM_MASK	R/W	X	Masking for the Buck1 current limit detection interrupt (BUCK1_ILIM_INT in INT_BUCK register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the BUCK1_ILIM_STAT status bit in the BUCK_STAT register.
3	BUCK0_PGF_MASK	R/W	X	Masking of the Power Good invalid detection for the Buck0 power good interrupt (BUCK0_PG_INT in INT_BUCK register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STAT register.
2	BUCK0_PGR_MASK	R/W	X	Masking of the Power Good valid detection for the Buck0 power good interrupt (BUCK0_PG_INT in INT_BUCK register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the BUCK0_PG_STAT status bit in the BUCK_STAT register.
1	Reserved - do not use	R	0	
0	BUCK0_ILIM_MASK	R/W	X	Masking for the Buck0 current limit detection interrupt (BUCK0_ILIM_INT in INT_BUCK register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the BUCK0_ILIM_STAT status bit in the BUCK_STAT register.

### 7.6.1.36 LDO\_MASK

LDO\_MASK is shown in [Table 7-79](#), Address: 0x23

**Table 7-78. LDO\_MASK Register**

D7	D6	D5	D4	D3	D2	D1	D0
LDO1_PGF_MASK	LDO1_PGR_MASK	Reserved - do not use	LDO1_ILIM_MASK	LDO0_PGF_MASK	LDO0_PGR_MASK	Reserved - do not use	LDO0_ILIM_MASK

**Table 7-79. LDO\_MASK Register Field Descriptions**

Bits	Field	Type	Default	Description
7	LDO1_PGF_MASK	R/W	X	Masking of the Power Good invalid detection for the LDO1 power good interrupt (LDO1_PG_INT in INT_LDO register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the LDO1_PG_STAT status bit in the LDO_STAT register.
6	LDO1_PGR_MASK	R/W	X	Masking of the Power Good valid detection for the LDO1 power good interrupt (LDO1_PG_INT in INT_LDO register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the LDO1_PG_STAT status bit in the LDO_STAT register.
5	Reserved - do not use	R	0	
4	LDO1_ILIM_MASK	R/W	X	Masking for the LDO1 current limit detection interrupt (LDO1_ILIM_INT in INT_LDO register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the LDO1_ILIM_STAT status bit in the LDO_STAT register.

**Table 7-79. LDO\_MASK Register Field Descriptions (continued)**

Bits	Field	Type	Default	Description
3	LDO0_PGF_MASK	R/W	X	Masking of the Power Good invalid detection for the LDO0 power good interrupt (LDO0_PG_INT in INT_LDO register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the LDO0_PG_STAT status bit in the LDO_STAT register.
2	LDO0_PGR_MASK	R/W	X	Masking of Power Good valid detection for the LDO0 power good interrupt (LDO0_PG_INT in INT_LDO register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the LDO0_PG_STAT status bit in the LDO_STAT register.
1	Reserved - do not use	R	0	
0	LDO0_ILIM_MASK	R/W		Masking for the LDO0 current limit detection interrupt (LDO0_ILIM_INT in INT_LDO register): 0 - Interrupt is generated. 1 - Interrupt is not generated. This bit does not affect the LDO0_ILIM_STAT status bit in the LDO_STAT register.

**7.6.1.37 SEL\_I\_LOAD**SEL\_I\_LOAD is shown in [Table 7-81](#), Address: 0x24**Table 7-80. SEL\_I\_LOAD Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use							LOAD_CURRENT_BUCK_SELECT

**Table 7-81. SEL\_I\_LOAD Register Field Descriptions**

Bits	Field	Type	Default	Description
7:1	Reserved - do not use	R/W	000 0000	
0	LOAD_CURRENT_BUCK_SELECT	R/W	0	Start the current measurement on the selected regulator: 0 - Buck0 1 - Buck1 The measurement is started when the register is written. If the selected buck is master, then the measurement result is a sum current of the master and slave buck. If the selected buck is slave, then the measurement result is a current of the selected slave buck.

**7.6.1.38 I\_LOAD\_2**I\_LOAD\_2 is shown in [Table 7-83](#), Address: 0x25**Table 7-82. I\_LOAD\_2 Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved - do not use							BUCK_LOAD_CURRENT[8]

**Table 7-83. I\_LOAD\_2 Register Field Descriptions**

Bits	Field	Type	Default	Description
7:1	Reserved - do not use	R	000 0000	
0	BUCK_LOAD_CURRENT[8]	R	0	This register describes the MSB bit of the average load current on the selected regulator with a resolution of 20 mA per LSB and maximum 10.22-A current.

### 7.6.1.39 I\_LOAD\_1

I\_LOAD\_1 is shown in [Table 7-85](#), Address: 0x26

**Table 7-84. I\_LOAD\_1 Register**

D7	D6	D5	D4	D3	D2	D1	D0
BUCK_LOAD_CURRENT[7:0]							

**Table 7-85. I\_LOAD\_1 Register Field Descriptions**

Bits	Field	Type	Default	Description
7:0	BUCK_LOAD_CURRENT[7:0]	R	0000 0000	This register describes 8 LSB bits of the average load current on the selected regulator with a resolution of 20 mA per LSB and maximum 10.22-A current.

## 8 Application and Implementation

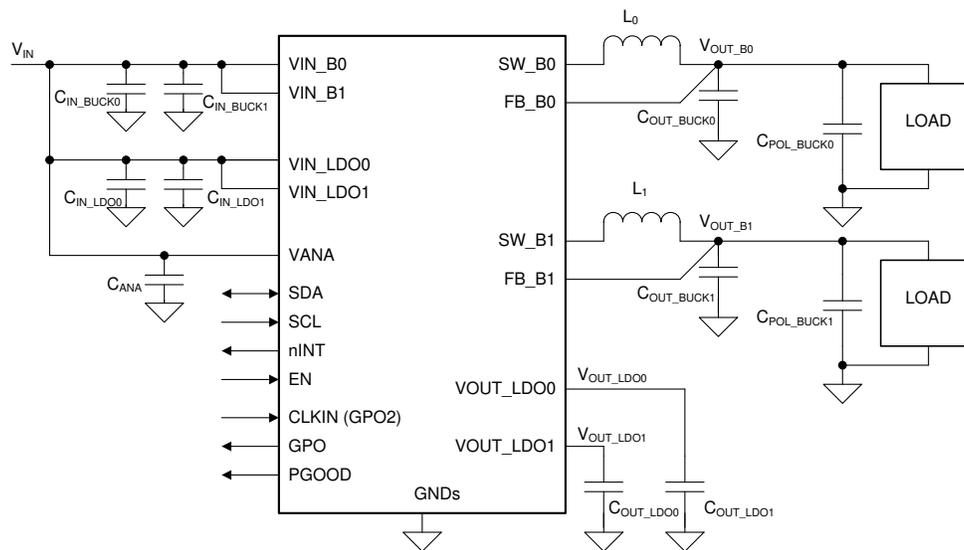
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

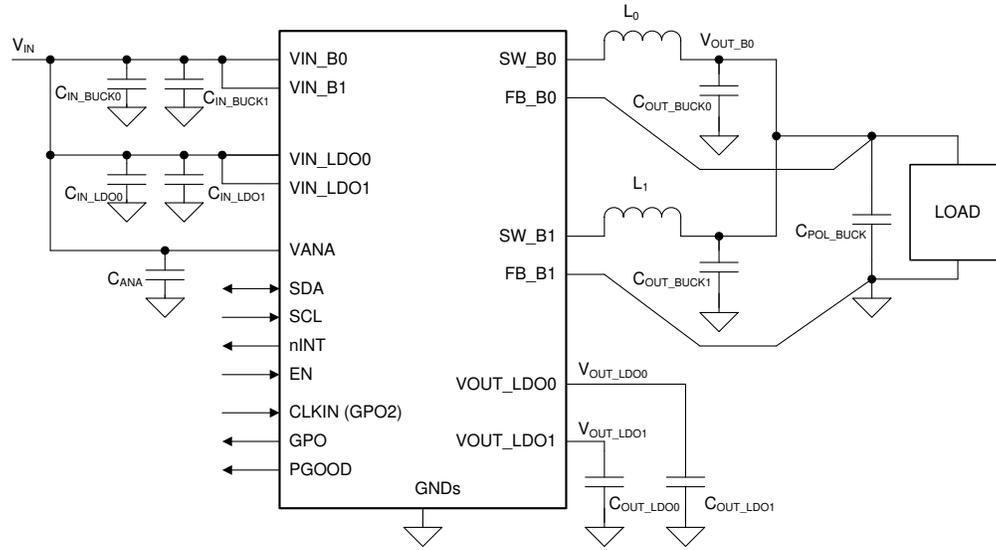
The LP8733xx-Q1 is a power management unit including two step-down regulators, two linear regulators, and two general-purpose digital output signals.

### 8.2 Typical Applications



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**Figure 8-1. Two Single-Phase Buck Outputs Configuration**



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Figure 8-2. Single Dual-Phase Buck Output Configuration

## 8.2.1 Design Requirements

### 8.2.1.1 Inductor Selection

The inductors  $L_0$  and  $L_1$  are shown in the [Section 8.2](#). The inductance and DCR of the inductor affects the control loop of the buck regulator. TI recommends using inductors similar to those listed in [Table 8-1](#). Pay attention to the saturation current and temperature rise current of the inductor. Check that the saturation current is higher than the peak current limit and the temperature rise current is higher than the maximum expected rms output current. The minimum effective inductance to ensure good performance is  $0.22 \mu\text{H}$  at maximum peak output current over the operating temperature range. DC resistance of the inductor must be less than  $0.05 \Omega$  for good efficiency at high-current conditions. The inductor AC loss also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Shielded inductors are preferred, as they radiate less noise.

Table 8-1. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS L × W × H (mm)	RATED DC CURRENT $I_{\text{SAT}}$ maximum (typical) / $I_{\text{TEMP}}$ maximum (typical) (A)	DCR typical / maximum (mΩ)
TOKO	DFE252012PD-R47M	$0.47 \mu\text{H}$ (20%)	$2.5 \times 2 \times 1.2$	$5.2 (-) / 4 (-)^{(1)}$	— / 27
Tayo Yuden	MDMK2020TR47MM V	$0.47 \mu\text{H}$ (20%)	$2 \times 2 \times 1.2$	$4.2 (4.8) / 2.3 (2.45)$	40 / 46

(1) Operating temperature range is up to  $125^\circ\text{C}$  including self temperature rise.

### 8.2.1.2 Buck Input Capacitor Selection

The input capacitors  $C_{\text{IN\_BUCK}0}$  and  $C_{\text{IN\_BUCK}1}$  are shown in the [Section 8.2](#). A ceramic input bypass capacitor of  $10 \mu\text{F}$  is required for each phase of the regulator. Place the input capacitor as close as possible to the  $\text{VIN\_Bx}$  pin and  $\text{PGND\_Bx}$  pin of the device. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. Also, the DC bias characteristics capacitors must be considered. The minimum effective input capacitance to ensure good performance is  $1.9 \mu\text{F}$  per buck input at maximum input voltage including tolerances, ambient temperature range, and aging (assuming at least  $22 \mu\text{F}$  of additional capacitance is common for all the power input pins on the system power rail). See [Table 8-2](#).

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. The low ESR of the ceramic capacitor provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. In addition, ferrite can be used in front of the input capacitor to reduce the EMI.

**Table 8-2. Recommended Buck Input Capacitor (X7R Dielectric)**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L × W × H (mm)	VOLTAGE RATING
Murata	GCM21BR71A106KE22	10 $\mu$ F (10%)	0805	2 × 1.25 × 1.25	10 V

### 8.2.1.3 Buck Output Capacitor Selection

The output capacitor  $C_{OUT\_BUCK0}$  and  $C_{OUT\_BUCK1}$  are shown in [Section 8.2](#). A ceramic local output capacitor of 22  $\mu$ F is required per phase. Use ceramic capacitors, X7R type; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. The output filter capacitor smooths out current flow from the inductor to the load, which helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. The minimum effective output capacitance to ensure good performance is 10  $\mu$ F per phase, including the DC voltage rolloff, tolerances, aging, and temperature effects.

The output voltage ripple is caused by the charging and discharging of the output capacitor and due to its  $R_{ESR}$ . The  $R_{ESR}$  is frequency dependent (and temperature dependent); ensure the value used for selection process is at the switching frequency of the part. See [Table 8-3](#).

POL capacitors  $C_{POL\_BUCKx}$  can be used to improve load transient performance and to decrease the ripple voltage. A higher output capacitance improves the load step behavior, reduces the output voltage ripple, and decreases the PFM switching frequency. However, output capacitance higher than 150  $\mu$ F per phase is not necessarily of any benefit. The output capacitor may be the limiting factor in the output voltage ramp, see [Section 6](#) for maximum output capacitance for different slew-rate settings. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at start-up, the time required to charge the output capacitor to target value might be longer. At shutdown, the output voltage is discharged to a 0.6 V level using forced-PWM operation. This can increase the input voltage if the load current is small and the output capacitor is large compared to input capacitor. Below the 0.6 V level, the output capacitor is discharged by the internal discharge resistor, and with large capacitor more time is required to settle  $V_{OUT}$  down as a consequence of the increased time constant.

**Table 8-3. Recommended Buck Output Capacitors (X7R Dielectric)**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L × W × H (mm)	VOLTAGE RATING
Murata	GCM31CR71A226KE02	22 $\mu$ F (10%)	1206	3.2 × 1.6 × 1.6	10 V

### 8.2.1.4 LDO Input Capacitor Selection

The input capacitors  $C_{IN\_LDO0}$  and  $C_{IN\_LDO1}$  are shown in the [Table 8-4](#). A ceramic input capacitor of 2.2  $\mu$ F, 6.3 V is sufficient for most applications. Place the input capacitor as close as possible to the  $V_{IN\_LDOx}$  pin and AGND pin of the device. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. DC bias characteristics of capacitors must be considered, the minimum effective input capacitance to ensure good performance is 0.6  $\mu$ F per LDO input at maximum input voltage including tolerances, ambient temperature range, and aging. See [Table 8-4](#).

**Table 8-4. Recommended LDO Input Capacitors (X7R Dielectric)**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L × W × H (mm)	VOLTAGE RATING
Murata	GCM188R70J225KE22	2.2 $\mu$ F (10%)	0603	1.6 × 0.8 × 0.8	6.3 V
Murata	GCM21BR71C475KA73	4.7 $\mu$ F (10%)	0805	2 × 1.25 × 1.25	16 V

### 8.2.1.5 LDO Output Capacitor Selection

The output capacitors  $C_{OUT\_LDO0}$  and  $C_{OUT\_LDO1}$  are shown in the [Section 8.2](#). A ceramic output capacitor of minimum 1.0  $\mu$ F is required. Place the output capacitor as close to the  $V_{OUT\_LDOx}$  pin and AGND pin of the device as possible. Use X7R type of capacitors, not Y5V or F. DC bias characteristics of capacitors must be

considered, the minimum effective output capacitance to ensure good performance is 0.4  $\mu\text{F}$  per LDO input at maximum input voltage including tolerances, ambient temperature range, and aging. See [Table 8-5](#).

Note: the output capacitor requirements excludes any capacitance seen at the point of load and only refers to the capacitance seen close to the device. Additional capacitance placed near the load can be supported, but the end application system should be evaluated for stability and to ensure the sequencing requirements are met. The shutdown decay will be longer with higher output capacitance, which can also impact the startup time. Total output capacitance should be kept below 100  $\mu\text{F}$ .

The output capacitance must be smaller than the input capacitance to ensure the stability of the LDO. With a 1- $\mu\text{F}$  output capacitor, TI recommends using at least a 2.2- $\mu\text{F}$  input capacitor; with a 2.2- $\mu\text{F}$  output capacitor at least 4.7- $\mu\text{F}$  input capacitance.

The VANA input is used to supply analog and digital circuits in the device. See [Table 8-6](#) for recommended components from for VANA input supply filtering.

**Table 8-5. Recommended LDO Output Capacitors (X7R Dielectric)**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L × W × H (mm)	VOLTAGE RATING
Murata	GCM188R71C105KA64	1 $\mu\text{F}$ (10%)	0603	1.6 × 0.8 × 0.8	16 V
Murata	GCM188R70J225KE22	2.2 $\mu\text{F}$ (10%)	0603	1.6 × 0.8 × 0.8	6.3 V

**Table 8-6. Recommended Supply Filtering Components**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L × W × H (mm)	VOLTAGE RATING
Murata	GCM155R71C104KA55	100 nF (10%)	0402	1 × 0.5 × 0.5	16 V
Murata	GCM188R71C104KA37	100 nF (10%)	0603	1.6 × 0.8 × 0.8	16 V

### 8.2.1.6 Current Limit vs. Maximum Output Current

The inductor current ripple can be calculated using [Equation 1](#) and [Equation 2](#):

$$D = \frac{V_{OUT}}{V_{IN(max)} \times \eta} \quad (1)$$

$$\Delta I_L = \frac{(V_{IN(max)} - V_{OUT}) \times D}{f_{SW} \times L} \quad (2)$$

Example using [Equation 1](#) and [Equation 2](#):

$$V_{IN(max)} = 5.5 \text{ V}$$

$$V_{OUT} = 1 \text{ V}$$

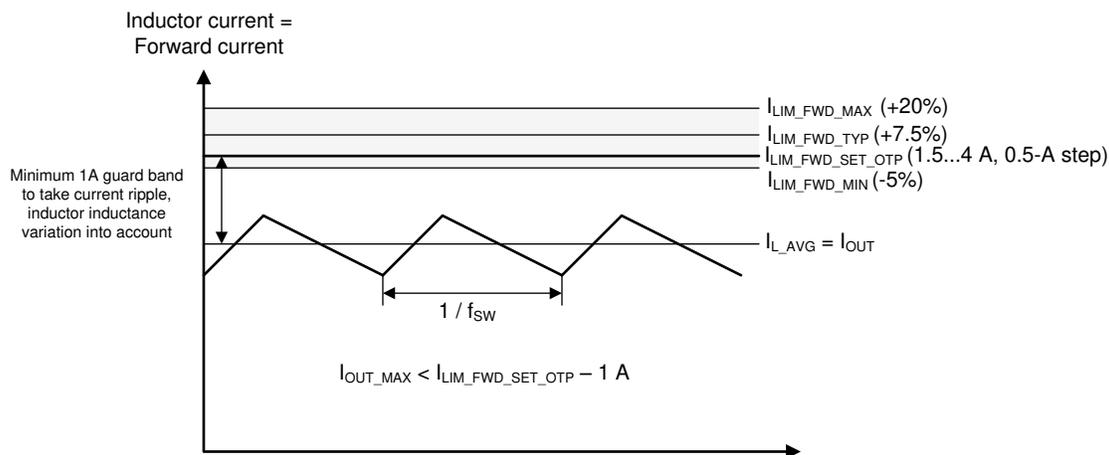
$$\eta = 0.75$$

$$f_{SW} = 1.8 \text{ MHz}$$

$$L = 0.38 \text{ } \mu\text{H}$$

$$\text{then } D = 0.242 \text{ and } \Delta I_L = 1.59 \text{ A}$$

Peak current is half of the current ripple. If  $I_{LIM\_FWD\_SET\_OTP}$  is 3 A, the minimum forward current limit would be 2.85 A when taking the –5% tolerance into account. In this case the difference between set peak current and maximum load current = 0.795 A + 0.15 A = 0.945 A.



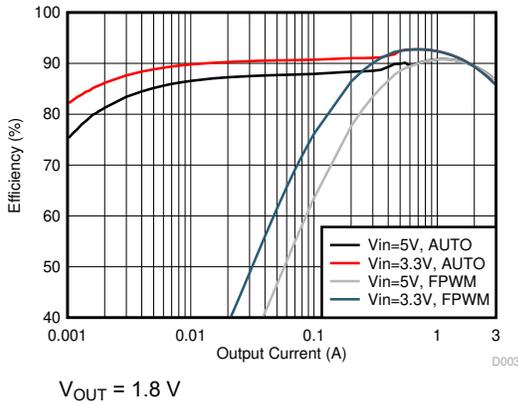
**Figure 8-3. Current Limit vs Maximum Output Current**

### 8.2.2 Detailed Design Procedure

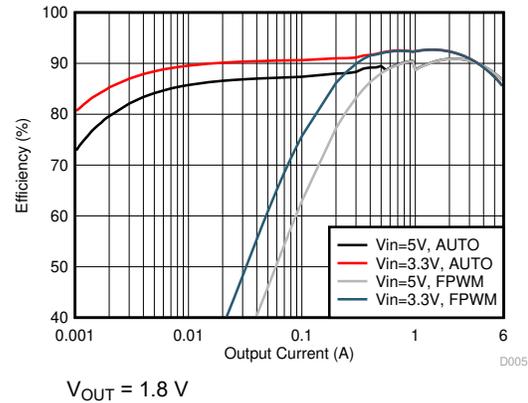
The performance of the LP8733xx-Q1 device depends greatly on the care taken in designing the printed circuit board (PCB). The use of low-inductance and low serial-resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention must be given to decoupling the power supplies. Decoupling capacitors must be connected close to the device and between the power and ground pins to support high peak currents being drawn from system power rail during turnon of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance, and capacitance can become performance limiting items. The separate buck regulator power pins  $V_{IN\_Bx}$  are not connected together internally. Connect the  $V_{IN\_Bx}$  power connections together outside the package using power plane construction.

### 8.2.3 Application Curves

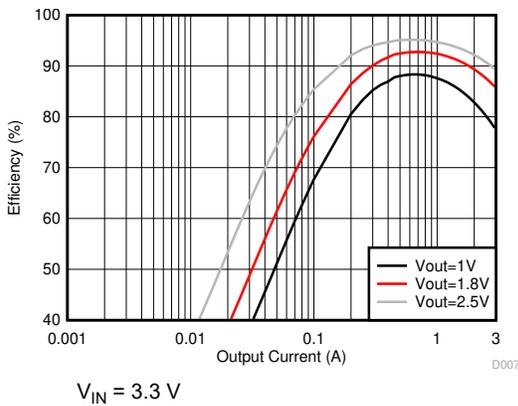
Measurements are done using typical application set up with connections shown in Section 8.2. Graphs may not reflect the OTP default settings. Unless otherwise specified:  $V_{(VIN\_Bx)} = V_{(VIN\_LDOx)} = V_{(VANA)} = 3.7\text{ V}$ ,  $V_{OUT\_Bx} = 1\text{ V}$ ,  $V_{OUT\_LDOx} = 1\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $L = 0.47\text{ }\mu\text{H}$  (TOKO DFE252012PD-R47M),  $C_{OUT\_BUCK} = 22\text{ }\mu\text{F}$  / phase, and  $C_{POL\_BUCK} = 22\text{ }\mu\text{F}$ ,  $C_{OUT\_LDO} = 1\text{ }\mu\text{F}$ .



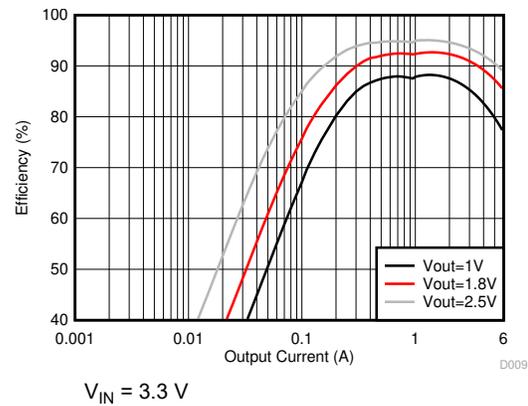
**Figure 8-4. Buck Efficiency in PFM/PWM and Forced PWM Mode (Single-Phase Output)**



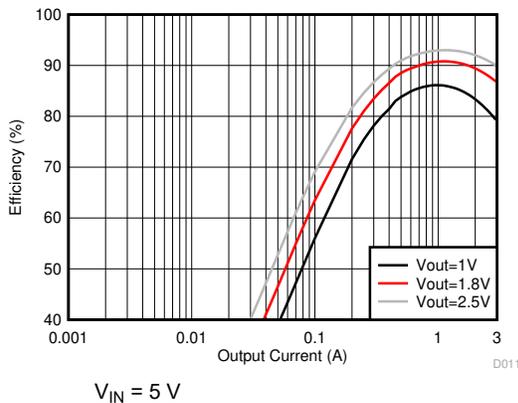
**Figure 8-5. Buck Efficiency in PFM/PWM and Forced PWM Mode (Dual-Phase Output)**



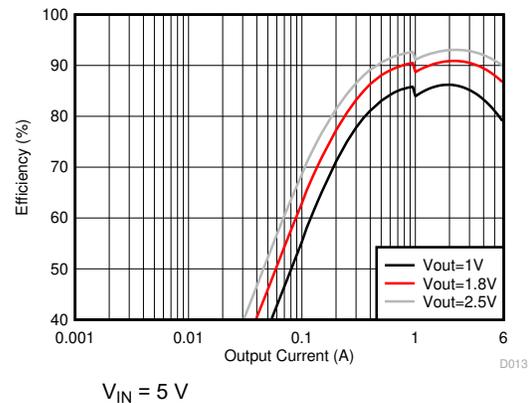
**Figure 8-6. Buck Efficiency in Forced PWM Mode (Single-Phase Output)**



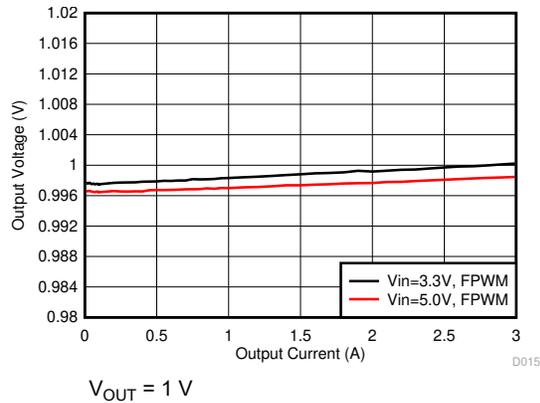
**Figure 8-7. Buck Efficiency in Forced PWM Mode (Dual-Phase Output)**



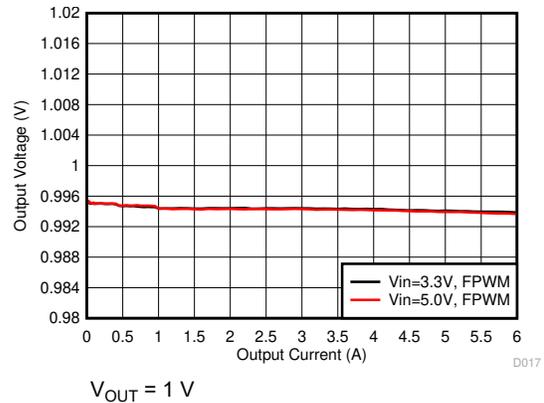
**Figure 8-8. Buck Efficiency in Forced PWM Mode (Single-Phase Output)**



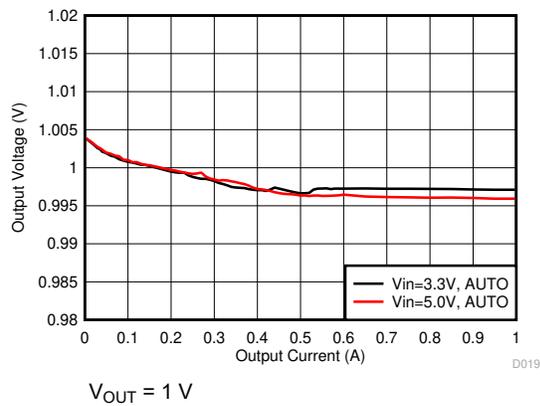
**Figure 8-9. Buck Efficiency in Forced PWM Mode (Dual-Phase Output)**



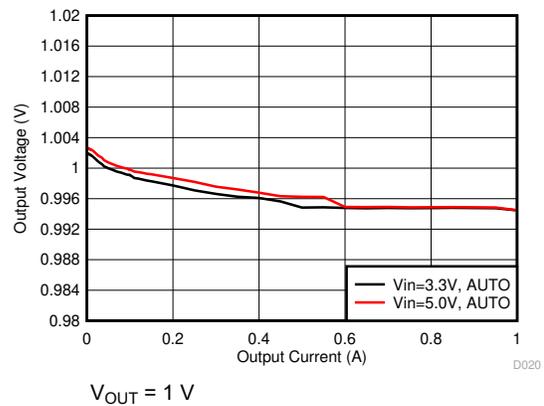
**Figure 8-10. Buck Output Voltage vs Load Current in Forced PWM Mode (Single-Phase Output)**



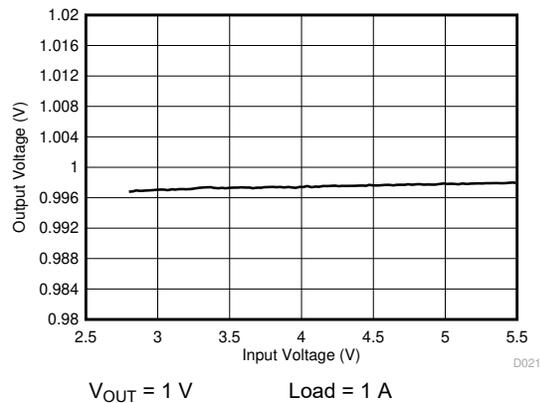
**Figure 8-11. Buck Output Voltage vs Load Current in Forced PWM Mode (Dual-Phase Output)**



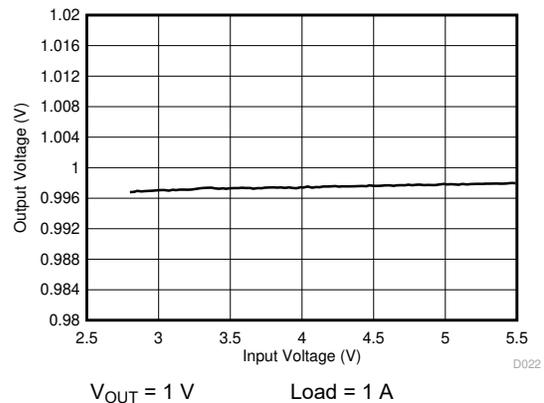
**Figure 8-12. Buck Output Voltage vs Load Current in PFM/PWM Mode (Single-Phase Output)**



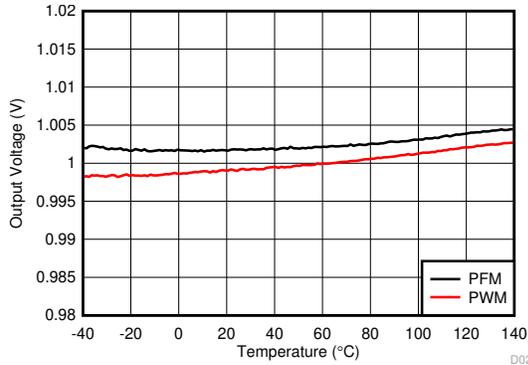
**Figure 8-13. Buck Output Voltage vs Load Current in PFM/PWM Mode (Dual-Phase Output)**



**Figure 8-14. Buck Output Voltage vs Input Voltage in PWM Mode (Single-Phase Output)**

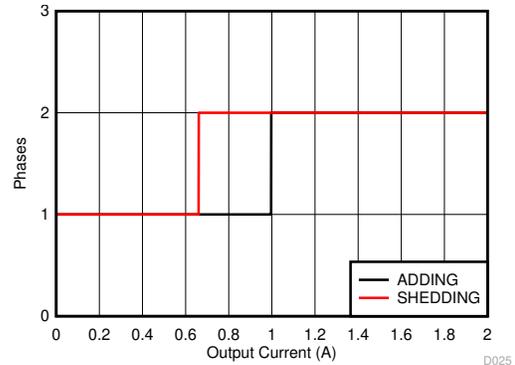


**Figure 8-15. Buck Output Voltage vs Input Voltage in PWM Mode (Dual-Phase Output)**



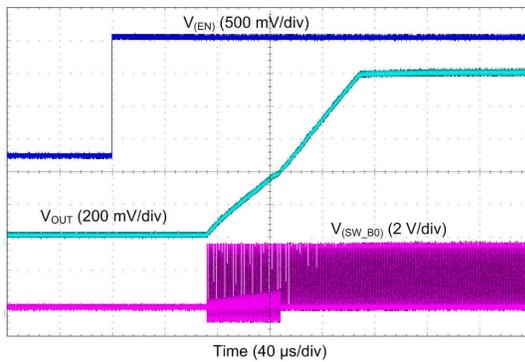
Load = 1 A (PWM) and 0.1 A (PFM)

Figure 8-16. Buck Output Voltage vs Temperature



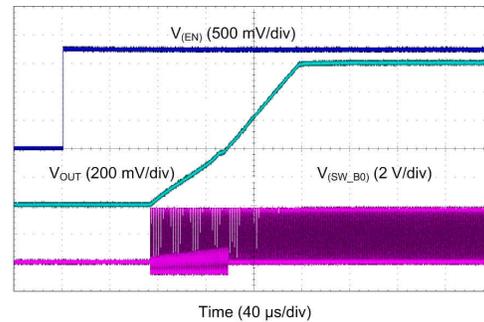
$V_{IN} = 3.7 V$

Figure 8-17. Buck Phase Adding and Shedding vs Load Current (Dual-Phase Output)



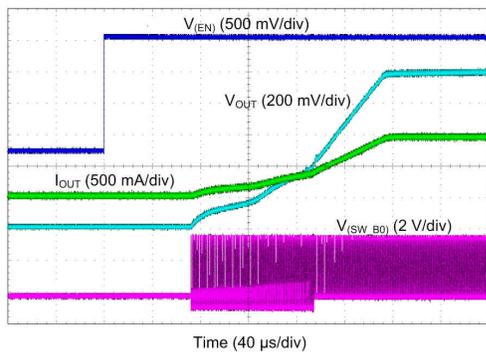
Slew-rate = 10 mV/μs  $I_{LOAD} = 0 A$   $V_{OUT} = 1 V$

Figure 8-18. Buck Start-Up With EN1, Forced PWM Mode (Single-Phase Output)



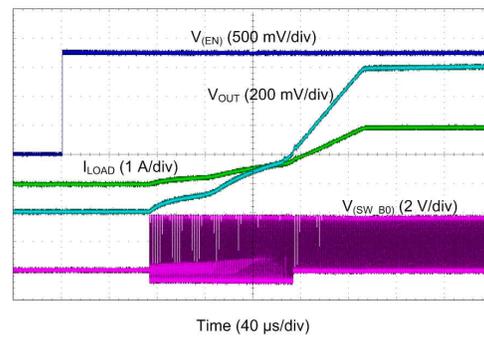
Slew-rate = 10 mV/μs  $I_{LOAD} = 0 A$   $V_{OUT} = 1 V$

Figure 8-19. Buck Start-Up With EN1, Forced PWM Mode (Dual-Phase Output)



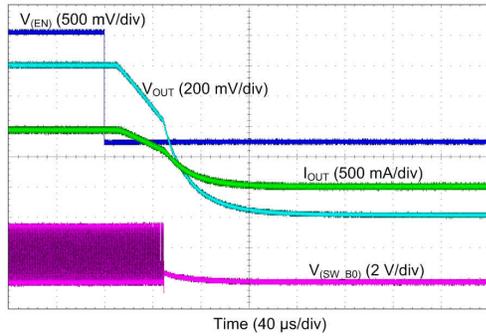
Slew-rate = 10 mV/μs  $R_{LOAD} = 1 \Omega$   $V_{OUT} = 1 V$

Figure 8-20. Buck Start-Up with EN1, Forced PWM Mode (Single-Phase Output)



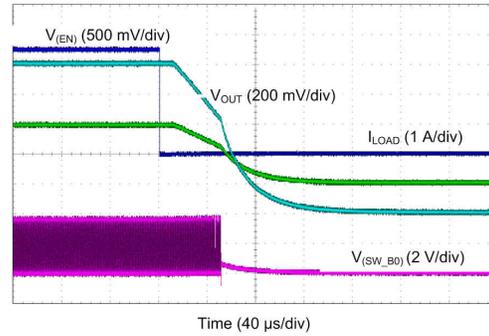
Slew-rate = 10 mV/μs  $R_{LOAD} = 0.5 \Omega$   $V_{OUT} = 1 V$

Figure 8-21. Buck Start-Up with EN1, Forced PWM Mode (Dual-Phase Output)



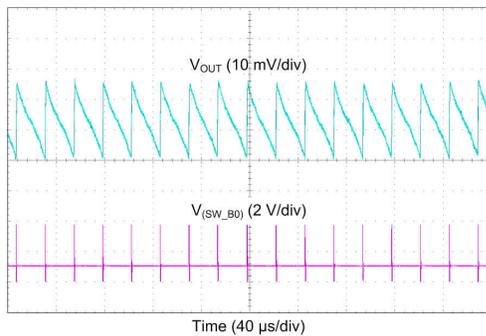
Slew-rate = 10 mV/μs       $R_{LOAD} = 1 \Omega$        $V_{OUT} = 1 V$

**Figure 8-22. Buck Shutdown With EN1, Forced PWM Mode (Single-Phase Output)**



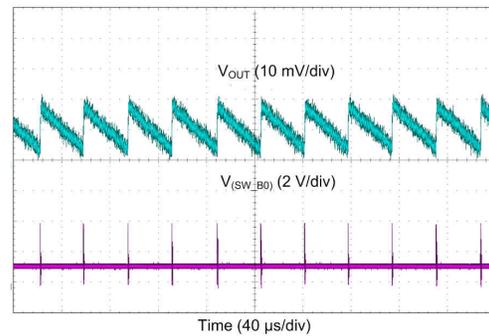
Slew-rate = 10 mV/μs       $R_{LOAD} = 0.5 \Omega$        $V_{OUT} = 1 V$

**Figure 8-23. Buck Shutdown With EN1, Forced PWM Mode (Dual-Phase Output)**



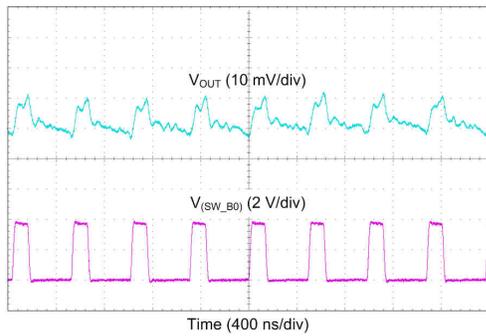
$I_{OUT} = 10 mA$

**Figure 8-24. Buck Output Voltage Ripple, PFM Mode (Single-Phase Output)**



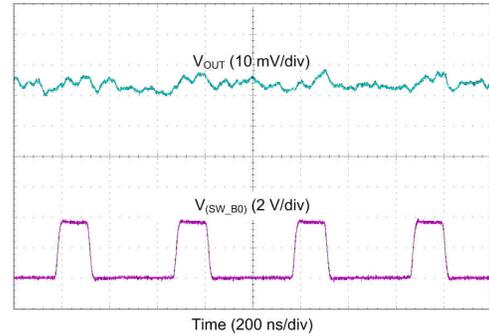
$I_{OUT} = 10 mA$

**Figure 8-25. Buck Output Voltage Ripple, PFM Mode (Dual-Phase Output)**



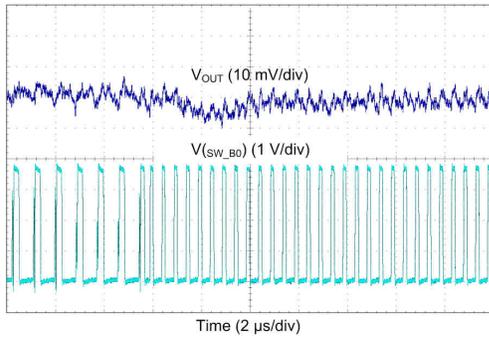
$I_{OUT} = 200 mA$

**Figure 8-26. Buck Output Voltage Ripple, Forced PWM Mode (Single-Phase Output)**

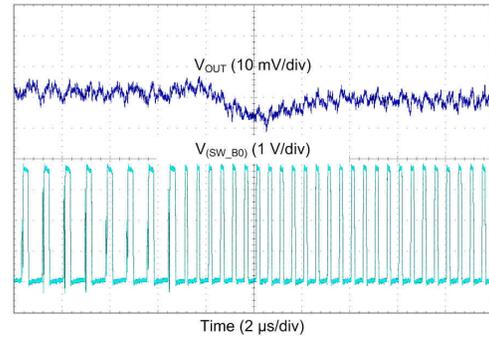


$I_{OUT} = 200 mA$

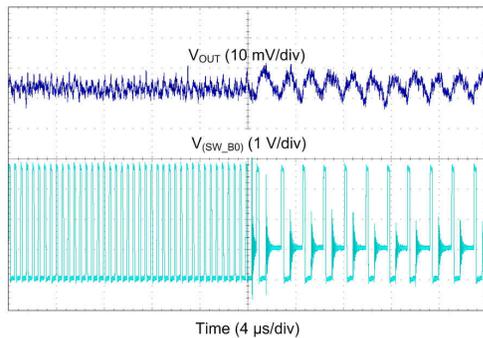
**Figure 8-27. Buck Output Voltage Ripple, Forced PWM Mode (Dual-Phase Output)**



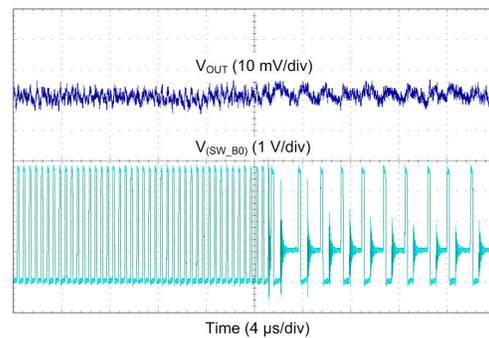
**Figure 8-28. Buck Transient From PFM-to-PWM Mode (Single-Phase Output)**



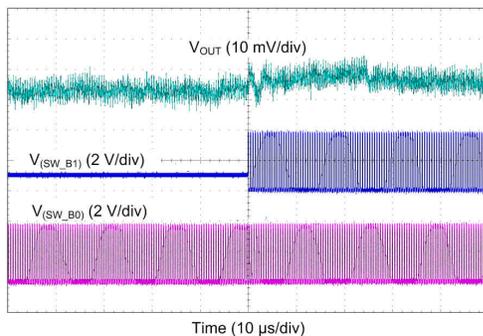
**Figure 8-29. Buck Transient From PFM-to-PWM Mode (Dual-Phase Output)**



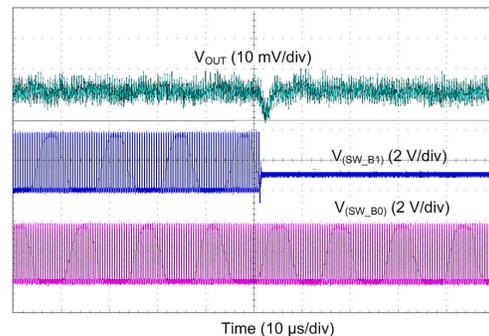
**Figure 8-30. Buck Transient From PWM-to-PFM Mode (Single-Phase Output)**



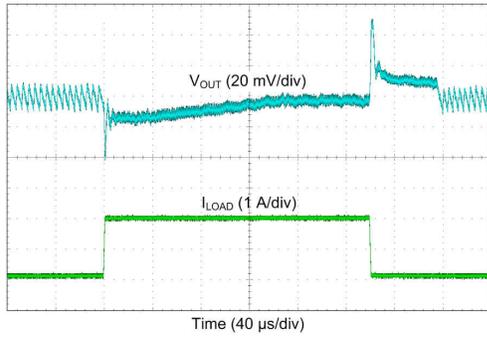
**Figure 8-31. Buck Transient From PWM-to-PFM Mode (Dual-Phase Output)**



**Figure 8-32. Buck Transient From 1-Phase to 2-Phase Operation (Dual-Phase Output)**

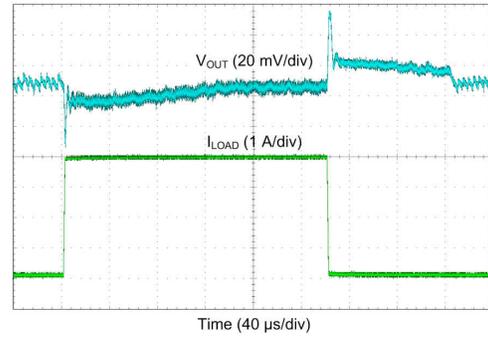


**Figure 8-33. Buck Transient From 2-Phase to 1-Phase Operation (Dual-Phase Output)**



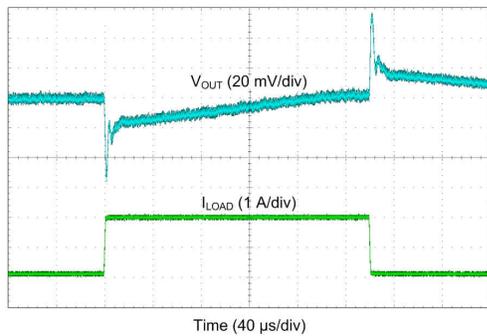
$I_{OUT} = 0.1\text{ A} \rightarrow 2\text{ A} \rightarrow 0.1\text{ A}$      $T_R = T_F = 400\text{ ns}$

**Figure 8-34. Buck Transient Load Step Response, AUTO Mode (Single-Phase Output)**



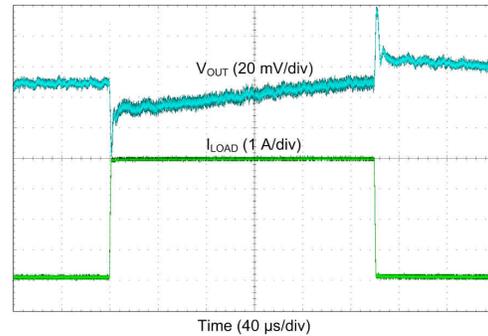
$I_{OUT} = 0.1\text{ A} \rightarrow 4\text{ A} \rightarrow 0.1\text{ A}$      $T_R = T_F = 400\text{ ns}$

**Figure 8-35. Buck Transient Load Step Response, AUTO Mode (Dual-Phase Output)**



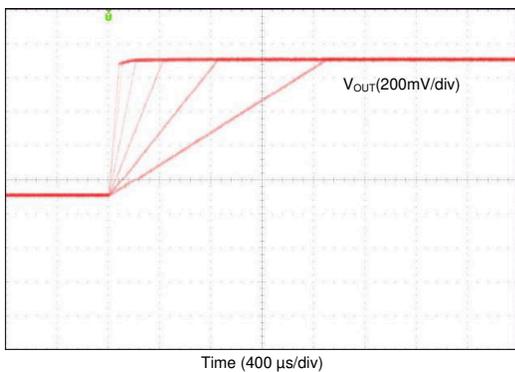
$I_{OUT} = 0.1\text{ A} \rightarrow 2\text{ A} \rightarrow 0.1\text{ A}$      $T_R = T_F = 400\text{ ns}$

**Figure 8-36. Buck Transient Load Step Response, Forced PWM Mode (Single-Phase Output)**

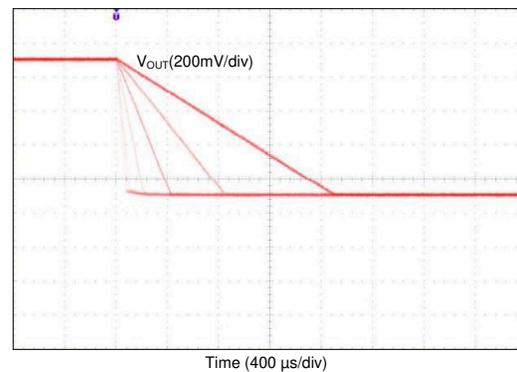


$I_{OUT} = 0.1\text{ A} \rightarrow 4\text{ A} \rightarrow 0.1\text{ A}$      $T_R = T_F = 400\text{ ns}$

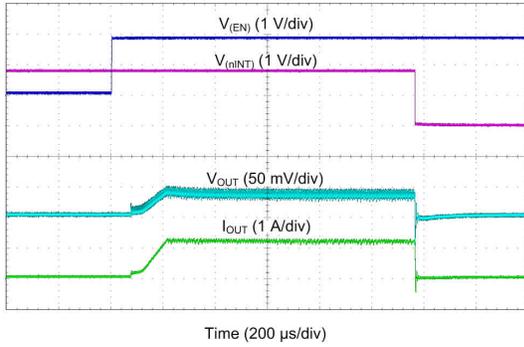
**Figure 8-37. Buck Transient Load Step Response, Forced PWM Mode (Dual-Phase Output)**



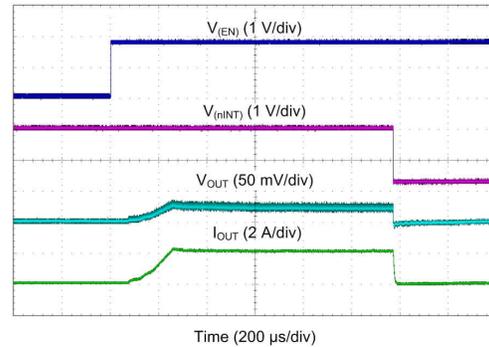
**Figure 8-38. Buck  $V_{OUT}$  Transition from 0.6 V to 1.4 V With Different Slew Rate Settings**



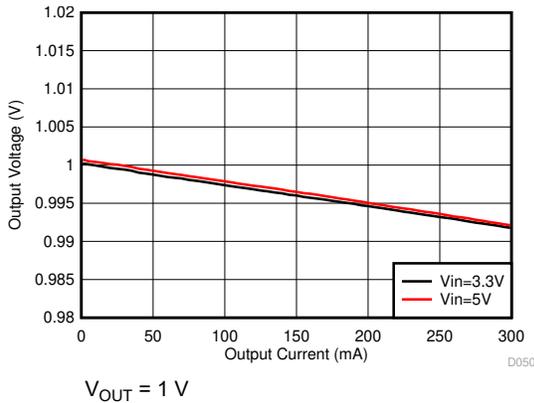
**Figure 8-39. Buck  $V_{OUT}$  Transition from 1.4 V to 0.6 V With Different Slew Rate Settings**



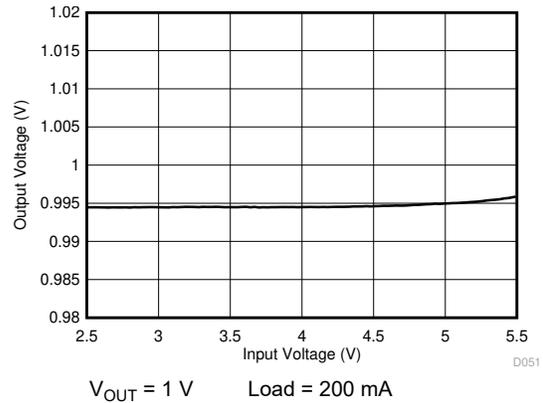
**Figure 8-40. Buck Start-Up With Short on Output (Single-Phase Output)**



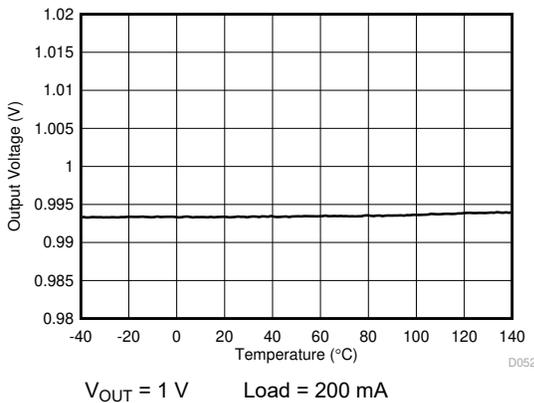
**Figure 8-41. Buck Start-Up With Short on Output (Dual-Phase Output)**



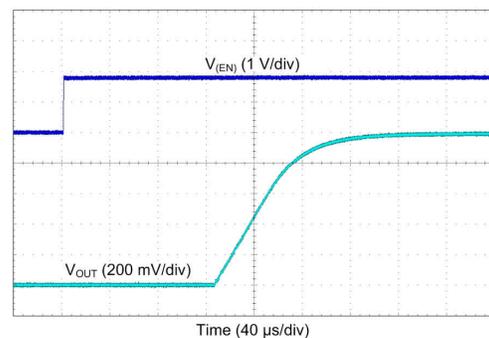
**Figure 8-42. LDO Output Voltage vs Load Current**



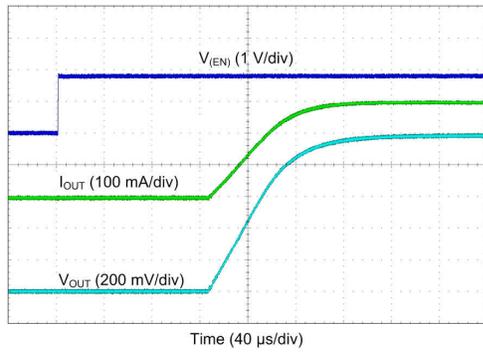
**Figure 8-43. LDO Output Voltage vs Input Voltage**



**Figure 8-44. LDO Output Voltage vs Temperature**

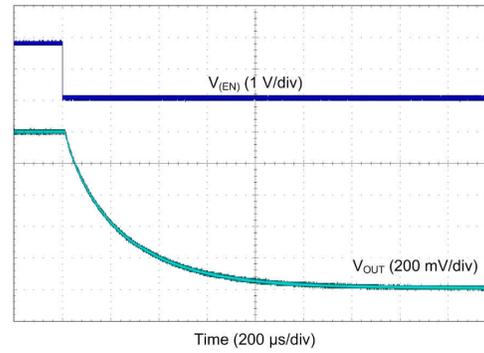


**Figure 8-45. LDO Start-Up**



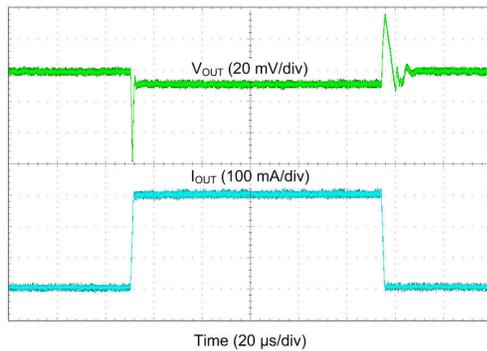
$R_{LOAD} = 3.3 \Omega$        $V_{OUT} = 1 V$

**Figure 8-46. LDO Start-Up**



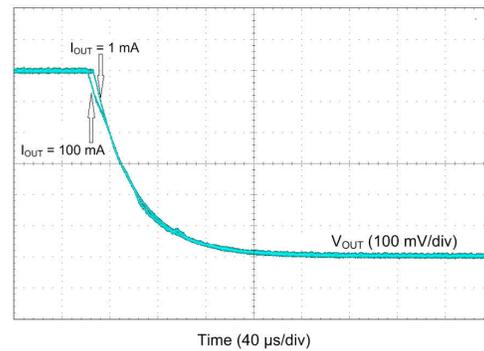
$I_{LOAD} = 0 A$        $V_{OUT} = 1 V$

**Figure 8-47. LDO Shutdown**

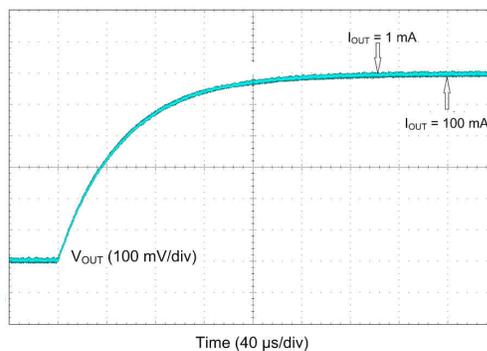


$I_{OUT} = 0 A \rightarrow 0.3 A \rightarrow 0 A$        $T_R = T_F = 1 \mu s$

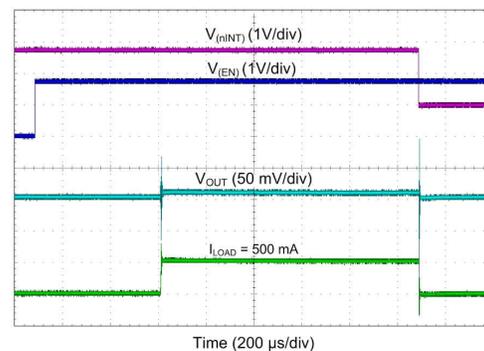
**Figure 8-48. LDO Transient Load Step Response**



**Figure 8-49. LDO  $V_{OUT}$  Transition from 1.8 V to 1.2 V**



**Figure 8-50. LDO  $V_{OUT}$  Transition from 1.2 V to 1.8 V**



Start-up  
delay is 500  
 $\mu s$

**Figure 8-51. LDO Start-Up With Short on Output**

## 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.8 V and 5.5 V. The VANA input and VIN\_Bx buck inputs must be connected together, and they must use the same input supply. This input supply must be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail must be low enough that the input current transient does not cause too high a drop in the LP8733xx-Q1 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP8733xx-Q1, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The VIN\_LDOx LDO input supply voltage range is 2.5 V to 5.5 V and can be higher or lower than VANA supply voltage.

## 10 Layout

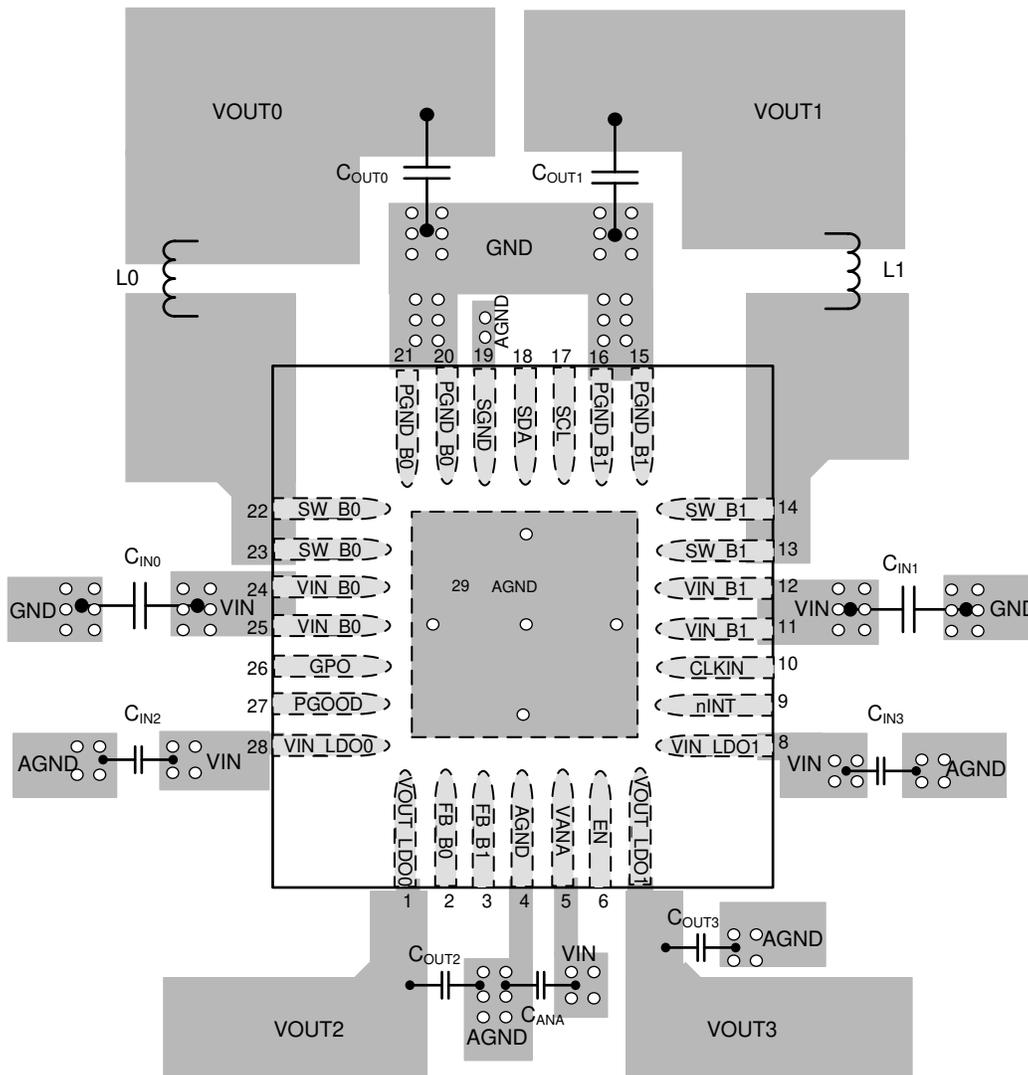
### 10.1 Layout Guidelines

The high frequency and large switching currents of the LP8733xx-Q1 make the choice of layout important. Good power supply results only occur when care is given to proper design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to several amps, good power supply layout is much more difficult than most general PCB design. Use the following steps as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place  $C_{IN}$  as close as possible to the VIN\_Bx pin and the PGND\_Bx pin. Route the  $V_{IN}$  trace wide and thick to avoid IR drops. The trace between the positive node of the input capacitor and the VIN\_Bx pins of LP8733xx-Q1, as well as the trace between the negative node of the input capacitor and the power PGND\_Bx pins, must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor — parasitic inductance on these traces must be kept as small as possible for proper device operation. The parasitic inductance can be reduced by using a ground plane as close as possible to the top layer by using thin dielectric layer between the top layer and the ground plane.
2. The output filter, consisting of L and COUT, converts the switching signal at SW\_Bx to the noiseless output voltage. The output filter must be placed as close as possible to the device, keeping the switch node small for best EMI behavior. Route the traces between the output capacitors of the LP8733xx-Q1 and the input capacitors of the load direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VANA and AGND) must be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VANA pin.
4. If remote voltage sensing can be used for the load, connect the LP8733xx-Q1 feedback pins FB\_Bx to the respective sense pins on the load capacitor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND\_Bx, VIN\_Bx, and SW\_Bx, as well as high bandwidth signals such as the I<sup>2</sup>C. Avoid both capacitive and inductive coupling by keeping the sense lines short and direct, and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. If series resistors are used for load current measurement, place them after connection of the voltage feedback.
5. PGND\_Bx, VIN\_Bx and SW\_Bx must be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND\_Bx, VIN\_Bx and SW\_Bx.
6. LDO performance (PSRR, noise, and transient response) depend on the layout of the PCB. Best performance is achieved by placing CIN and COUT as close to the LP8733xx-Q1 device as practical. The ground connections for CIN and COUT must be back to the LP8733xx-Q1 AGND with as wide and as short of a copper trace as is practical and with multiple vias if routing is done on other layer. Avoid connections using long trace lengths, narrow trace widths, or connection through small via. These add parasitic inductances and resistance that results in inferior performance, especially during transient conditions.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces can sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ( $R_{\theta JA}$ ) and junction-to-board ( $R_{\theta JB}$ ) thermal resistances, thereby reducing the device junction temperature,  $T_J$ . TI strongly recommends performance of a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process by using a thermal modeling analysis software.

## 10.2 Layout Example



**Figure 10-1. LP8733xx-Q1 Board Layout**

In dual-phase buck configuration, short VOUT0 and VOUT1 together.

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

#### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LP873300RHDRQ1</a>	Active	Production	VQFN (RHD)   28	3000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	LP8733 00-Q1
LP873300RHDRQ1.A	Active	Production	VQFN (RHD)   28	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8733 00-Q1
<a href="#">LP873300RHDTQ1</a>	Active	Production	VQFN (RHD)   28	250   SMALL T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	LP8733 00-Q1
LP873300RHDTQ1.A	Active	Production	VQFN (RHD)   28	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8733 00-Q1
<a href="#">LP873344RHDRQ1</a>	Active	Production	VQFN (RHD)   28	3000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	LP8733 44-Q1
LP873344RHDRQ1.A	Active	Production	VQFN (RHD)   28	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8733 44-Q1
<a href="#">LP873344RHDTQ1</a>	Active	Production	VQFN (RHD)   28	250   SMALL T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	LP8733 44-Q1
LP873344RHDTQ1.A	Active	Production	VQFN (RHD)   28	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8733 44-Q1
<a href="#">LP873344RHDRQ1</a>	Active	Production	VQFN (RHD)   28	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LP8733 4A-Q1
LP873344RHDRQ1.A	Active	Production	VQFN (RHD)   28	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LP8733 4A-Q1

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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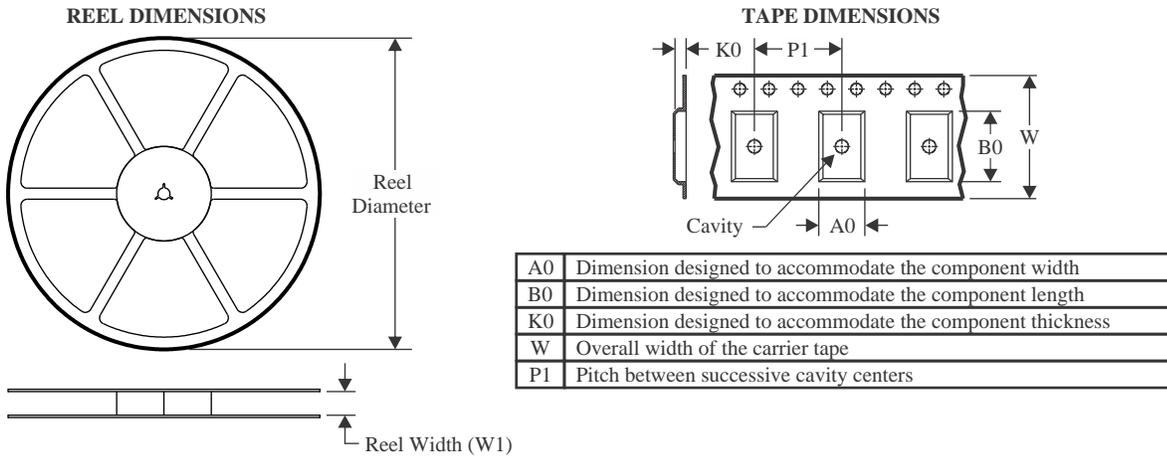
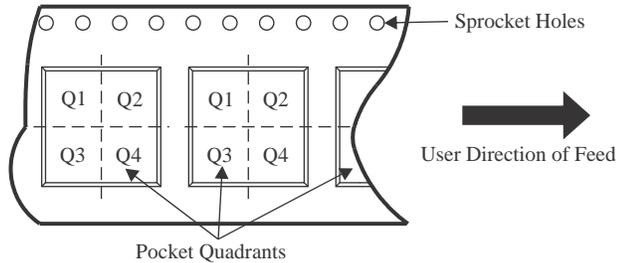
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LP8733-Q1 :**

- Catalog : [LP8733](#)

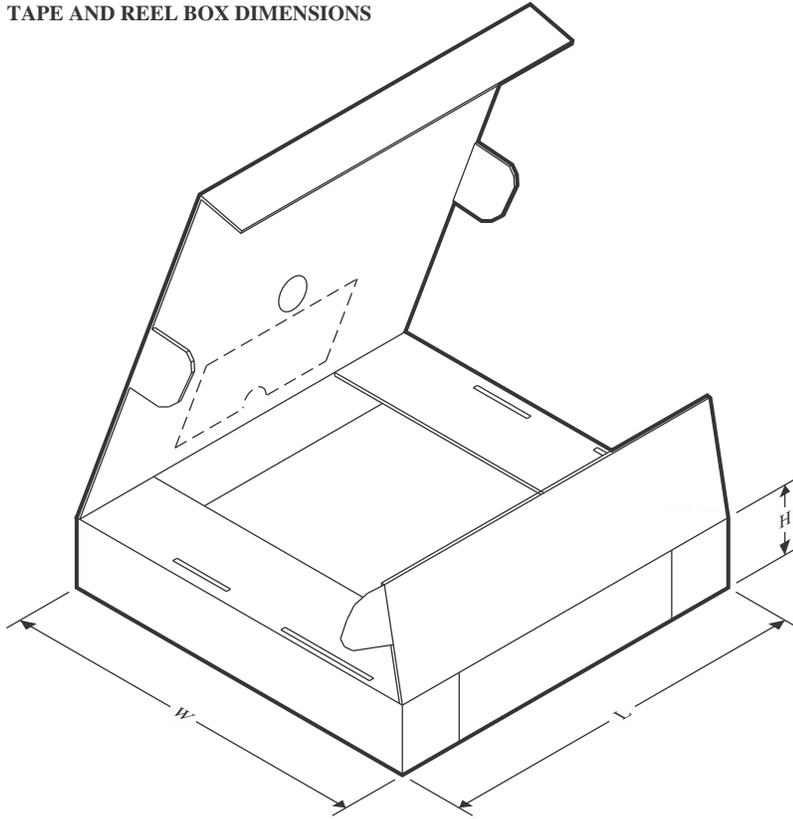
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP873300RHDRQ1	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LP873300RHDTQ1	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LP873344RHDRQ1	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LP873344RHDTQ1	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LP873344ARHDRQ1	VQFN	RHD	28	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP873300RHDRQ1	VQFN	RHD	28	3000	367.0	367.0	35.0
LP873300RHDTQ1	VQFN	RHD	28	250	210.0	185.0	35.0
LP873344RHDRQ1	VQFN	RHD	28	3000	367.0	367.0	35.0
LP873344RHDTQ1	VQFN	RHD	28	250	210.0	185.0	35.0
LP87334ARHDRQ1	VQFN	RHD	28	3000	367.0	367.0	38.0

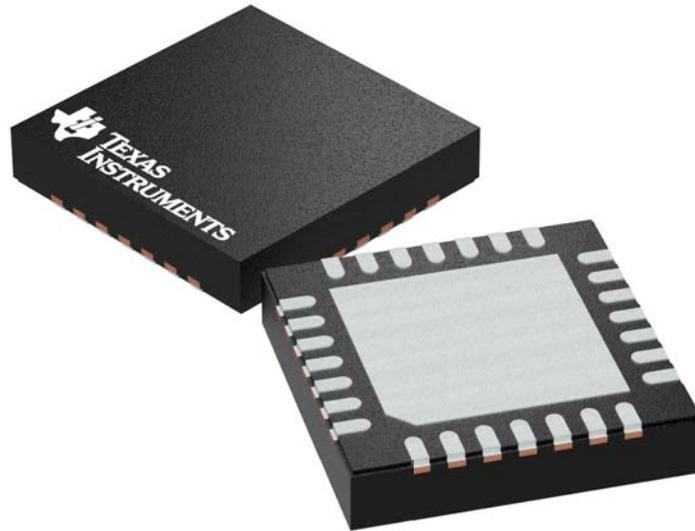
**GENERIC PACKAGE VIEW**

**RHD 28**

**VQFN - 1 mm max height**

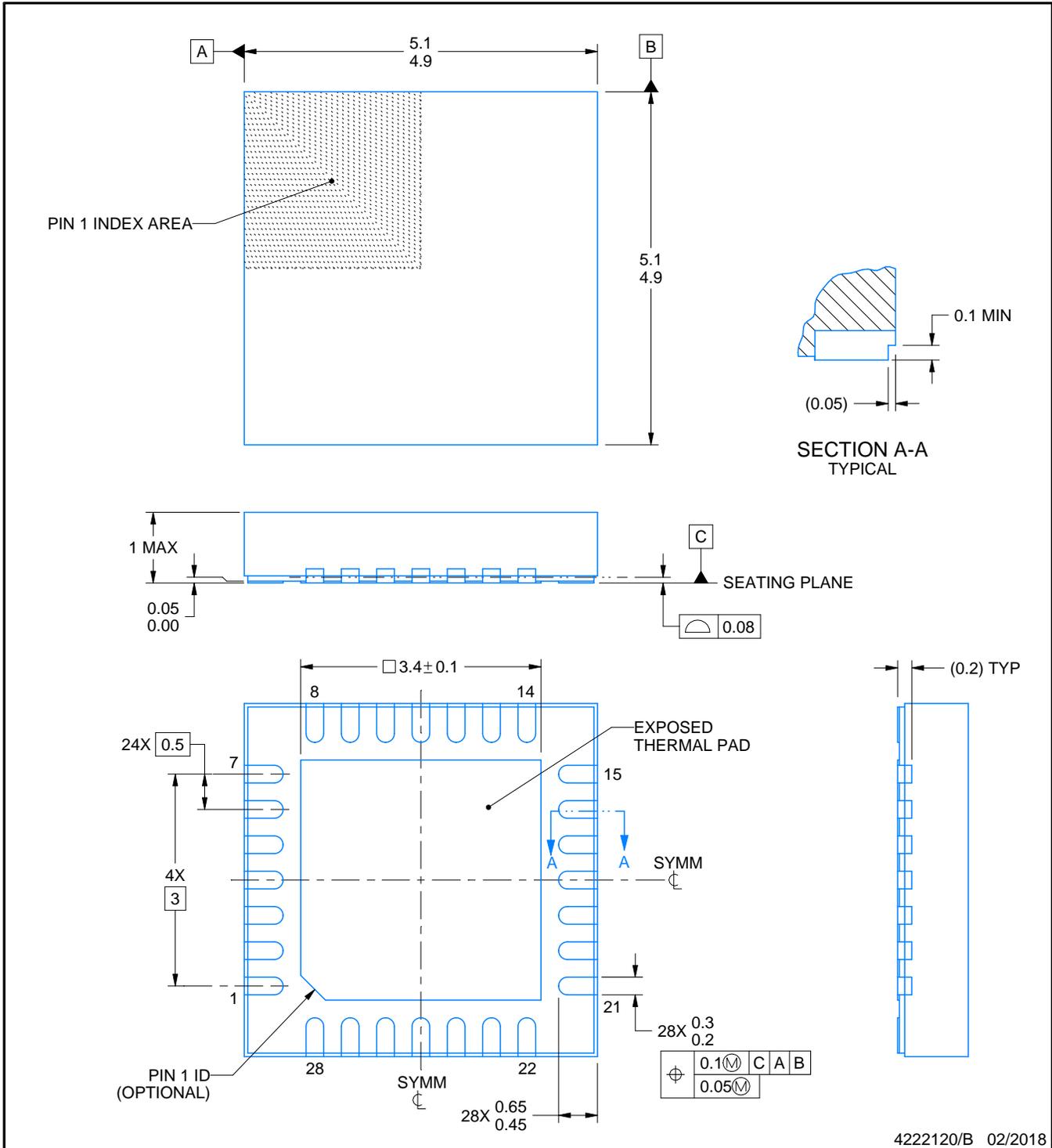
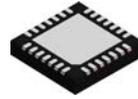
**5 x 5 mm, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204400/G



NOTES:

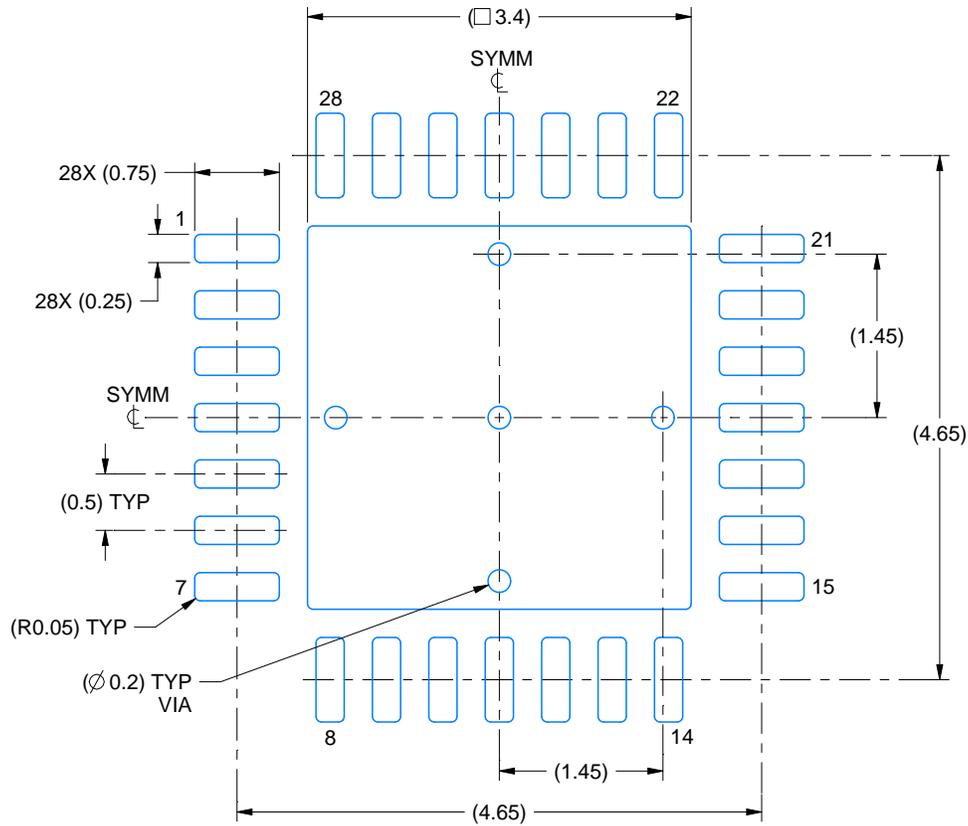
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

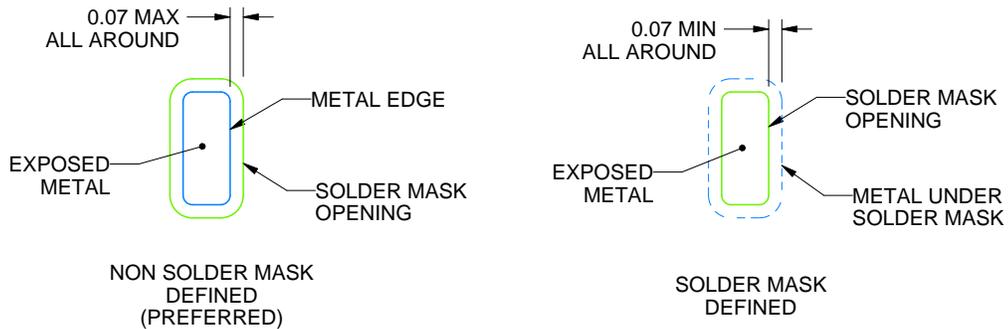
RHD0028W

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

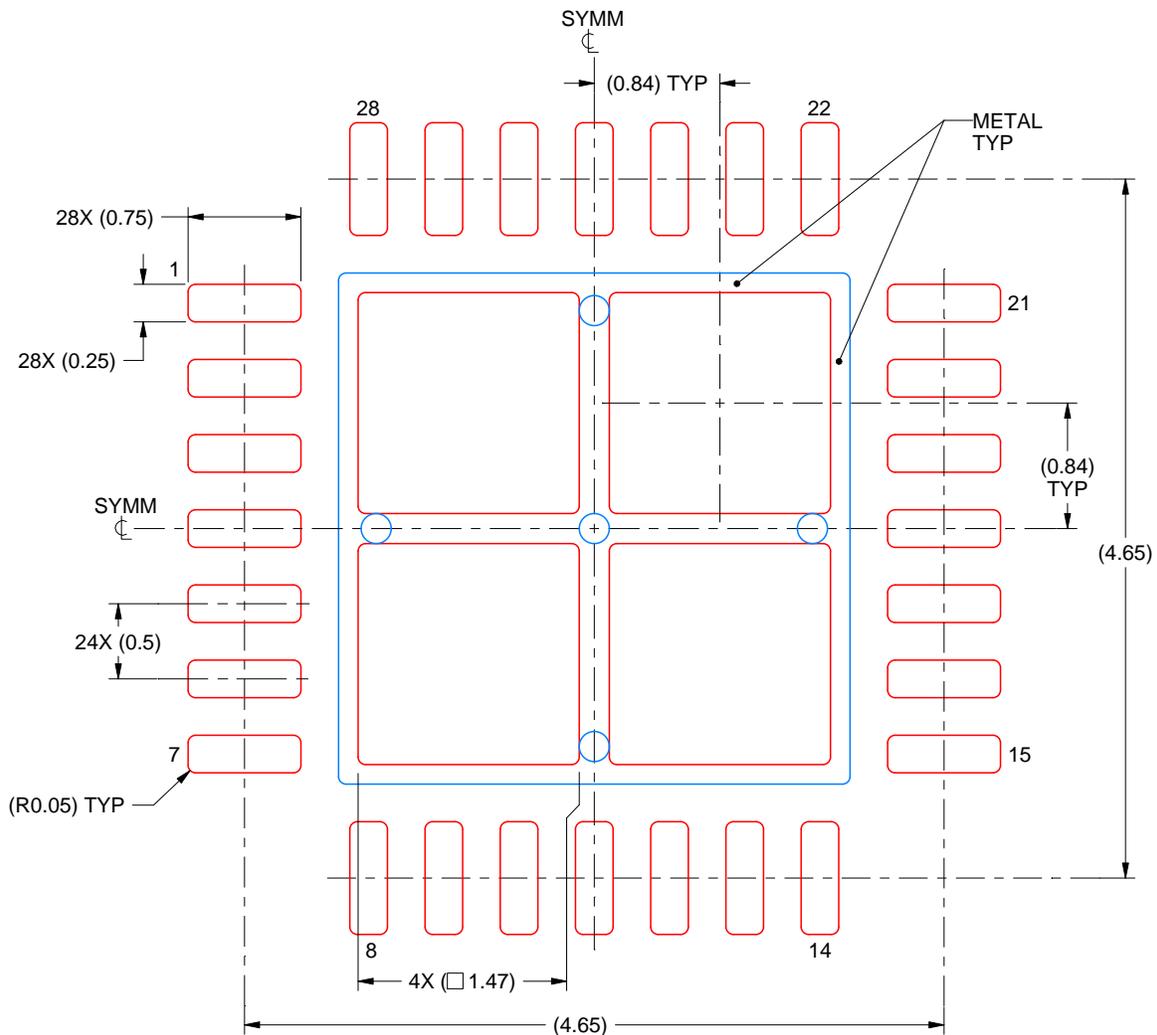
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RHD0028W

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
EXPOSED PAD  
75% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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