SY89322V

3.3V/5V Dual LVTTL/LVCMOS-to-Differential LVPECL Translator

Features

- 3.3V and 5V Power Supply Options
- 300 ps Typical Propagation Delay
- Differential LVPECL Output
- PNP LVTTL Inputs for Minimal Loading
- Flow-Through Pinouts
- Q Output will Default High with Inputs Open
- Maximum Frequency Range of 800 MHz
- Available in Ultra-Small 8-Lead (2 mm x 2 mm) VDFN Package

General Description

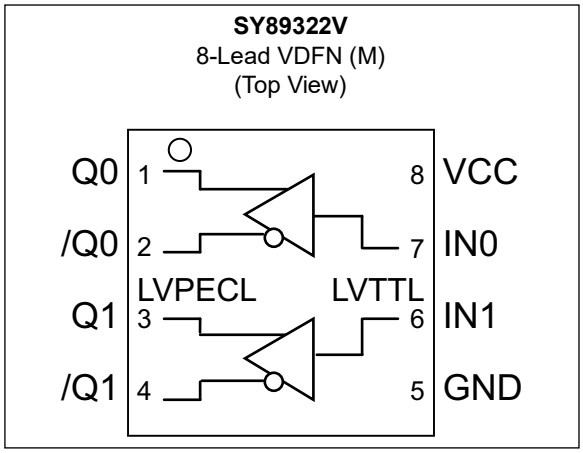
The SY89322V is a dual TTL/CMOS-to-differential PECL translator. Capable of running from a 3.3V or 5V supply, the part can be used in either LVTTL/LVCMOS/LVPECL or TTL/CMOS/PECL systems.

The device requires only a single positive supply of 3.3V or 5V; no negative supply is required.

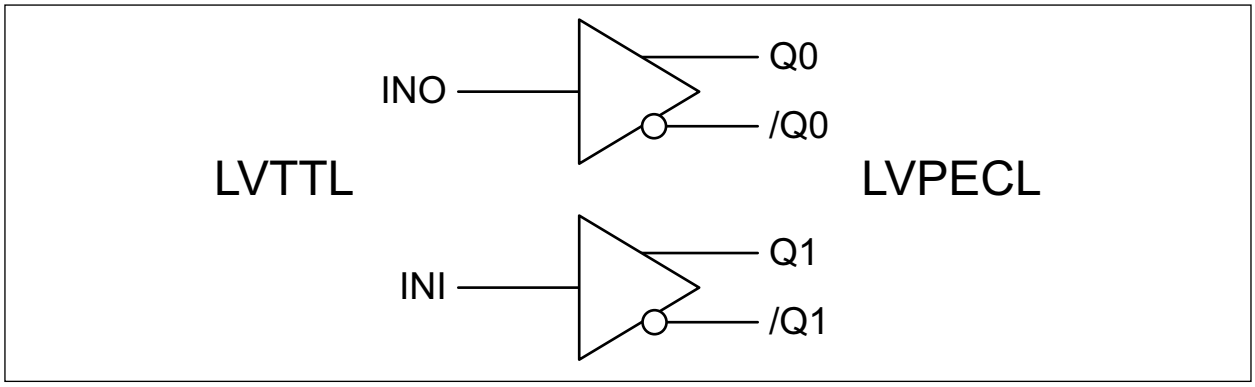
The SY89322V is functionally equivalent to the SY100EPT22V, but in an ultra-small 8-lead VDFN package that features a 70% smaller footprint. The ultra-small package and the low skew, dual gate design of the SY89322V makes it ideal for those applications where space, performance, and low power consumption are at a premium.

Package Type

SY89322V
8-Lead VDFN (M)
(Top View)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +6.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Continuous Output Current (I_{OUT}) ..... 50 mA
LVPECL Surge Output Current (I_{OUT}) ..... 100 mA
Input Current (Source or Sink Current on IN) ..... ±50 mA

Operating Ratings ‡

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Supply Voltage (V_{CC}) ..... +4.5V to +5.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	—
		4.5	5.0	5.5	V	—
Power Supply Current	I_{CC}	—	—	25	mA	—

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10% or +5.0V ±10%; T_A = –40°C to +85°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input High Current	I_{IH}	—	—	20	µA	V_{IN} = 2.7V
		—	—	100	µA	V_{IN} = V_{CC}
Input Low Current	I_{IL}	—	—	–0.2	mA	V_{IN} = 0.5V
Input Clamp Voltage	V_{IK}	—	—	–1.2	V	I_{IN} = –18 mA

PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10% or 5V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC} – 2V, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	V_{CC} – 1.080	—	V_{CC} – 0.880	V	—
Output Low Voltage	V_{OL}	V_{CC} – 1.830	—	V_{CC} – 1.550	V	—

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10% or 5V ±10%; R_L = 50Ω to V_{CC} – 2V, T_A = –40°C to +85°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Operating Frequency	f_{MAX}	—	—	800	MHz	—
Propagation Delay	t_{PD}	100	—	600	ps	IN-to-Q
Within-Device Skew	t_{SKEW}	—	—	100	ps	Note 1
Part-to-Part Skew		—	—	500	ps	Note 1
Cycle-to-Cycle Jitter	t_{JITTER}	—	—	2	ps_{RMS}	Note 2
Total Jitter		—	—	25	ps_{PP}	Note 3
Rise/Fall Time, 20% to 80%	t_r/t_f	200	—	500	ps	—

Note 1: Same transition at common V_{CC} levels.

2: Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, Tn–Tn–1 where T is the time between rising edges of the output signal.

3: Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Package Thermal Resistances (Note 1)						
Thermal Resistance, VDFN 8-Ld	θ_{JA}	—	93	—	°C/W	Still-Air
	θ_{JA}	—	87	—	°C/W	500 lpfm
	Ψ_{JB}	—	60	—	°C/W	Junction-to-board

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in a still air unless otherwise stated.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Type	Description
1, 2 3, 4	Q0, /Q0 Q1, /Q1	100K ECL Output	Differential LVPECL Outputs: Default to LOW if IN input left open. See the LVPECL Output Interface Applications section for recommendations on terminations.
5	GND, Exposed Pad	Ground	GND and exposed pad must be tied to ground plane.
6, 7	IN1, IN0	TTL/LVTTL Input	Single-ended TTL Inputs.
8	VCC	Power	Positive Power Supply: Bypass with 0.1 µF//0.01 µF low ESR capacitors.

3.0 LVPECL OUTPUT INTERFACE APPLICATIONS

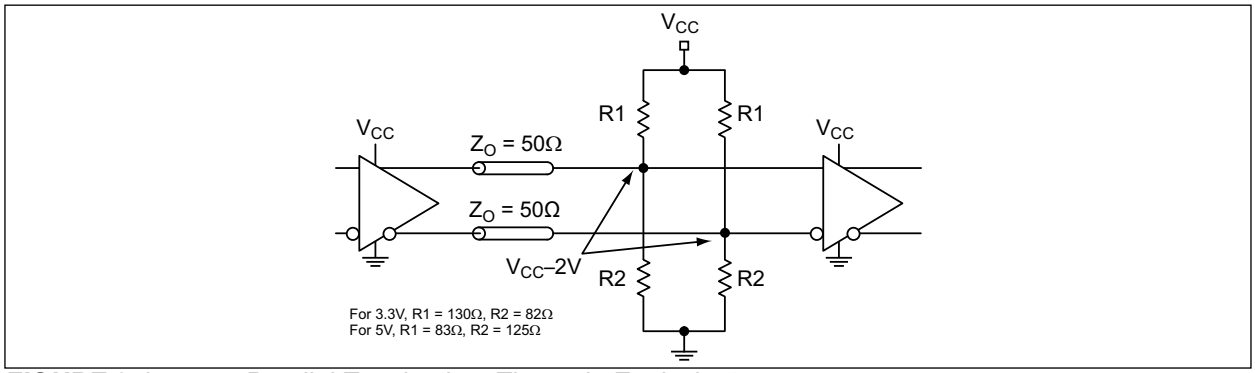


FIGURE 3-1: *Parallel Termination: Thevenin Equivalent.*

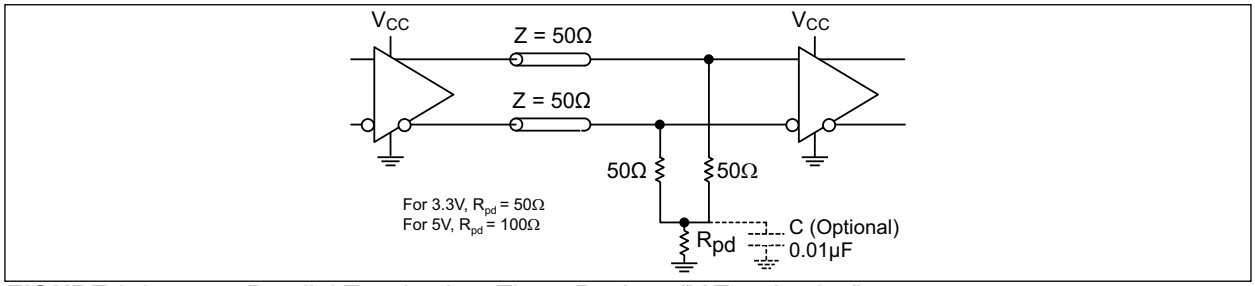


FIGURE 3-2: *Parallel Termination: Three-Resistor "Y-Termination".*

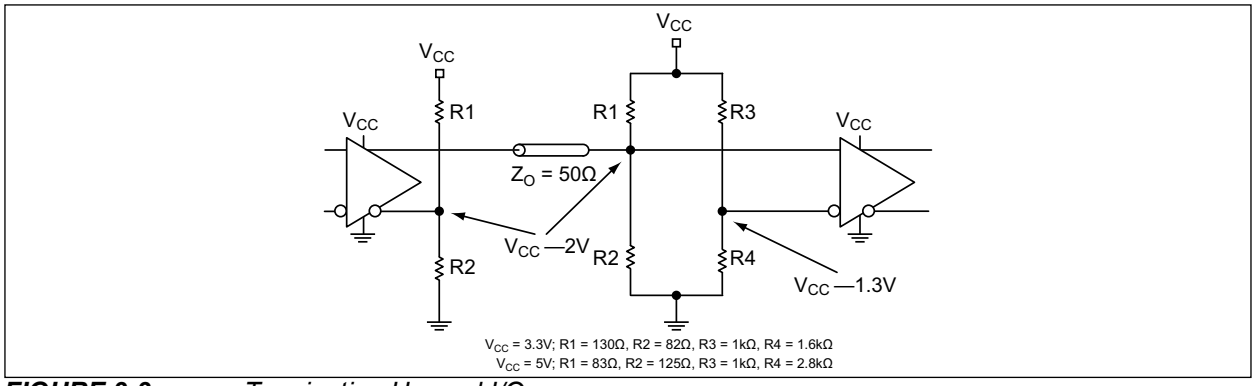
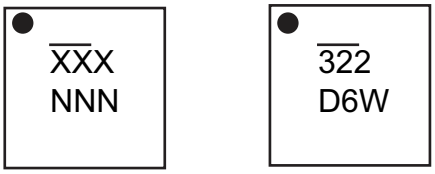


FIGURE 3-3: *Terminating Unused I/O.*

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead VDFN* Example

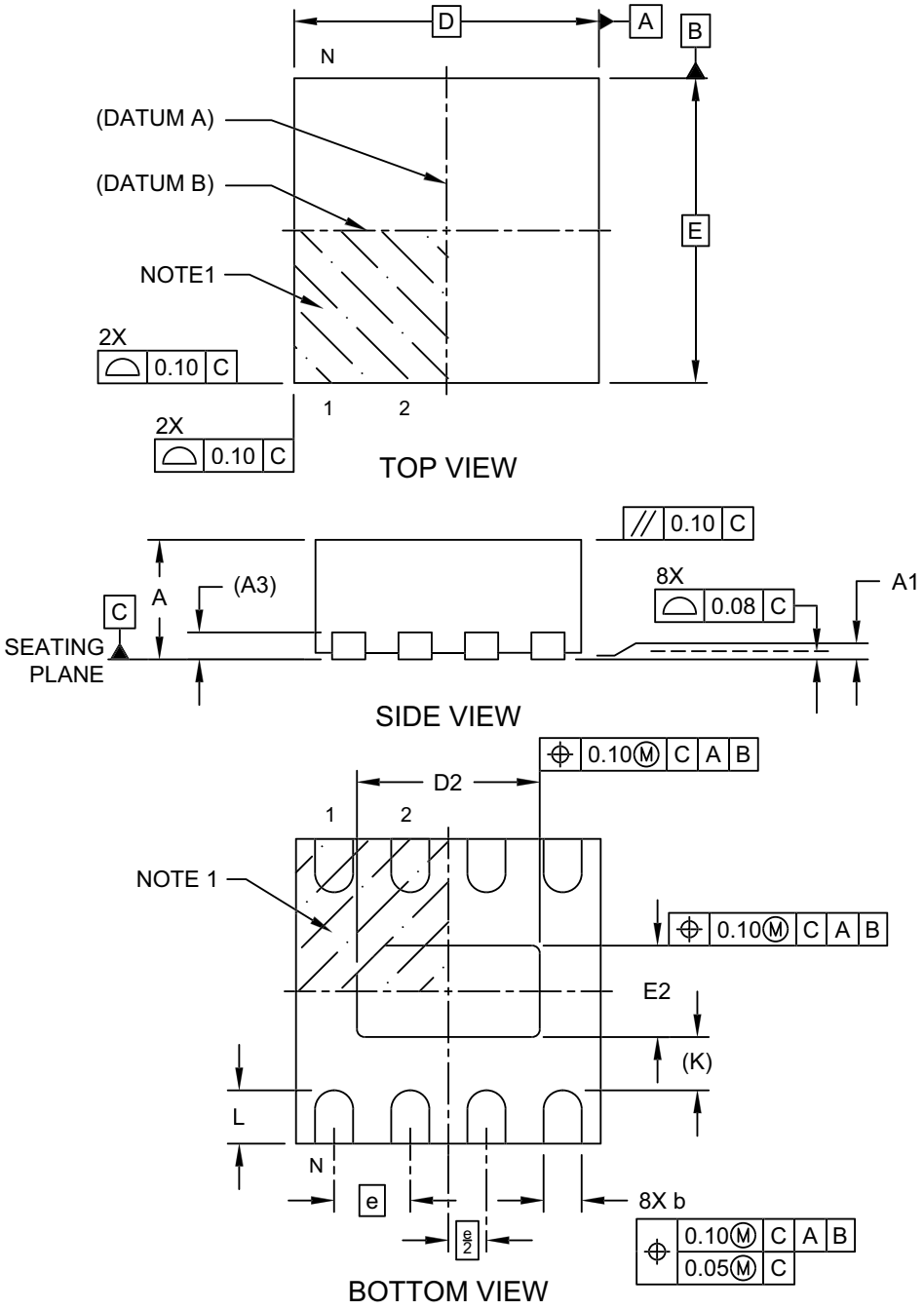


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

8-Lead Very Thin Plastic Dual Flat, No Lead Package (6XW) - 2x2x1.0 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00637 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (6XW) - 2x2x1.0 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

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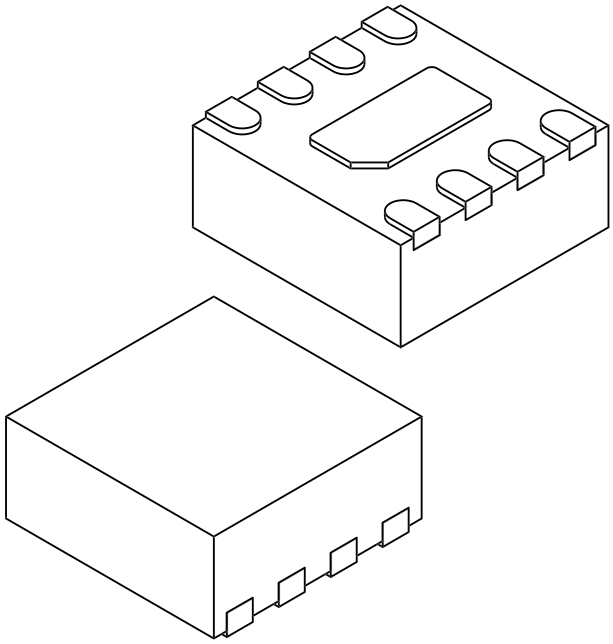

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.10	1.20	1.30
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.50	0.60	0.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K		0.35 REF	

Notes:

1. Pin 1 visual index feature may vary but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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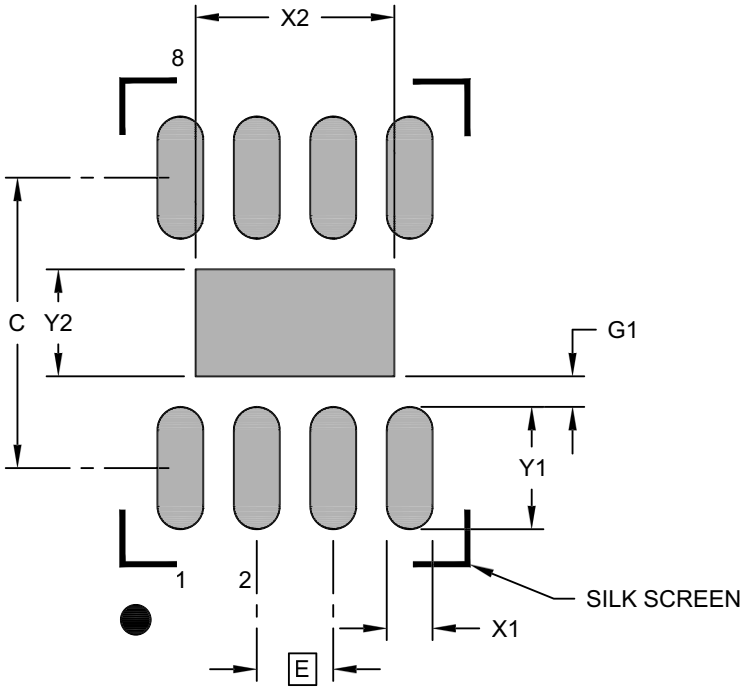
8-Lead Very Thin Plastic Dual Flat, No Lead Package (6XW) - 2x2x1.0 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.30
Optional Center Pad Length	Y2			0.70
Contact Pad Spacing	C		1.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, please refer to current industry standard IPC-7093

Microchip Technology Drawing C04-02637 Rev. B

APPENDIX A: REVISION HISTORY

Revision A (May 2024)

- Converted Micrel document SY89322V to Microchip data sheet template DS20006904A.
- Minor text changes throughout.

Revision B (June 2025)

- Updated the package outline drawing.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	[-XX]
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY89322:	3.3V/5V Dual LVTTL/LVCMOS-to-Differential LVPECL Translator	
Supply Voltage:	V	=	3.3V/5V
Package:	M	=	8-Lead 2 mm x 2 mm VDFN
Temperature Range:	G	=	–40°C to +85°C
Media Type:	TR	=	1,000/Reel

Examples:

a) SY89322VMG-TR:

SY89322, 3.3V/5V Supply Voltage, 8-Lead VDFN, –40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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