

5-V PECL-to-TTL Translator

FEATURES

- 3ns (TYP) Propagation Delay
- Operating Range: $V_{CC} = 4.2\text{ V}$ to 5.7 V with $GND = 0\text{ V}$
- 24-mA TTL Output
- Deterministic Output Value for Open Input Conditions or When Inputs $< 1.3\text{ V}$
- Built-In Temperature Compensation
- Drop-In Compatible to the MC10ELT21, MC100ELT21

APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion for Clock or Data

DESCRIPTION

The SN65ELT21 is a differential PECL-to-TTL translator. It operates on +5-V supply and ground only. The device includes circuitry to maintain Q to a low logic level when inputs are in an open condition or $< 1.3\text{ V}$.

The V_{BB} pin is a reference voltage output for the device. When the device is used in single-ended mode, the unused input should be tied to V_{BB} . This reference voltage can also be used to bias the input when it is ac coupled. When it is used, place a $0.01\mu\text{F}$ decoupling capacitor between V_{CC} and V_{BB} . Also limit the sink/source current to $< 0.5\text{ mA}$ to V_{BB} . Leave V_{BB} open when it is not used.

The SN65ELT21 is housed in an industry standard SOIC-8 package and is also available in an optional TSSOP-8 package.

PIN ASSIGNMENT

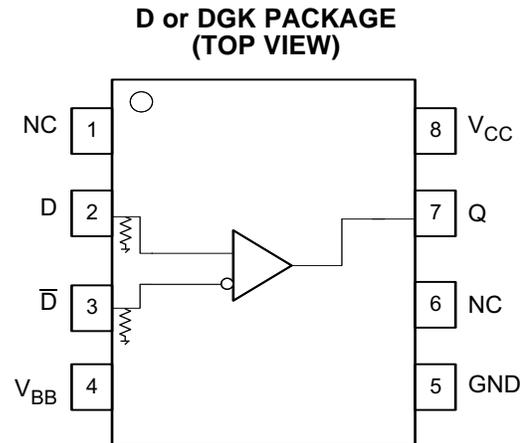


Table 1. Pin Descriptions

PIN	FUNCTION
D, \bar{D}	PECL data inputs
Q	TTL output
V_{CC}	Positive supply
V_{EE}	Negative supply
V_{BB}	Reference voltage output

ORDERING INFORMATION⁽¹⁾⁽²⁾

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65ELT21D	ELT21	SOIC	NiPdAu
SN65ELT21DGK	SIII	SOIC-TSSOP	NiPdAu

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Leaded device options are not initially available; contact a sales representative for further details.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute PECL mode supply voltage	V_{CC} (GND = 0 V)	6	V
Sink/source current, V_{BB}		± 0.5	mA
PECL input voltage	GND = 0 V, $V_I \leq V_{CC}$	6	V
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A < 25^\circ\text{C}$ (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT NO AIRFLOW	DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC	79		°C/W
		SOIC-TSSOP	120		
θ_{JC}	Junction-to-case thermal resistance	SOIC	98		°C/W
		SOIC-TSSOP	74		

KEY ATTRIBUTES

CHARACTERISTICS	VALUE	
Internal input pull-down resistor	50 k Ω	
Moisture sensitivity level	Level 1	
Flame ability rating (oxygen index: 28 to 34)	UL 94 V-0 at 0.125 in	
Electrostatic discharge	Human body model	2 kV
	Charged-device model	1.5 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test		

PECL DC CHARACTERISTICS

At $V_{CC} = 5.0\text{ V}$, $GND = 0.0\text{ V}$ (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	$T_A = -40^\circ\text{C}$			$T_A = 25^\circ\text{C}$			$T_A = 85^\circ\text{C}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage, single-ended	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Low-level input voltage, single-ended	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output reference voltage	3.62	3.69	3.74	3.62	3.69	3.74	3.62	3.69	3.74	V
V_{IHCMR}	High-level input voltage, common-mode range, differential	See ⁽³⁾			2.2		5.0	2.2		5.0	V
I_{IH}	High-level input current			150			150			150	μA
I_{IL}	Low-level input current	0.5			0.5			0.5			μA

- (1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input parameters vary 1:1 with V_{CC} . V_{CC} can vary +0.7 V / -0.8 V.
- (3) $V_{IHCMR(\min)}$ varies 1:1 with GND , $V_{IHCMR(\max)}$ varies 1:1 with V_{CC} .

TTL DC CHARACTERISTICS

At $V_{CC} = 4.2\text{ V}$ to 5.7 V , $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	Power supply current			20	mA
I_{CCL}	Power supply current			20	mA
V_{OH}	High-level output voltage	$I_{OH} = -3.0\text{ mA}$		2.4	See ⁽²⁾ V
V_{OL}	Low-level output voltage	$I_{OL} = 24\text{ mA}$		0.5	V
I_{OS}	Output short circuit current	-150		-60	mA

- (1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) $V_{OH(\max)}$ level is $V_{CC} - 0.7$.

AC CHARACTERISTICS

At $V_{CC} = 4.2\text{ V}$ to 5.7 V , $GND = 0.0\text{ V}$ (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	$T_A = -40^\circ\text{C}$			$T_A = 25^\circ\text{C}$			$T_A = 85^\circ\text{C}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum switching frequency	At $V_{ol} < 0.5\text{ V}$ (See Figure 4)			200			200			MHz
$t_{\text{PLH}}/t_{\text{PHL}}$	Propagation delay times	2		4.5	2		4.5	2		4.5	ns
t_{JITTER}	Random clock jitter (RMS)		5	20		5	20		5	20	ps
V_{PP}	Input swing	See ⁽³⁾			200		1000	200		1000	mV
t_r/t_f	Output rise/fall times	Q (10%–90%)			750			780			ps

- (1) The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) $R_L = 500\ \Omega$ to GND and $C_L = 20\text{ pF}$ to GND . See Figure 1.
- (3) $V_{\text{PP}(\min)}$ is minimum input swing for which ac parameters are assured.

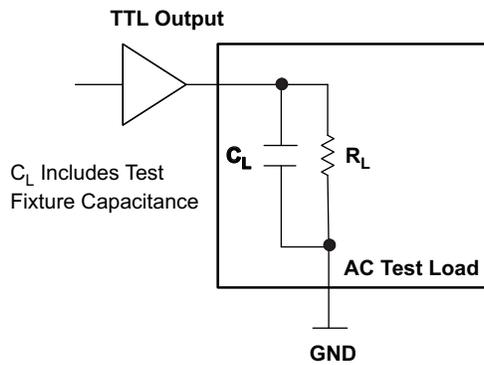


Figure 1. TTL Output AC Test Loading Condition

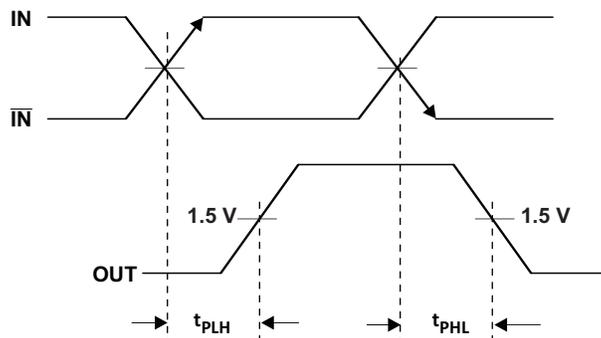


Figure 2. Output Propagation Delay

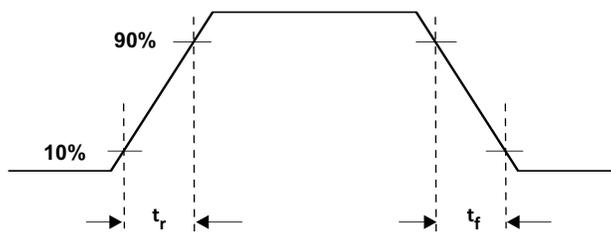
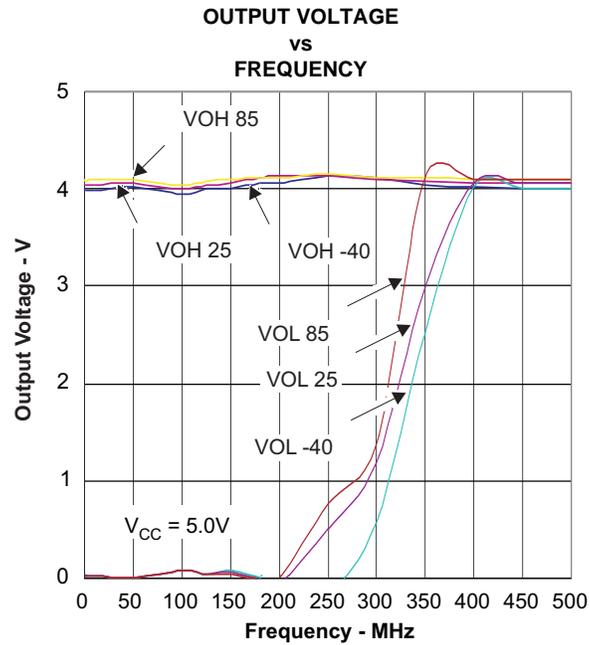


Figure 3. Output Rise and Fall Times



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65ELT21D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT21
SN65ELT21D.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT21
SN65ELT21DGK	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIII
SN65ELT21DGK.B	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIII
SN65ELT21DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIII
SN65ELT21DGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIII
SN65ELT21DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT21
SN65ELT21DR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT21

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

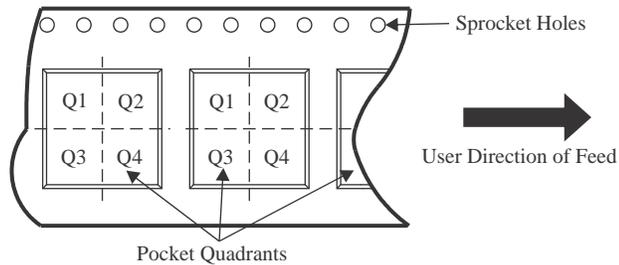
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


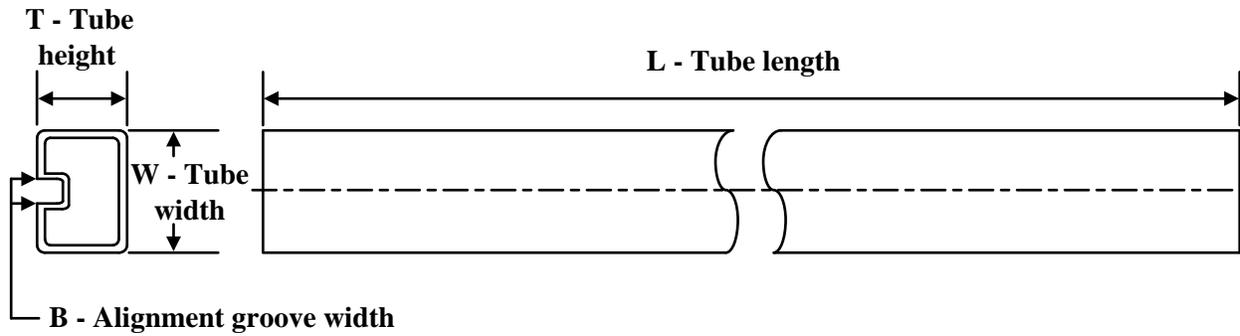
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ELT21DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65ELT21DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ELT21DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
SN65ELT21DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65ELT21D	D	SOIC	8	75	506.6	8	3940	4.32
SN65ELT21D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65ELT21DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65ELT21DGK.B	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

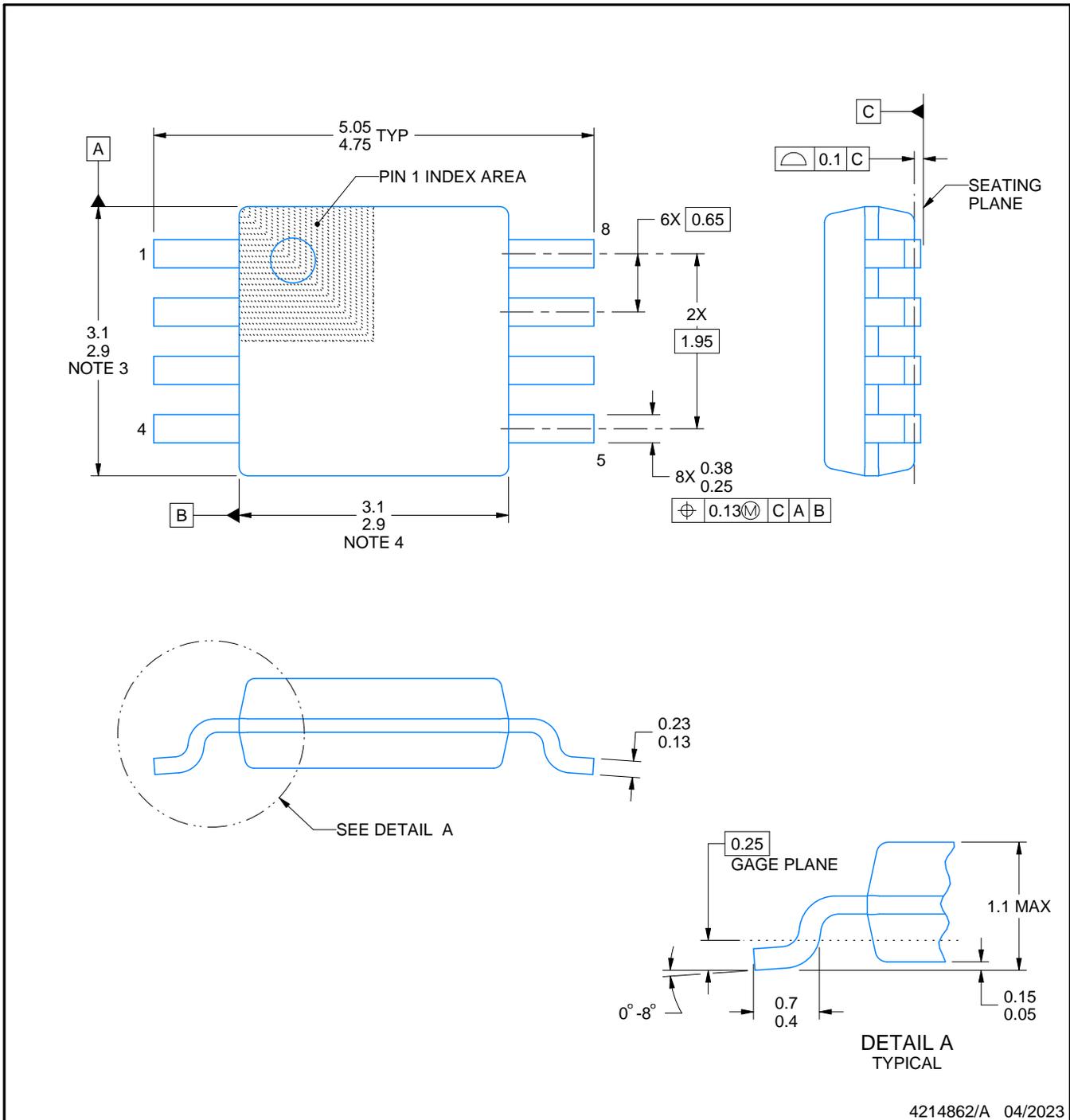
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

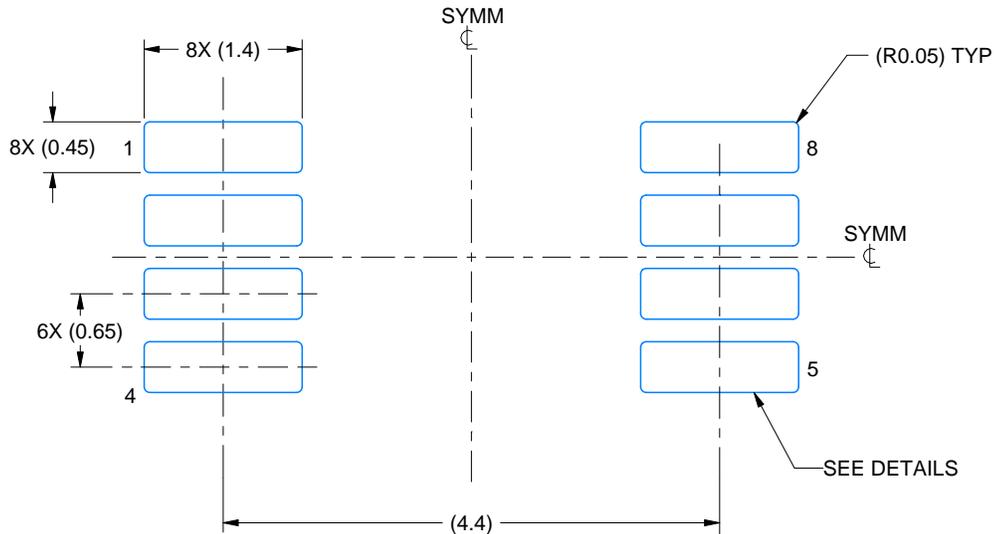
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

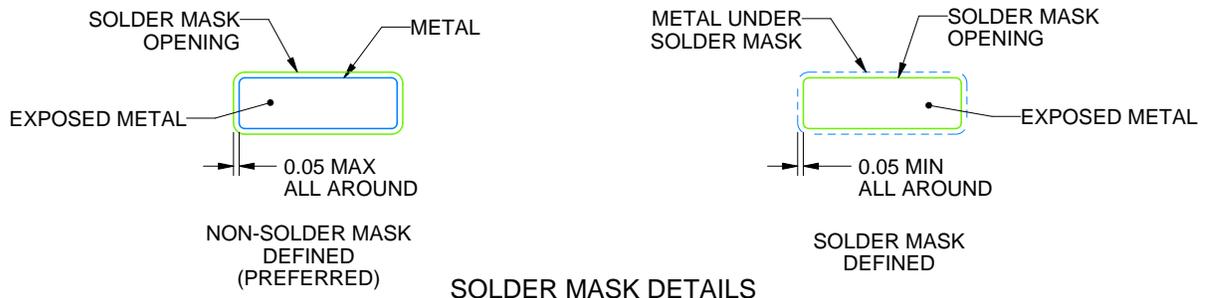
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

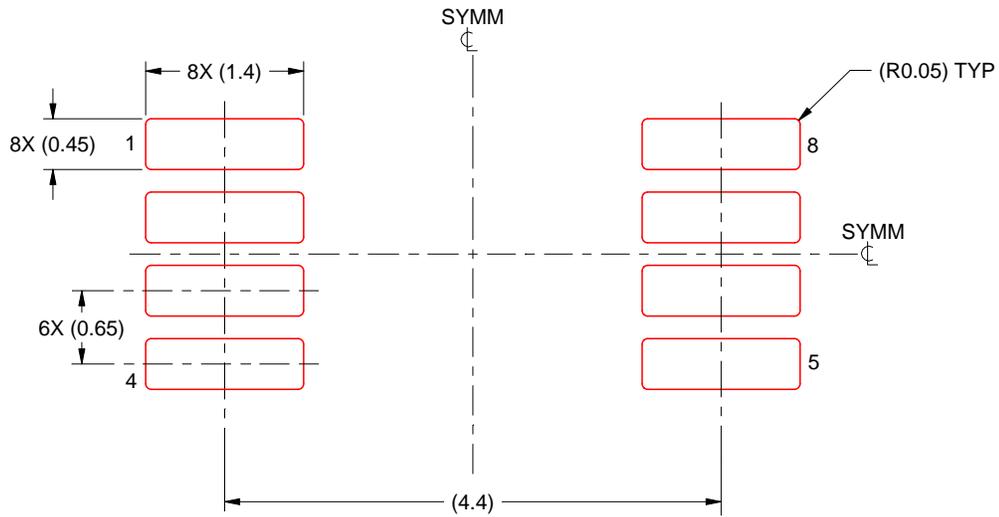
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

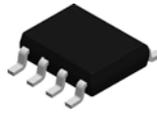


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

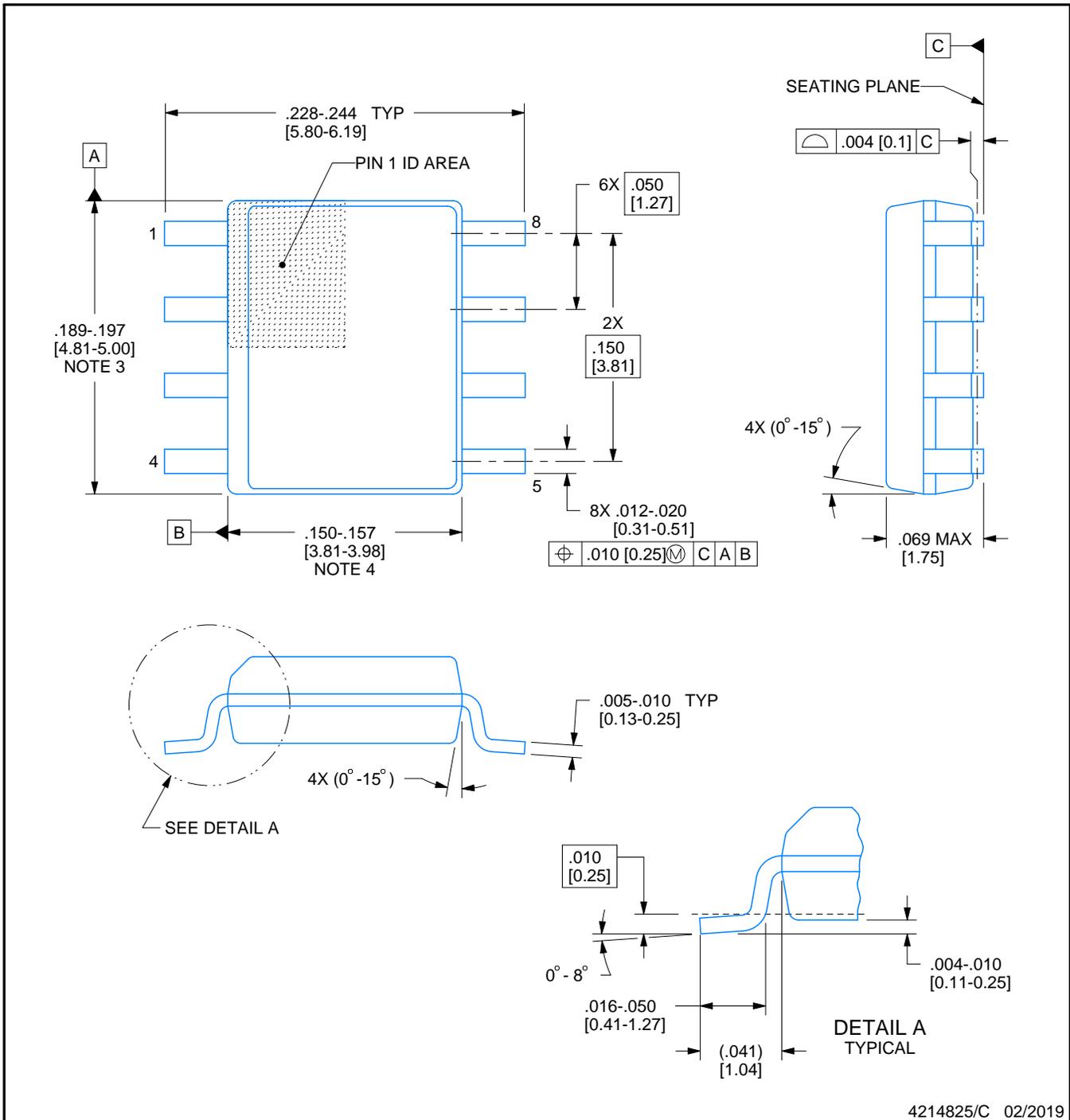


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

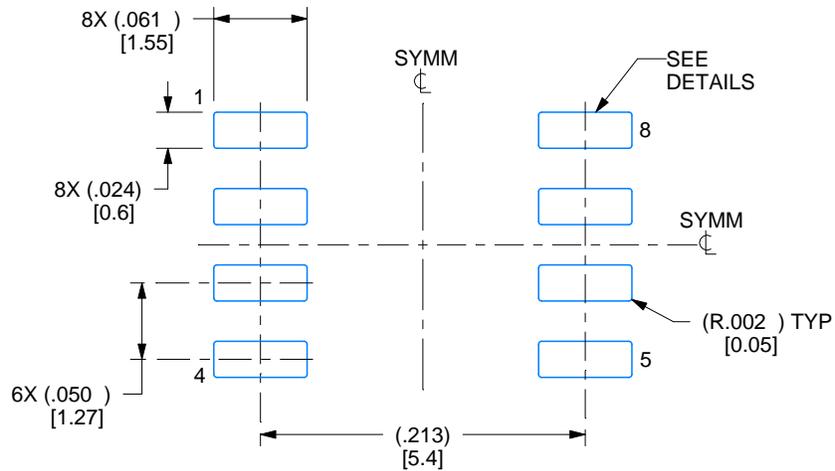
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

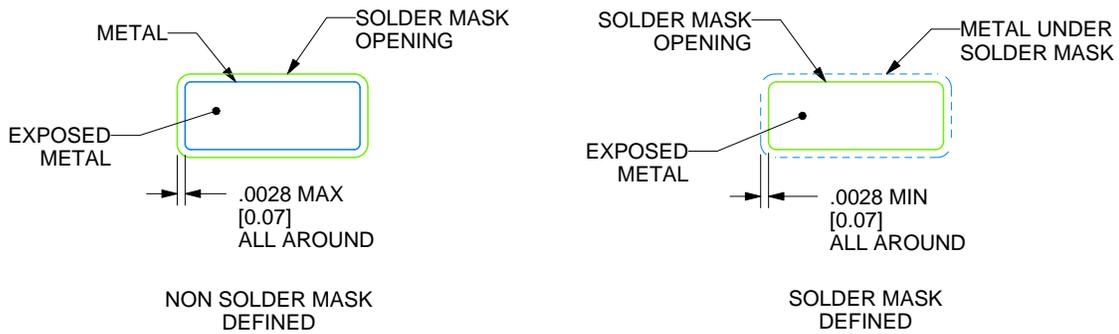
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

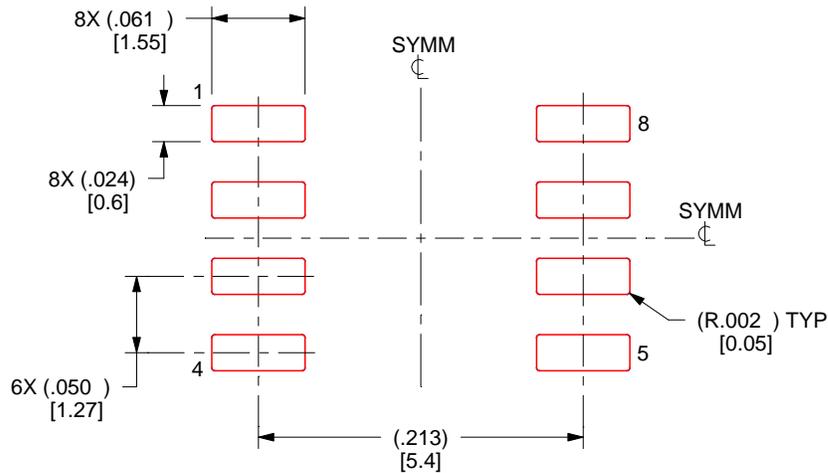
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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