

# OPAx170 36-V, Single-Supply, SOT553, Low-Power Operational Amplifiers Value Line Series

## 1 Features

- Supply Range: 2.7 V to 36 V,  $\pm 1.35$  V to  $\pm 18$  V
- Low Noise: 19 nV/ $\sqrt{\text{Hz}}$
- RFI Filtered Inputs
- Input Range Includes the Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- Gain Bandwidth: 1.2 MHz
- Low Quiescent Current: 110  $\mu\text{A}$  per Amplifier
- High Common-Mode Rejection: 120 dB
- Low Bias Current: 15 pA (Maximum)
- Industry-Standard Packages and *micro* Packages Available
- Create a Custom Design Using the OPAx170 With the [WEBENCH® Power Designer](#)

## 2 Applications

- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators
- Battery-Powered Instruments
- Test Equipment

## 3 Description

The OPA170, OPA2170, and OPA4170 devices (OPAx170) are a family of 36-V, single-supply, low-noise operational amplifiers (op amps) that feature micro packages with the ability to operate on supplies ranging from 2.7 V ( $\pm 1.35$  V) to 36 V ( $\pm 18$  V). They offer good offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

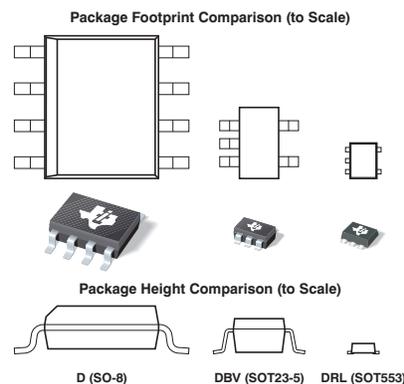
Unlike most op amps, which are specified at only one supply voltage, the OPAx170 family of op amps is specified from 2.7 V to 36 V. Input signals beyond the supply rails do not cause phase reversal. The OPAx170 family is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the positive rail for normal operation. Note that these devices can operate with full rail-to-rail input 100 mV beyond the positive rail, but with reduced performance within 2 V of the positive rail. The OPAx170 op amps are specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA170	SOIC (8)	4.90 mm x 3.91 mm
	SOT (5)	1.60 mm x 1.20 mm
	SOT-23 (5)	2.90 mm x 1.60 mm
OPA2170	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	VSSOP (8), <i>micro size</i>	2.30 mm x 2.00 mm
	WSON (8)	2.00 mm x 2.00 mm
OPA4170	SOIC (14)	8.65 mm x 3.91 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Smallest Packaging for 36-V Operational Amplifiers



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Applications</b> ..... 1 <b>3 Description</b> ..... 1 <b>4 Revision History</b> ..... 2 <b>5 Device Comparison Table</b> ..... 3 <b>6 Pin Configuration and Functions</b> ..... 4 <b>7 Specifications</b> ..... 7 7.1 Absolute Maximum Ratings ..... 7 7.2 ESD Ratings ..... 7 7.3 Recommended Operating Conditions ..... 7 7.4 Thermal Information: OPA170 ..... 8 7.5 Thermal Information: OPA2170 ..... 8 7.6 Thermal Information: OPA4170 ..... 8 7.7 Electrical Characteristics ..... 9 7.8 Typical Characteristics ..... 11 <b>8 Detailed Description</b> ..... 18 8.1 Overview ..... 18 8.2 Functional Block Diagram ..... 18 8.3 Feature Description ..... 18	8.4 Device Functional Modes ..... 22 <b>9 Application and Implementation</b> ..... 23 9.1 Application Information ..... 23 9.2 Typical Application ..... 23 <b>10 Power Supply Recommendations</b> ..... 26 <b>11 Layout</b> ..... 26 11.1 Layout Guidelines ..... 26 11.2 Layout Example ..... 26 <b>12 Device and Documentation Support</b> ..... 28 12.1 Device Support ..... 28 12.2 Documentation Support ..... 29 12.3 Related Links ..... 29 12.4 Receiving Notification of Documentation Updates ..... 29 12.5 Community Resources ..... 29 12.6 Trademarks ..... 30 12.7 Electrostatic Discharge Caution ..... 30 12.8 Glossary ..... 30 <b>13 Mechanical, Packaging, and Orderable Information</b> ..... 30
------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2017) to Revision E	Page
• Changed minimum supply voltage from –20 V to 0 V in <i>Absolute Maximum Ratings</i> table ..... 7	7
• Changed maximum supply voltage from 20 V to 40 V in <i>Absolute Maximum Ratings</i> table ..... 7	7

Changes from Revision C (March 2016) to Revision D	Page
• Added <i>WEBENCH</i> links and sections and <i>Receiving Notification of Documentation Updates</i> ..... 1	1
• Added 8-Pin DSG (WSO) package ..... 1	1
• Changed values in <i>Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application</i> from: 250 Ω to: 2.5 Ω ..... 20	20

Changes from Revision B (September 2012) to Revision C	Page
• Added current package designators to <i>Features</i> list and final paragraph of <i>Description</i> section ..... 1	1
• Added <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Recommended Operating Conditions</i> table, <i>Detailed Description</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... 1	1

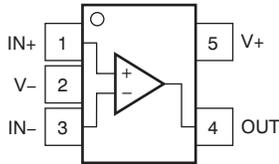
Changes from Revision A (September 2011) to Revision B	Page
• Added "Value Line Series" to document title ..... 1	1

## 5 Device Comparison Table

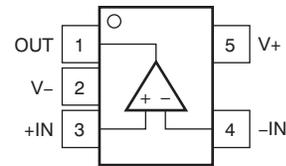
DEVICE	NO OF CHANNELS	PACKAGE-LEAD						
		SOT	SOT23-5	D	DSG	VSSOP	VSSOP (micro size)	TSSOP
OPA170	1	5	5	8	—	—	—	—
OPA2170	2	—	—	8	8	8	8	—
OPA4170	4	—	—	14	—	—	—	14

## 6 Pin Configuration and Functions

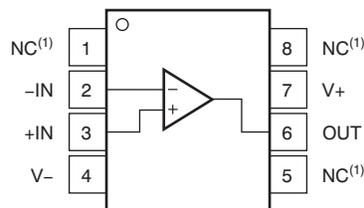
**OPA170 DRL Package  
5-Pin SOT  
Top View**



**OPA170 DBV Package  
5-Pin SOT-23  
Top View**



**OPA170 D Package  
8-Pin SOIC  
Top View**

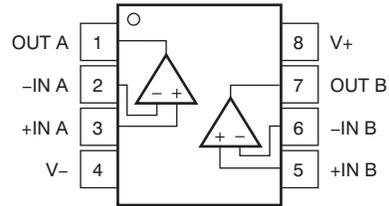


### Pin Functions: OPA170

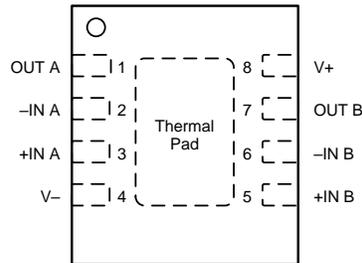
NAME	PIN			I/O	DESCRIPTION
	SOT	SOT-23	D		
IN- (-IN)	3	4	2	I	Negative (inverting) input
IN+ (+IN)	1	3	3	I	Positive (noninverting) input
NC <sup>(1)</sup>	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	4	1	6	O	Output
V+	5	5	7	—	Positive (highest) power supply
V-	2	2	4	—	Negative (lowest) power supply

(1) NC indicates no internal connection.

**OPA2170 D, DGK, and DCU Packages  
8-Pin VSSOP, SOIC, and VSSOP (micro size)  
Top View**

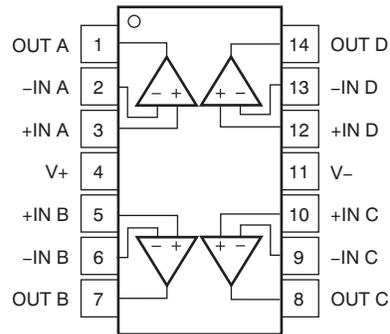


**OPA2170 DSG Package  
8-Pin WSON  
Top View**



**Pin Functions: OPA2170**

NAME	PIN				I/O	DESCRIPTION
	SOIC	VSSOP	VSSOP (micro size)	WSON		
-IN A	2	2	2	2	I	Inverting input, channel A
-IN B	6	6	6	6	I	Inverting input, channel B
+IN A	3	3	3	3	I	Noninverting input, channel A
+IN B	5	5	5	5	I	Noninverting input, channel B
OUT A	1	1	1	1	O	Output, channel A
OUT B	7	7	7	7	O	Output, channel B
V-	4	4	4	4	—	Negative (lowest) power supply
V+	8	8	8	8	—	Positive (highest) power supply

**OPA4170 D and PW Packages  
14-Pin SOIC and TSSOP  
Top View**

**Pin Functions: OPA4170**

NAME	PIN		I/O	DESCRIPTION
	SOIC	TSSOP		
-IN A	2	2	I	Inverting input, channel A
-IN B	6	6	I	Inverting input, channel B
-IN C	9	9	I	Inverting input, channel C
-IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V-	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage	0	40	V
Single supply voltage		40	V
Signal input pin voltage	(V <sub>-</sub> ) – 0.5	(V <sub>+</sub> ) + 0.5	V
Signal input pin current	–10	10	mA
Output short-circuit current <sup>(2)</sup>	Continuous		
Operating ambient temperature, T <sub>A</sub>	–55	150	°C
Junction temperature, T <sub>J</sub>		150	°C
Storage temperature, T <sub>stg</sub>	–65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage (V <sub>+</sub> – V <sub>-</sub> )	2.7	36	V
T <sub>A</sub>	Operating temperature	–40	125	°C

## 7.4 Thermal Information: OPA170

THERMAL METRIC <sup>(1)</sup>		OPA170			UNIT
		D (SOIC)	DBV (SOT-23)	DRL (SOT)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	245.8	208.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.9	133.9	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	83.6	42.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	35.5	18.2	0.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	89.5	83.1	42.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Thermal Information: OPA2170

THERMAL METRIC <sup>(1)</sup>		OPA2170				UNIT
		D (SOIC)	DCU (VSSOP, micro size)	DGK (VSSOP)	DSG (WSON)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	175.2	180	71.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.1	74.9	55	89.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	22.2	130	38.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	18.2	1.6	5.3	3.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	53.8	22.8	120	38.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	13	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.6 Thermal Information: OPA4170

THERMAL METRIC <sup>(1)</sup>		OPA4170		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	13.5	0.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.7 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$T_A = 25^\circ\text{C}$		0.25	$\pm 1.8$	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 2$	mV
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 0.3$	$\pm 2$	$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage vs power supply	$V_S = 4\text{ V}$ to $36\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1	$\pm 5$	$\mu\text{V}/\text{V}$
	Channel separation, dc			5		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$T_A = 25^\circ\text{C}$		$\pm 8$	$\pm 15$	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 3.5$	nA
$I_{OS}$	Input offset current	$T_A = 25^\circ\text{C}$		$\pm 4$	$\pm 15$	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 3.5$	nA
<b>NOISE</b>						
	Input voltage noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		2		$\mu\text{V}_{PP}$
$e_n$	Input voltage noise density	$f = 100\text{ Hz}$		22		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		19		$\text{nV}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE</b>						
$V_{CM}$	Common-mode voltage range <sup>(1)</sup>		$(V-) - 0.1$		$(V+) - 2$	V
CMRR	Common-mode rejection ratio	$V_S = \pm 2\text{ V}$ , $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	90	104		dB
		$V_S = \pm 18\text{ V}$ , $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	104	120		dB
<b>INPUT IMPEDANCE</b>						
	Differential			$100 \parallel 3$		$\text{M}\Omega \parallel \text{pF}$
	Common-mode			$6 \parallel 3$		$10^{12}\ \Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$V_S = 4\text{ V}$ to $36\text{ V}$ , $(V-) + 0.35\text{ V} < V_O < (V+) - 0.35\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	110	130		dB
<b>FREQUENCY RESPONSE</b>						
GBP	Gain bandwidth product			1.2		MHz
SR	Slew rate	$G = +1$		0.4		$\text{V}/\mu\text{s}$
$t_s$	Settling time	To 0.1%, $V_S = \pm 18\text{ V}$ , $G = +1$ , 10-V step		20		$\mu\text{s}$
		To 0.01% (12-bit), $V_S = \pm 18\text{ V}$ , $G = +1$ , 10-V step		28		$\mu\text{s}$
	Overload recovery time	$V_{IN} \times \text{Gain} > V_S$		2		$\mu\text{s}$
THD+N	Total harmonic distortion + noise	$G = +1$ , $f = 1\text{ kHz}$ , $V_O = 3\text{ V}_{RMS}$		0.0002%		

(1) The input range can be extended beyond  $(V+) - 2\text{ V}$  up to  $V+$ . See the [Typical Characteristics](#) and [Application and Implementation](#) sections for additional information.

**Electrical Characteristics (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT</b>						
$V_O$	Voltage output swing from positive rail	$I_L = 0\text{ mA}$ , $V_S = 4\text{ V to }36\text{ V}$	10			mV
		$I_L$ sourcing $1\text{ mA}$ , $V_S = 4\text{ V to }36\text{ V}$	115			mV
$V_O$	Voltage output swing from negative rail	$I_L = 0\text{ mA}$ , $V_S = 4\text{ V to }36\text{ V}$			8	mV
		$I_L$ sinking $1\text{ mA}$ , $V_S = 4\text{ V to }36\text{ V}$			70	mV
$V_O$	Voltage output swing from rail	$V_S = 5\text{ V}$ , $R_L = 10\text{ k}\Omega$ ; $T_A = -40^\circ\text{C to }+125^\circ\text{C}$	(V-) + 0.03		(V+) – 0.05	V
		$R_L = 10\text{ k}\Omega$ , $A_{OL} \geq 110\text{ dB}$ , $T_A = -40^\circ\text{C to }+125^\circ\text{C}$	(V-) + 0.35		(V+) – 0.35	V
$I_{SC}$	Short-circuit current		–20		17	mA
$C_{LOAD}$	Capacitive load drive		See <a href="#">Typical Characteristics</a>			pF
$R_O$	Open-loop output resistance	$f = 1\text{ MHz}$ , $I_O = 0\text{ A}$		900		$\Omega$
<b>POWER SUPPLY</b>						
$V_S$	Specified voltage range		2.7		36	V
$I_Q$	Quiescent current per amplifier	$I_O = 0\text{ A}$ ; $T_A = 25^\circ\text{C}$		110	145	$\mu\text{A}$
		$I_O = 0\text{ A}$ ; $T_A = -40^\circ\text{C to }+125^\circ\text{C}$			155	$\mu\text{A}$
<b>TEMPERATURE</b>						
	Specified range		–40		125	$^\circ\text{C}$
	Operating range		–55		150	$^\circ\text{C}$

## 7.8 Typical Characteristics

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , (unless otherwise noted)

**Table 1. Characteristic Performance Measurements**

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	<a href="#">Figure 1</a>
Offset Voltage Drift Distribution	<a href="#">Figure 2</a>
Offset Voltage vs Temperature	<a href="#">Figure 3</a>
Offset Voltage vs Common-Mode Voltage	<a href="#">Figure 4</a>
Offset Voltage vs Common-Mode Voltage (Upper Stage)	<a href="#">Figure 5</a>
Offset Voltage vs Power Supply	<a href="#">Figure 6</a>
$I_B$ and $I_{OS}$ vs Common-Mode Voltage	<a href="#">Figure 7</a>
Input Bias Current vs Temperature	<a href="#">Figure 8</a>
Output Voltage Swing vs Output Current (Maximum Supply)	<a href="#">Figure 9</a>
CMRR and PSRR vs Frequency (Referred-to-Input)	<a href="#">Figure 10</a>
CMRR vs Temperature	<a href="#">Figure 11</a>
PSRR vs Temperature	<a href="#">Figure 12</a>
0.1-Hz to 10-Hz Noise	<a href="#">Figure 13</a>
Input Voltage Noise Spectral Density vs Frequency	<a href="#">Figure 14</a>
THD+N Ratio vs Frequency	<a href="#">Figure 15</a>
THD+N vs Output Amplitude	<a href="#">Figure 16</a>
Quiescent Current vs Temperature	<a href="#">Figure 17</a>
Quiescent Current vs Supply Voltage	<a href="#">Figure 18</a>
Open-Loop Gain and Phase vs Frequency	<a href="#">Figure 19</a>
Closed-Loop Gain vs Frequency	<a href="#">Figure 20</a>
Open-Loop Gain vs Temperature	<a href="#">Figure 21</a>
Open-Loop Output Impedance vs Frequency	<a href="#">Figure 22</a>
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	<a href="#">Figure 23</a> , <a href="#">Figure 24</a>
No Phase Reversal	<a href="#">Figure 25</a>
Positive Overload Recovery	<a href="#">Figure 26</a>
Negative Overload Recovery	<a href="#">Figure 27</a>
Small-Signal Step Response (100 mV)	<a href="#">Figure 28</a> , <a href="#">Figure 29</a>
Large-Signal Step Response	<a href="#">Figure 30</a> , <a href="#">Figure 31</a>
Large-Signal Settling Time (10-V Positive Step)	<a href="#">Figure 32</a>
Large-Signal Settling Time (10-V Negative Step)	<a href="#">Figure 33</a>
Short-Circuit Current vs Temperature	<a href="#">Figure 34</a>
Maximum Output Voltage vs Frequency	<a href="#">Figure 35</a>
EMIRR IN+ vs Frequency	<a href="#">Figure 36</a>

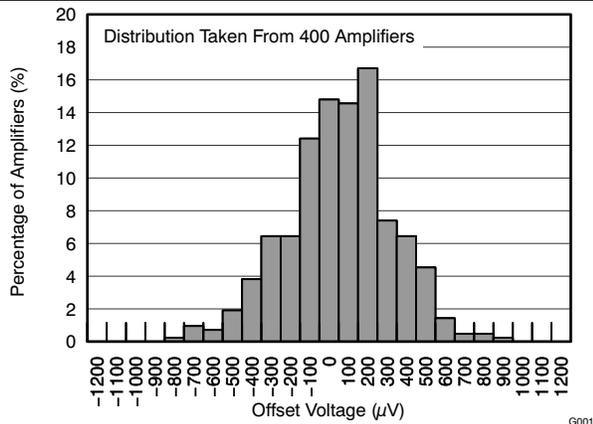


Figure 1. Offset Voltage Production Distribution

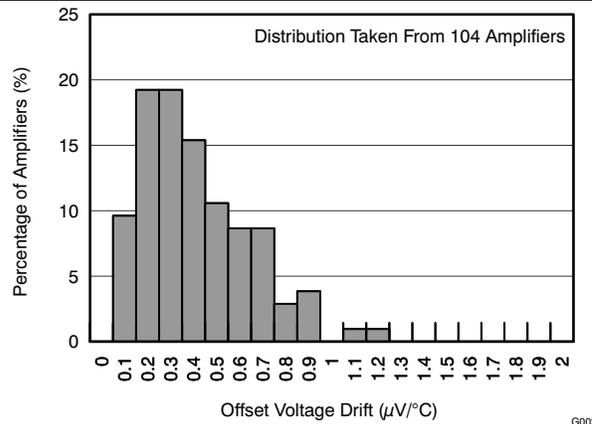


Figure 2. Offset Voltage Drift Distribution

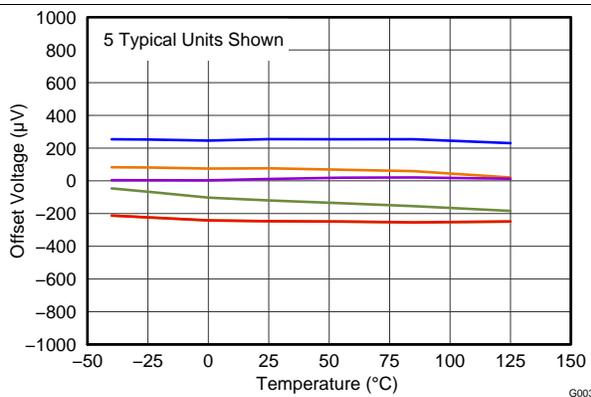


Figure 3. Offset Voltage vs Temperature

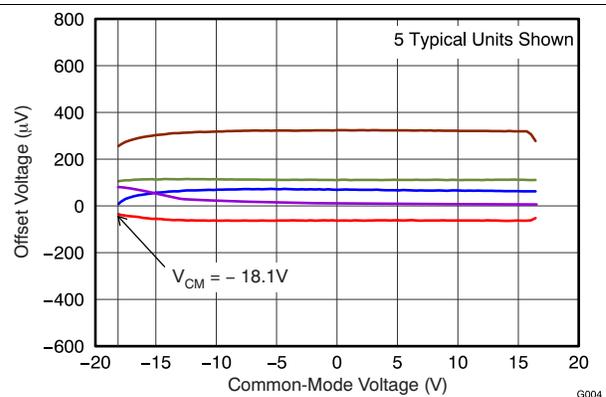


Figure 4. Offset Voltage vs Common-Mode Voltage

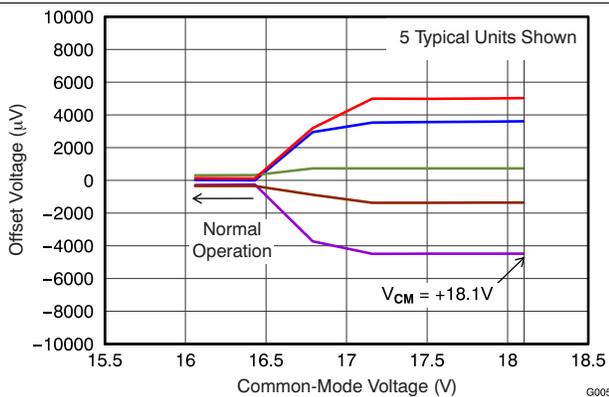


Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

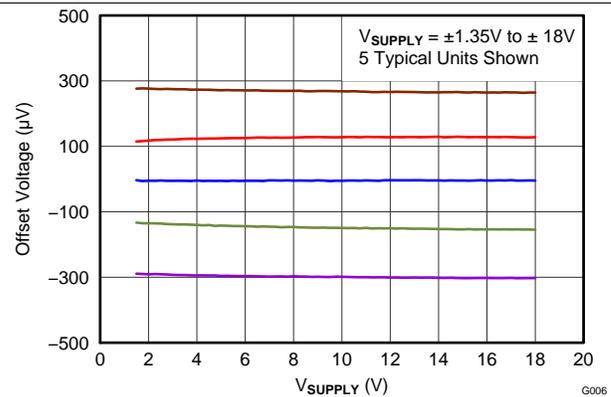


Figure 6. Offset Voltage vs Power Supply

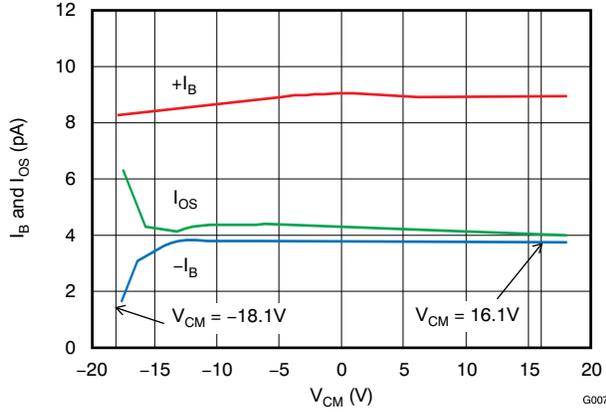


Figure 7.  $I_B$  and  $I_{OS}$  vs Common-Mode Voltage

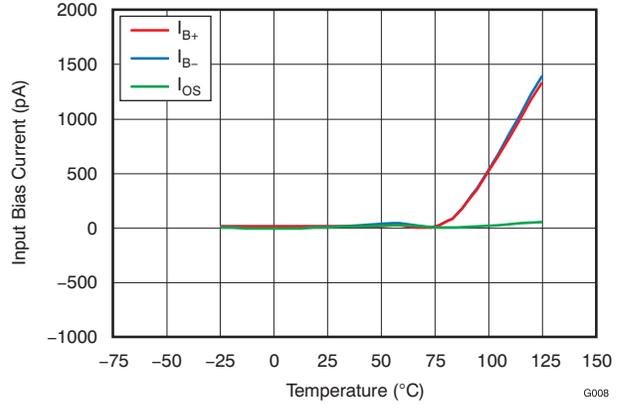


Figure 8. Input Bias Current vs Temperature

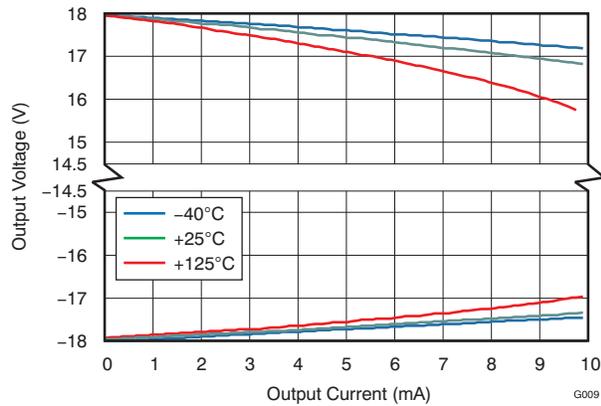


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

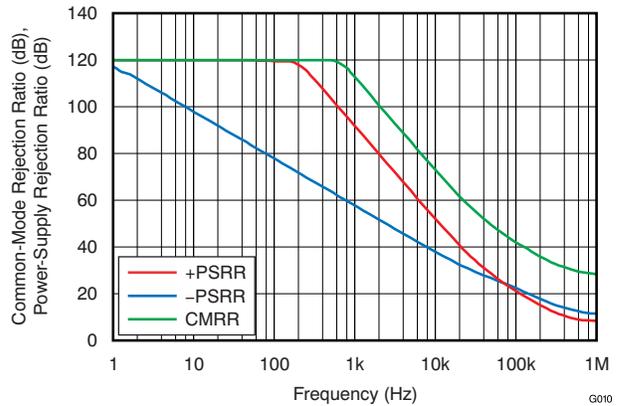


Figure 10. CMRR and PSRR vs Frequency (Referred-to Input)

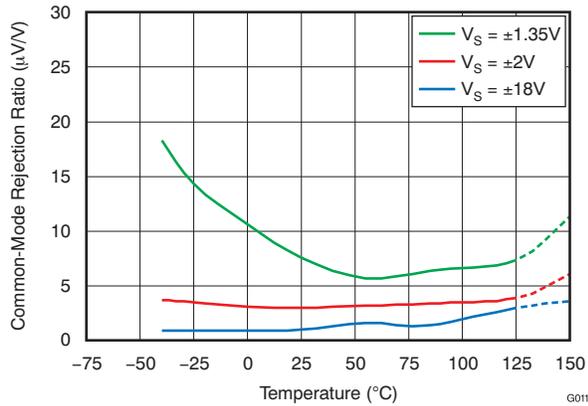


Figure 11. CMRR vs Temperature

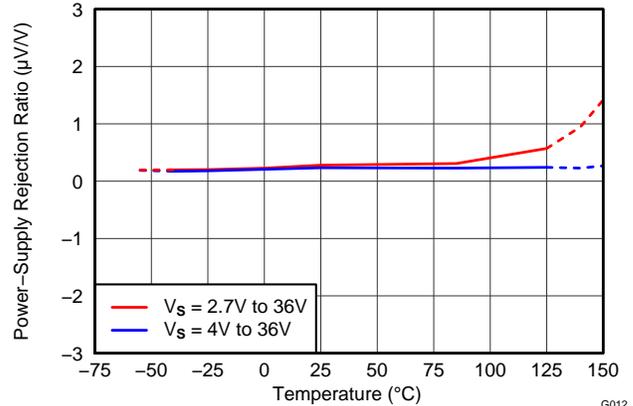


Figure 12. PSRR vs Temperature

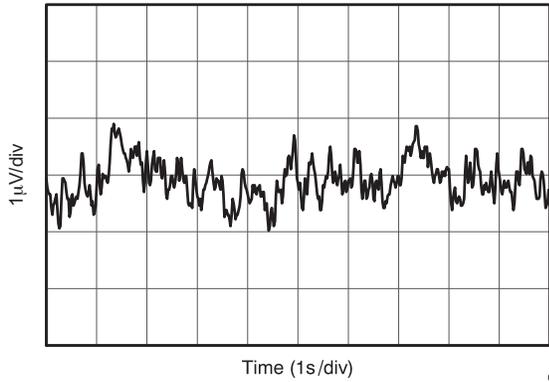


Figure 13. 0.1-Hz to 10-Hz Noise

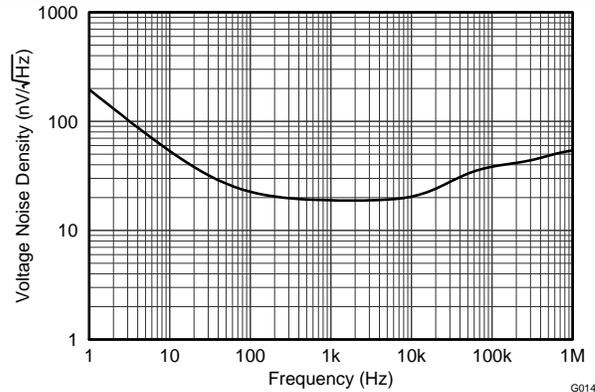


Figure 14. Input Voltage Noise Spectral Density vs Frequency

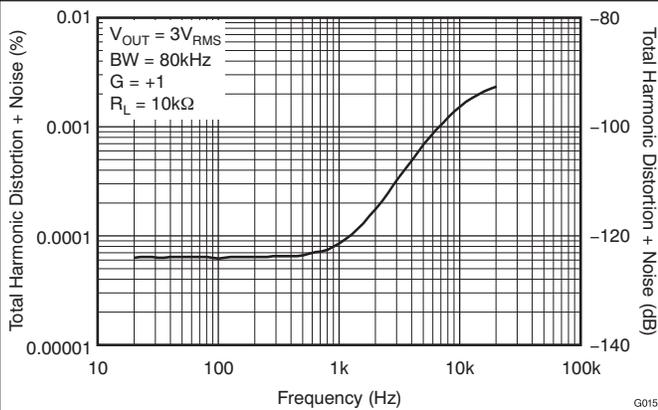


Figure 15. THD+N Ratio vs Frequency

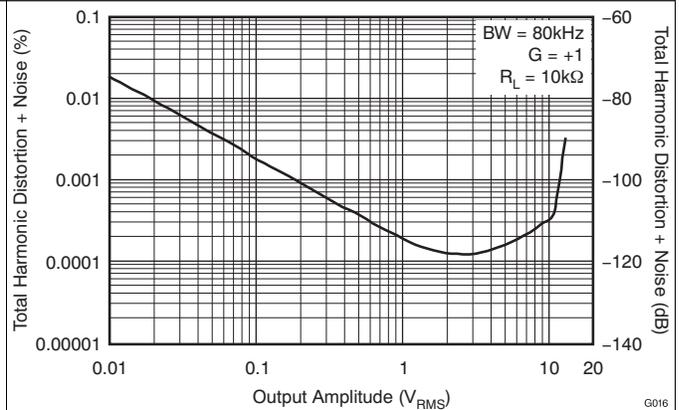


Figure 16. THD+N vs Output Amplitude

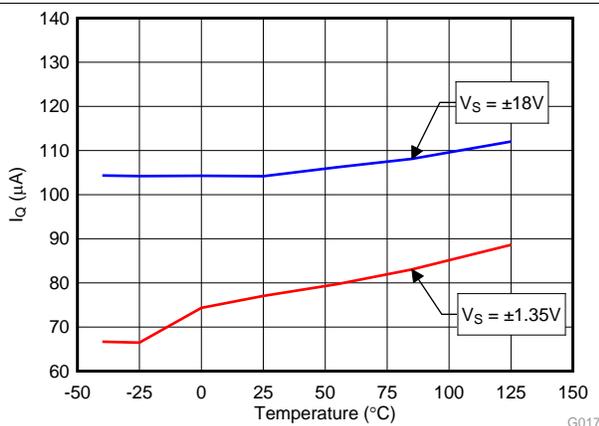


Figure 17. Quiescent Current vs Temperature

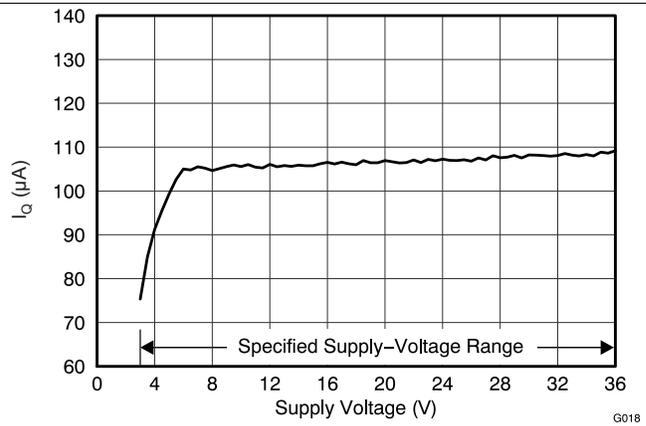


Figure 18. Quiescent Current vs Supply Voltage

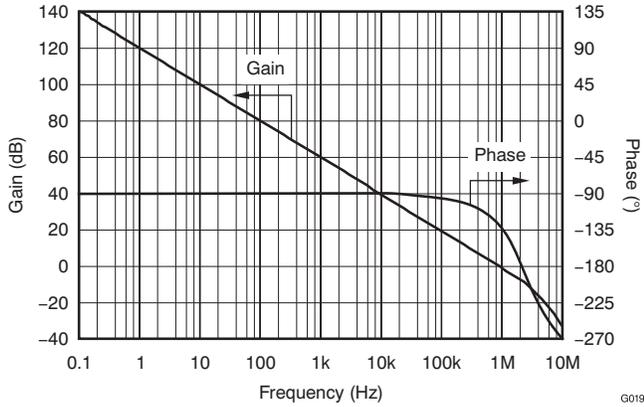


Figure 19. Open-Loop Gain and Phase vs Frequency

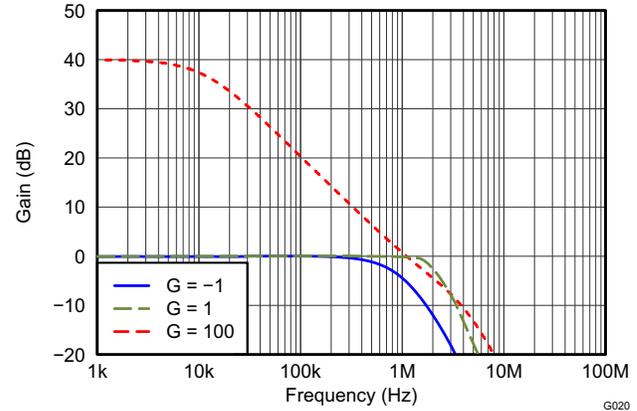


Figure 20. Closed-Loop Gain vs Frequency

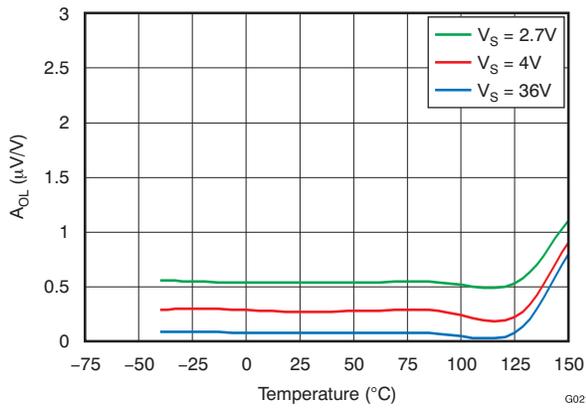


Figure 21. Open-Loop Gain vs Temperature

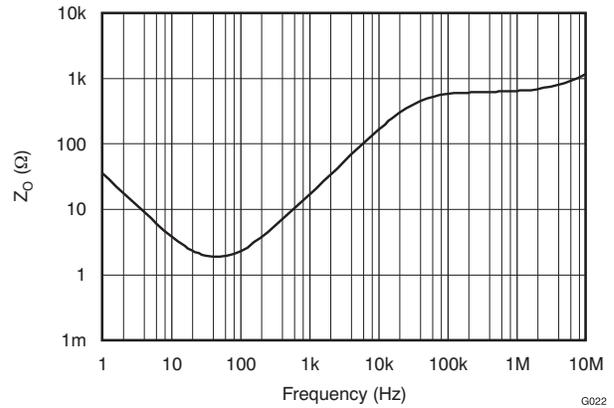


Figure 22. Open-Loop Output Impedance vs Frequency

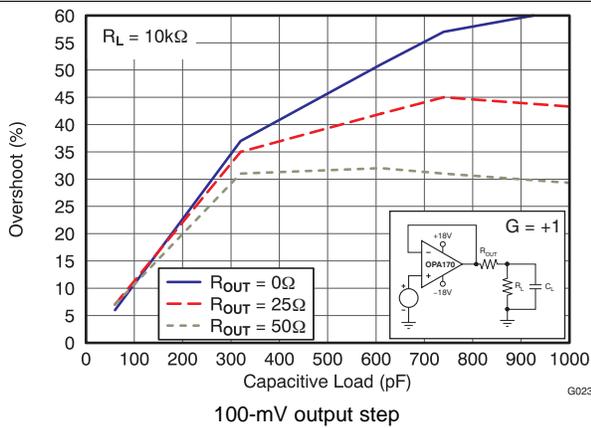


Figure 23. Small-Signal Overshoot vs Capacitive Load

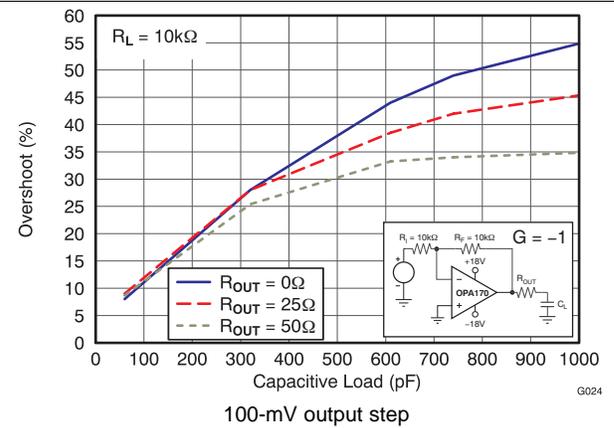


Figure 24. Small-Signal Overshoot vs Capacitive Load

OPA170, OPA2170, OPA4170

SBOS557E – AUGUST 2011 – REVISED APRIL 2018

www.ti.com

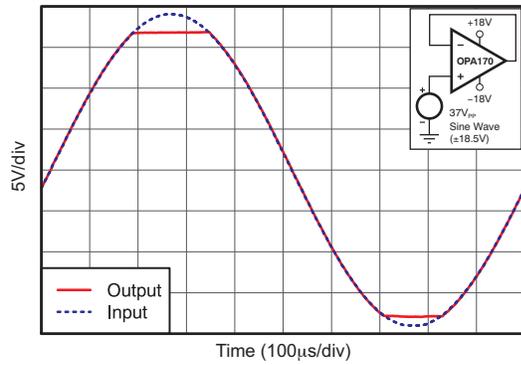


Figure 25. No Phase Reversal

G025

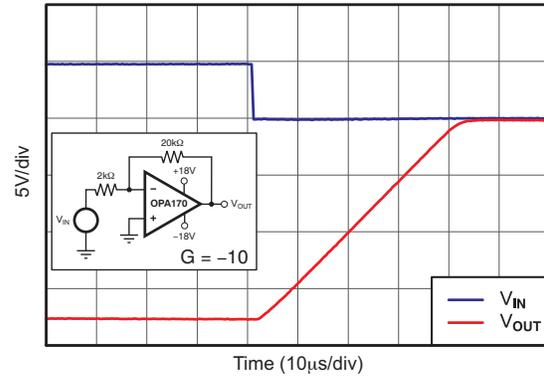


Figure 26. Positive Overload Recovery

G026

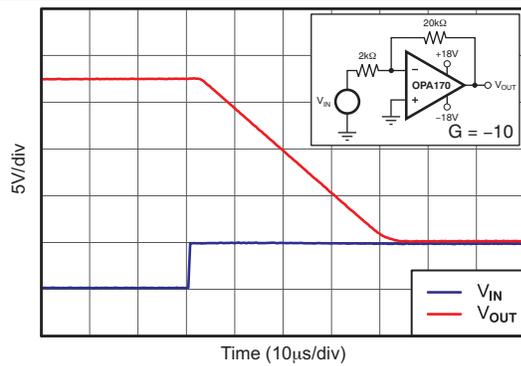


Figure 27. Negative Overload Recovery

G027

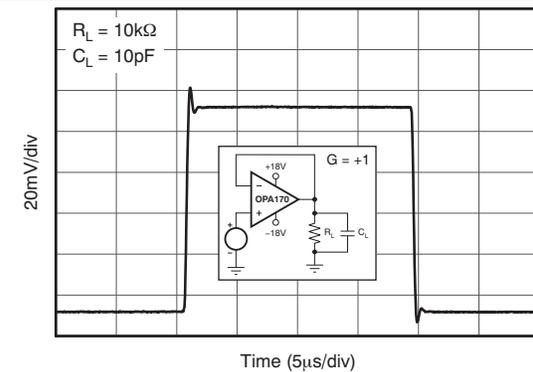


Figure 28. Small-Signal Step Response (100 mV)

G028

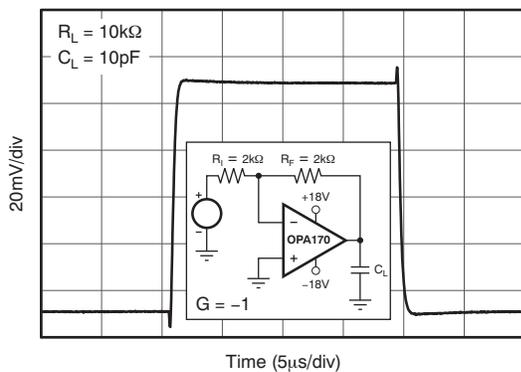


Figure 29. Small-Signal Step Response (100 mV)

G029

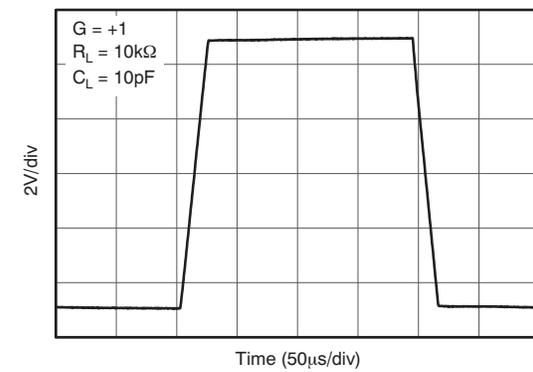


Figure 30. Large-Signal Step Response

G030

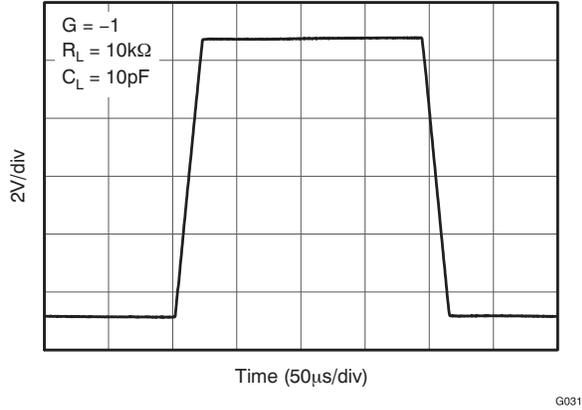


Figure 31. Large-Signal Step Response

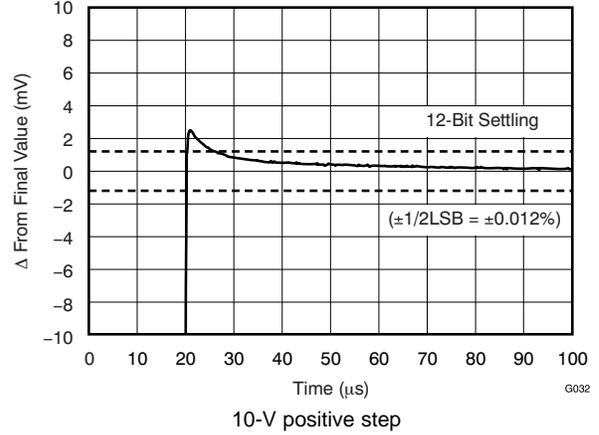


Figure 32. Large-Signal Settling Time

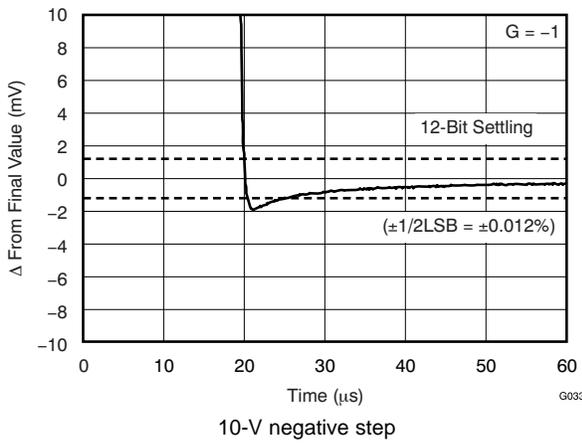


Figure 33. Large-Signal Settling Time

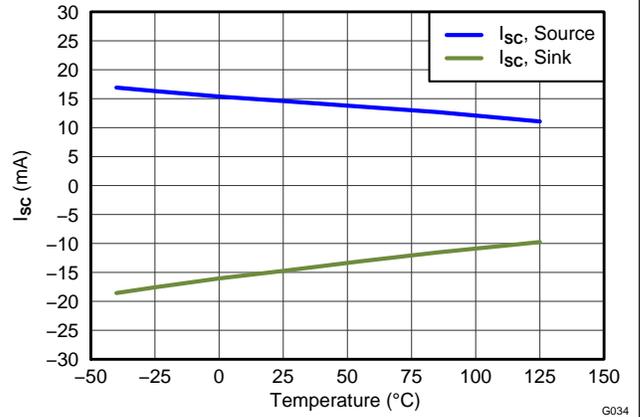


Figure 34. Short-Circuit Current vs Temperature

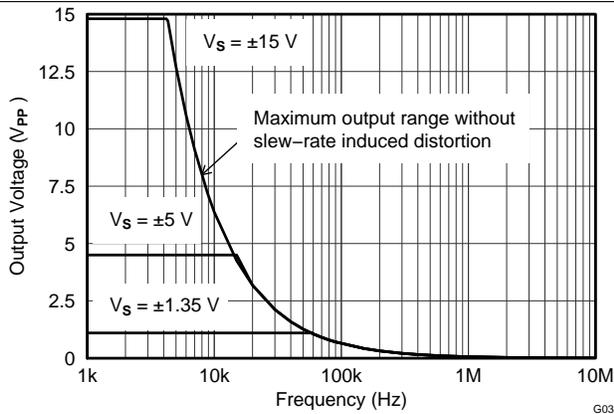


Figure 35. Maximum Output Voltage vs Frequency

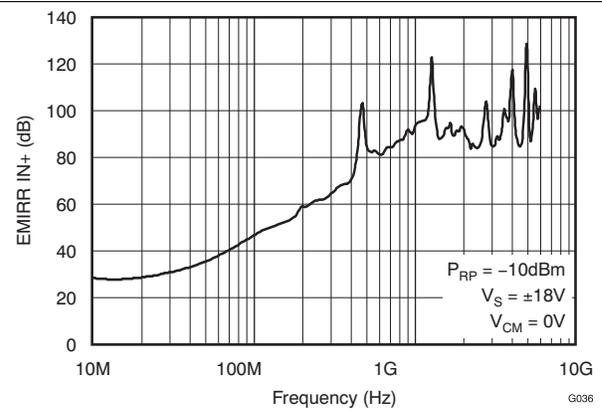


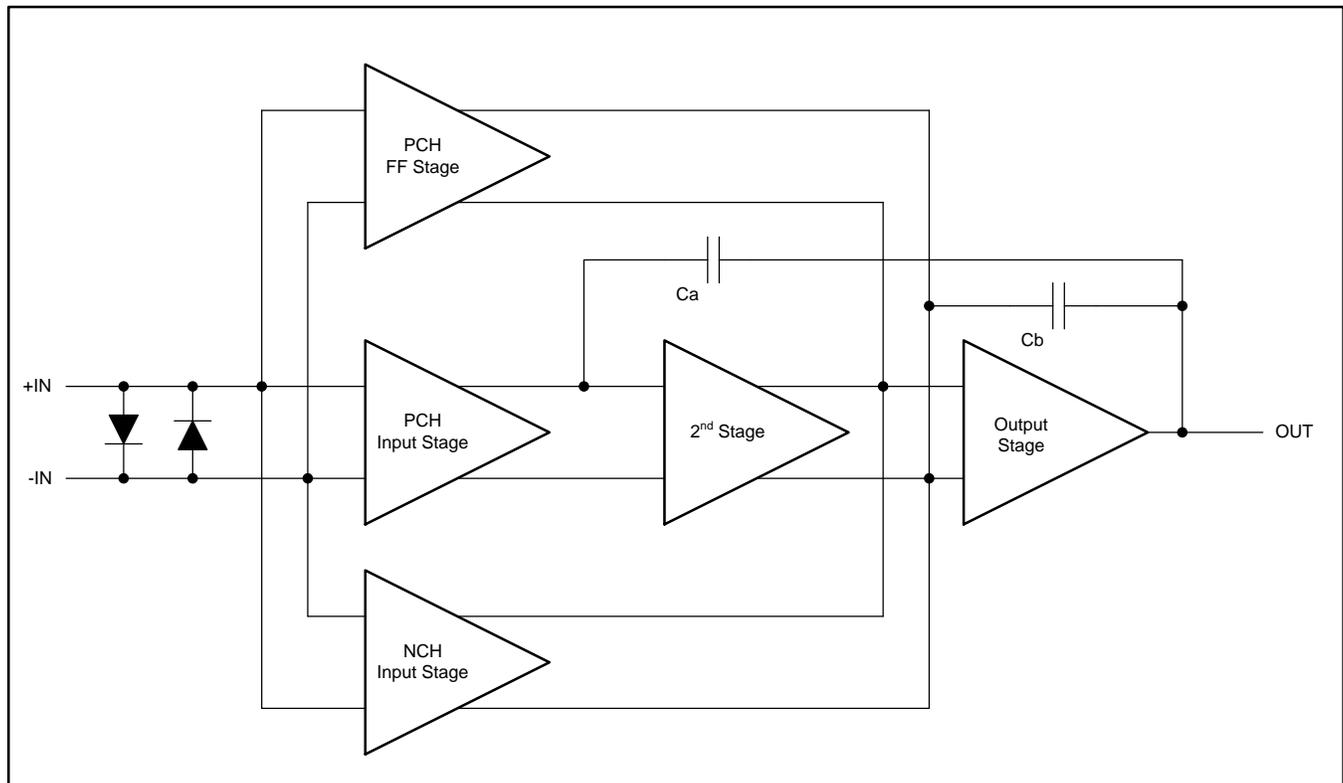
Figure 36. EMIRR IN+ vs Frequency

## 8 Detailed Description

### 8.1 Overview

The OPAx170 family of operational amplifiers provides high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only  $2 \mu\text{V}/^\circ\text{C}$  provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and  $A_{OL}$ .

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Operating Characteristics

The OPAx170 family of amplifiers is specified for operation from 2.7 V to 36 V ( $\pm 1.35 \text{ V}$  to  $\pm 18 \text{ V}$ ). Many of the specifications apply from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

## Feature Description (continued)

### 8.3.2 Phase-Reversal Protection

The OPAx170 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx170 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 37.

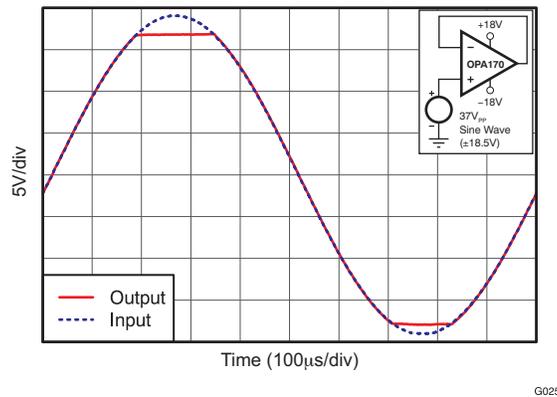
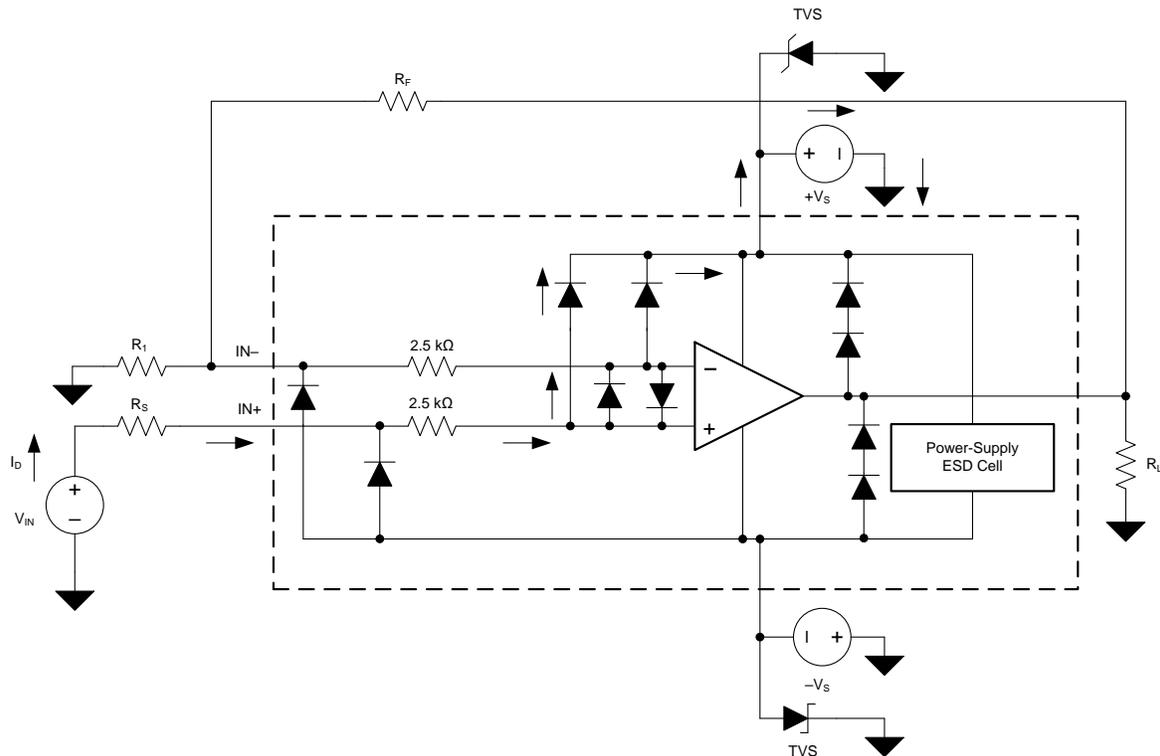


Figure 37. No Phase Reversal

### 8.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 38 illustrates the ESD circuits contained in the OPAx170 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

**Feature Description (continued)**


**Figure 38. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx170 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (refer to [Figure 38](#)), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

[Figure 38](#) shows a specific example where the input voltage ( $V_{IN}$ ) exceeds the positive supply voltage ( $V+$ ) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $V+$  can sink the current, one of the upper input steering diodes conducts and directs current to  $V+$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current,  $V_{IN}$  can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

## Feature Description (continued)

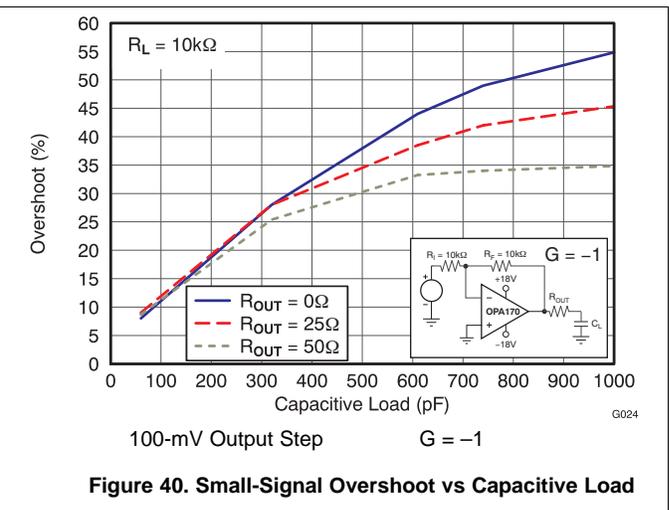
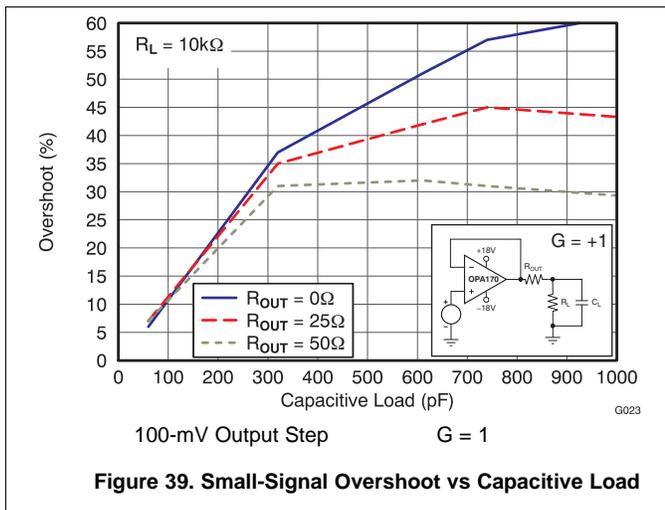
Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ( $V+$  or  $V-$ ) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see [Figure 38](#). Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPAX170 input pins are protected from excessive differential voltage with back-to-back diodes; see [Figure 38](#). In most circuit applications, the input protection circuitry has no effect. However, in low-gain or  $G = 1$  circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAX170. [Figure 38](#) illustrates an example configuration that implements a current-limiting feedback resistor.

### 8.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAX170 have been optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example,  $R_{OUT}$  equal to 50  $\Omega$ ) in series with the output. Refer to [Figure 39](#) and [Figure 40](#) illustrate graphs of small-signal overshoot versus capacitive load for several values of  $R_{OUT}$ . Also, refer to applications bulletin AB-028, [Feedback Plots Define Op Amp AC Performance](#), for details of analysis techniques and application circuits.



## 8.4 Device Functional Modes

### 8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx170 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in [Table 2](#).

**Table 2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply**

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
	vs temperature	12		μV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
Gain-bandwidth product		0.3		MHz
Slew rate		0.3		V/μs

### 8.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx170 is approximately 2 μs.

## 9 Application and Implementation

### NOTE

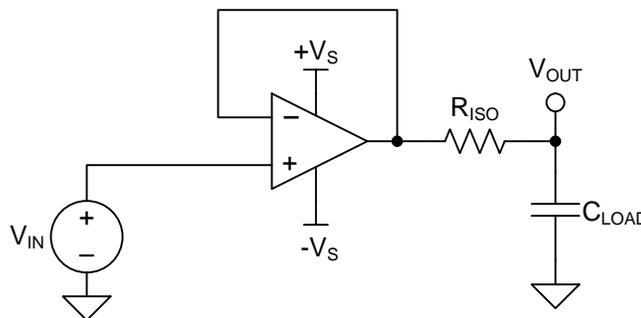
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The OPAx170 family of operational amplifiers provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1- $\mu\text{F}$  capacitors are adequate. Follow the additional recommendations in [Layout Guidelines](#) in order to achieve the maximum performance from this device. Many applications may introduce capacitive loading to the output of the amplifier (potentially causing instability). One method of stabilizing the amplifier in such applications is to add an isolation resistor between the amplifier output and the capacitive load. The design process for selecting this resistor is given in [Typical Application](#).

### 9.2 Typical Application

This circuit can be used to drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor ( $R_{\text{ISO}}$ ) to stabilize the output of an operational amplifier.  $R_{\text{ISO}}$  modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.



**Figure 41. Unity-Gain Buffer With  $R_{\text{ISO}}$  Stability Compensation**

#### 9.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V ( $\pm 15$  V)
- Capacitive loads: 100 pF, 1000 pF, 0.01  $\mu\text{F}$ , 0.1  $\mu\text{F}$ , and 1  $\mu\text{F}$
- Phase margin: 45° and 60°

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the OPAx170 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{\text{IN}}$ ), output voltage ( $V_{\text{OUT}}$ ), and output current ( $I_{\text{OUT}}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance

**Typical Application (continued)**

- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

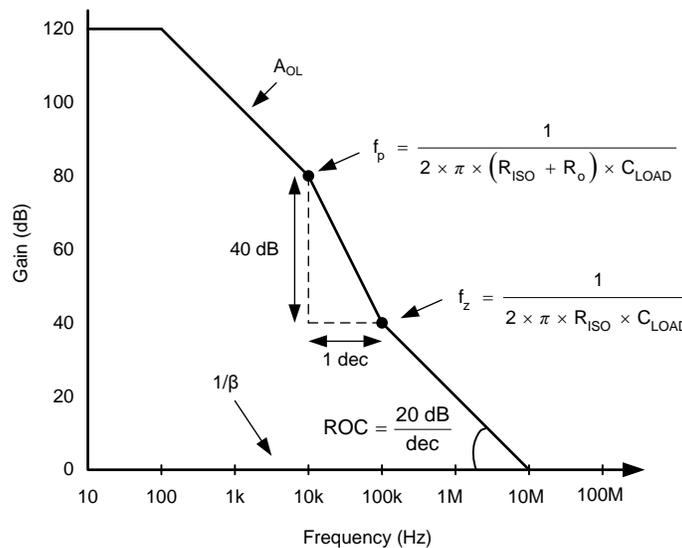
Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

**9.2.2.2 Unity-Gain Buffer**

Figure 41 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 41. Not shown in Figure 41 is the open-loop output resistance of the operational amplifier,  $R_o$ .

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \tag{1}$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole ( $f_p$ ) is determined by  $(R_o + R_{ISO})$  and  $C_{LOAD}$ . Components  $R_{ISO}$  and  $C_{LOAD}$  determine the frequency of the zero ( $f_z$ ). A stable system is obtained by selecting  $R_{ISO}$  such that the rate of closure (ROC) between the open-loop gain ( $A_{OL}$ ) and  $1/\beta$  is 20 dB/decade. Figure 42 depicts the concept. The  $1/\beta$  curve for a unity-gain buffer is 0 dB.



**Figure 42. Unity-Gain Amplifier With  $R_{ISO}$  Compensation**

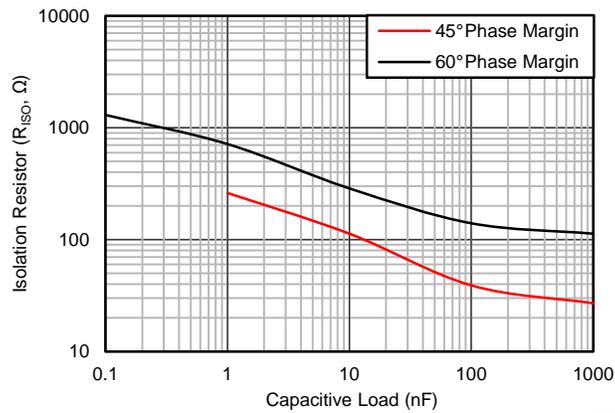
ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of  $R_o$ . In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA170, see the Precision Design, [Capacitive Load Drive Solution Using an Isolation Resistor](#).

**Table 3. Phase Margin versus Overshoot and AC Gain Peaking**

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

### 9.2.3 Application Curve

Using the described methodology, the values of  $R_{ISO}$  that yield phase margins of  $45^\circ$  and  $60^\circ$  for various capacitive loads were determined. The results are shown in Figure 43.



**Figure 43. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin**

## 10 Power Supply Recommendations

The OPAx170 is specified for operation from 2.7 V to 36 V ( $\pm 1.35$  V to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

### CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

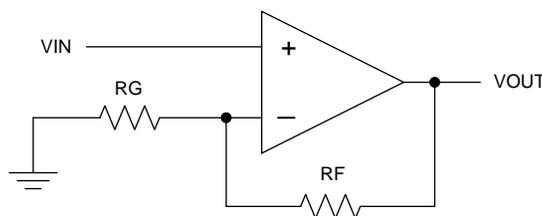
## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

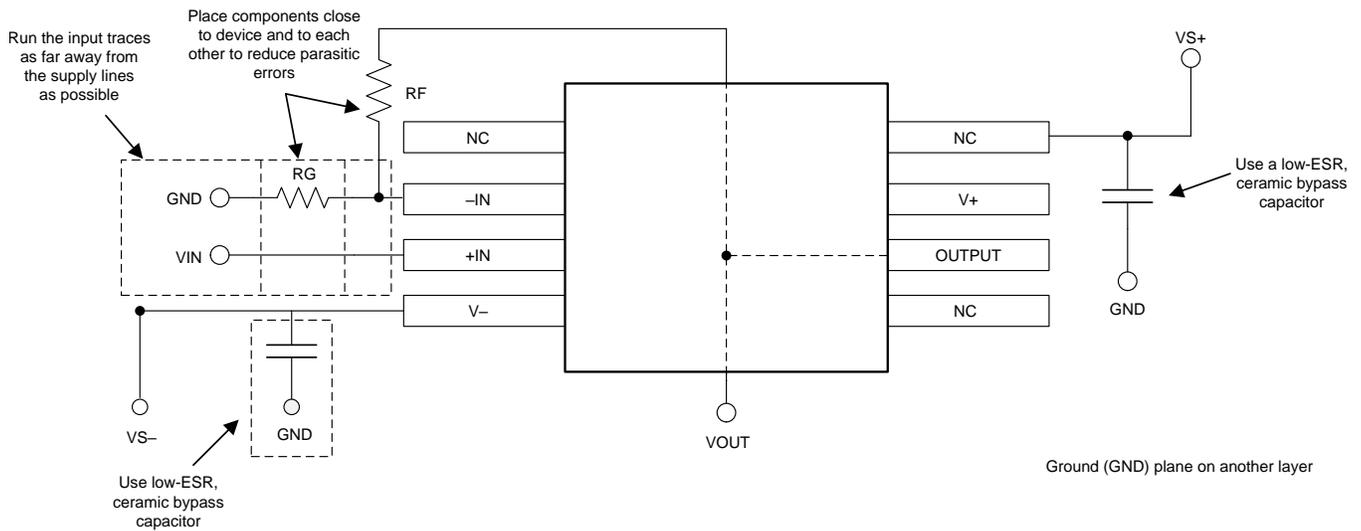
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see application report [SLOA089, Circuit Board Layout Techniques](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 45](#), keeping  $R_F$  and  $R_G$  close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 11.2 Layout Example



**Figure 44. Schematic Representation**

**Layout Example (continued)**



**Figure 45. Operational Amplifier Board Layout for a Noninverting Configuration**

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 12.1.2 Development Support

##### 12.1.2.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

---

#### NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

---

##### 12.1.2.2 DIP Adapter EVM

The [DIP Adapter EVM](#) tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

##### 12.1.2.3 Universal Operational Amplifier EVM

The [Universal Op Amp EVM](#) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT23 packages are all supported.

---

#### NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

---

##### 12.1.2.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at <http://www.ti.com/ww/en/analog/precision-designs/>.

## Device Support (continued)

### 12.1.2.5 WEBENCH® Filter Designer

**WEBENCH® Filter Designer** is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, **WEBENCH® Filter Designer** allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

### 12.1.2.6 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the OPAx170 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

## 12.2 Documentation Support

### 12.2.1 Related Documentation

For related documentation, see the following (available for download from [www.ti.com](http://www.ti.com)):

- [Feedback Plots Define Op Amp AC Performance](#)
- [Capacitive Load Drive Solution Using an Isolation Resistor](#)
- [Circuit Board Layout Techniques](#)

### 12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 4. Related Links**

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA170	<a href="#">Click here</a>				
OPA2170	<a href="#">Click here</a>				
OPA4170	<a href="#">Click here</a>				

### 12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## Community Resources (continued)

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.6 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

TINA, DesignSoft are trademarks of DesignSoft, Inc.

All other trademarks are the property of their respective owners.

## 12.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA170AID</a>	Active	Production	SOIC (D)   8	75   BULK	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O170A
OPA170AID.A	Active	Production	SOIC (D)   8	75   BULK	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O170A
<a href="#">OPA170AIDBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI
OPA170AIDBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI
OPA170AIDBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI
OPA170AIDBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI
<a href="#">OPA170AIDBVT</a>	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI
OPA170AIDBVT.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI
<a href="#">OPA170AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O170A
OPA170AIDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O170A
<a href="#">OPA170AIDRLR</a>	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAQ
OPA170AIDRLR.A	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAQ
<a href="#">OPA170AIDRLT</a>	Active	Production	SOT-5X3 (DRL)   5	250   SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAQ
OPA170AIDRLT.A	Active	Production	SOT-5X3 (DRL)   5	250   SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAQ
<a href="#">OPA2170AID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A
OPA2170AID.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A
<a href="#">OPA2170AIDCUR</a>	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC
OPA2170AIDCUR.A	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC
<a href="#">OPA2170AIDCUT</a>	Active	Production	VSSOP (DCU)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC
OPA2170AIDCUT.A	Active	Production	VSSOP (DCU)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC
OPA2170AIDCUTG4	Active	Production	VSSOP (DCU)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC
OPA2170AIDCUTG4.A	Active	Production	VSSOP (DCU)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC
<a href="#">OPA2170AIDGK</a>	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPNI
OPA2170AIDGK.A	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPNI
<a href="#">OPA2170AIDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU   SN   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPNI
OPA2170AIDGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPNI
OPA2170AIDGKRG4	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPNI
OPA2170AIDGKRG4.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPNI

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA2170AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A
OPA2170AIDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A
OPA2170AIDRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A
OPA2170AIDRG4.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A
<a href="#">OPA2170AIDSGR</a>	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1D4U
OPA2170AIDSGR.A	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1D4U
OPA2170AIDSGRG4	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1D4U
OPA2170AIDSGRG4.A	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1D4U
<a href="#">OPA2170AIDSGT</a>	Active	Production	WSON (DSG)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1D4U
OPA2170AIDSGT.A	Active	Production	WSON (DSG)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1D4U
<a href="#">OPA4170AID</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170
OPA4170AID.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170
<a href="#">OPA4170AIDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170
OPA4170AIDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170
OPA4170AIDRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170
OPA4170AIDRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170
<a href="#">OPA4170AIPW</a>	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170
OPA4170AIPW.A	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170
<a href="#">OPA4170AIPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170
OPA4170AIPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170
OPA4170AIPWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170
OPA4170AIPWRG4.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

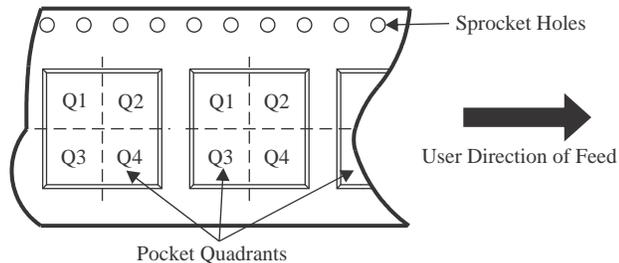
**OTHER QUALIFIED VERSIONS OF OPA170, OPA2170, OPA4170 :**

- Automotive : [OPA170-Q1](#), [OPA2170-Q1](#), [OPA4170-Q1](#)
- Enhanced Product : [OPA170-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA170AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA170AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA170AIDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA170AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA170AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA170AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA170AIDRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA170AIDRLT	SOT-5X3	DRL	5	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA2170AIDCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2170AIDCUT	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2170AIDCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2170AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2170AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2170AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2170AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2170AIDSGR	WSOP	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2170AIDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2170AIDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA4170AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4170AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4170AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4170AIPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

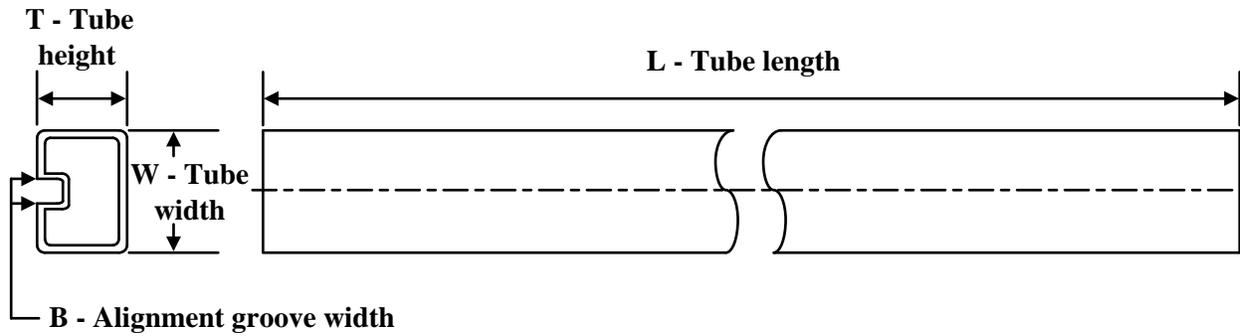
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA170AIDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA170AIDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA170AIDBVRG4	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA170AIDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA170AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA170AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA170AIDRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
OPA170AIDRLT	SOT-5X3	DRL	5	250	202.0	201.0	28.0
OPA2170AIDCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
OPA2170AIDCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
OPA2170AIDCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
OPA2170AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2170AIDGKRG4	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2170AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2170AIDRG4	SOIC	D	8	2500	356.0	356.0	35.0
OPA2170AIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA2170AIDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
OPA2170AIDSGT	WSON	DSG	8	250	210.0	185.0	35.0

---

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4170AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4170AIDRG4	SOIC	D	14	2500	356.0	356.0	35.0
OPA4170AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
OPA4170AIPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA170AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA170AID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2170AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2170AID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2170AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA2170AIDGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4170AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4170AID.A	D	SOIC	14	50	506.6	8	3940	4.32
OPA4170AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
OPA4170AIPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

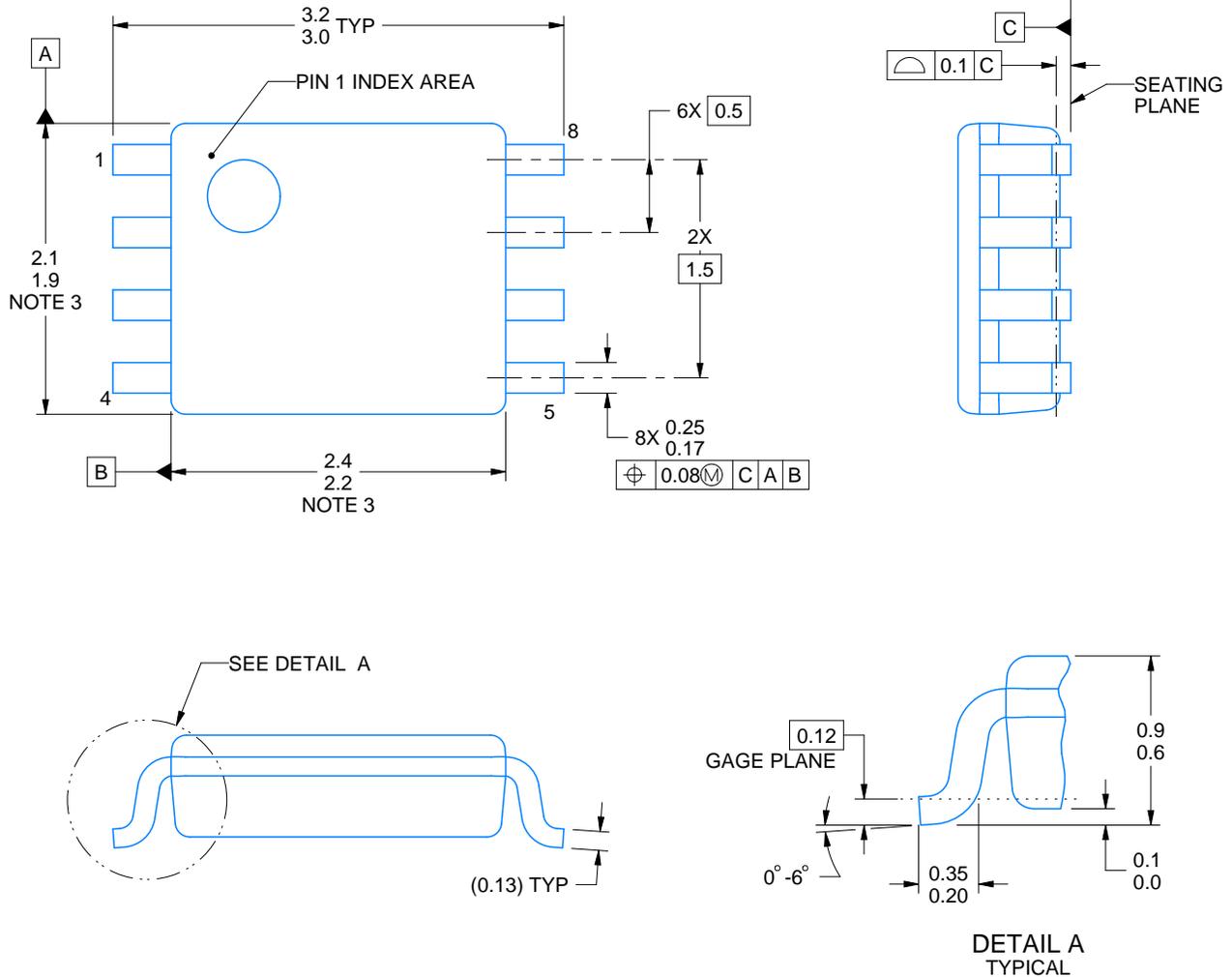
# DCU0008A



# PACKAGE OUTLINE

## VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

### NOTES:

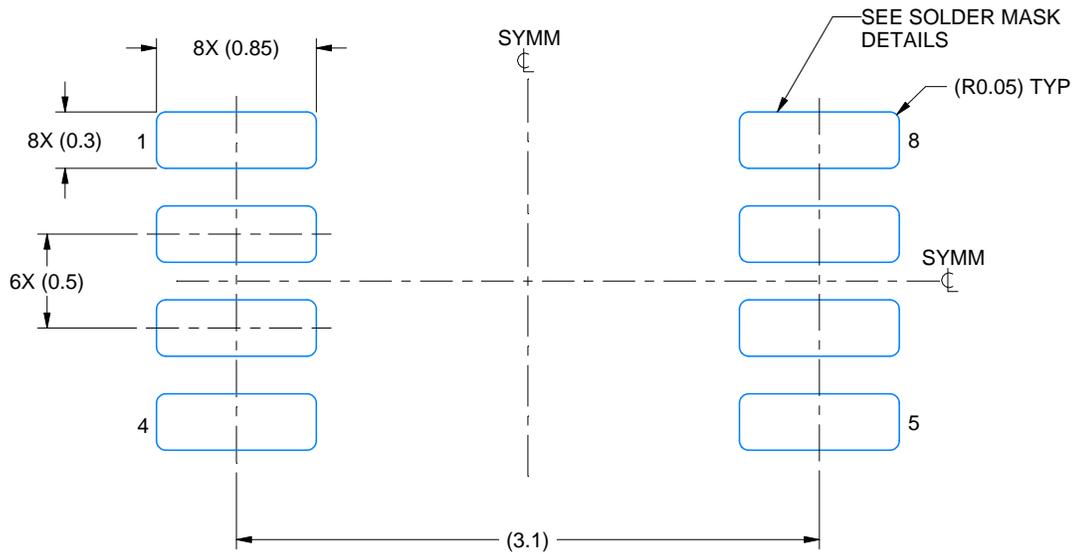
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

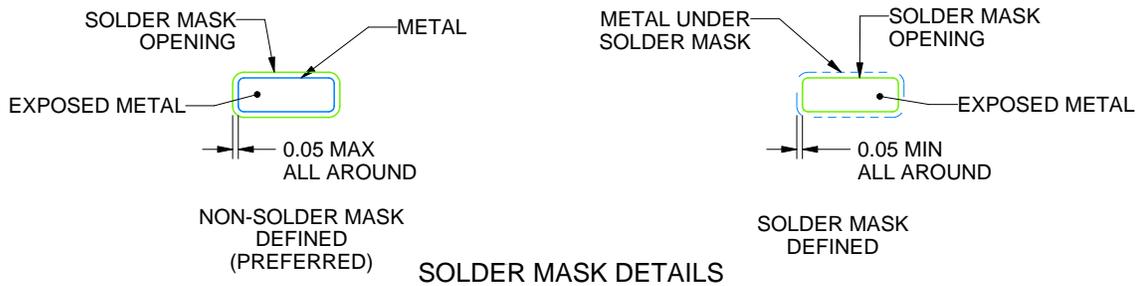
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

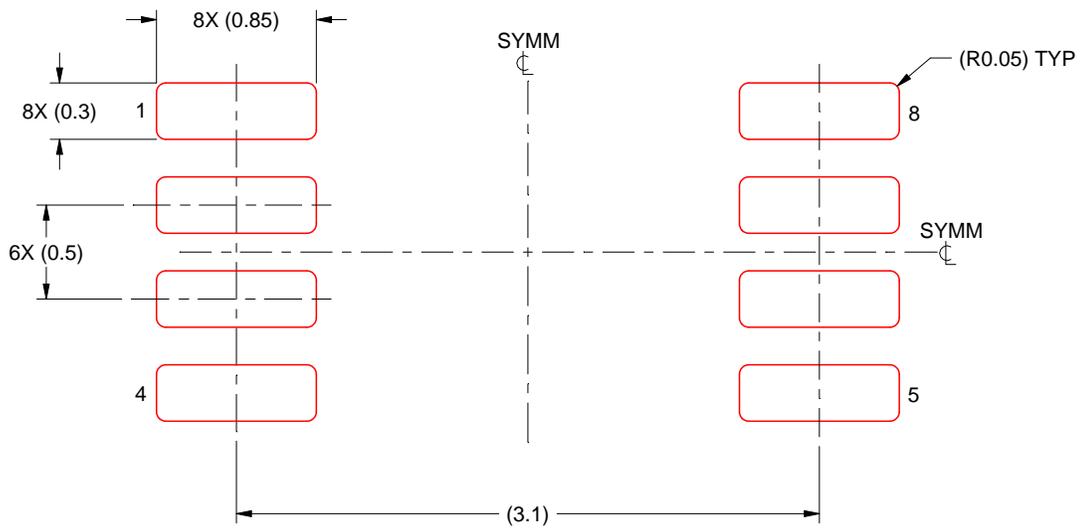
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

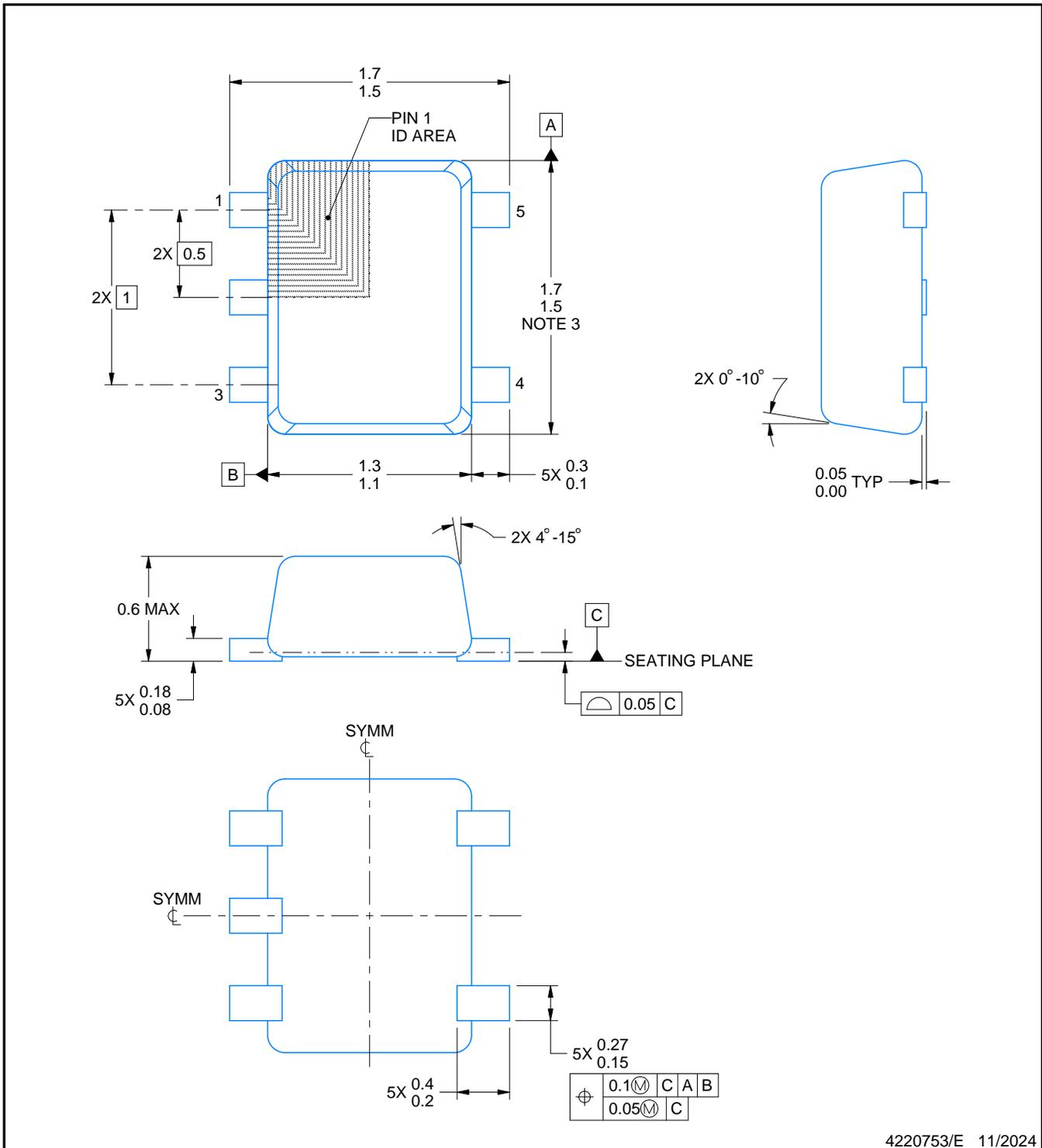
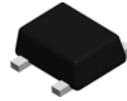


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220753/E 11/2024

NOTES:

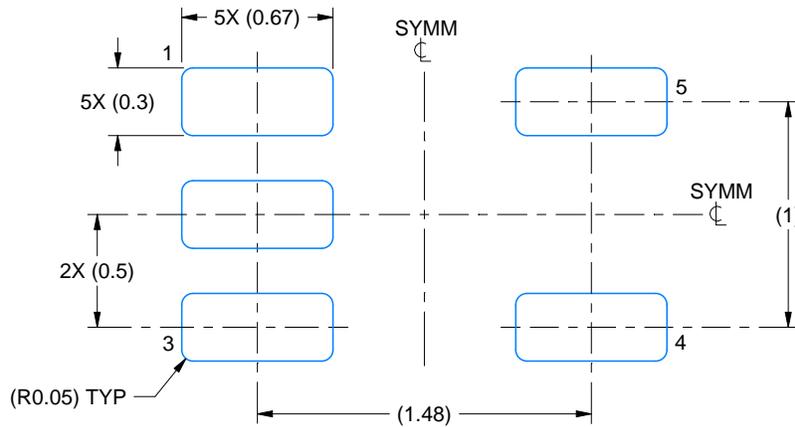
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

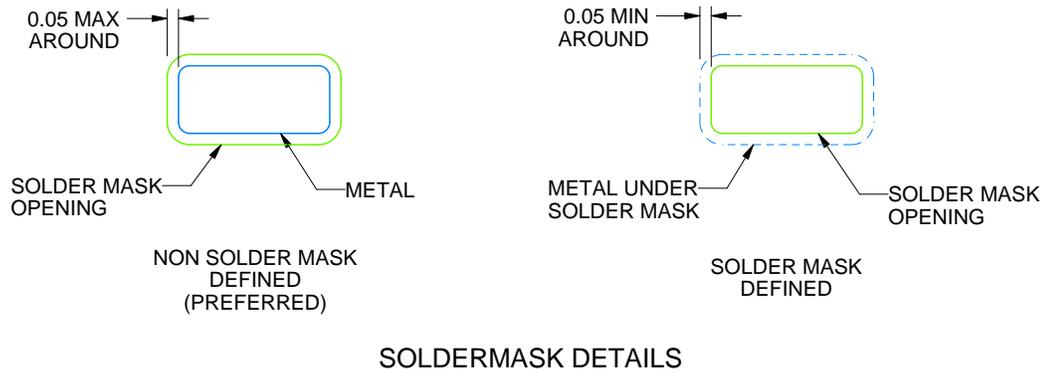
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

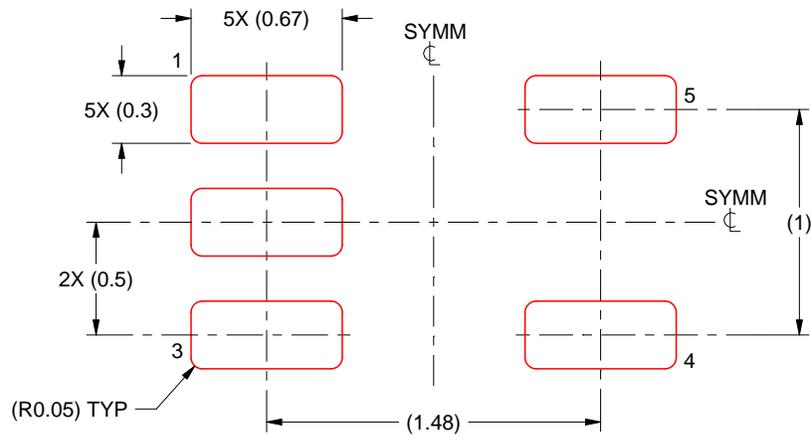
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

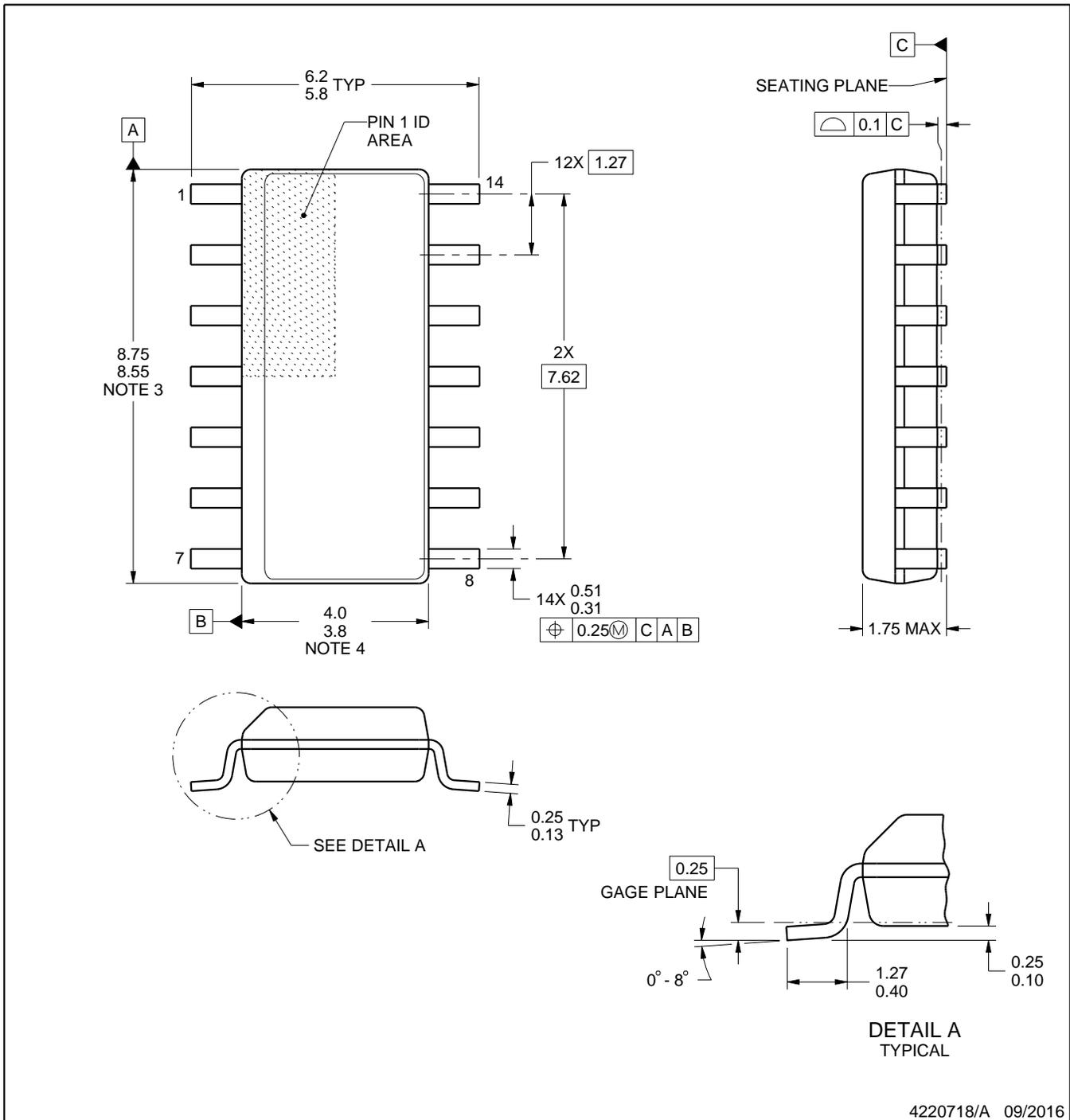
D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

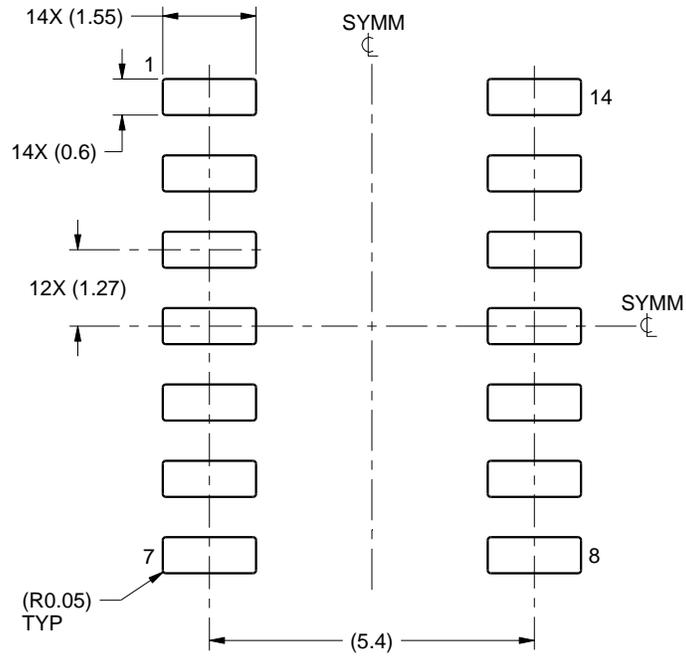
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

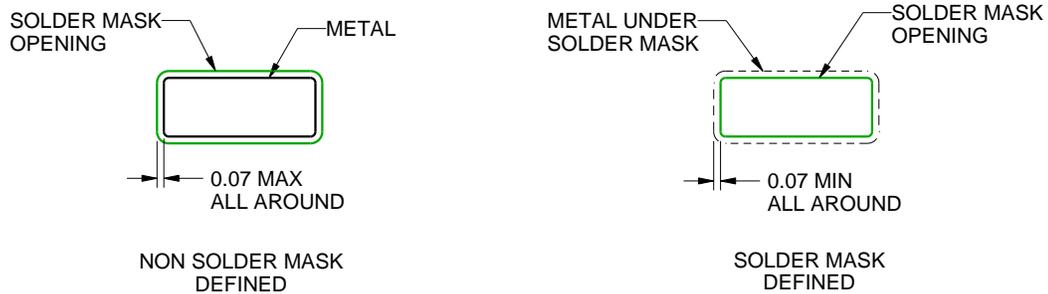
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



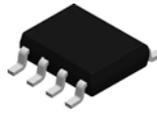
SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



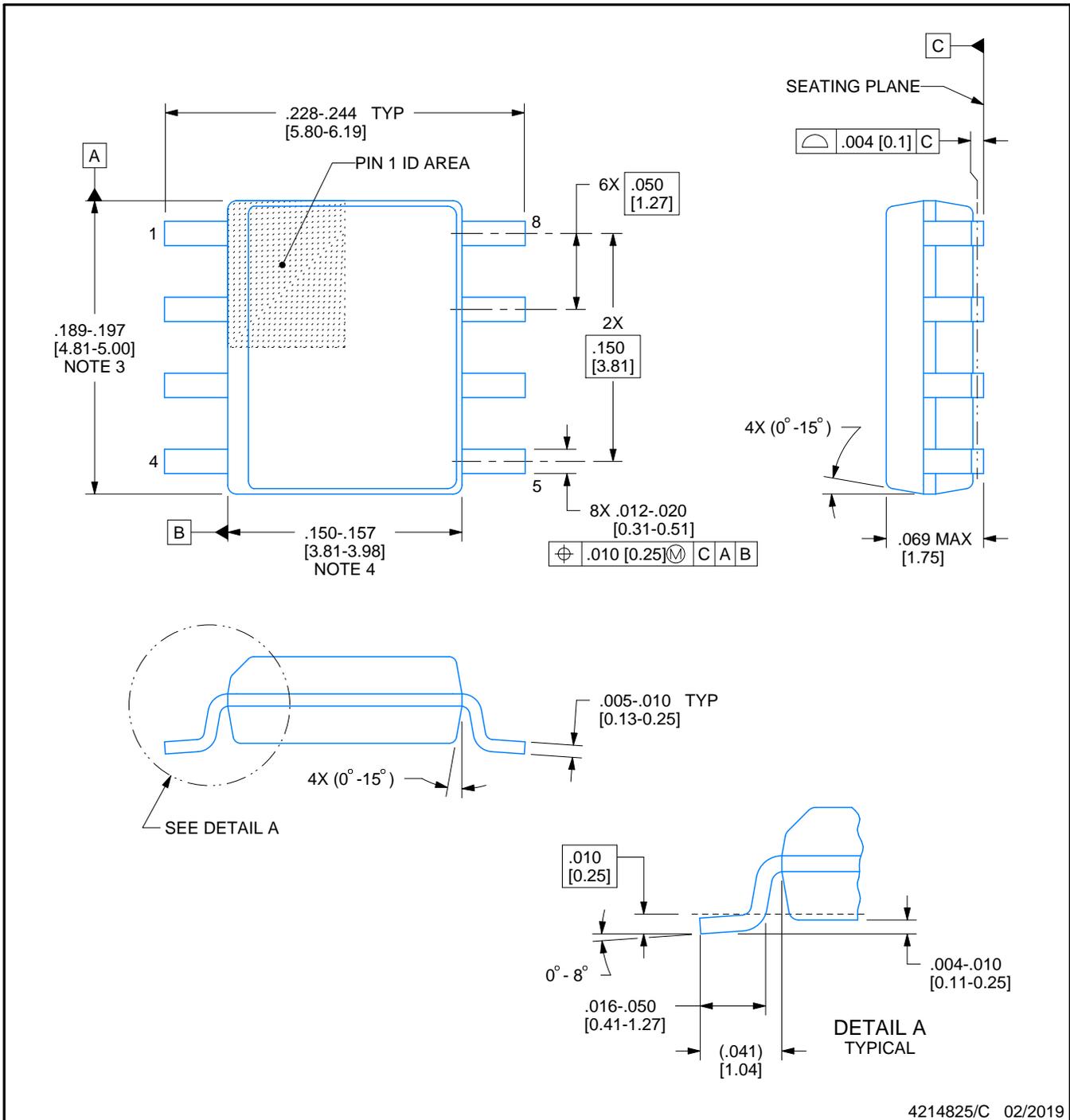


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

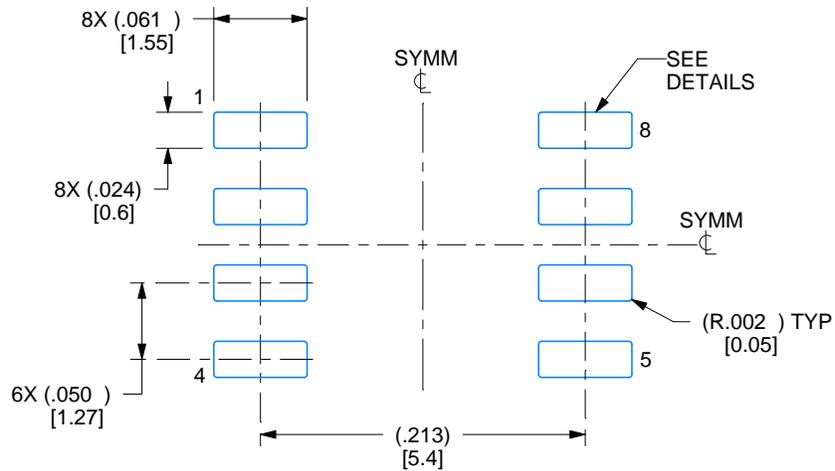
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

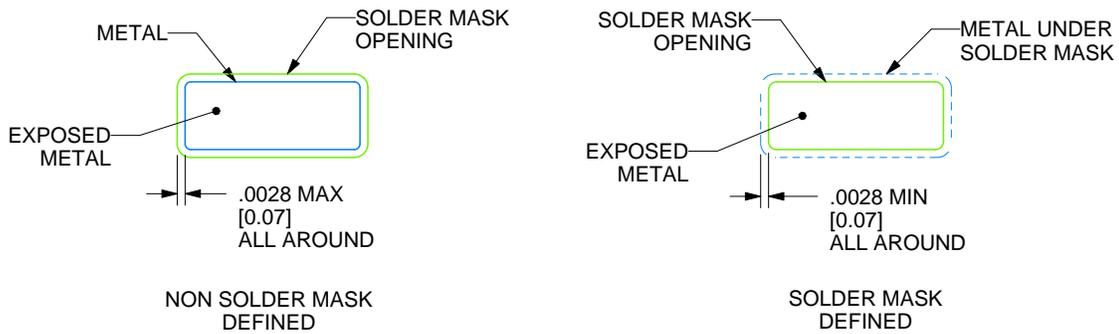
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

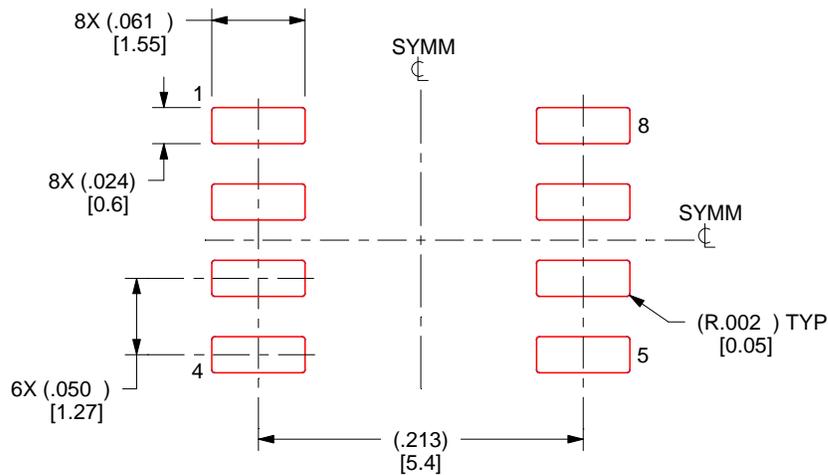
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

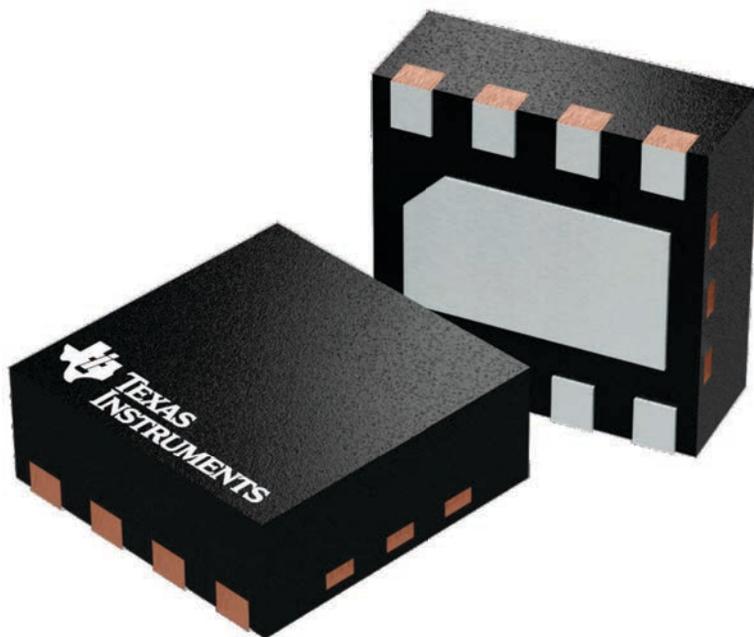
**DSG 8**

**WSON - 0.8 mm max height**

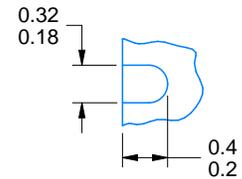
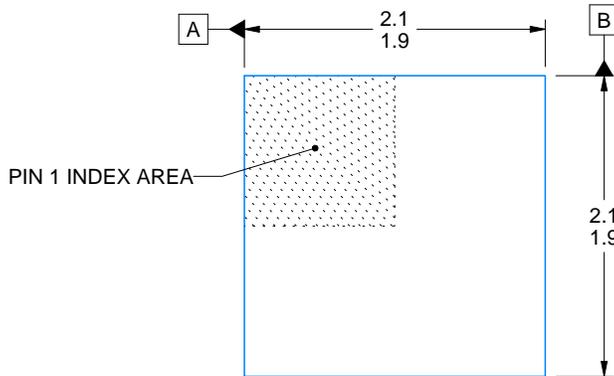
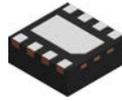
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

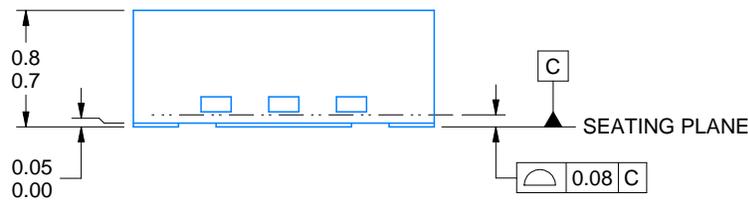
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



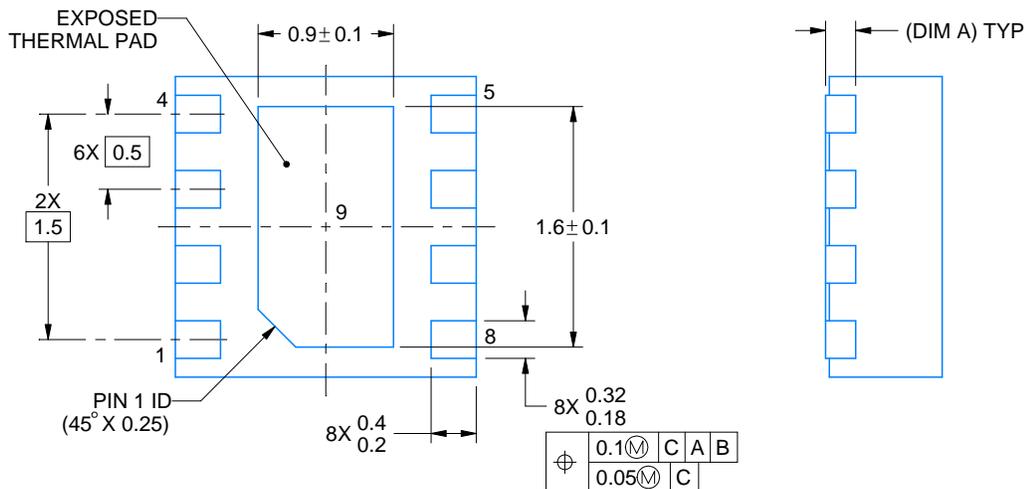
4224783/A



ALTERNATIVE TERMINAL SHAPE TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

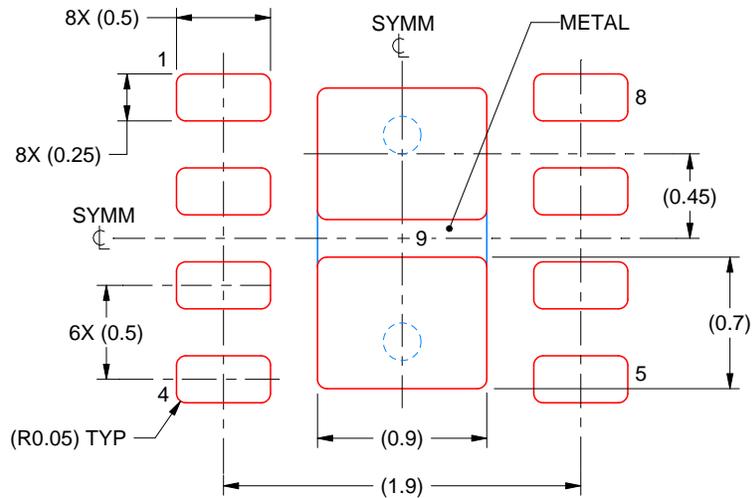


# EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



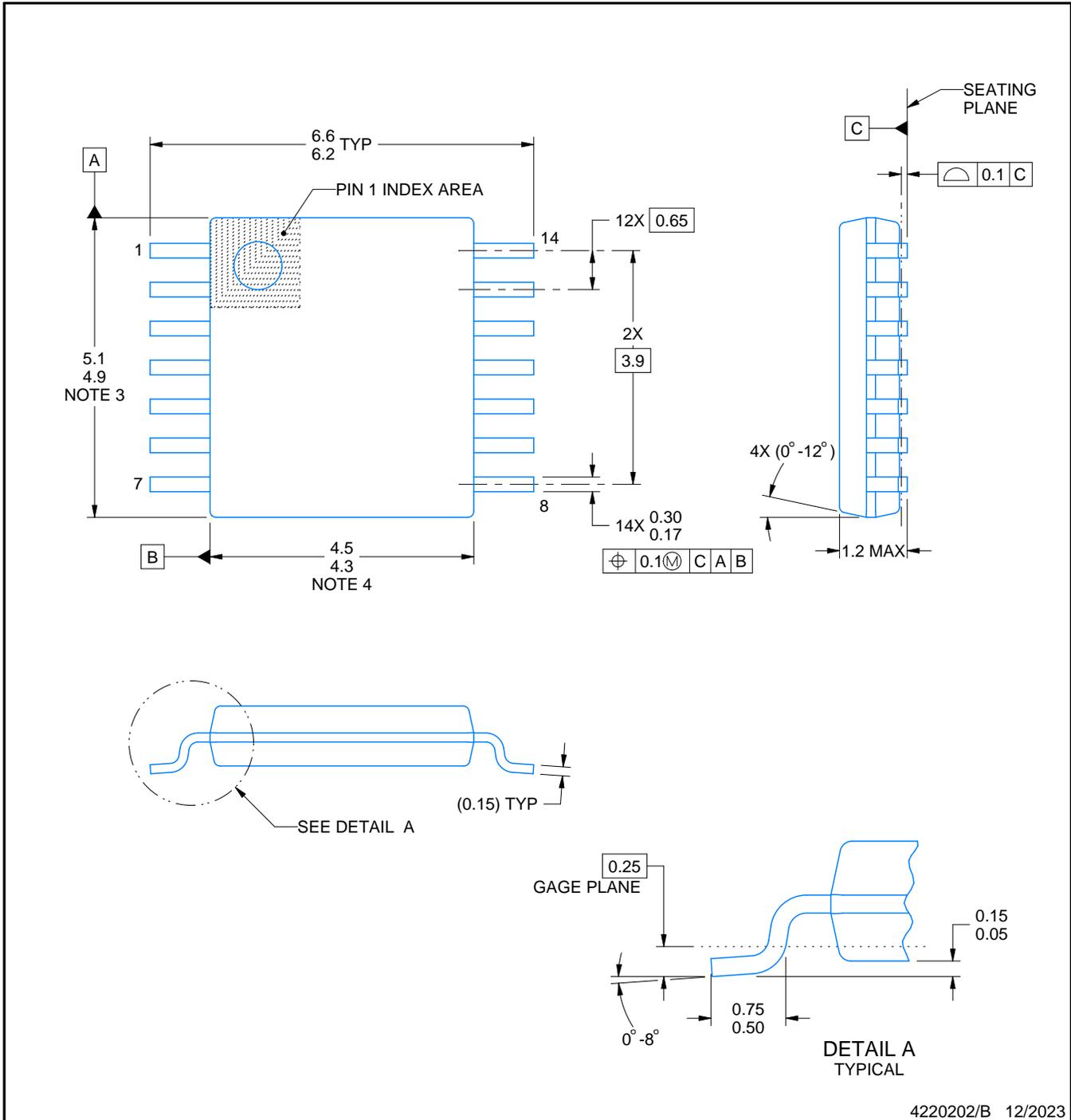
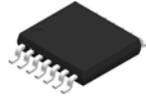
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220202/B 12/2023

NOTES:

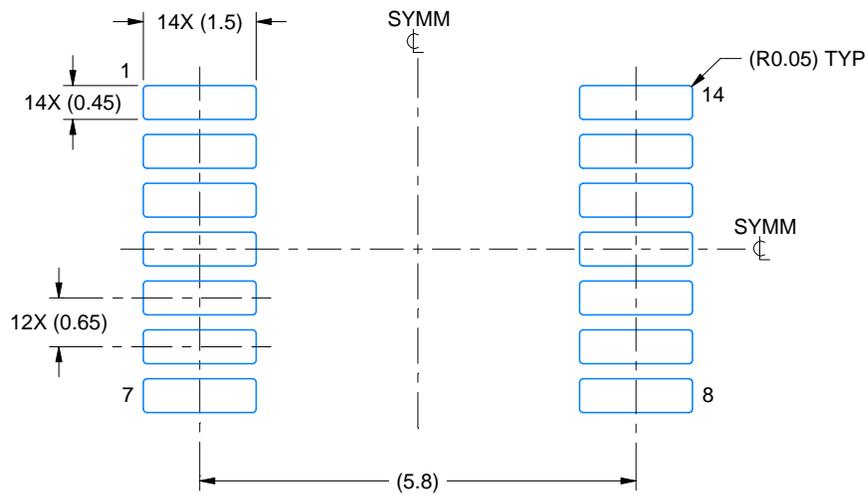
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

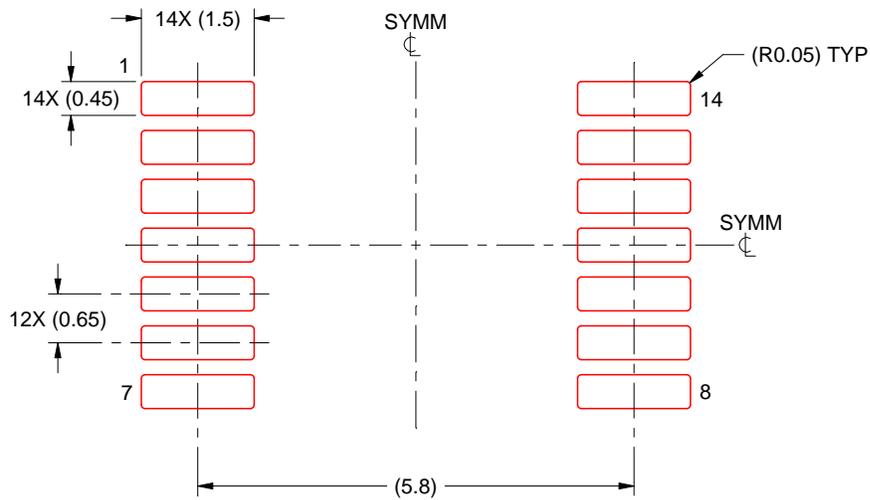
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

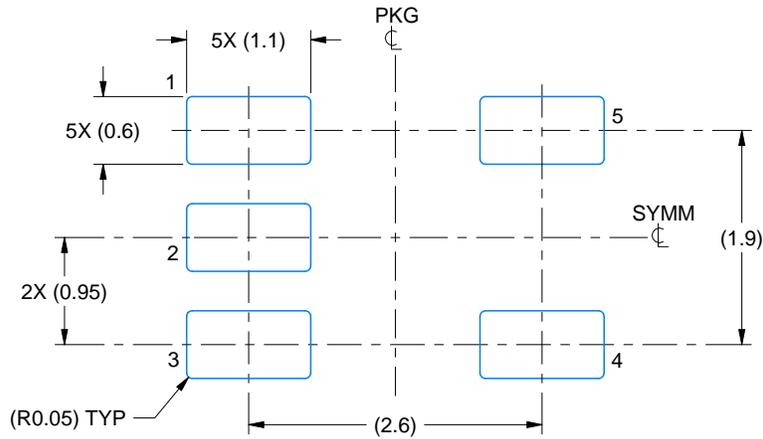


# EXAMPLE BOARD LAYOUT

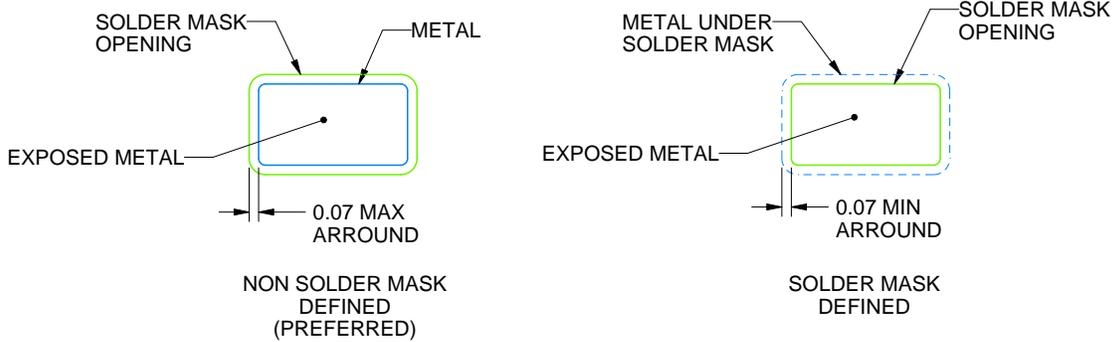
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

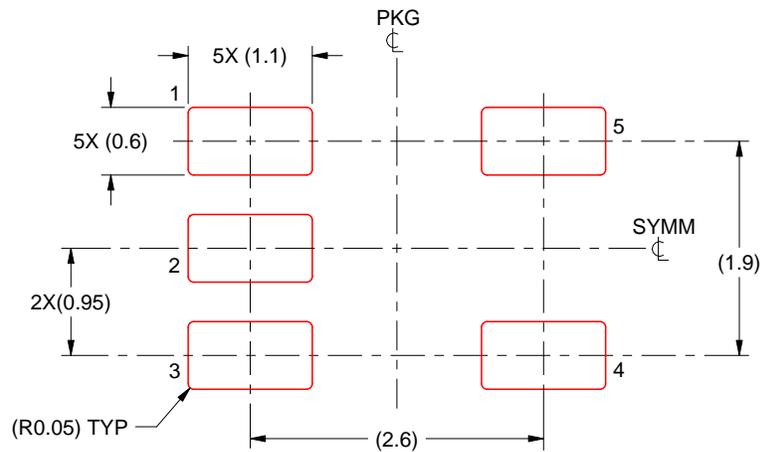
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

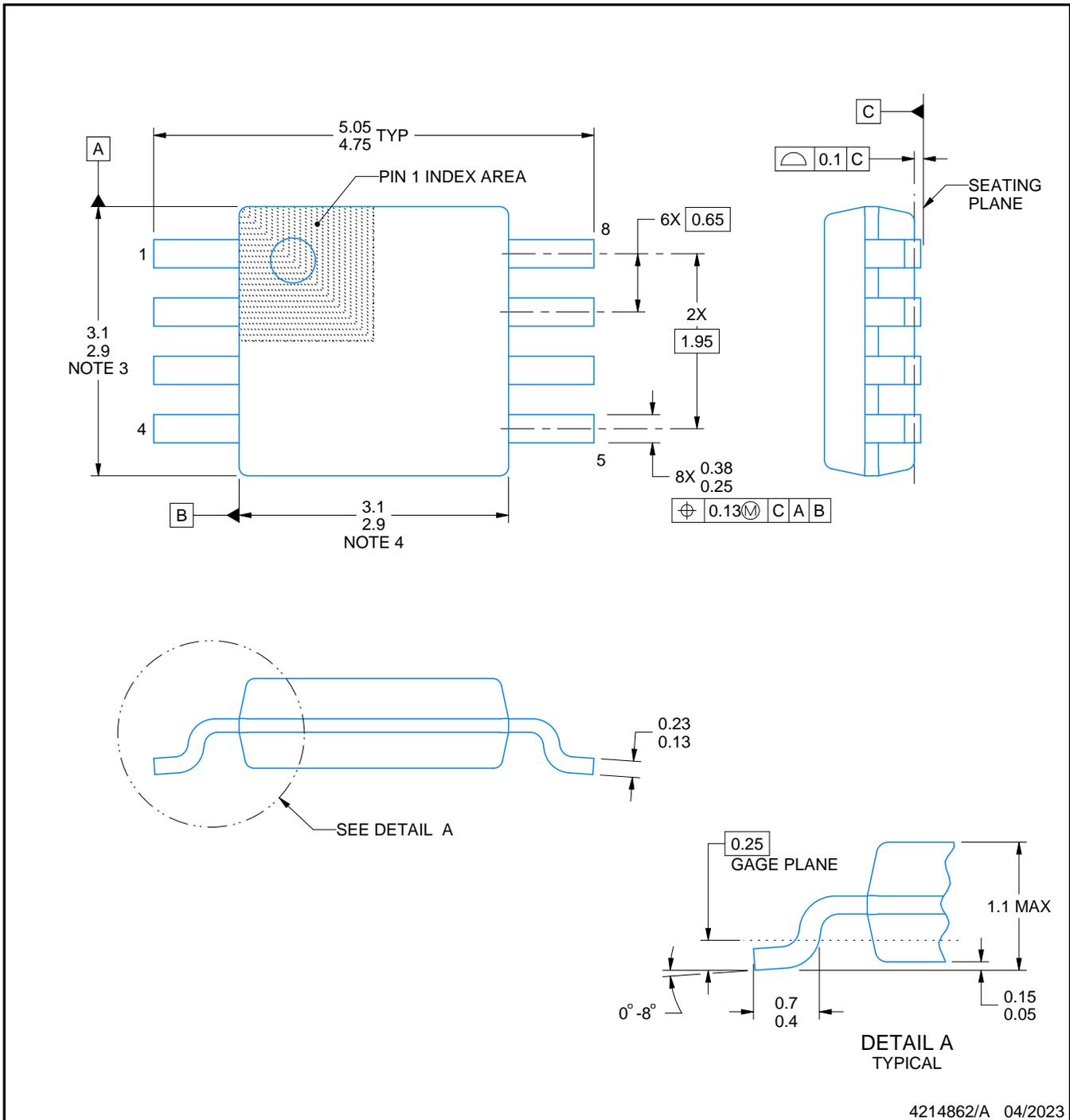
# DGK0008A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

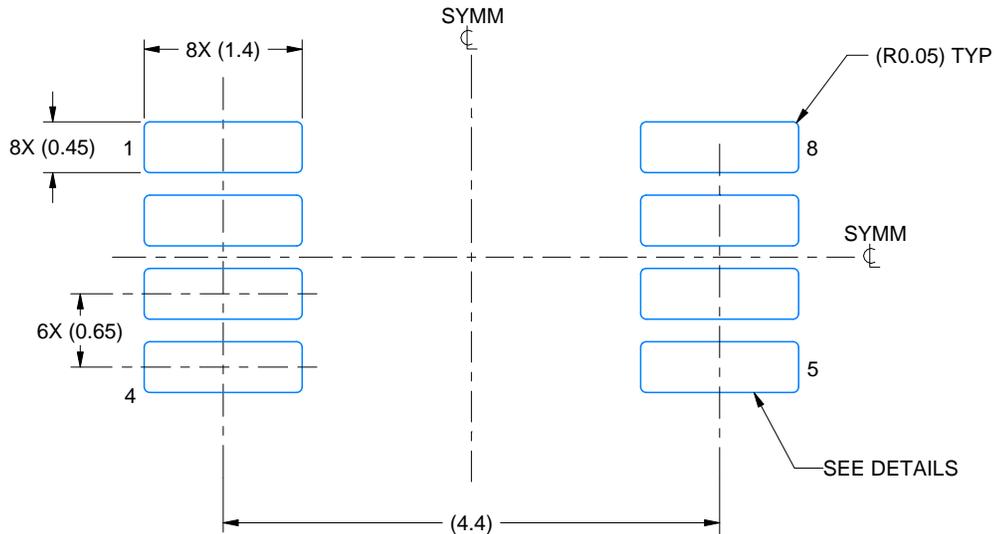
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

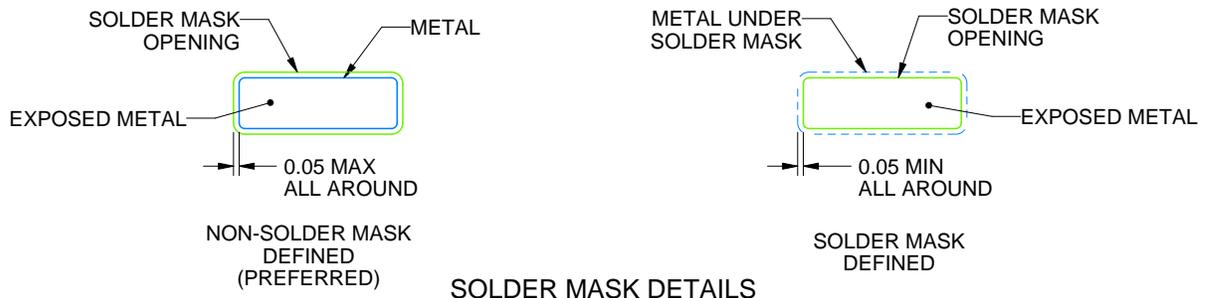
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

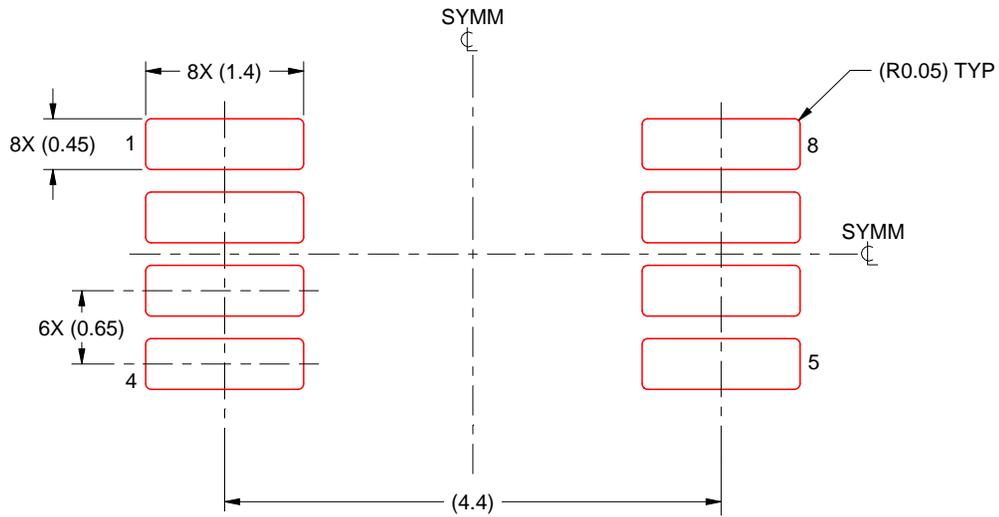
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated