

## TLC372 Dual Differential Comparators

### 1 Features

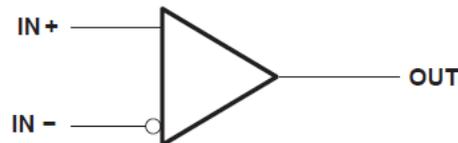
- Single or dual-supply operation
- Wide range of supply voltages: 3V to 16V
- Low supply current drain 150 $\mu$ A typical at 5V
- Fast response time: 200ns typical for TTL-Level input step
- Built-in ESD protection
- High input impedance: 10<sup>12</sup> $\Omega$  typical
- Extremely low input bias current: 5pA typical
- Ultra-stable low input offset voltage
- Common-mode input voltage range includes ground
- Output compatible with TTL, MOS, and CMOS
- Pin-compatible with LM393

### 2 Description

This device is fabricated using CMOS technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 3V to 16V. Each device features extremely high input impedance (typically greater than 10<sup>12</sup> $\Omega$ ), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 1000V ESD rating using human body model testing. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372C is characterized for operation from 0°C to 70°C. The TLC372I is characterized for operation from -40°C to 85°C. The TLC372M is characterized for operation over the full military temperature range of -55°C to 125°C. The TLC372Q is characterized for operation from -40°C to 125°C.



**Symbol (Each Comparator)**



## Table of Contents

<b>1 Features</b> .....	1	<b>8 Application and Implementation</b> .....	13
<b>2 Description</b> .....	1	8.1 Application Information.....	13
<b>3 Device Comparison Table</b> .....	3	8.2 Typical Applications.....	14
<b>4 Pin Configuration and Functions</b> .....	3	8.3 Power Supply Recommendations.....	15
<b>5 Specifications</b> .....	4	8.4 Layout.....	15
5.1 Absolute Maximum Ratings .....	4	<b>9 Device and Documentation Support</b> .....	17
5.2 Recommended Operating Conditions .....	4	9.1 Documentation Support.....	17
5.3 Electrical Characteristics.....	5	9.2 Receiving Notification of Documentation Updates...	17
5.4 Switching Characteristics .....	5	9.3 Support Resources.....	17
5.5 Electrical Characteristics.....	6	9.4 Trademarks.....	17
<b>6 Typical Characteristics</b> .....	7	9.5 Electrostatic Discharge Caution.....	17
<b>7 Detailed Description</b> .....	9	9.6 Glossary.....	17
7.1 Overview.....	9	<b>10 Revision History</b> .....	17
7.2 Functional Block Diagrams.....	9	<b>11 Mechanical, Packaging, and Orderable</b>	
7.3 Feature Description.....	9	<b>Information</b> .....	17
7.4 Device Functional Modes.....	9		

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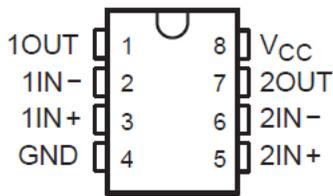
### 3 Device Comparison Table

#### Available Options <sup>(1)</sup>

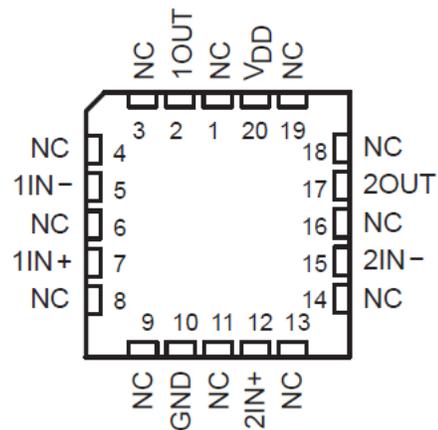
T <sub>A</sub>	V <sub>IO</sub> max at 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D) <sup>(2)</sup>	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	5mV	TLC372CD	—	—	TLC372CP	TLC372CPW	—
-40°C to 85°C	5mV	TLC372ID	—	—	TLC372IP	—	—
-55°C to 125°C	5mV	TLC372MD	TLC372MFK	TLC372MJG	TLC372MP	—	TLC372MU
-40°C to 125°C	5mV	TLC372QD	—	—	TLC372QP	—	—

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).  
 (2) The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC372CDR).

### 4 Pin Configuration and Functions

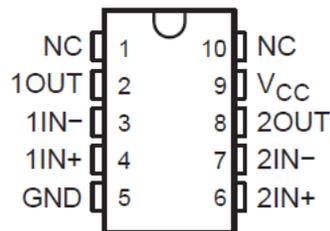


**Figure 4-1. TLC372C, TLC372I, TLC372M, TLC372QD, P, or PW Package  
TLC372M JG Package (Top View)**



A. NC- No internal connection.

**Figure 4-2. TLC372M FK Package (Top View)**



**Figure 4-3. TLC372M U Package (Top View)**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>DD</sub>	Supply voltage <sup>(2)</sup>		18	V	
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>		±18	V	
V <sub>I</sub>	Input voltage range	-0.3	V <sub>DD</sub>	V	
V <sub>O</sub>	Output voltage		18	V	
I <sub>I</sub>	Input current		±5	VmA	
I <sub>O</sub>	Output current		20	mA	
	Duration of output short circuit to ground <sup>(4)</sup>	Unlimited			
θ <sub>JA</sub>	Package thermal impedance <sup>(5) (6)</sup>	D package	97.1	°C/W	
		P package	84.6		
		PW package	149		
θ <sub>JC</sub>	Package thermal impedance <sup>(5) (6)</sup>	FK package	5.6	°C/W	
		JG package	14.5		
		U package	14.7		
T <sub>A</sub>	Operating free-air temperature range	TLC372C	0	70	°C
		TLC372I	-40	85	
		TLC372M	-55	125	
		TLC372Q	-40	125	
	Storage temperature range	-65	150	°C	
	Case temperature for 60 seconds	FK package	260	°C	
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	D package	260	°C	
		P package			
		PW package			
	Lead temperature 1.6mm (1/16 inch) from case for 60 seconds	JG package	300	°C	
		U package			

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential voltages are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V<sub>DD</sub> can cause excessive heating and eventual device destruction.
- (5) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JEDEC 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

### 5.2 Recommended Operating Conditions

		TLC372C		TLC372I		TLC372M		TLC372Q		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V <sub>DD</sub>	Supply voltage	3	16	3	16	4	16	4	16	V	
V <sub>IC</sub>	Common-mode input voltage	V <sub>DD</sub> = 5V	0	3.5	0	3.5	0	3.5	0	3.5	V
		V <sub>DD</sub> = 10V	0	8.5	0	8.5	0	8.5	0	8.5	
T <sub>A</sub>	Operating free-air temperature,	0	70	-40	85	-55	125	-40	125	°C	

### 5.3 Electrical Characteristics

at specified free-air temperature,  $V_{DD} = 5V$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$ <sup>(1)</sup>	TLC372C			TLC372I			TLC372M, TLC372Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_{IC} = V_{ICRmin}^{(2)}$		25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
$I_{IO}$	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
$I_{IB}$	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
$V_{ICR}$	Common-mode input voltage range			25°C	0 to $V_{DD} - 1$			0 to $V_{DD} - 1$			0 to $V_{DD} - 1$			V
				Full range	0 to $V_{DD} - 1.5$			0 to $V_{DD} - 1.5$			0 to $V_{DD} - 1.5$			
$I_{OH}$	High-level output current	$V_{ID} = 1V$	$V_{OH} = 5V$	25°C		0.1		0.1			0.1			nA
			$V_{OH} = 15V$	Full range			1		1			3		$\mu A$
$V_{OL}$	Low-level output voltage	$V_{ID} = -1V$	$I_{OL} = 4mA$	25°C		150	400		150	400		150	400	mV
				Full range			700		700		700			
$I_{OL}$	Low-level output current	$V_{ID} = -1V$	$V_{OL} = 1.5V$	25°C		6	16		6	16		6	16	mA
$I_{DD}$	Supply current (two comparators)	$V_{ID} = 1V$	No load	25°C		150	300		150	300		150	300	$\mu A$
				Full range			400		400		400			

- (1) All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC372C, -40°C to 85°C for TLC372I, and -55°C to 125°C for TLC372M and -40°C to 125°C for TLC372Q.
- (2) The offset voltage limits given are the maximum values required to drive the output above 4V or below 400mV with a 10kΩ resistor between the output and  $V_{DD}$ . They can be verified by applying the limit value to the input and checking for the appropriate output state.

### 5.4 Switching Characteristics

$V_{DD} = 5V$ ,  $T_A = 25°C$

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	$R_L$ connected to 5V through 5.1kΩ, $C_L = 15pF$ <sup>(1)</sup> <sup>(2)</sup>	100mV input step with 10mV overdrive		200		ns
		100mV overdrive		100		

- (1)  $C_L$  includes probe and jig capacitance.
- (2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

## 5.5 Electrical Characteristics

at specified free-air temperature,  $V_{DD} = 5V$ ,  $T_A = 25^\circ C$  (unless otherwise noted)

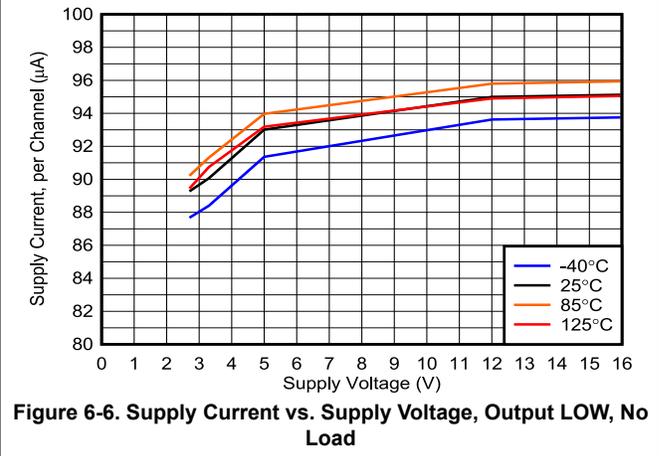
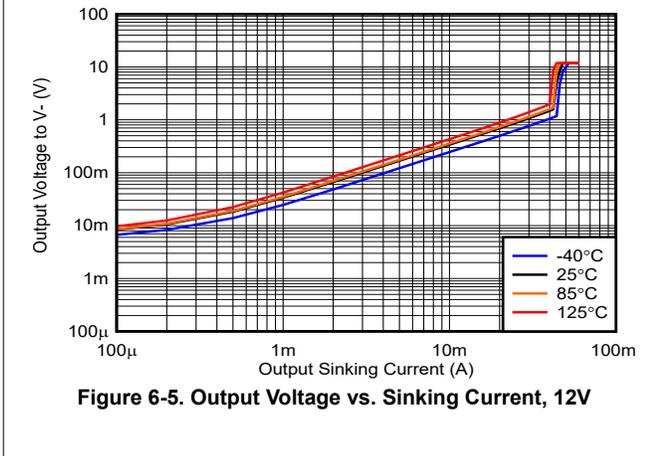
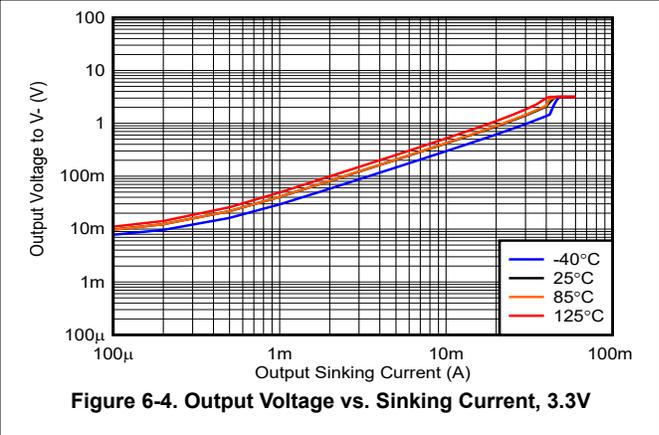
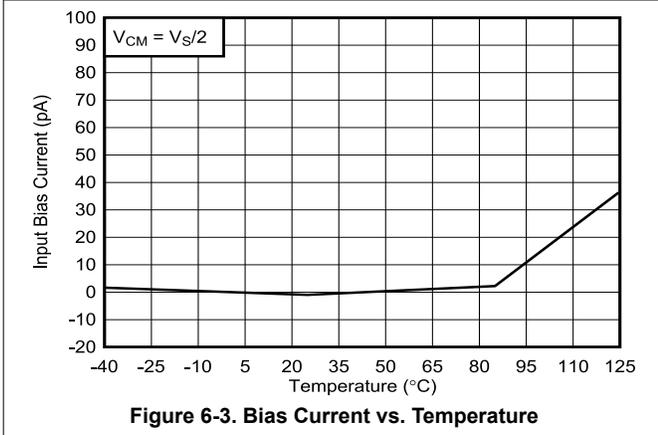
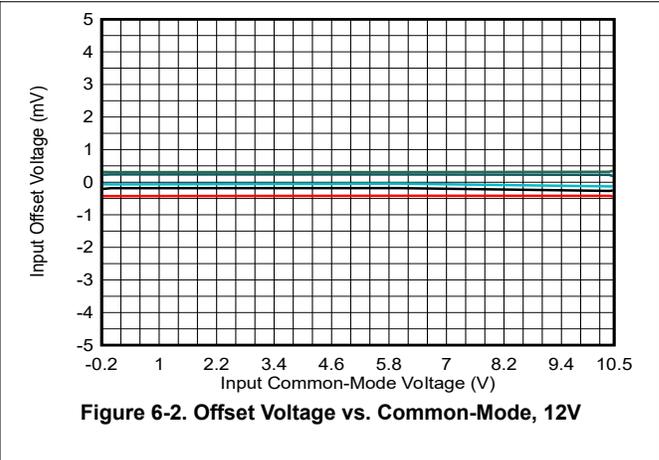
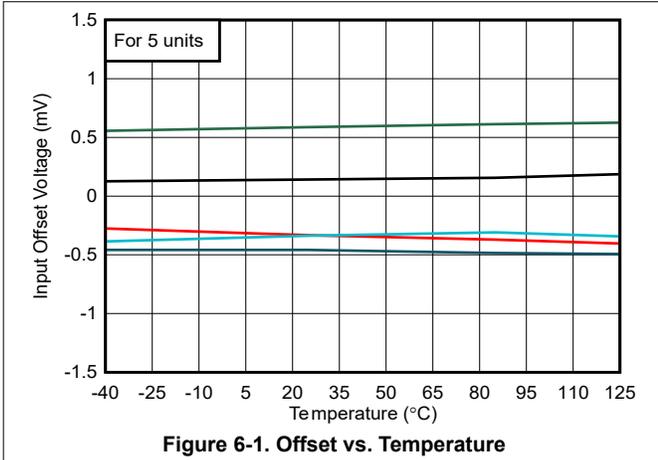
PARAMETER		TEST CONDITIONS <sup>(1)</sup>		TLC372Y			UNIT
				MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_{IC} = V_{ICRmin}^{(2)}$		1	5		mV
$I_{IO}$	Input offset current			1			pA
$I_{IB}$	Input bias current			5			pA
$V_{ICR}$	Common-mode input voltage range			0 to $V_{DD} - 1$			V
$I_{OH}$	High-level output current	$V_{ID} = 1V$	$V_{OH} = 5V$	0.1			nA
$V_{OL}$	Low-level output voltage	$V_{ID} = -1V$	$I_{OL} = 4mA$	150	400		mV
$I_{OL}$	Low-level output current	$V_{ID} = -1V$	$V_{OL} = 1.5V$	6	16		mA
$I_{DD}$	Supply current (two comparators)	$V_{ID} = 1V$	No load	150	300		$\mu A$

(1) All characteristics are measured with zero common-mode input voltage unless otherwise noted.

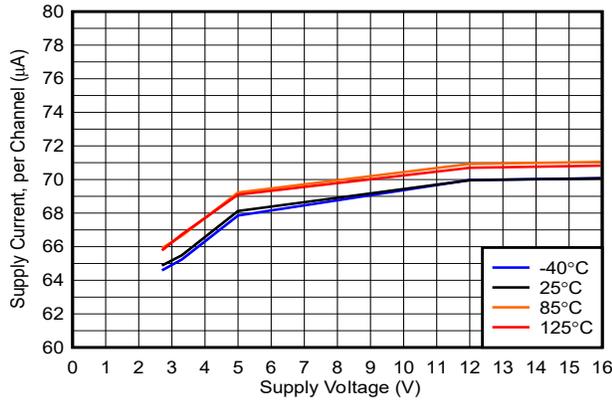
(2) The offset voltage limits given are the maximum values required to drive the output above 4V or below 400mV with a 10k $\Omega$  resistor between the output and  $V_{DD}$ . They can be verified by applying the limit value to the input and checking for the appropriate output state.

## 6 Typical Characteristics

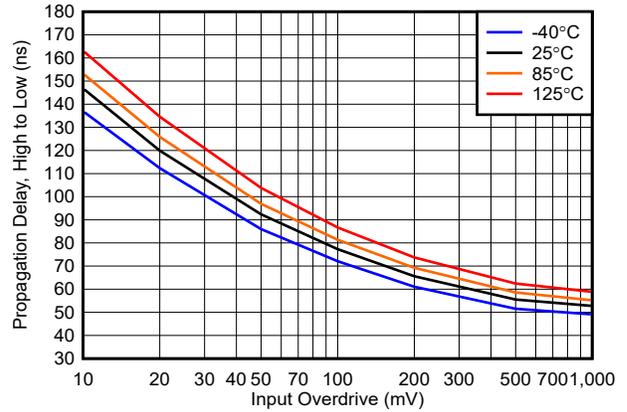
At  $T_A = 25^\circ\text{C}$ ,  $V_S = 12\text{V}$ ,  $V_{CM} = V_S/2\text{V}$ ,  $C_L = 15\text{pF}$ , Input Overdrive = Input Underdrive =  $100\text{mV}$ ,  $R_{PU} = 10\text{k}\Omega$ , unless otherwise noted.



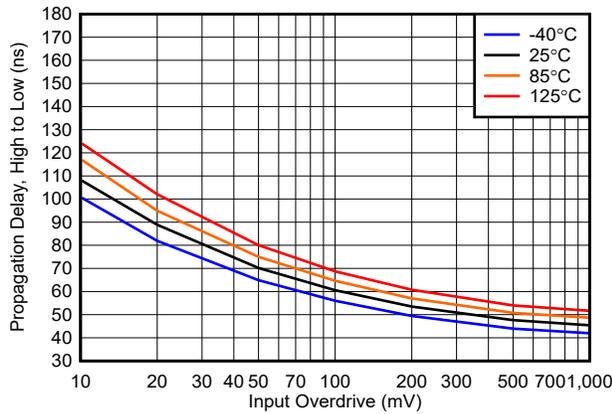
## 6 Typical Characteristics (continued)



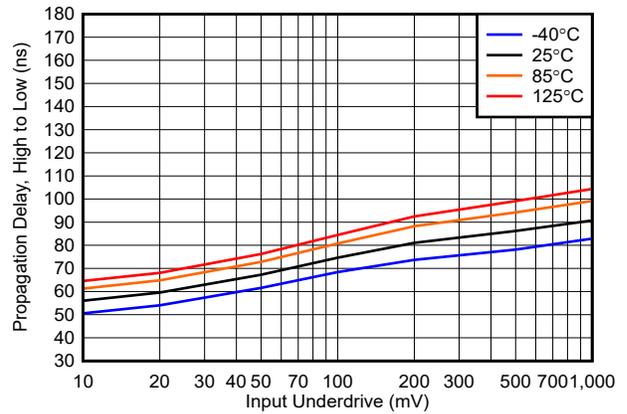
**Figure 6-7. Supply Current vs. Supply Voltage, Output HIGH, No Load**



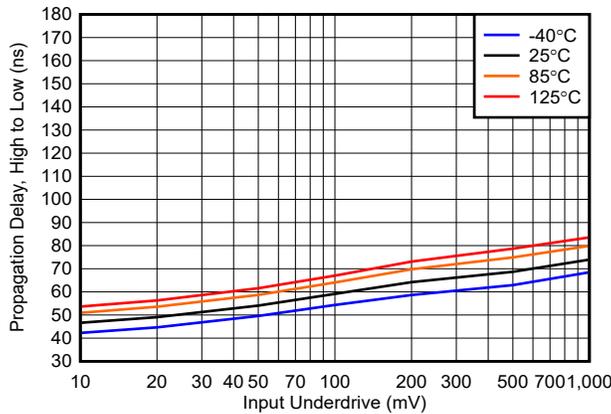
**Figure 6-8. Propagation Delay, (High to Low) vs. Input Overdrive, 3.3V**



**Figure 6-9. Propagation Delay, (High to Low) vs. Input Overdrive, 12V**



**Figure 6-10. Propagation Delay, (High to Low) vs. Input Underdrive, 3.3V**



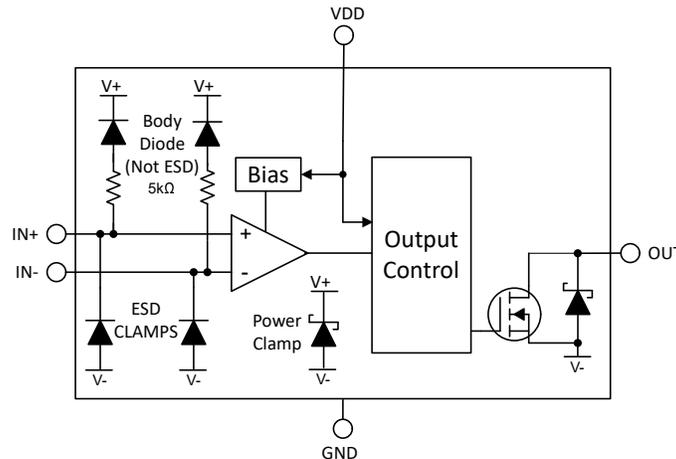
**Figure 6-11. Propagation Delay, (High to Low) vs. Input Underdrive, 12V**

## 7 Detailed Description

### 7.1 Overview

The TLC372 device is a micro-power comparator with open-drain output. Operating down to 3V while only consuming only 75µA per channel, the TLC372 is excellent for power conscious applications.

### 7.2 Functional Block Diagrams



**Figure 7-1. Block Diagram**

### 7.3 Feature Description

The TLC372 comparator consists of a CMOS differential pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The output consists of an open-drain output stage capable of sinking current with a negative differential input voltage.

### 7.4 Device Functional Modes

#### 7.4.1 Input

The TLC3x2 input voltage range extends from  $V_-$  to 1.5V below  $V_+$  over the full temperature range. The differential input voltage ( $V_{ID}$ ) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input voltages stay within the specified range.

#### 7.4.2 ESD Protection

The TLC3x2 input and output ESD protection contains a conventional diode-type "upper" ESD clamp between the I/O pins and  $V_+$ , and a "lower" ESD clamp between the I/O pins and  $V_-$ . The inputs or output must not exceed the supply rails by more than 300mV. TI does not recommend applying signals to the inputs with no supply voltage.

When the inputs are connected to a low impedance source, such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10mA or less, though TI recommends limiting the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

#### 7.4.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency chatter as the device triggers on its own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage.

### 7.4.4 Open-Drain Output

The TLC3x2 features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 16V, independent of the comparator supply voltage (VDD). The open-drain output allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower value pull-up resistor values can help increase the rising edge rise-time, but at the expense of increasing VOL and higher power dissipation. The rise-time is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) creates an exponential rising edge due to the output RC time constant and increase the rise-time.

Directly shorting the output to VDD can result in thermal runaway and eventual device destruction at high (>12V) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused open drain outputs can be left floating, or can be tied to the GND pin if floating pins are not desired.

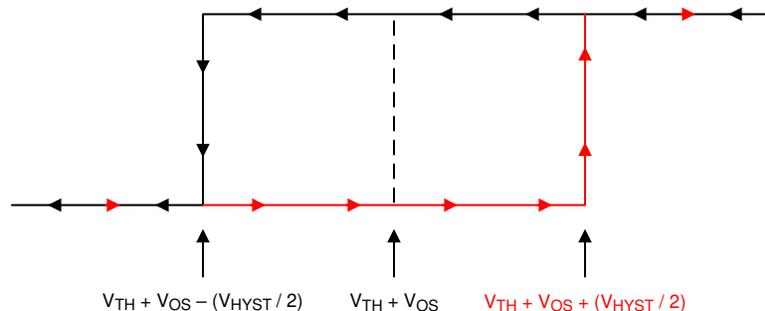
### 7.4.5 Hysteresis

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This typically occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in [Figure 7-2](#). This curve is a function of three components:  $V_{TH}$ ,  $V_{OS}$ , and  $V_{HYST}$ :

- $V_{TH}$  is the actual set voltage or threshold trip voltage.
- $V_{OS}$  is the internal offset voltage between  $V_{IN+}$  and  $V_{IN-}$ . This voltage is added to  $V_{TH}$  to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$  is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

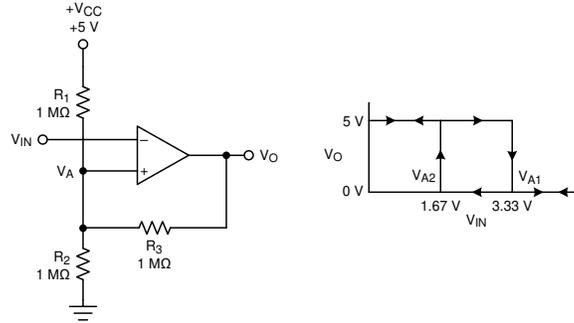


**Figure 7-2. Hysteresis Transfer Curve**

For more information, please see Application Note SBOA219 "[Comparator with and without hysteresis circuit](#)".

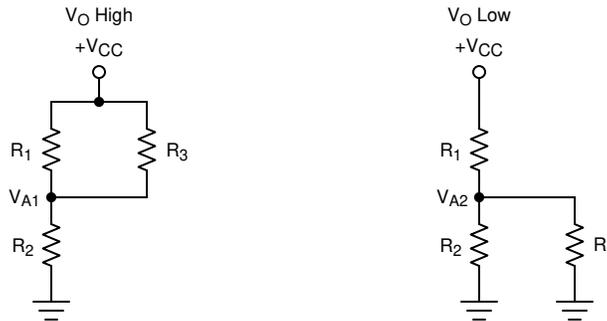
#### 7.4.5.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage ( $V_{CC}$ ), as shown below.



**Figure 7-3. Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown below.



**Figure 7-4. Inverting Configuration Resistor Equivalent Networks**

When  $V_{IN}$  is less than  $V_A$ , the output voltage is high (for simplicity, assume  $V_O$  switches as high as  $V_{CC}$ ). The three network resistors can be represented as  $R1 \parallel R3$  in series with  $R2$ , as shown above on the left.

The equation below defines the high-to-low trip voltage ( $V_{A1}$ ).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When  $V_{IN}$  is greater than  $V_A$ , the output voltage is low. In this case, the three network resistors can be presented as  $R2 \parallel R3$  in series with  $R1$ , as shown above on the right.

Use the equation below to define the low to high trip voltage ( $V_{A2}$ ).

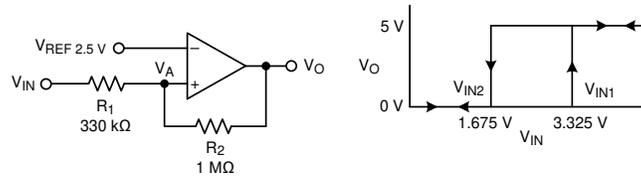
$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

The equation below defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

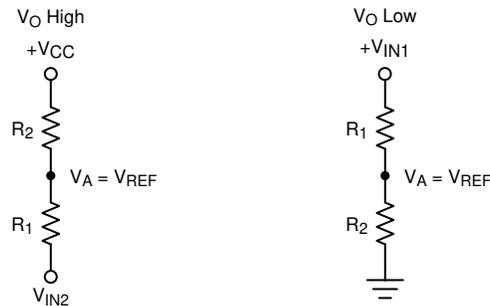
#### 7.4.5.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference ( $V_{REF}$ ) at the inverting input, as shown in [Figure 7-5](#).



**Figure 7-5. Non-Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in [Figure 7-6](#).



**Figure 7-6. Non-Inverting Configuration Resistor Networks**

When  $V_{IN}$  is less than  $V_{REF}$ , the output is low. For the output to switch from low to high,  $V_{IN}$  must rise above the  $V_{IN1}$  threshold. Use [Equation 4](#) to calculate  $V_{IN1}$ .

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When  $V_{IN}$  is greater than  $V_{REF}$ , the output is high. For the comparator to switch back to a low state,  $V_{IN}$  must drop below  $V_{IN2}$ . Use [Equation 5](#) to calculate  $V_{IN2}$ .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between  $V_{IN1}$  and  $V_{IN2}$ , as shown in [Equation 6](#).

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

For more information, please see Application Notes SNOA997 "[Inverting comparator with hysteresis circuit](#)" and SBOA313 "[Non-Inverting Comparator With Hysteresis Circuit](#)".

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Basic Comparator Definitions

##### 8.1.1.1 Operation

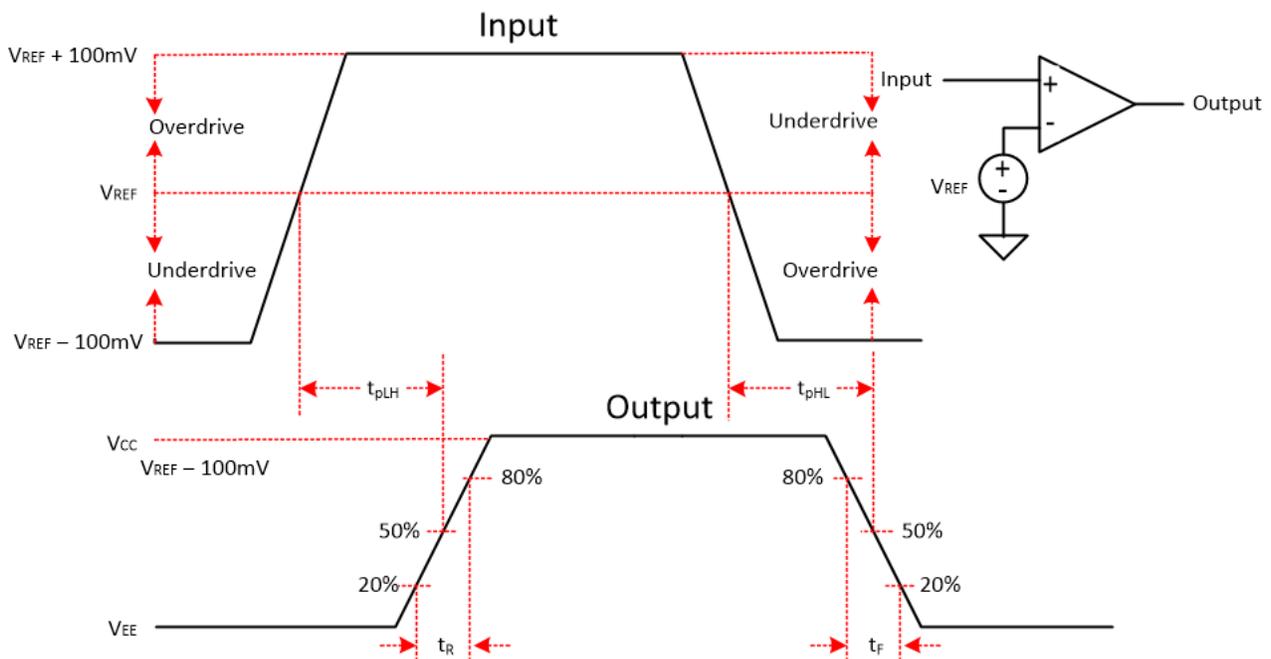
The basic comparator compares the input voltage ( $V_{IN}$ ) on one input to a reference voltage ( $V_{REF}$ ) on the other input. In the [Figure 8-1](#) example below, if  $V_{IN}$  is less than  $V_{REF}$ , the output voltage ( $V_O$ ) is logic low ( $V_{OL}$ ). If  $V_{IN}$  is greater than  $V_{REF}$ , the output voltage ( $V_O$ ) is in a high-Z state. [Table 8-1](#) summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

**Table 8-1. Output Conditions**

Inputs Condition	Output
$IN+ > IN-$	HIGH ( $V_{OH}$ )
$IN+ = IN-$	Indeterminate (chatters - see <a href="#">Hysteresis</a> )
$IN+ < IN-$	LOW ( $V_{OL}$ )

##### 8.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as  $t_{pLH}$  and  $t_{pHL}$  in [Figure 8-1](#) and is measured from the mid-point of the input to the midpoint of the output. Likewise, propagation varies with what is called overdrive ( $V_{OD}$ ) and underdrive ( $V_{UD}$ ) voltage levels (see section below).



**Figure 8-1. Comparator Timing Diagram**

### 8.1.1.3 Overdrive and Underdrive Voltage

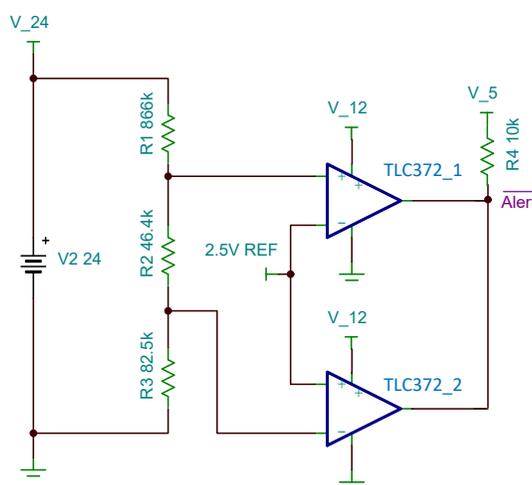
The overdrive voltage,  $V_{OD}$ , is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the [Figure 8-1](#) example. Similarly, underdrive voltage,  $V_{UD}$ , is how far below REF the input starts. The overdrive and underdrive voltages influence the propagation delay ( $t_p$ ). See curves in the Typical Characteristics section for more details. The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, apply the highest amount of overdrive possible. Contrary to overdrive voltage, larger underdrive voltage causes propagation delay to increase.

The risetime ( $t_r$ ) and falltime ( $t_f$ ) is the time from the 20% and 80% points of the output waveform.

## 8.2 Typical Applications

### 8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. The figure below shows a simple window comparator circuit monitoring a 24V PLC power supply.



**Figure 8-2. Window Comparator**

#### 8.2.1.1 Design Requirements

For this design, follow these design requirements:

- UV\_Alert (logic low output) when the 24V supply is less than 19.2V
- OV\_Alert (logic low output) when the 24V supply is greater than 30V
- Current dissipated in the resistor string is 30uA
- Comparator operates from the 5V supply
- 2.5V external reference is utilized

#### 8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in the circuit above where the 2.5V REF from the TLC372 is used as the reference voltage and the resistor string of R1, R2, and R3 define the upper and lower threshold voltages for the 24V PLC power supply. When the comparator detects that the 24V supply has exceeded the maximum voltage of 30V or has drooped below the minimum voltage of 19.2V, OV\_Alert and UV\_Alert nets are pulled to a logic LOW state.

The first step is to determine the sum total resistance of the resistor string (R1, R2, R3) using the dissipation limit of 30uA. With a maximum operating voltage of 30V, the resistor string draws 30uA if the total resistance of R1+R2+R3 is 1Mohm.

The second step is to set the value of R3 such that the lower comparator changes output state from HIGH to LOW when the 24V supply reaches 30V. This is achieved when the voltage at the junction of R2 and R3 is equal

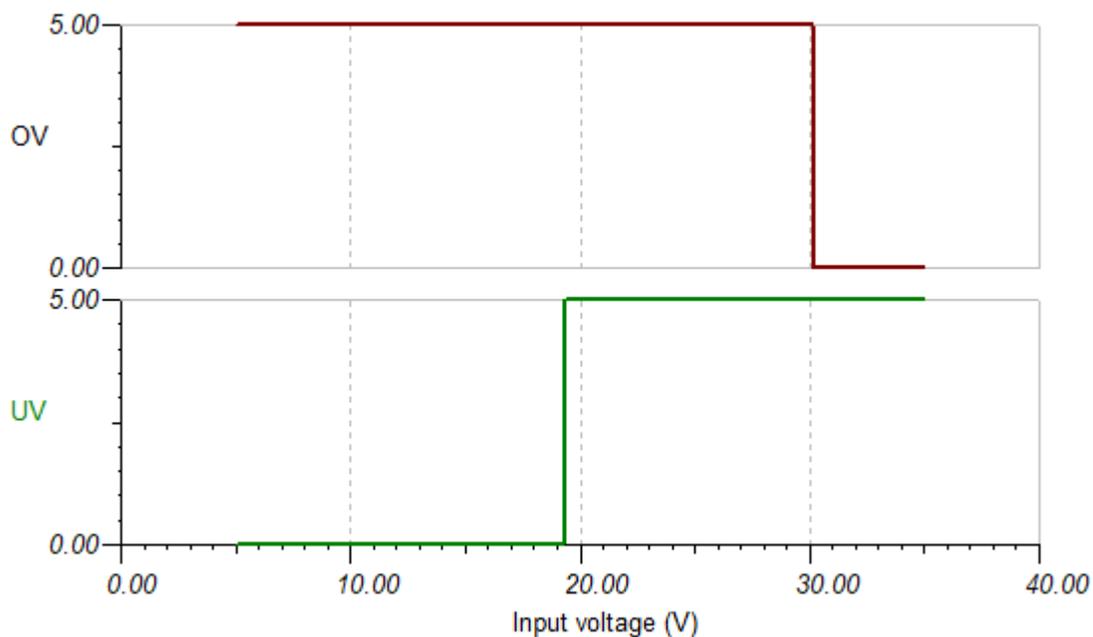
to the reference voltage of 2.5V. Since 30uA is passing through the resistor string at 30V, R3 can be calculated from  $2.5V / 30\mu A$  which is approximately 83.3kohms.

The third step is to set the value of R2 such that the upper comparator changes output state from HIGH to LOW when the 24V supply reaches 19.2V. This is achieved when the voltage at the junction of R1 and R2 is equal to the reference voltage of 2.5V. Since 19.2uA passes through the resistor string at 19.2V, R2 can be calculated from  $(2.5V / 19.2\mu A) - R3$  which is approximately 46.9kohms.

Lastly, the value of R1 is calculated from 1Mohm - (R2 + R3) which is approximately 870kohms. Please note that standard 1% resistor values were selected for the circuit

The respective comparator outputs (OV\_Alert and UV\_Alert) are LOW when the 24V PLC power supply is less than 19.2V or greater than 30V. Likewise, the respective comparator outputs are HIGH when the 24V supply is within the range of 19.2V to 30V (within the "window"), as shown below.

### 8.2.1.3 Application Curve



**Figure 8-3. Window Comparator Results**

## 8.3 Power Supply Recommendations

Due to the fast output edge rates, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1μF ceramic bypass capacitor directly between V+ pin and ground pins. Narrow, peak currents are drawn during the output transition time. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies (V+ and V-), or "single" supplies (V+ and GND), with GND applied to the V- pin. Input signals must stay within the specified input range (between V+ and V-) for either type. Note that with a "split" supply the output swings "low" ( $V_{OL}$ ) to V- potential and not GND.

## 8.4 Layout

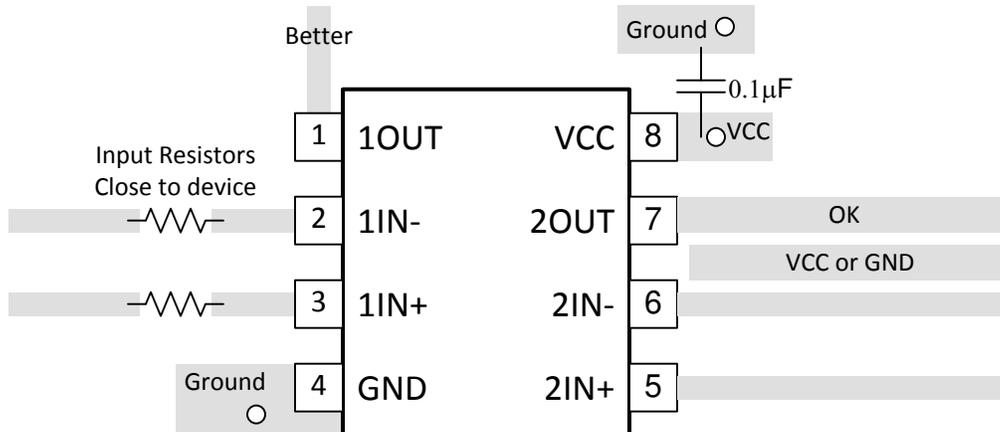
### 8.4.1 Layout Guidelines

For accurate comparator applications, a clean, stable power supply is important to minimize output glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The

bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V+ and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V+ or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value ( $\leq 100$  ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

**8.4.2 Layout Example**



**Figure 8-4. Dual Layout Example**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision E (July 2008) to Revision F (June 2025)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updates throughout data sheet to reflect performance of new die.....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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