

SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

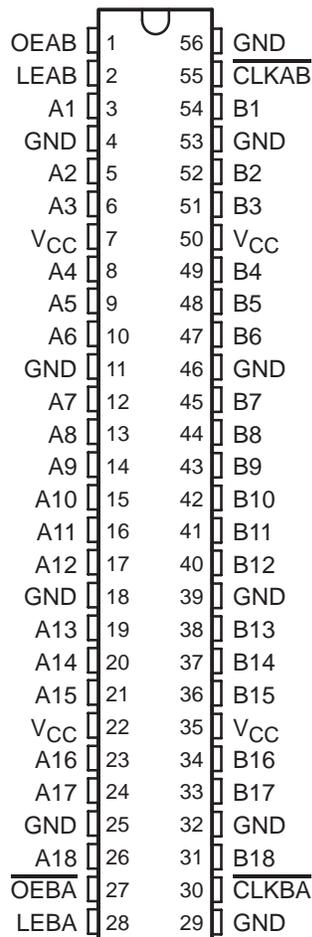
SCBS701F – JULY 1997 – REVISED SEPTEMBER 2003

- Members of the Texas Instruments Widebus™ Family
- UBT™ Transceivers Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

The 'LVTH16500 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTH16500 . . . WD PACKAGE
SN74LVTH16500 . . . DGG OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVTH16500DL	LVTH16500
		Tape and reel	SN74LVTH16500DLR	
	TSSOP – DGG	Tape and reel	SN74LVTH16500DGGR	LVTH16500
	VFBGA – GQL	Tape and reel	SN74LVTH16500GQLR	LL500
VFBGA – ZQL (Pb-free)	SN74LVTH16500ZQLR			
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16500WD	SNJ54LVTH16500WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus and UBT are trademarks of Texas Instruments.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

SN54LVTH16500, SN74LVTH16500

3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS701F – JULY 1997 – REVISED SEPTEMBER 2003

description/ordering information (continued)

Data flow in each direction is controlled by output-enable (\overline{OEBA} and \overline{OEAB}), latch-enable (LEAB and LEBA), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

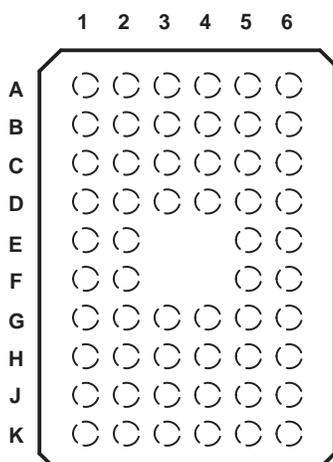
Data flow for B to A is similar to that of A to B, but uses $\overline{OEB\bar{A}}$, LEBA, and \overline{CLKBA} . The output enables are complementary (OEAB is active high and \overline{OEBA} is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

GQL OR ZQL PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	A1	LEAB	OEAB	GND	\overline{CLKAB}	B1
B	A3	A2	GND	GND	B2	B3
C	A5	A4	V_{CC}	V_{CC}	B4	B5
D	A7	A6	GND	GND	B6	B7
E	A9	A8			B8	B9
F	A10	A11			B11	B10
G	A12	A13	GND	GND	B13	B12
H	A14	A15	V_{CC}	V_{CC}	B15	B14
J	A16	A17	GND	GND	B17	B16
K	A18	\overline{OEBA}	LEBA	GND	\overline{CLKBA}	B18

SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS701F – JULY 1997 – REVISED SEPTEMBER 2003

FUNCTION TABLE†

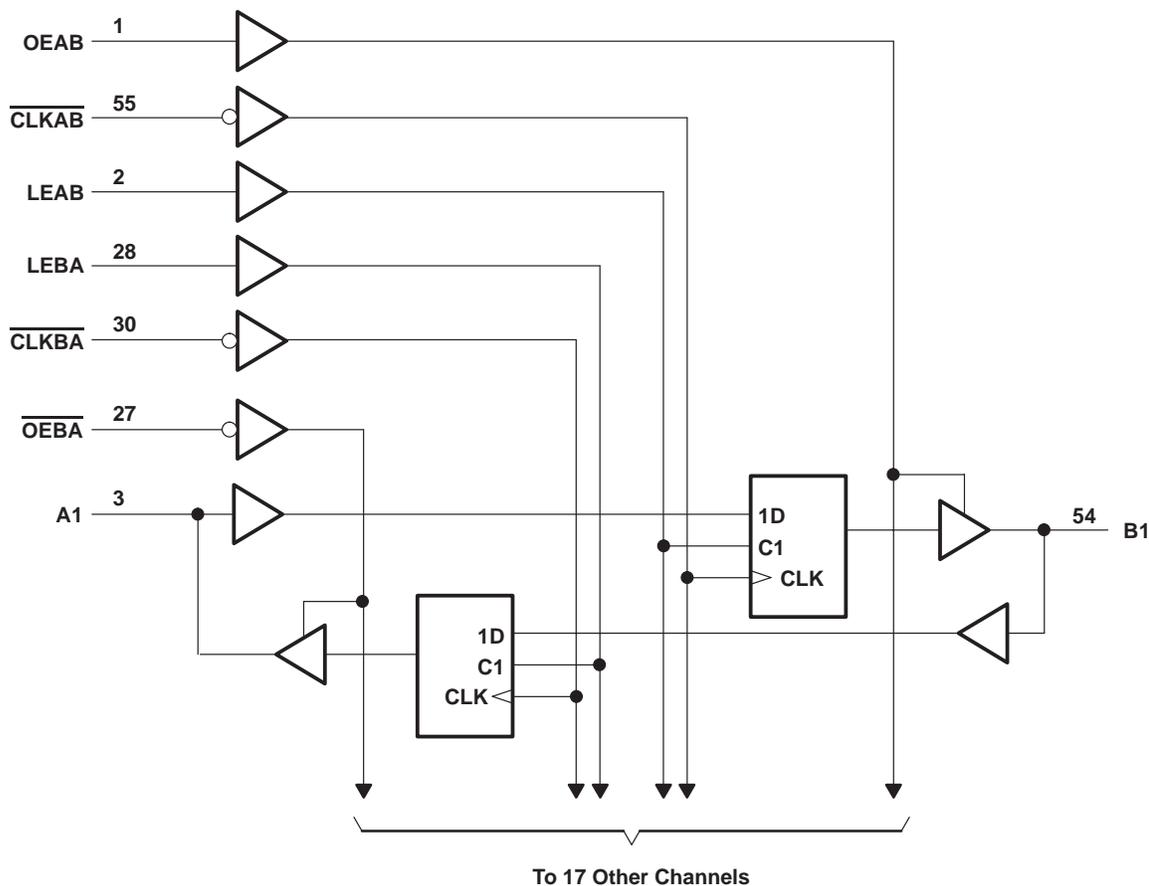
INPUTS				OUTPUT B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ ‡
H	L	L	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.

SN54LVTH16500, SN74LVTH16500

3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS701F – JULY 1997 – REVISED SEPTEMBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16500	96 mA
SN74LVTH16500	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16500	48 mA
SN74LVTH16500	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DL package	56°C/W
GQL/ZQL package	42°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

	SN54LVTH16500		SN74LVTH16500		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage		5.5		5.5	V
I_{OH} High-level output current		-24		-32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate	200		200		μ s/V
T_A Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS701F – JULY 1997 – REVISED SEPTEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH16500		SN74LVTH16500		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2	V	
V_{OH}	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$		V	
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$		2			2		
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2	V	
		$I_{OL} = 24\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4		0.4		
		$I_{OL} = 32\text{ mA}$		0.5		0.5		
		$I_{OL} = 48\text{ mA}$		0.55				
		$I_{OL} = 64\text{ mA}$				0.55		
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1		± 1	μA	
		$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$		10		10		
	A or B ports‡	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$		20			20
			$V_I = V_{CC}$		1			1
		$V_I = 0$		-5		-5		
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$					± 100	μA	
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	75		75	μA	
			$V_I = 2\text{ V}$	-75		-75		
		$V_{CC} = 3.6\text{ V}\S$, $V_I = 0\text{ to }3.6\text{ V}$				± 500		
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE}/\overline{OE} = \text{don't care}$			$\pm 100^*$		± 100	μA	
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE}/\overline{OE} = \text{don't care}$			$\pm 100^*$		± 100	μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19		0.19	mA	
		Outputs low		5		5		
		Outputs disabled		0.19		0.19		
$\Delta I_{CC}\P$	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2		0.2	mA	
C_i	$V_I = 3\text{ V or }0$			4		4	pF	
C_{iO}	$V_O = 3\text{ V or }0$			10		10	pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}\text{ or GND}$.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LVTH16500, SN74LVTH16500

3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS701F – JULY 1997 – REVISED SEPTEMBER 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH16500				SN74LVTH16500				UNIT	
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency	150		150		150		150		MHz	
t_w	Pulse duration	LE high		3.3		3.3		3.3		ns	
		$\overline{\text{CLK}}$ high or low		3.3		3.3		3.3			
t_{su}	Setup time	A before $\overline{\text{CLKAB}}\downarrow$		3.1		3.1		2.9		ns	
		B before $\overline{\text{CLKBA}}\downarrow$		3.1		3.1		2.9			
		A or B before LE \downarrow	$\overline{\text{CLK}}$ high		1.5		0.6		1.4		
			$\overline{\text{CLK}}$ low		3.1		2.5		2.9		
t_h	Hold time	A or B after $\overline{\text{CLK}}\downarrow$		0.4		0.4		0.4		ns	
		A or B after LE \downarrow		1.7		1.7		1.6			

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

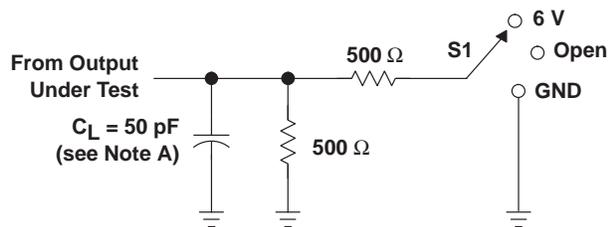
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16500				SN74LVTH16500				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
f_{max}			150		150		150			150	MHz
t_{PLH}	B or A	A or B	1.2 3.9		4.1		1.3 2.8 3.7			4	ns
t_{PHL}			1.2 3.9		4.1		1.3 2.6 3.7			4	
t_{PLH}	LEBA or LEAB	A or B	1.4 5.5		5.9		1.5 3.8 5.1			5.7	ns
t_{PHL}			1.4 5.5		5.9		1.5 3.8 5.1			5.7	
t_{PLH}	$\overline{\text{CLKBA}}$ or $\overline{\text{CLKAB}}$	A or B	1.2 5.3		6.1		1.3 3.6 5			5.9	ns
t_{PHL}			1.2 5.3		6.1		1.3 3.5 5			5.9	
t_{PZH}	$\overline{\text{OEBA}}$ or OEAB	A or B	1.2 5.1		5.8		1.3 3.6 4.8			5.5	ns
t_{PZL}			1.2 5.1		5.8		1.3 3.6 4.8			5.5	
t_{PHZ}	$\overline{\text{OEBA}}$ or OEAB	A or B	1.6 6.1		6.6		1.7 4.5 5.8			6.3	ns
t_{PLZ}			1.6 6.1		6.6		1.7 4.1 5.8			6.3	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

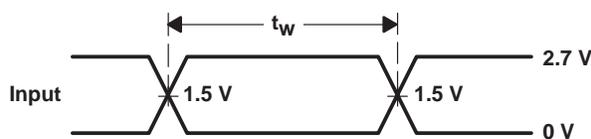


PARAMETER MEASUREMENT INFORMATION

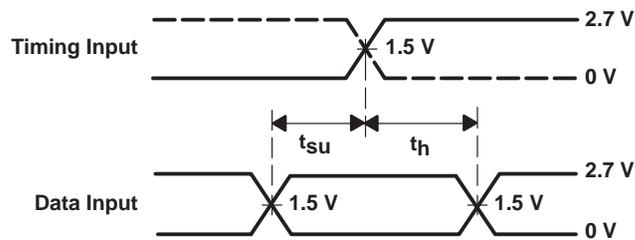


LOAD CIRCUIT

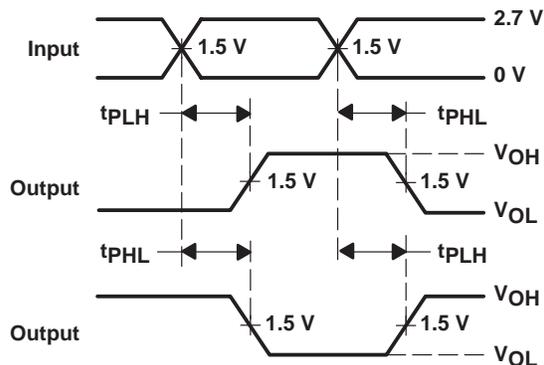
TEST	S1
t_{PHL}/t_{PLH}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



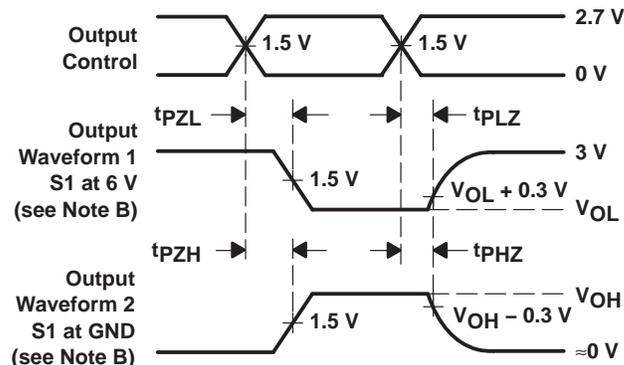
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVTH16500DGGRG4	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500
74LVTH16500DGGRG4.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500
SN74LVTH16500DGGR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500
SN74LVTH16500DGGR.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500
SN74LVTH16500DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500
SN74LVTH16500DL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

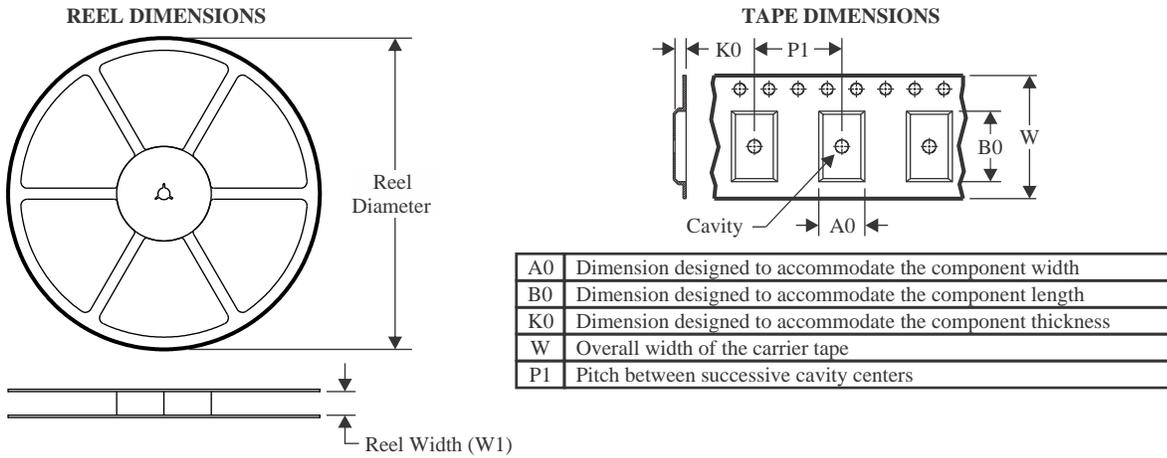
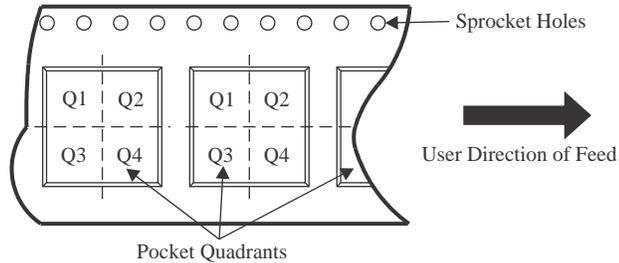
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVTH16500DGGRG4	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74LVTH16500DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVTH16500DGGRG4	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74LVTH16500DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0

TUBE

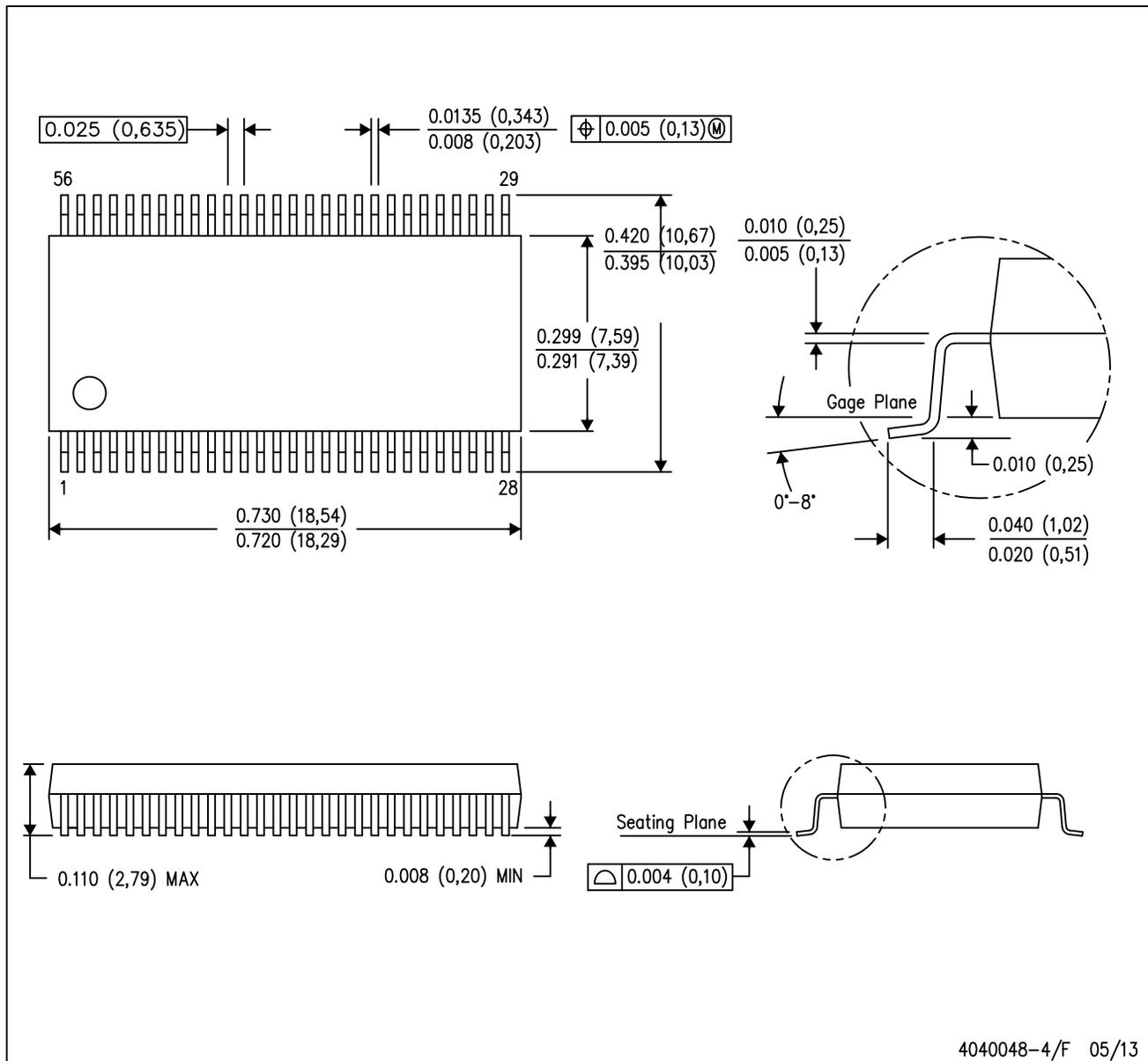

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVTH16500DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74LVTH16500DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

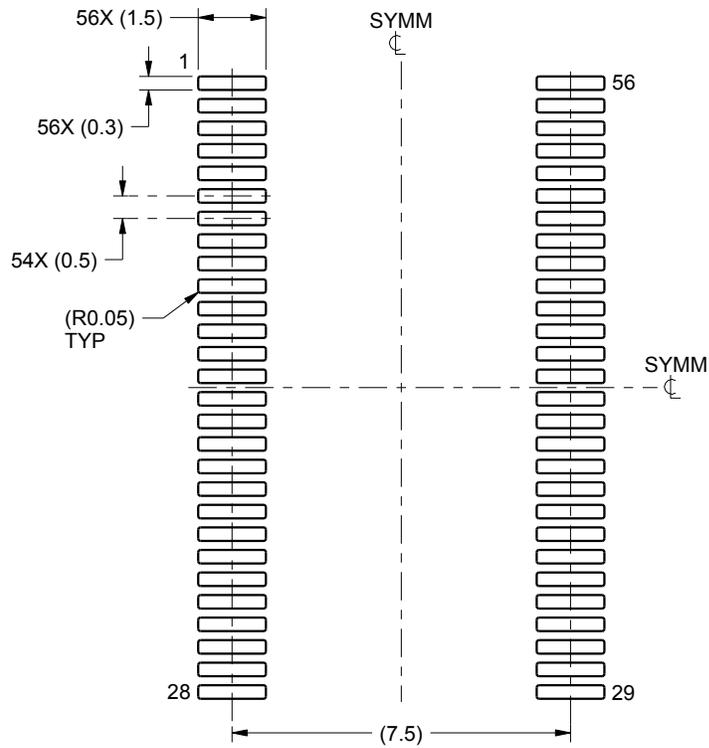
PowerPAD is a trademark of Texas Instruments.

EXAMPLE BOARD LAYOUT

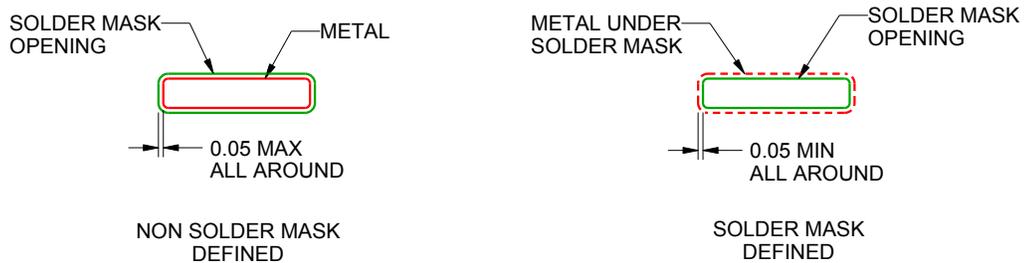
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

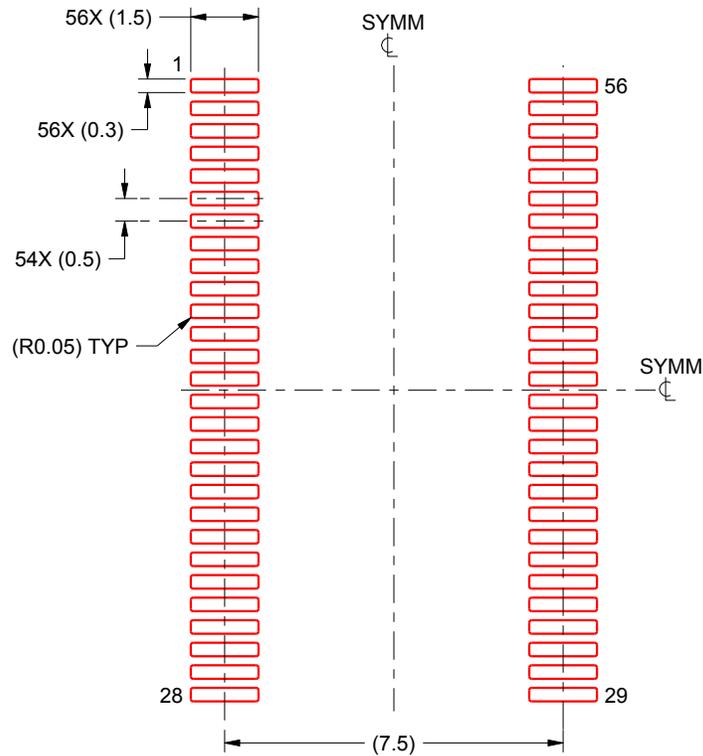
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated