

- Member of the Texas Instruments Widebus™ Family
- DOC™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

description

A Dynamic Output Control (DOC™) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to TI application reports *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

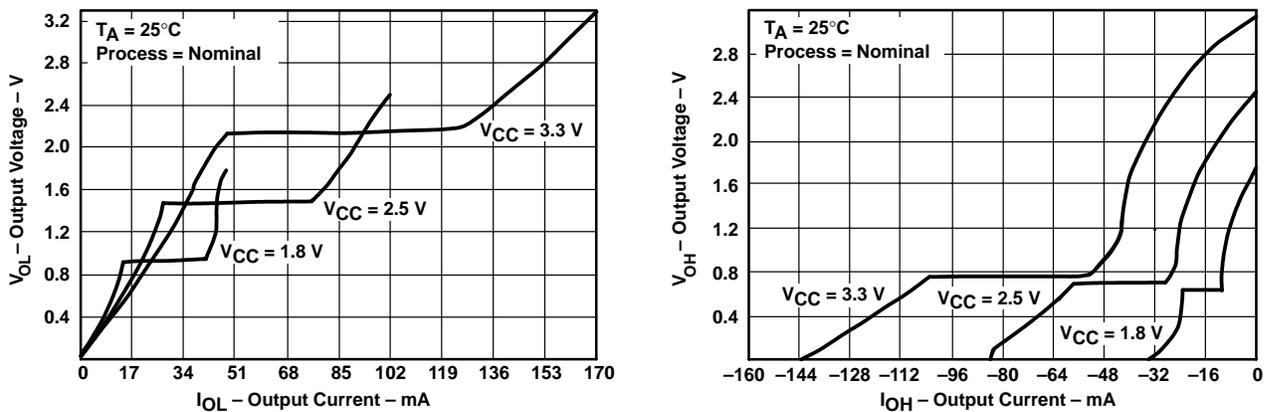


Figure 1. Output Voltage vs Output Current

This 18-bit universal bus driver is operational at 1.2-V to 3.6-V V_{CC} , but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



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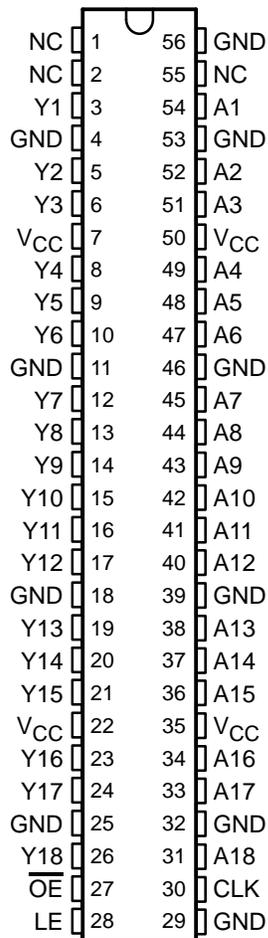
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SN74AVC16835
18-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

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terminal assignments

DGG OR DGV PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AVC16835DGGR	AVC16835
	TVSOP – DGV	Tape and reel	SN74AVC16835DGVR	CVA835

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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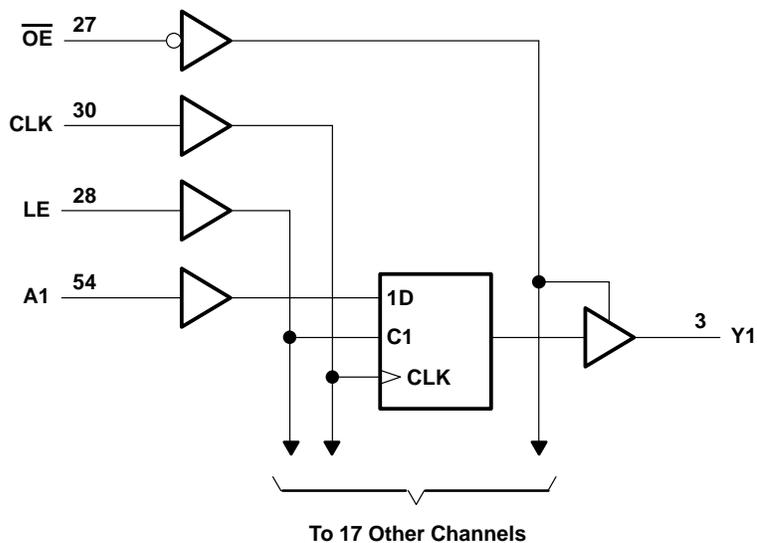
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FUNCTION TABLE
(each universal bus driver)

INPUTS				OUTPUT
\overline{OE}	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	Y_0^\dagger

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes low

logic diagram (positive logic)



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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.4	3.6	V
		Data retention only	1.2		
V _{IH}	High-level input voltage	V _{CC} = 1.2 V	V _{CC}		V
		V _{CC} = 1.4 V to 1.6 V	0.65 × V _{CC}		
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.2 V	GND		V
		V _{CC} = 1.4 V to 1.6 V	0.35 × V _{CC}		
		V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.8		
V _I	Input voltage	0	3.6	V	
V _O	Output voltage	Active state	0	V _{CC}	V
		3-state	0	3.6	
I _{OHS}	Static high-level output current†	V _{CC} = 1.4 V to 1.6 V	–2		mA
		V _{CC} = 1.65 V to 1.95 V	–4		
		V _{CC} = 2.3 V to 2.7 V	–8		
		V _{CC} = 3 V to 3.6 V	–12		
I _{OLS}	Static low-level output current†	V _{CC} = 1.4 V to 1.6 V	2		mA
		V _{CC} = 1.65 V to 1.95 V	4		
		V _{CC} = 2.3 V to 2.7 V	8		
		V _{CC} = 3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.4 V to 3.6 V		5	ns/V
T _A	Operating free-air temperature	–40	85	°C	

† Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of ±24 mA at 2.5-V V_{CC}. See Figure 1 for V_{OL} vs I_{OL} and V_{OH} vs I_{OH} characteristics. Refer to TI application reports *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}		I _{OHS} = -100 μA,	1.4 V to 3.6 V	V _{CC} -0.2			V
		I _{OHS} = -2 mA, V _{IH} = 0.91 V	1.4 V	1.05			
		I _{OHS} = -4 mA, V _{IH} = 1.07 V	1.65 V	1.2			
		I _{OHS} = -8 mA, V _{IH} = 1.7 V	2.3 V	1.75			
		I _{OHS} = -12 mA, V _{IH} = 2 V	3 V	2.3			
V _{OL}		I _{OLS} = 100 μA	1.4 V to 3.6 V			0.2	V
		I _{OLS} = 2 mA, V _{IL} = 0.49 V	1.4 V			0.4	
		I _{OLS} = 4 mA, V _{IL} = 0.57 V	1.65 V			0.45	
		I _{OLS} = 8 mA, V _{IL} = 0.7 V	2.3 V			0.55	
		I _{OLS} = 12 mA, V _{IL} = 0.8 V	3 V			0.7	
I _I		V _I = V _{CC} or GND	3.6 V			±2.5	μA
I _{off}		V _I or V _O = 3.6 V	0			±10	μA
I _{OZ}		V _O = V _{CC} or GND, \overline{OE} = V _{CC}	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
C _i	CLK input	V _I = V _{CC} or GND	2.5 V	4		pF	
			3.3 V	4			
	Control inputs	V _I = V _{CC} or GND	2.5 V	4			
			3.3 V	4			
	Data inputs	V _I = V _{CC} or GND	2.5 V	2.5			
			3.3 V	2.5			
C _o	Outputs	V _O = V _{CC} or GND	2.5 V	6.5		pF	
			3.3 V	6.5			

† Typical values are measured at T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)

		V _{CC} = 1.2 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency					150		150		150		MHz
t _w	Pulse duration	LE high				3.3		3.3		3.3		ns
		CLK high or low				3.3		3.3		3.3		
t _{su}	Setup time	Data before CLK↑		1	0.9	0.7		0.7		0.7		ns
		Data before LE↓	CLK high	1.7	1.6	1.2		0.8		0.8		
			CLK low	2	0.9	0.7		0.5		0.5		
t _h	Hold time	Data after CLK↑		1.5	1.3	1		0.9		1.3		ns
		Data after LE↓	CLK high	3.2	2.4	2		1.7		1.6		
			CLK low	2.8	2.1	1.7		1.5		1.4		



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18-BIT UNIVERSAL BUS DRIVER
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.2 V	V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}						150		150		150		MHz
t _{pd}	A	Y	4.5	1.2	6.2	1.3	5.5	1	3.1	0.9	2.5	ns
	LE		6.2	1.6	9.4	1.3	7.2	1.1	4.7	0.9	3.8	
	CLK		5.2	1.6	7.8	1.5	6	1	3.7	0.8	3.1	
t _{en}	\overline{OE}	Y	7.1	2.4	10.2	2.2	8.8	1.5	6.7	1.2	6.2	ns
t _{dis}	\overline{OE}	Y	6.9	2.2	10.3	2	8.4	1.2	5.3	1.1	5.3	ns

switching characteristics, T_A = 0°C to 85°C, C_L = 0 pF†

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t _{pd}	A	Y	0.6	1.3	ns
	CLK		0.7	1.5	

† Texas Instruments SPICE simulation data

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	C _L = 0, f = 10 MHz	45	48	52	pF
	Outputs disabled		23	25	28	

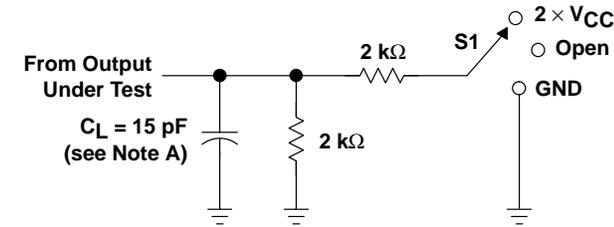


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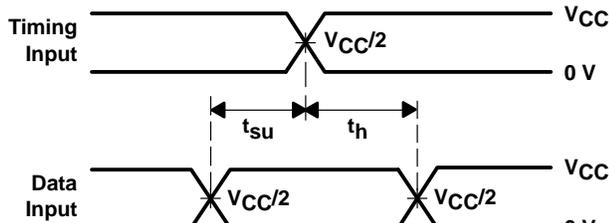
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2\text{ V AND }1.5\text{ V} \pm 0.1\text{ V}$

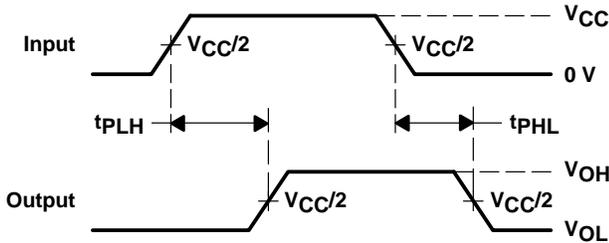


LOAD CIRCUIT

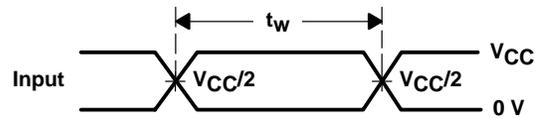
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



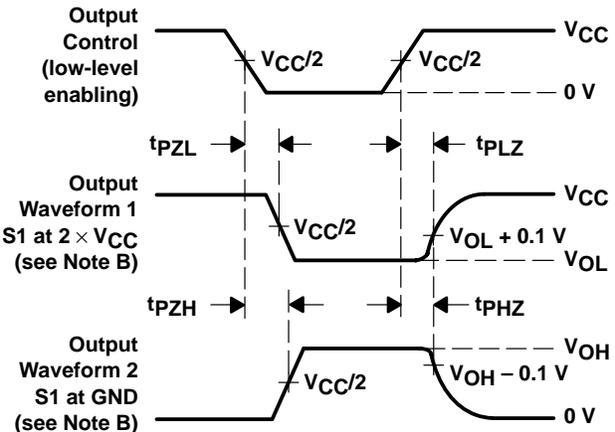
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



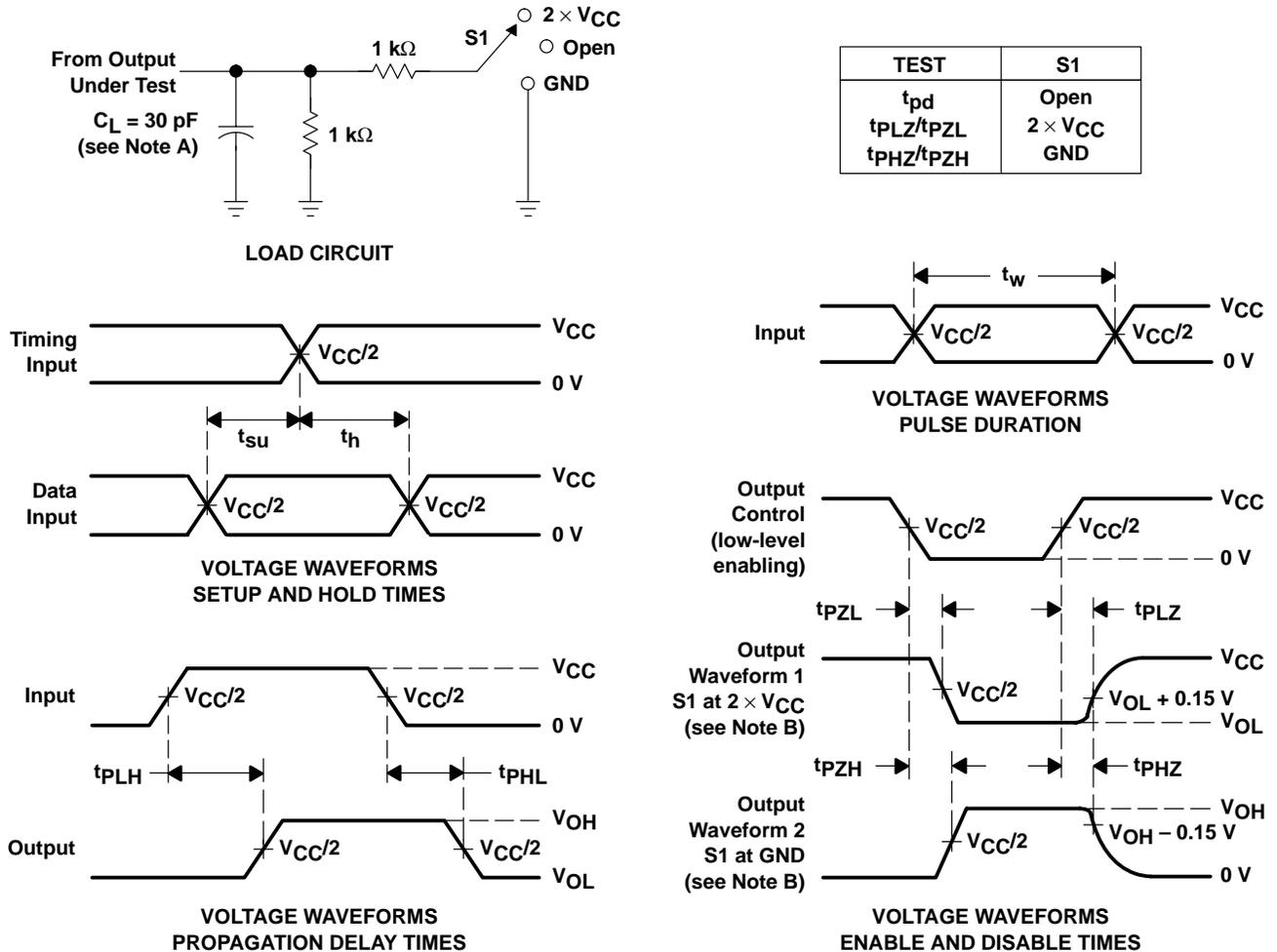
**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

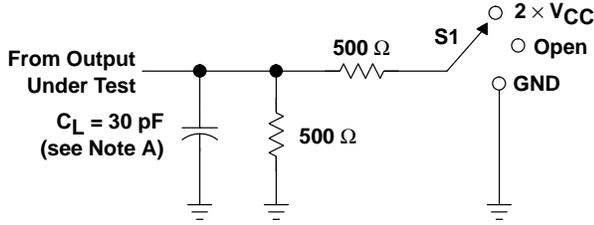
Figure 3. Load Circuit and Voltage Waveforms

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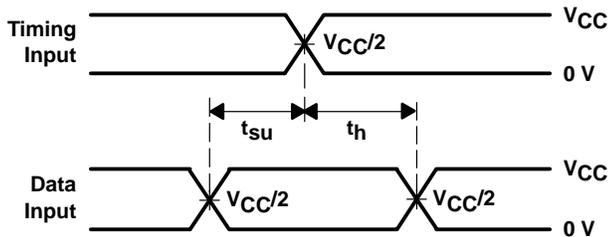
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

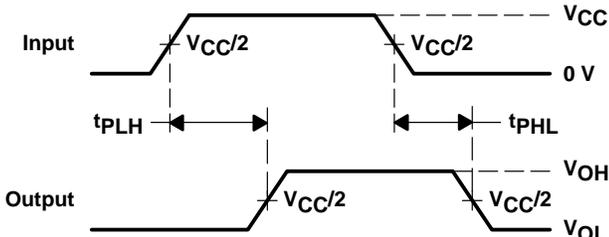


LOAD CIRCUIT

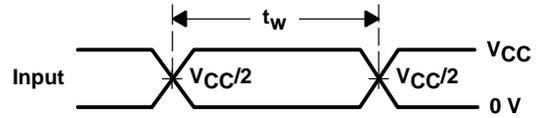
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



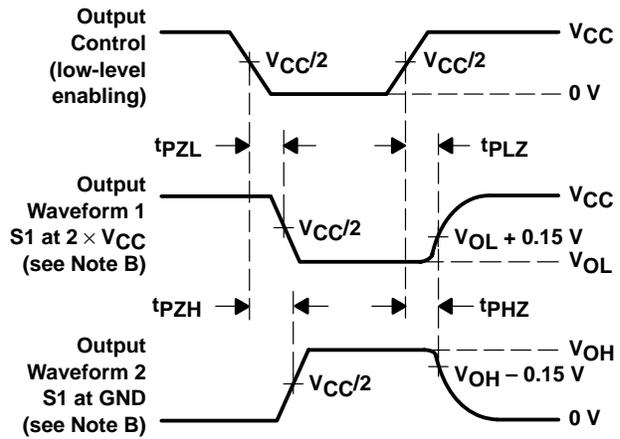
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

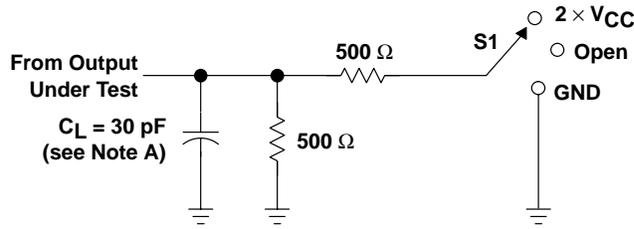
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms



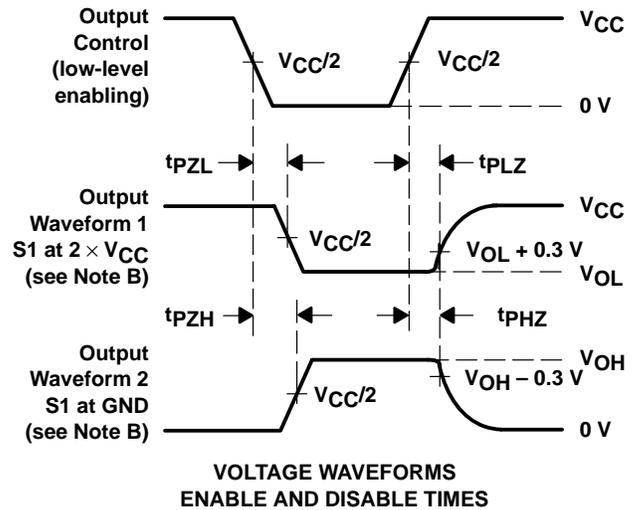
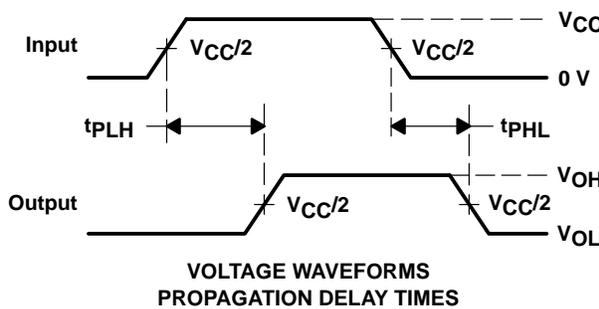
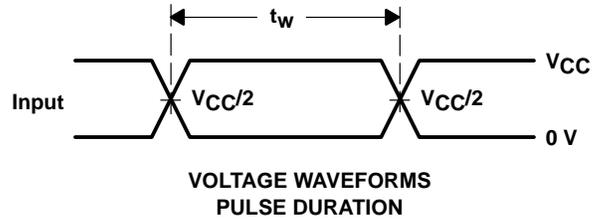
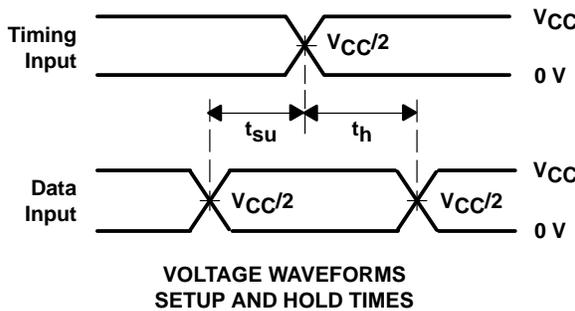
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AVC16835DGVR	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVA835
SN74AVC16835DGVR.B	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVA835

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC16835DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

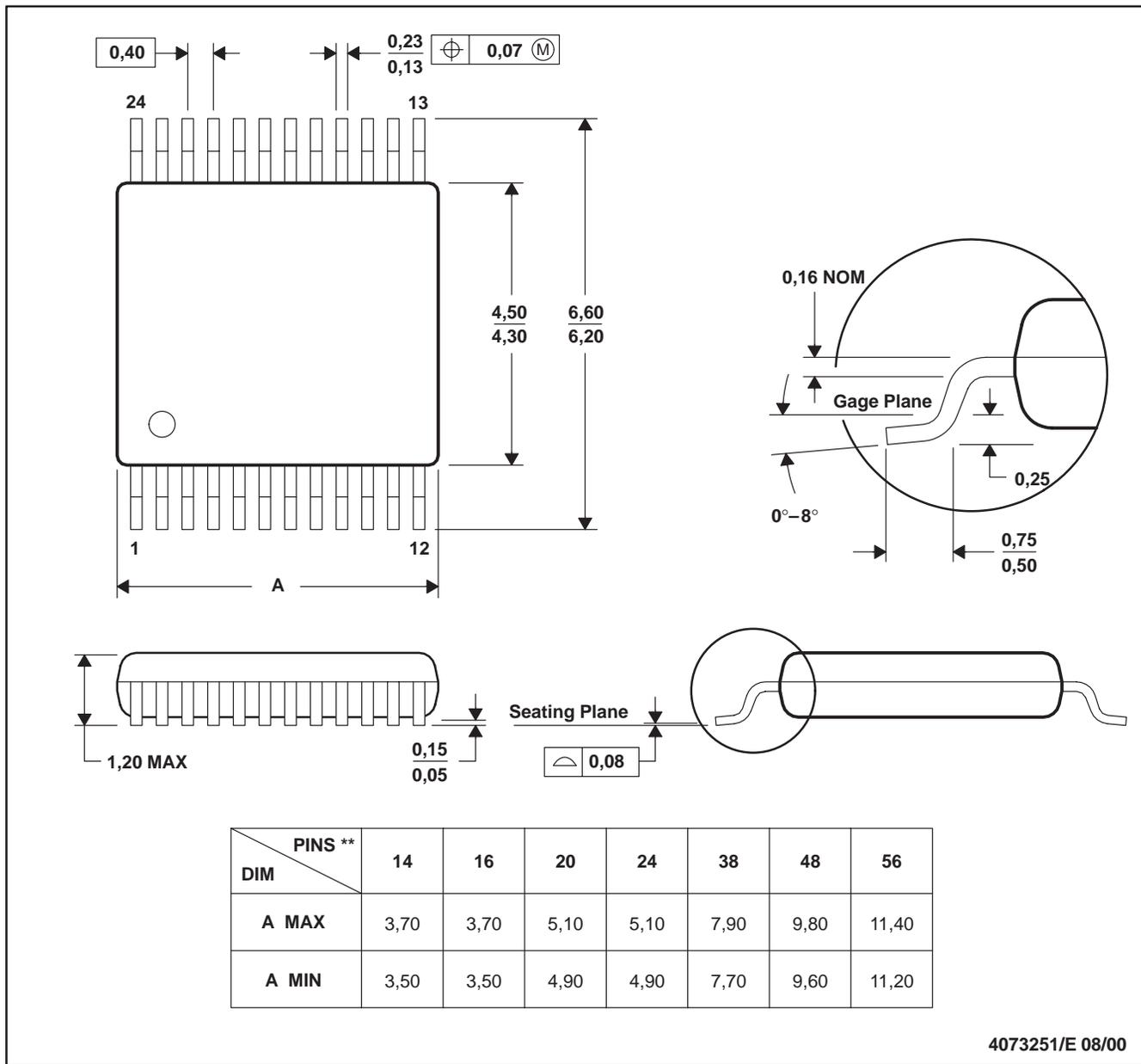

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC16835DGVR	TVSOP	DGV	56	2000	356.0	356.0	45.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

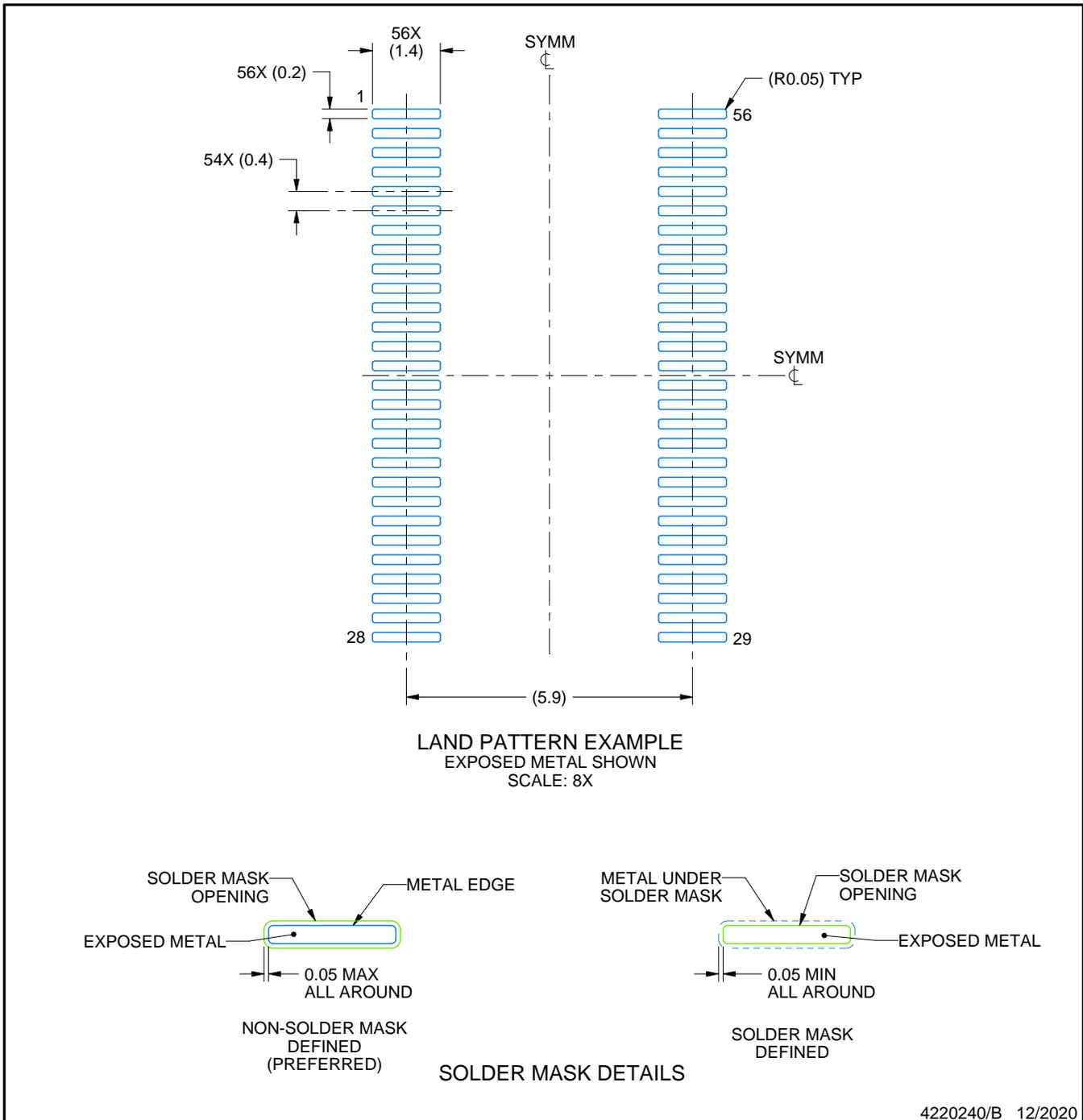
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

EXAMPLE BOARD LAYOUT

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220240/B 12/2020

NOTES: (continued)

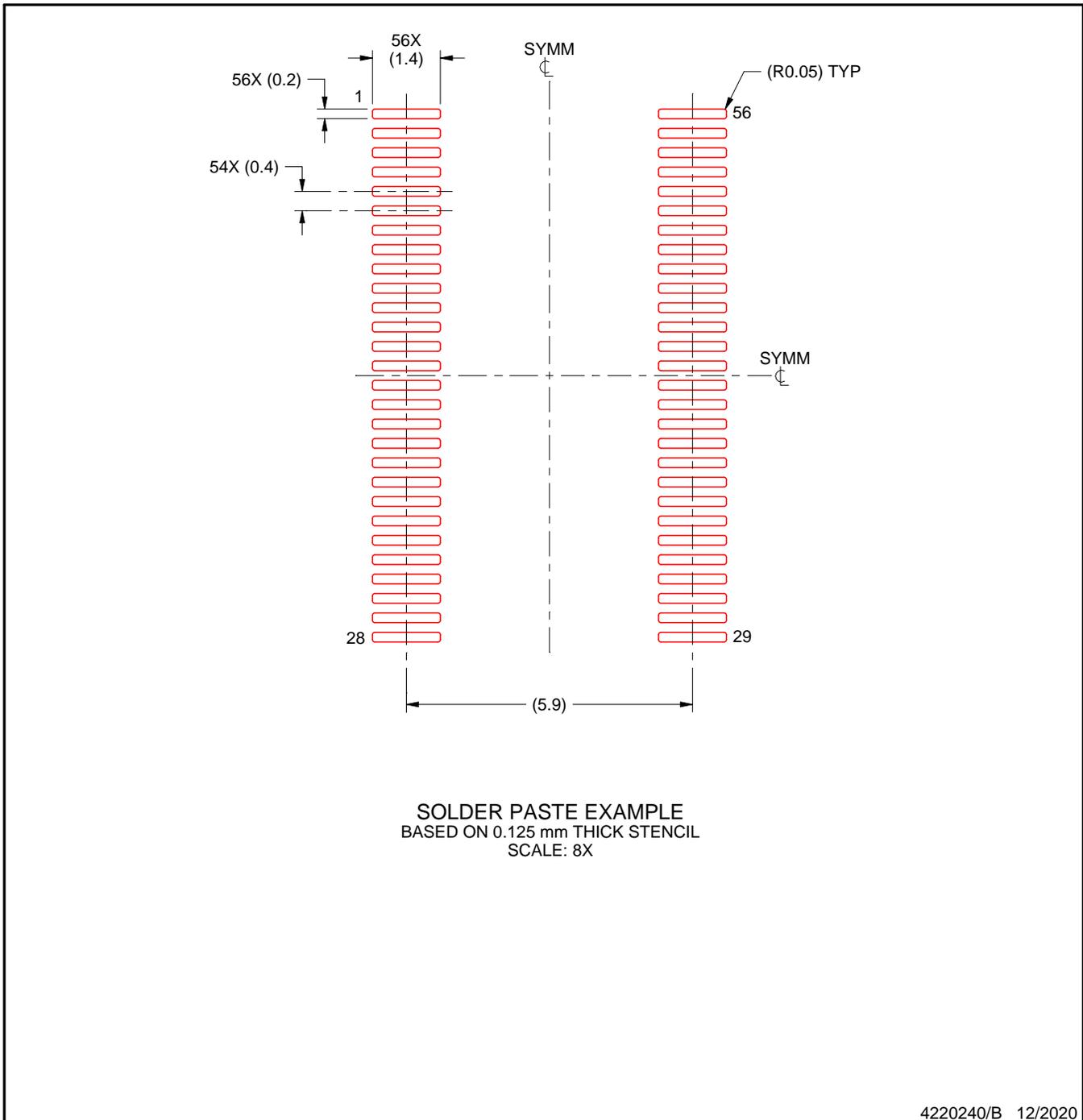
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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