

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Ideal for Use in PC133 Register DIMM
- Typical Output Skew . . . <250 ps
- $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$. . . Normal Range
- $V_{CC} = 2.7\text{ V}$ to 3.6 V . . . Extended Range
- $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$
- Rail-to-Rail Output Swing for Increased Noise Margin
- Balanced Output Drivers . . . $\pm 18\text{ mA}$
- Low Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

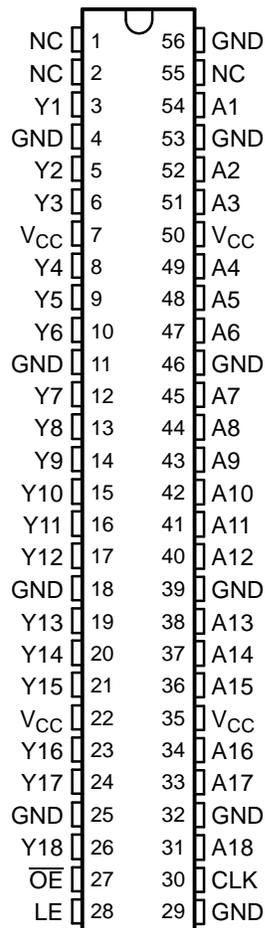
DESCRIPTION/ORDERING INFORMATION

This 18-bit universal bus driver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN74ALVCF162835 has series damping resistors in the device output structure that reduce switching noise in 128-MB and 256-MB SDRAM modules. Designed with a drive capability of $\pm 18\text{ mA}$, this device is a midway drive between the SN74ALVC162835 ($\pm 12\text{ mA}$) and SN74ALVC16835 ($\pm 24\text{ mA}$).

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCF162835DL	
		Tape and reel	SN74ALVCF162835DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCF162835GR	ALVCF162835
	TVSOP - DGV	Tape and reel	SN74ALVCF162835VR	VF2835

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN74ALVCF162835

3.3-V CMOS 18-BIT UNIVERSAL BUS DRIVER

WITH 3-STATE OUTPUTS

SCES397A—JULY 2002—REVISED AUGUST 2004

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74ALVCF162835 is a faster version of the SN74ALVC162835. It is suitable for PC133 applications and, particularly, SDRAM modules clocked at 133 MHz.

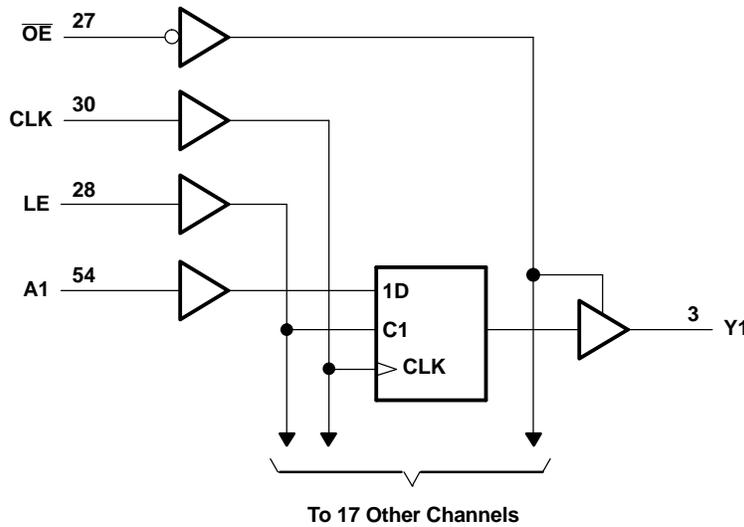
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

INPUTS				OUTPUT
\overline{OE}	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	$Y_0^{(1)}$

(1) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I < V_{CC}$		-50 mA
I_{OK}	Output clamp current	$V_O < 0$		-50 mA
I_O	Continuous output current			±50 mA
Continuous current through each V_{CC} or GND				±100 mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package		64 °C/W
		DGV package		48
		DL package		56
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V		1.7 V
		$V_{CC} = 2.7$ V to 3.6 V		2
V_{IL}	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V		0.7 V
		$V_{CC} = 2.7$ V to 3.6 V		0.8
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3$ V		-6 mA
				-8
		$V_{CC} = 2.7$ V		-6
				-12
I_{OL}	Low-level output current	$V_{CC} = 3$ V		-8 mA
				-18
		$V_{CC} = 2.3$ V		6
				8
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		6
				12
		$V_{CC} = 3$ V		8
				18
$\Delta t/\Delta v$	Input transition rise or fall rate			10 ns/V
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCF162835

3.3-V CMOS 18-BIT UNIVERSAL BUS DRIVER

WITH 3-STATE OUTPUTS

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -0.1 mA	2.3 V to 3.6 V	V _{CC} - 0.2			V
	I _{OH} = -6 mA	2.3 V	1.9			
	I _{OH} = -8 mA		1.7			
	I _{OH} = -6 mA		2.7 V	2.2		
	I _{OH} = -12 mA	2				
	I _{OH} = -8 mA	2.4				
	I _{OH} = -18 mA	3 V	2			
V _{OL}	I _{OL} = 0.1 mA	2.3 V to 3.6 V	0.2			V
	I _{OL} = 6 mA	2.3 V	0.4			
	I _{OL} = 8 mA		0.55			
	I _{OL} = 6 mA		2.7 V	0.4		
	I _{OL} = 12 mA	0.6				
	I _{OL} = 8 mA	0.55				
	I _{OL} = 18 mA	3 V	0.8			
V _{IK}	V _{CC} = 2.3 V, I _I = -18 mA	3.6 V	-1.2			V
V _{hys}	V _{CC} = 3.6 V	3.6 V	100			mV
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	0.1 40			μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			μA
C _i	Inputs V _I = 0 V	3.3 V	3.5			pF
C _o	Outputs V _O = 0 V	3.3 V	4.5			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 2)

		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency	150		150		150		MHz	
t _w	Pulse duration	LE high		3.3		3.3		ns	
		CLK high or low		3.3		3.3			
t _{su}	Setup time	Data before CLK↑		1.8		1.5		ns	
		Data before LE↓	CLK high		1.9		1.6		
			CLK low		1.3		1.1		
t _h	Hold time	Data after CLK↑		0.6		0.6		ns	
		Data after LE↓	CLK high or low		1.4		1.7		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	A	Y	1	4		4.6	1	3.5	ns
	LE		1.3	5.5		5.4	1.3	4.6	
	CLK		1.4	5.9		5.6	1.4	3.5	
t_{en}	\overline{OE}	Y	1.4	5.9		6	1.1	5	ns
t_{dis}	\overline{OE}	Y	1	4.7		4.6	1.3	4.2	ns
$t_{sk(o)}$								500	ps

SWITCHING CHARACTERISTICS

from 0°C to 65°C, $C_L = 50\text{ pF}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.15\text{ V}$		UNIT
			MIN	MAX	
t_{pd}	CLK	Y	1.8	3.5	ns

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	
C_{pd}	Power dissipation capacitance	$C_L = 0\text{ pF}, f = 10\text{ MHz}$	27	33	pF
			Outputs enabled	16	
	Outputs disabled				

SN74ALVCF162835

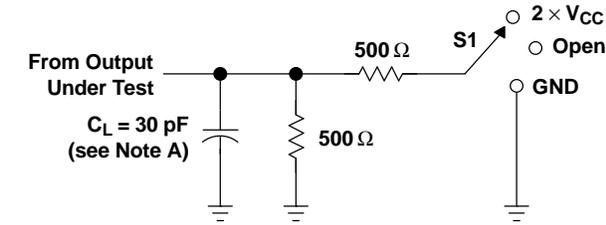
3.3-V CMOS 18-BIT UNIVERSAL BUS DRIVER

WITH 3-STATE OUTPUTS

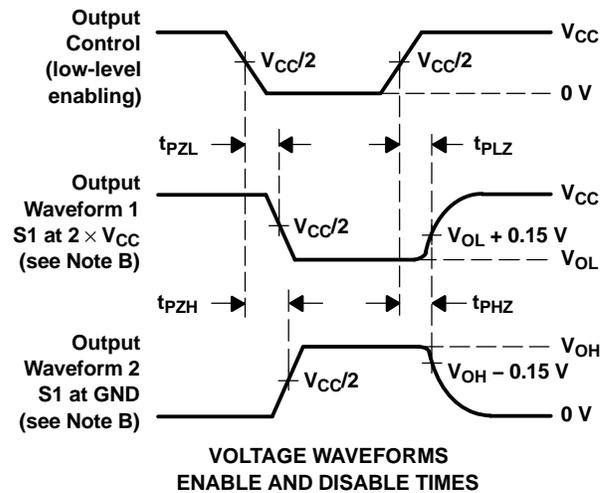
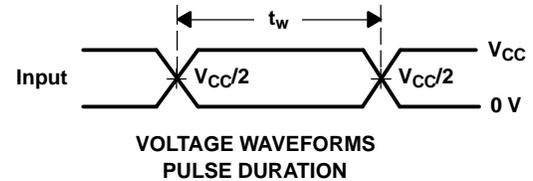
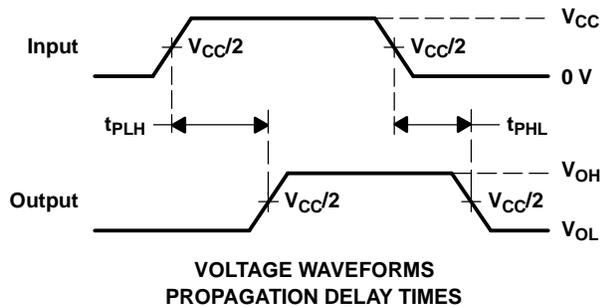
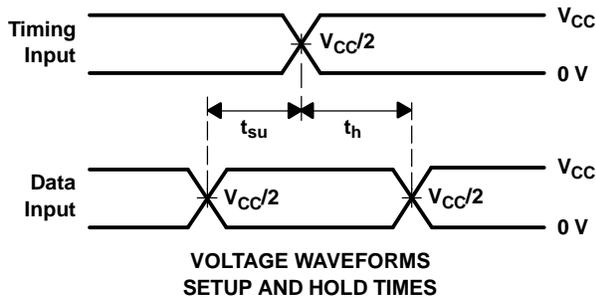
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PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

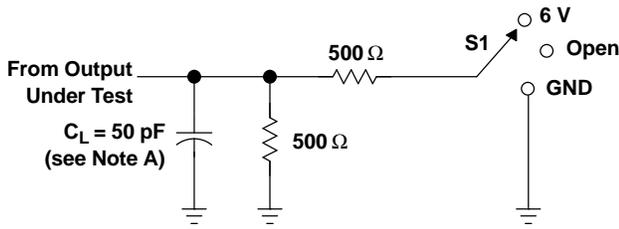


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

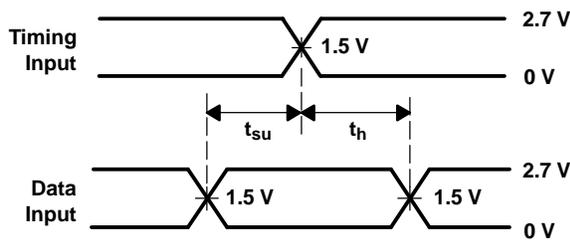
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$

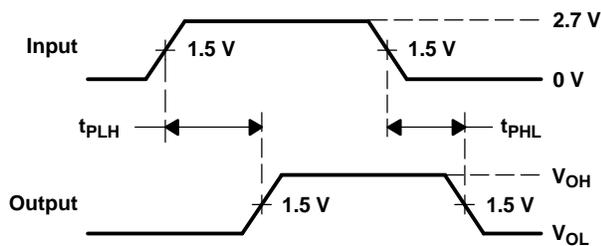


LOAD CIRCUIT

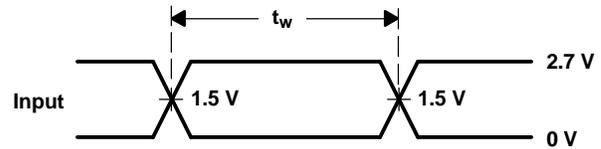
TEST	S1
t_{pd}	Open
t_{pLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



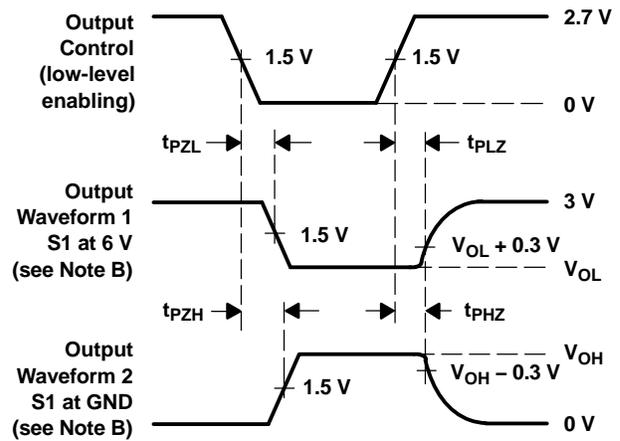
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 F. t_{pZL} and t_{pZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVCF162835GR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCF162835
SN74ALVCF162835GR.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCF162835
SN74ALVCF162835VR	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VF2835
SN74ALVCF162835VR.B	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VF2835

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

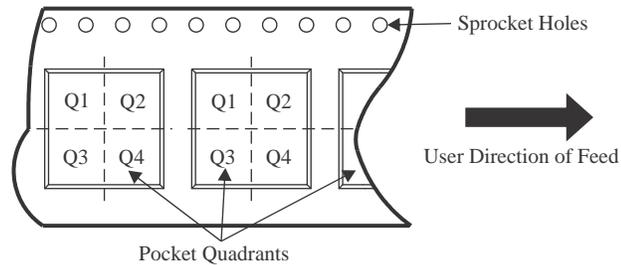
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCF162835GR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ALVCF162835VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

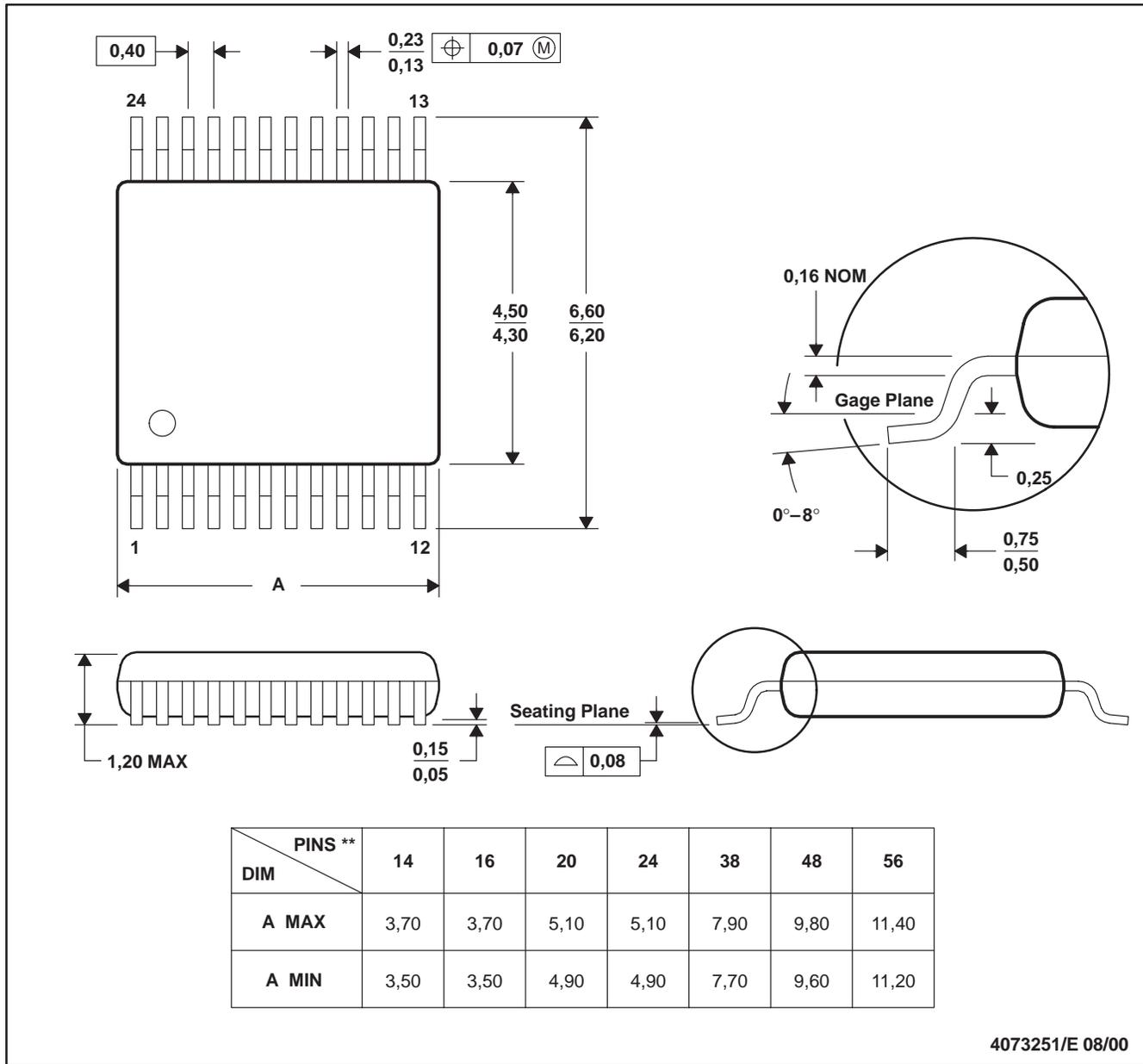

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCF162835GR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ALVCF162835VR	TVSOP	DGV	56	2000	356.0	356.0	45.0

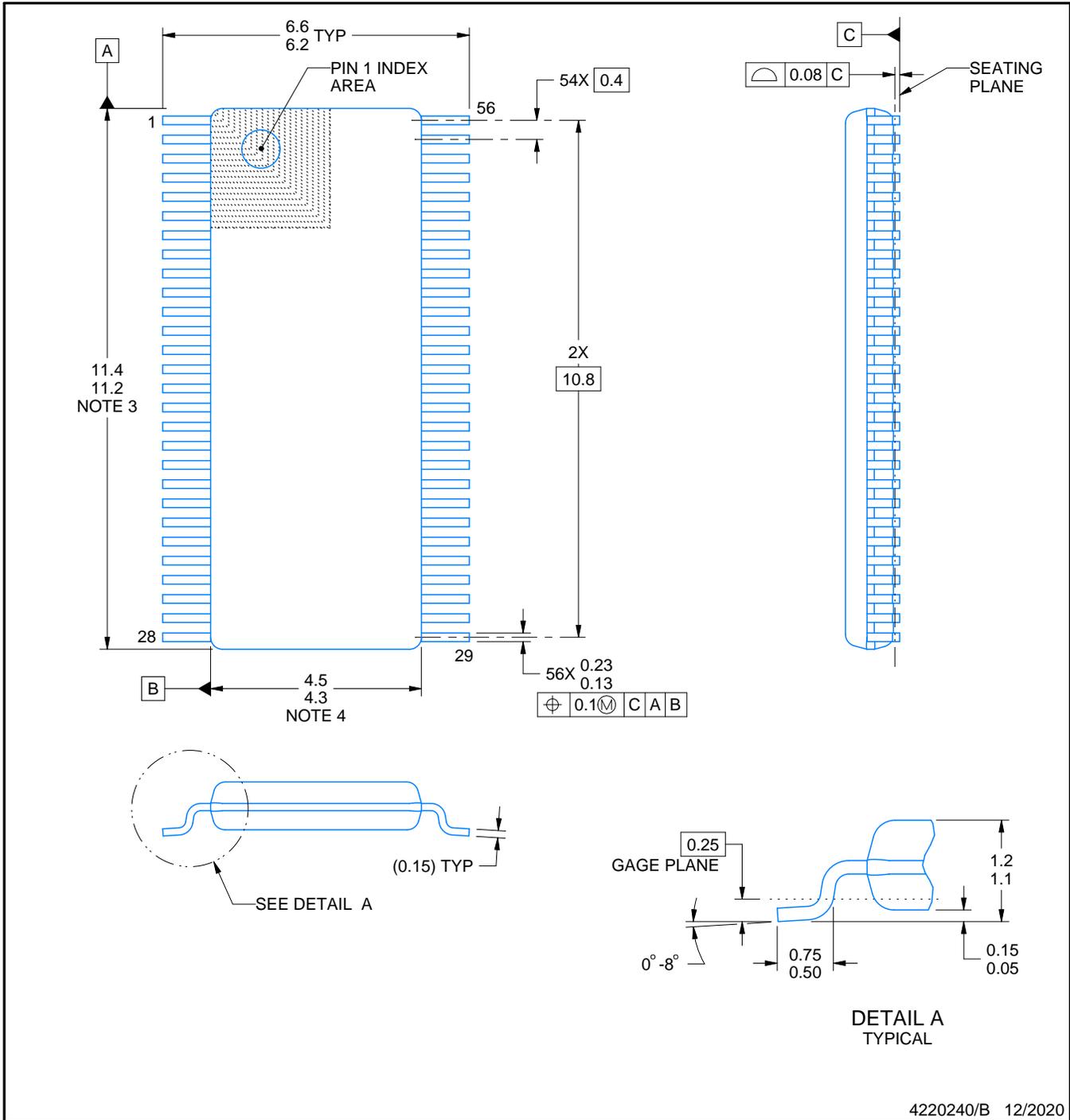
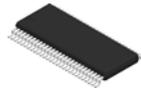
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



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NOTES:

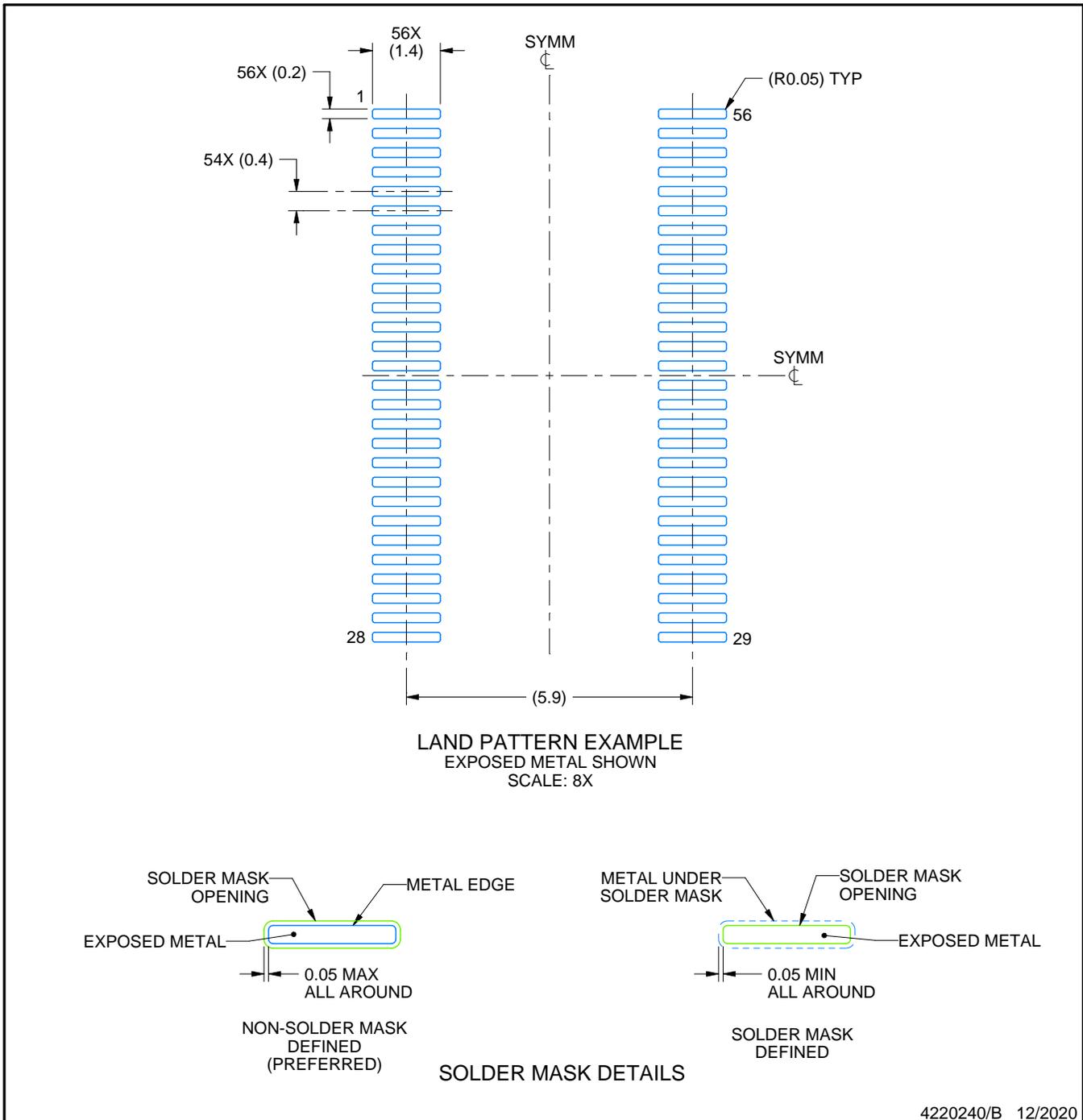
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.

EXAMPLE BOARD LAYOUT

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

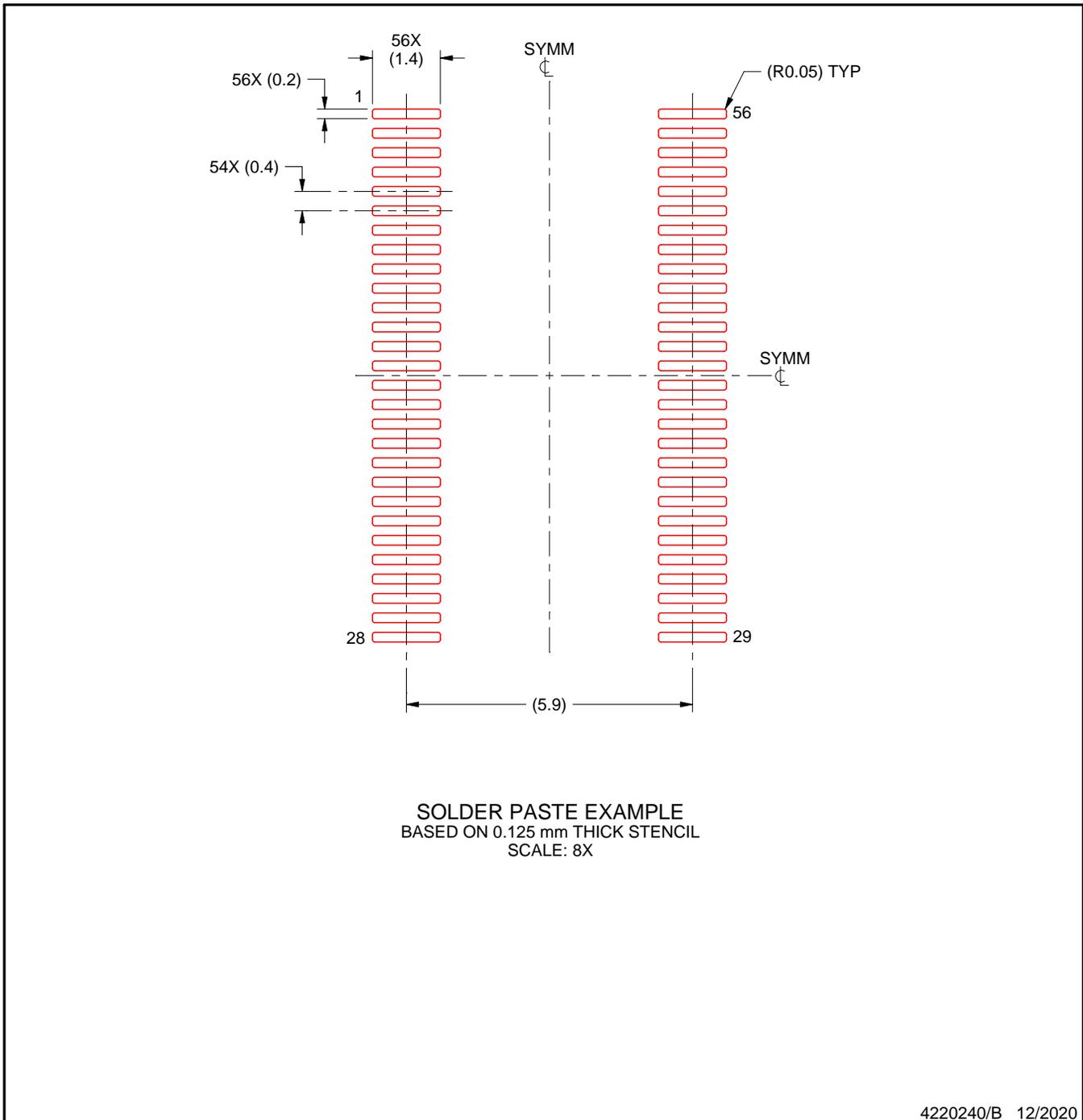
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0056A

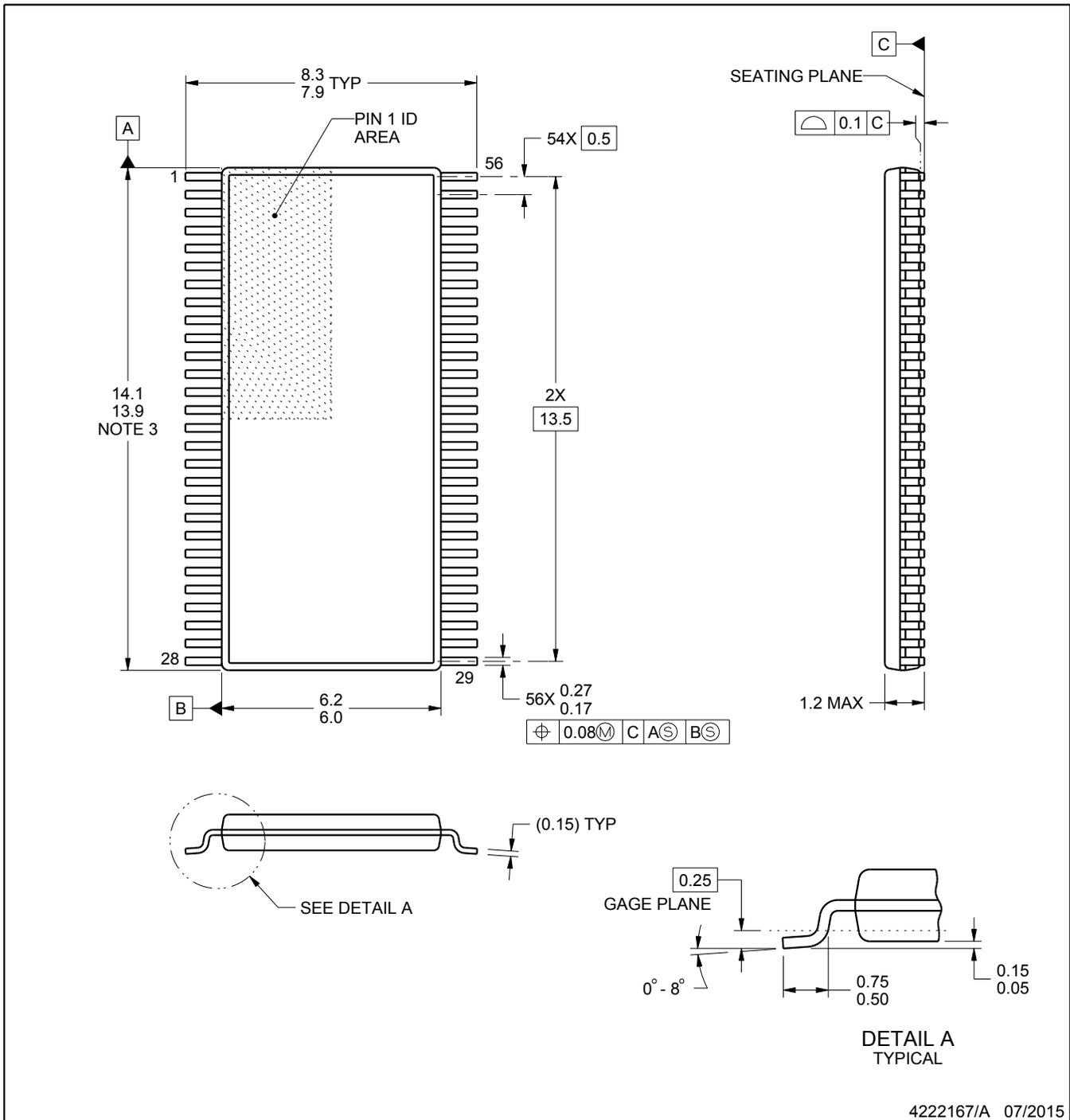
TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4222167/A 07/2015

NOTES:

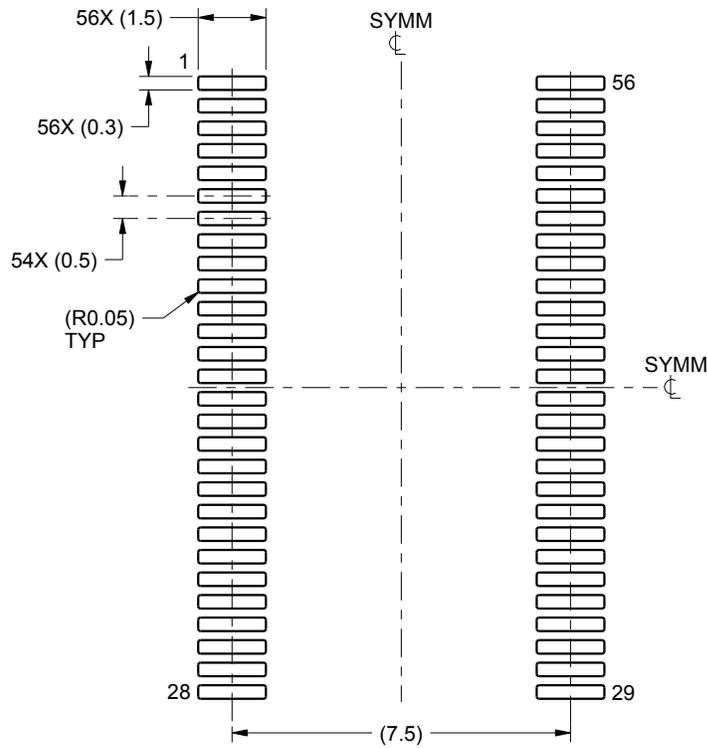
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

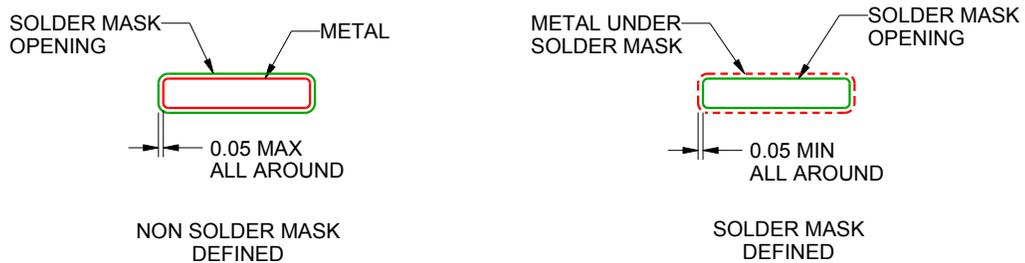
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

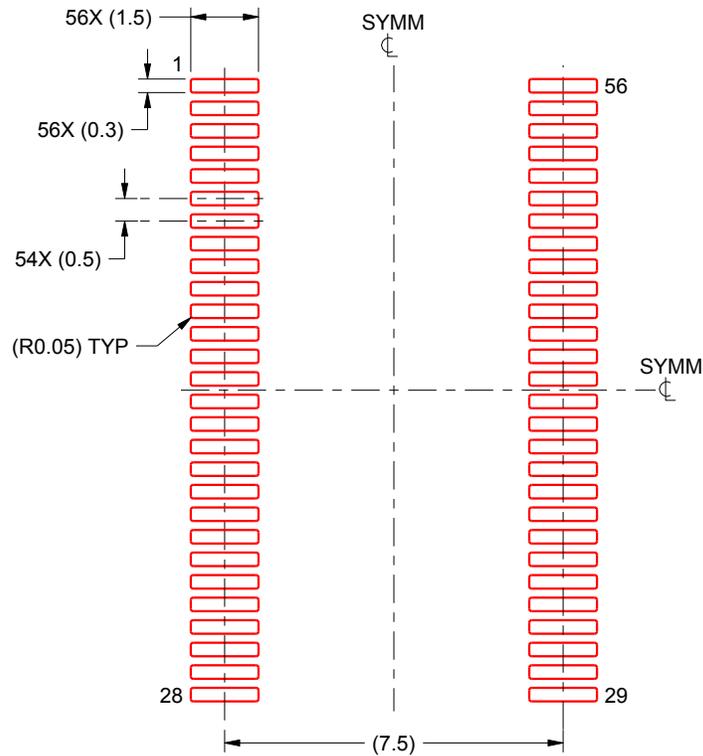
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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