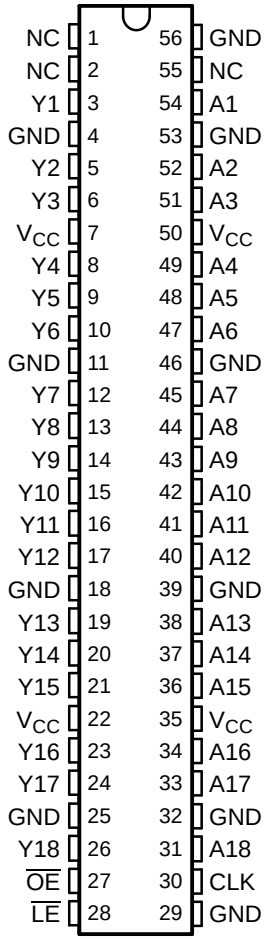
SN74ALVCF162834
3.3-V CMOS 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCES409B – AUGUST 2002 – REVISED OCTOBER 2004

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **Ideal for Use in PC133 Register DIMM**
- **Typical Output Skew . . . <250 ps**
- **V_{CC} = 3.3 V ± 0.3 V . . . Normal Range**
- **V_{CC} = 2.7 V to 3.6 V . . . Extended Range**
- **V_{CC} = 2.5 V ± 0.2 V**
- **Rail-to-Rail Output Swing for Increased Noise Margin**
- **Balanced Output Drivers . . . ±18 mA**
- **Low Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC − No internal connection

DESCRIPTION/ORDERING INFORMATION

This 18-bit universal bus driver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable ($\overline{LE}$) input is low. When $\overline{LE}$ is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The ALVCF162834 has series damping resistors in the device output structure that reduce switching noise in 128-MB and 256-MB SDRAM modules. Designed with a drive capability of ±18 mA, this device is a midway drive between the ALVC162834 (±12 mA) and ALVC16834 (±24 mA).

The SN74ALVCF162834 is a faster version of the SN74ALVC162834. It is suitable for PC133 applications, particularly for SDRAM modules clocked at 133 MHz.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCF162834DL	ALVCF162834
		Tape and reel	SN74ALVCF162834DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCF162834GR	ALVCF162834
	TVSOP - DGV	Tape and reel	SN74ALVCF162834VR	VF162834

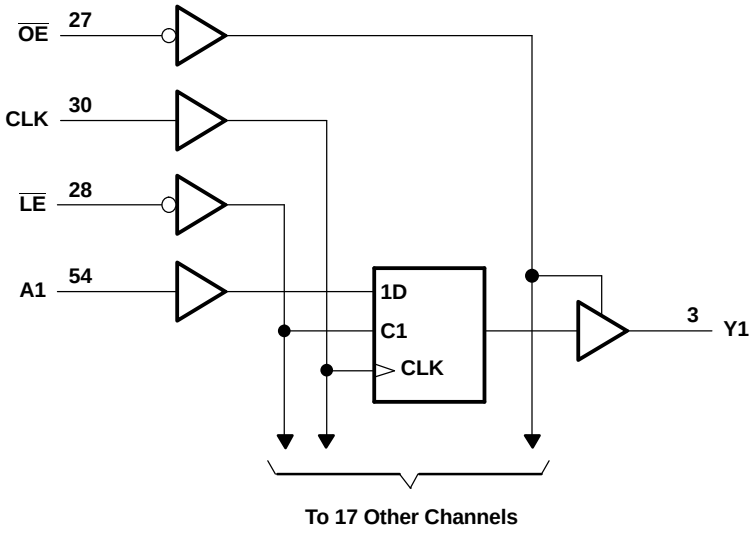
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUT Y
$\overline{OE}$	$\overline{LE}$	CLK	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y_0 (1)

(1) Output level before the indicated steady-state conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range(2)		-0.5	4.6	V
V_O	Output voltage range(2)(3)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		-50	mA
I_{OK}	Output clamp current	V_O < 0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DGG package		64	°C/W
		DGV package		48	
		DL package		56	
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		-6	mA
				-8	
		V_{CC} = 2.7 V		-6	
				-12	
		V_{CC} = 3 V		-8	
				-18	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
				8	
		V_{CC} = 2.7 V		6	
				12	
		V_{CC} = 3 V		8	
				18	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = -0.1 mA	2.3 V to 3.6 V	V_{CC} - 0.2			V
		I_{OH} = -6 mA	2.3 V	1.9			
		I_{OH} = -8 mA		1.7			
		I_{OH} = -6 mA	2.7 V	2.2			
		I_{OH} = -12 mA		2			
		I_{OH} = -8 mA	3 V	2.4			
		I_{OH} = -18 mA		2			
V_{OL}		I_{OL} = 0.1 mA	2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA	2.3 V			0.4	
		I_{OL} = 8 mA				0.55	
		I_{OL} = 6 mA	2.7 V			0.4	
		I_{OL} = 12 mA				0.6	
		I_{OL} = 8 mA	3 V			0.55	
		I_{OL} = 18 mA				0.8	
V_{IK}		V_{CC} = 2.3 V, I_I = -18 mA	3.6 V			-1.2	V
V_{hys}		V_{CC} = 3.6 V	3.6 V		100		mV
I_I		V_I = V_{CC} or GND	3.6 V			±5	µA
I_{OZ}		V_O = V_{CC} or GND	3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V		0.1	40	µA
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Inputs	V_I = 0 V	3.3 V		3		pF
C_o	Outputs	V_O = 0 V	3.3 V		4		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 2)

				V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				150		150		150	MHz
t_w	Pulse duration	$\overline{LE}$ low		3.3		3.3		3.3		ns
		CLK high or low		3.3		3.3		3.3		
t_{su}	Setup time	Data before CLK↑		1.8		1.5		1		ns
		Data before $\overline{LE}$↑	CLK high	1.9		1.6		1.5		
			CLK low	1.3		1.1		1		
t_h	Hold time	Data after CLK↑		0.6		0.6		0.6		ns
		Data after $\overline{LE}$↑	CLK high or low	1.4		1.7		1.4		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	A	Y	1	4		4.6	1	3.5	ns
	$\overline{LE}$		1.3	5.5		5.4	1.3	4.6	
	CLK		1.4	5.9		5.6	1.4	3.5	
t_{en}	$\overline{OE}$	Y	1.4	5.9		6	1.1	5	ns
t_{dis}	$\overline{OE}$	Y	1	4.7		4.6	1.3	4.2	ns
$t_{sk(o)}$								500	ps

SWITCHING CHARACTERISTICS

from 0°C to 65°C, C_L = 50 pF

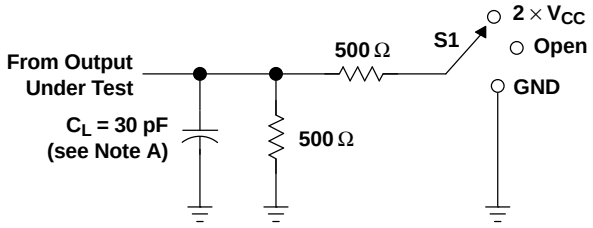
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t_{pd}	CLK	Y	1.8	3.5	ns

OPERATING CHARACTERISTICS

T_A = 25°C

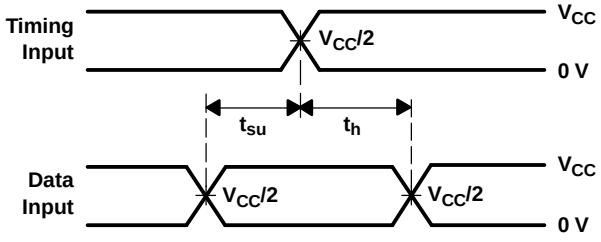
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0, f = 10 MHz	28	33	pF
		Outputs disabled		16	21	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

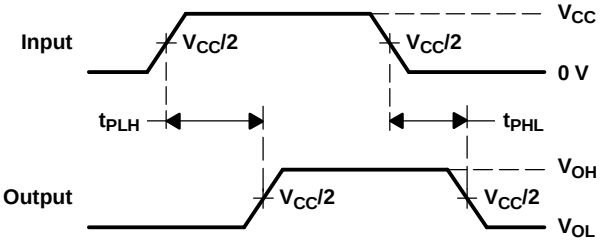


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

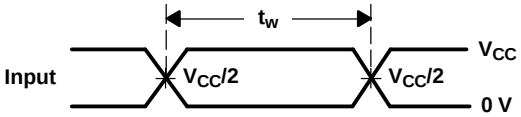
LOAD CIRCUIT



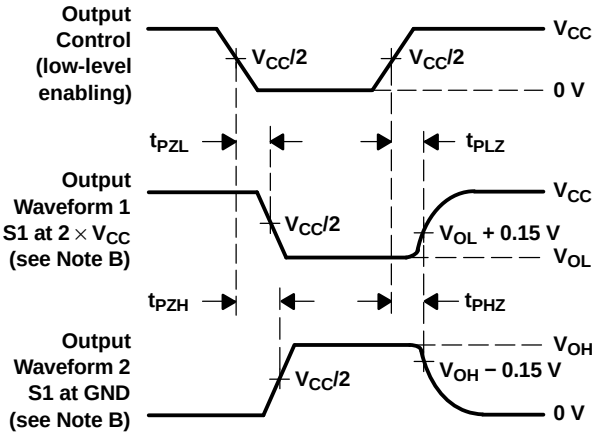
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

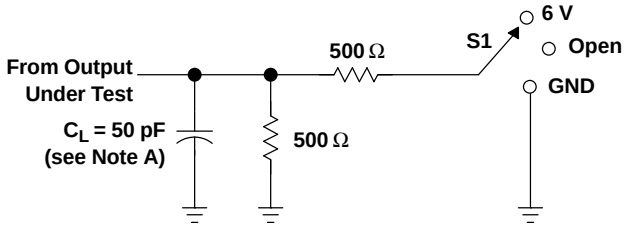


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

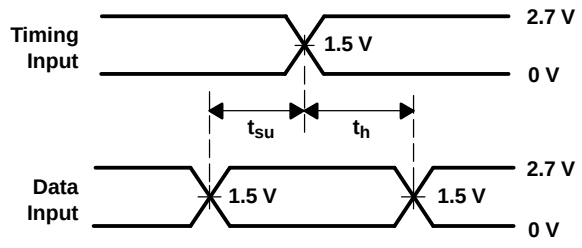
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

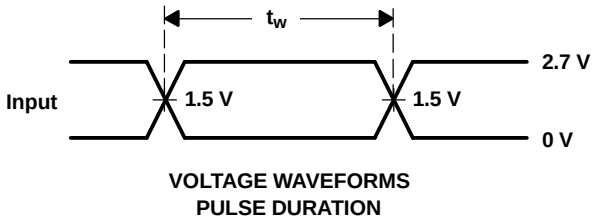


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

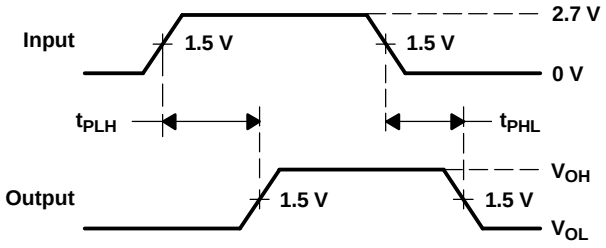
LOAD CIRCUIT



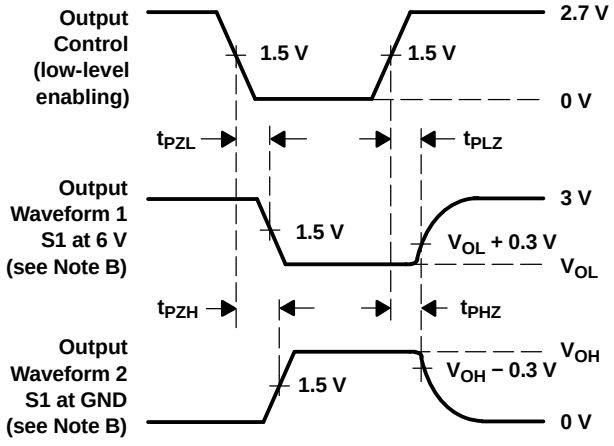
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVCF162834DL	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCF162834
SN74ALVCF162834DL.B	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCF162834

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

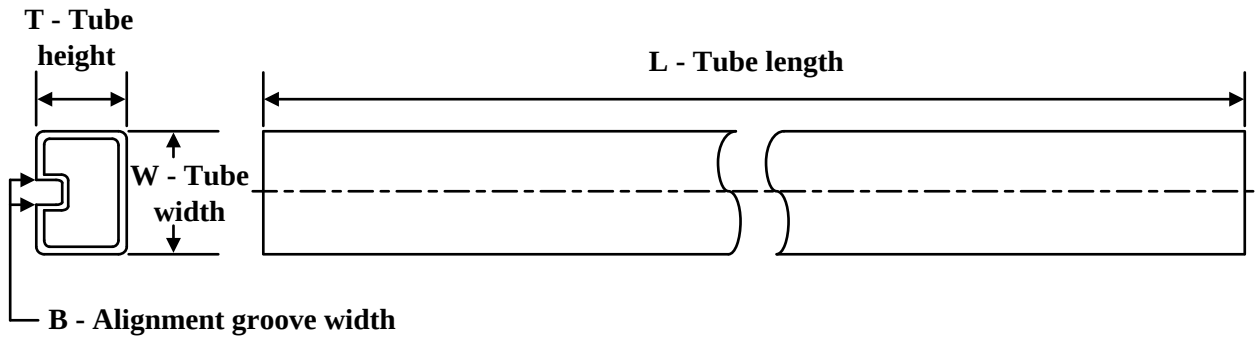
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

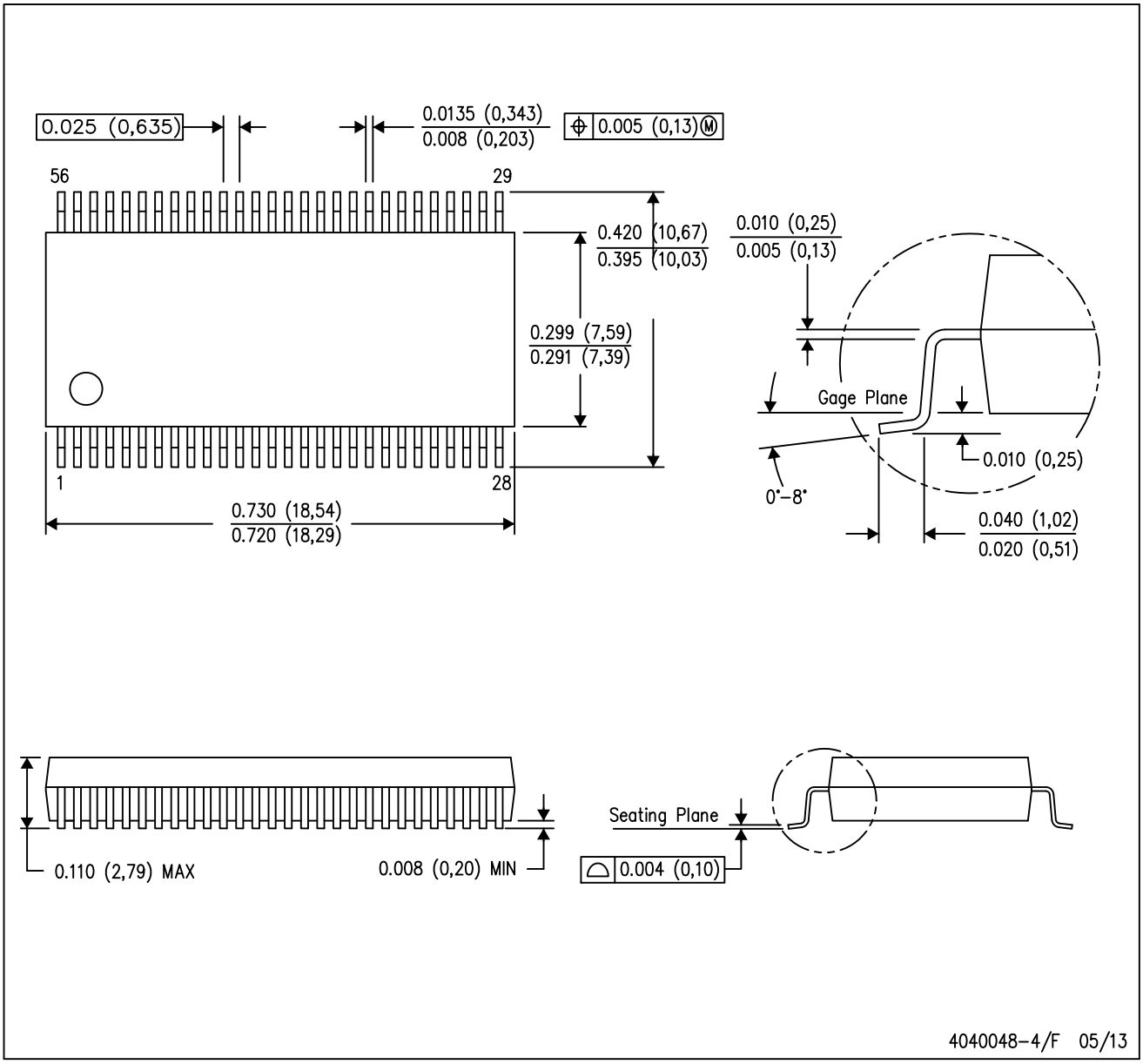
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALVCF162834DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ALVCF162834DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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