



**SN54ABT16601, SN74ABT16601**  
**18-BIT UNIVERSAL BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

SCBS210C – JUNE 1992 – REVISED JANUARY 1997

**FUNCTION TABLE†**

INPUTS					OUTPUT B
CLKENAB	OEAB	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B <sub>0</sub> ‡
H	L	L	X	X	B <sub>0</sub> ‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B <sub>0</sub> ‡
L	L	L	H	X	B <sub>0</sub> §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established

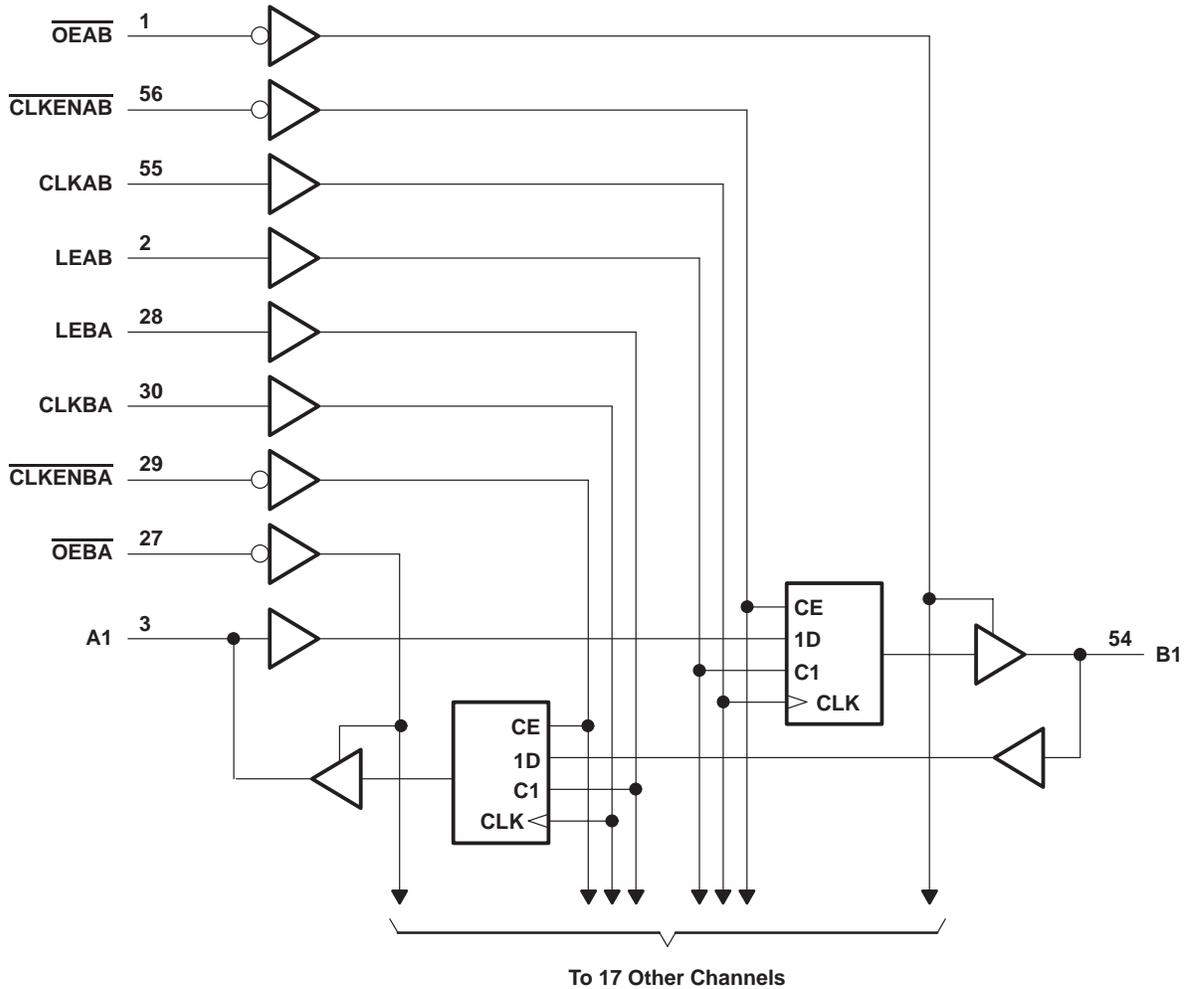
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low



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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_{OL}$ : SN54ABT16601 .....	96 mA
SN74ABT16601 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	81°C/W
DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.



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## recommended operating conditions (see Note 3)

		SN54ABT16601		SN74ABT16601		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT16601		SN74ABT16601		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V	
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$		2.5		2.5		2.5		V	
	$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$		3		3		3			
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$		2		2				
		$I_{OH} = -32\text{ mA}$		2*			2			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.55		0.55			V	
		$I_{OL} = 64\text{ mA}$		0.55*			0.55			
$V_{hys}$			100						mV	
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$ or GND		$\pm 1$		$\pm 1$		$\pm 1$	$\mu\text{A}$	
	A or B ports			$\pm 20^{**}$		$\pm 100$		$\pm 20$		
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O \leq 4.5\text{ V}$			$\pm 100$				$\pm 100$	$\mu\text{A}$	
$I_{CEX}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$	Outputs high		50		50		50	$\mu\text{A}$	
$I_O^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
$I_{OZH}^\S$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			10		10		10	$\mu\text{A}$	
$I_{OZL}^\S$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.5\text{ V}$			-10		-10		-10	$\mu\text{A}$	
$I_{CC}$	A or B ports	$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high	1.9	3		2		3	mA
		Outputs low	28	36		35		36		
		Outputs disabled	1.6	3		2		3		
$\Delta I_{CC}^\parallel$	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND			50				50	$\mu\text{A}$	
						1.5			mA	
$C_i$	Control inputs	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$		3					pF	
$C_{iO}$	A or B ports	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$		9					pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

\*\* This limit applies only to the SN74ABT16601.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.



# SN54ABT16601, SN74ABT16601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

		SN54ABT16601		SN74ABT16601		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	150	0	150	MHz
$t_w$	Pulse duration	LEAB or LEBA high		2.5		ns
		CLKAB or CLKBA high or low		3		
$t_{\text{su}}$	Setup time	A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$		4.6		ns
		A before LEAB $\downarrow$ or B before LEBA $\downarrow$	CLK high	2.5		
			CLK low	1.3		
		CLKEN before CLK $\uparrow$		2.9		
$t_h$	Hold time	A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$		0.4		ns
		A after LEAB $\downarrow$ or B after LEBA $\downarrow$		2.8		
		CLKEN after CLK $\uparrow$		0		

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16601				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			MIN		MAX
			MIN	TYP	MAX			
$f_{\text{max}}$			150	200		150	MHz	
$t_{\text{PLH}}$	A or B	B or A	1.5	2.5	4.1	1	4.6	ns
$t_{\text{PHL}}$			1.5	3.4	4.7	1	5.1	
$t_{\text{PLH}}$	LEAB or LEBA	B or A	2	3.4	4.7	1	5.6	ns
$t_{\text{PHL}}$			2	3.7	5	1	5.5	
$t_{\text{PLH}}$	CLKAB or CLKBA	B or A	1.5	3.2	4.5	1	5.2	ns
$t_{\text{PHL}}$			1.5	3.2	4.4	1	5	
$t_{\text{PZH}}$	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A	2	4	5	1	5.7	ns
$t_{\text{PZL}}$			2	4.2	5.6	1	6	
$t_{\text{PHZ}}$	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A	2	4.5	5.8	1	6.8	ns
$t_{\text{PLZ}}$			1.5	3.4	5.3	1	6.3	

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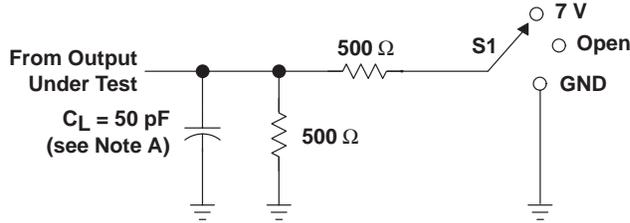
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16601				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
$f_{max}$			150	200		150	MHz	
$t_{PLH}$	A or B	B or A	1.5	2.5	3.6	1.5	4	ns
$t_{PHL}$			1.5	3.4	4.7	1.5	4.9	
$t_{PLH}$	LEAB or LEBA	B or A	2	3.4	4.7	2	5	ns
$t_{PHL}$			2	3.7	5	2	5.2	
$t_{PLH}$	CLKAB or CLKBA	B or A	1.5	3.2	4.5	1.5	4.7	ns
$t_{PHL}$			1.5	3.2	4.4	1.5	4.6	
$t_{PZH}$	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4	5	2	5.5	ns
$t_{PZL}$			2	4.2	5.6	2	5.8	
$t_{PHZ}$	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.5	5.4	2	6.2	ns
$t_{PLZ}$			1.5	3.4	4.7	1.5	5.4	

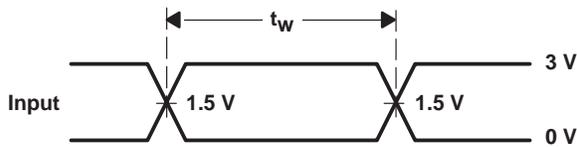


PARAMETER MEASUREMENT INFORMATION

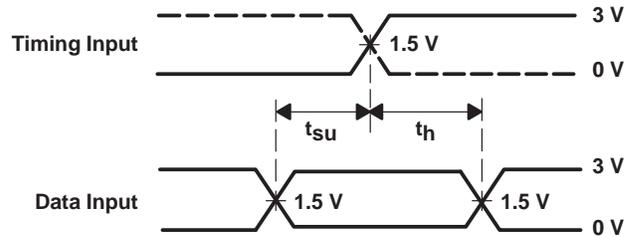


LOAD CIRCUIT

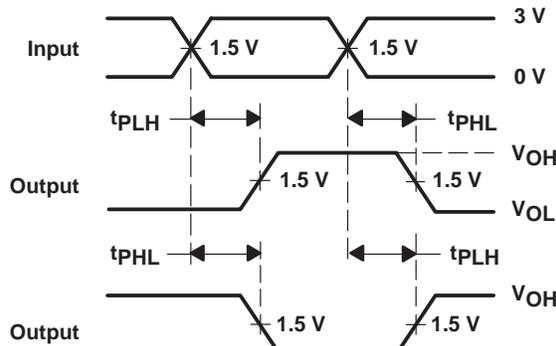
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



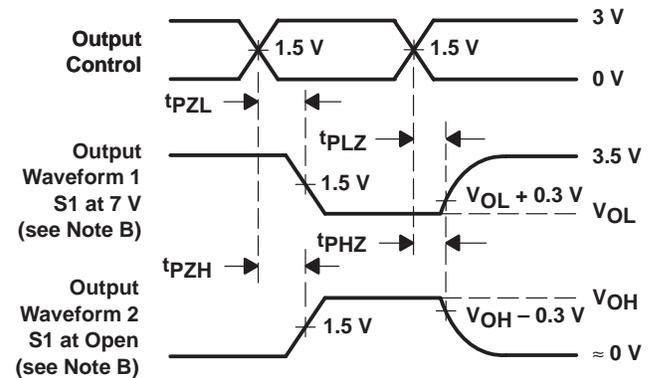
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74ABT16601DGGR</a>	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16601
SN74ABT16601DGGR.B	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16601
<a href="#">SN74ABT16601DL</a>	Active	Production	SSOP (DL)   56	20   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16601
SN74ABT16601DL.B	Active	Production	SSOP (DL)   56	20   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16601
<a href="#">SN74ABT16601DLR</a>	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16601
SN74ABT16601DLR.B	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16601

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

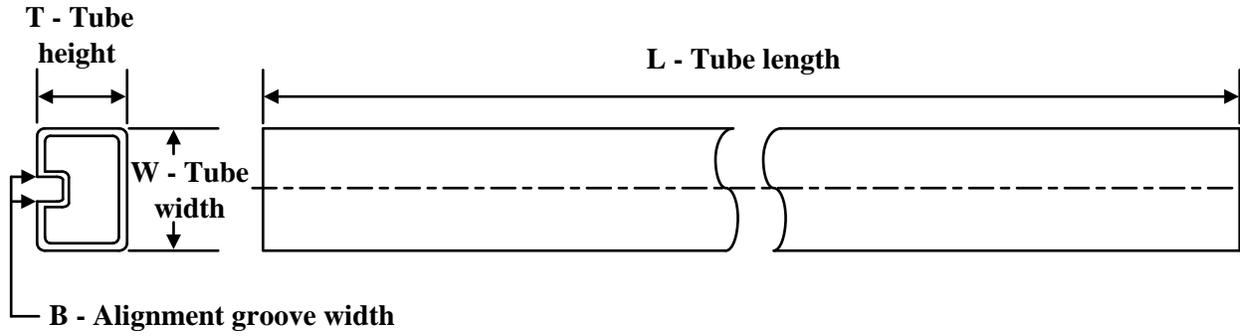

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16601DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ABT16601DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16601DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ABT16601DLR	SSOP	DL	56	1000	356.0	356.0	53.0

**TUBE**


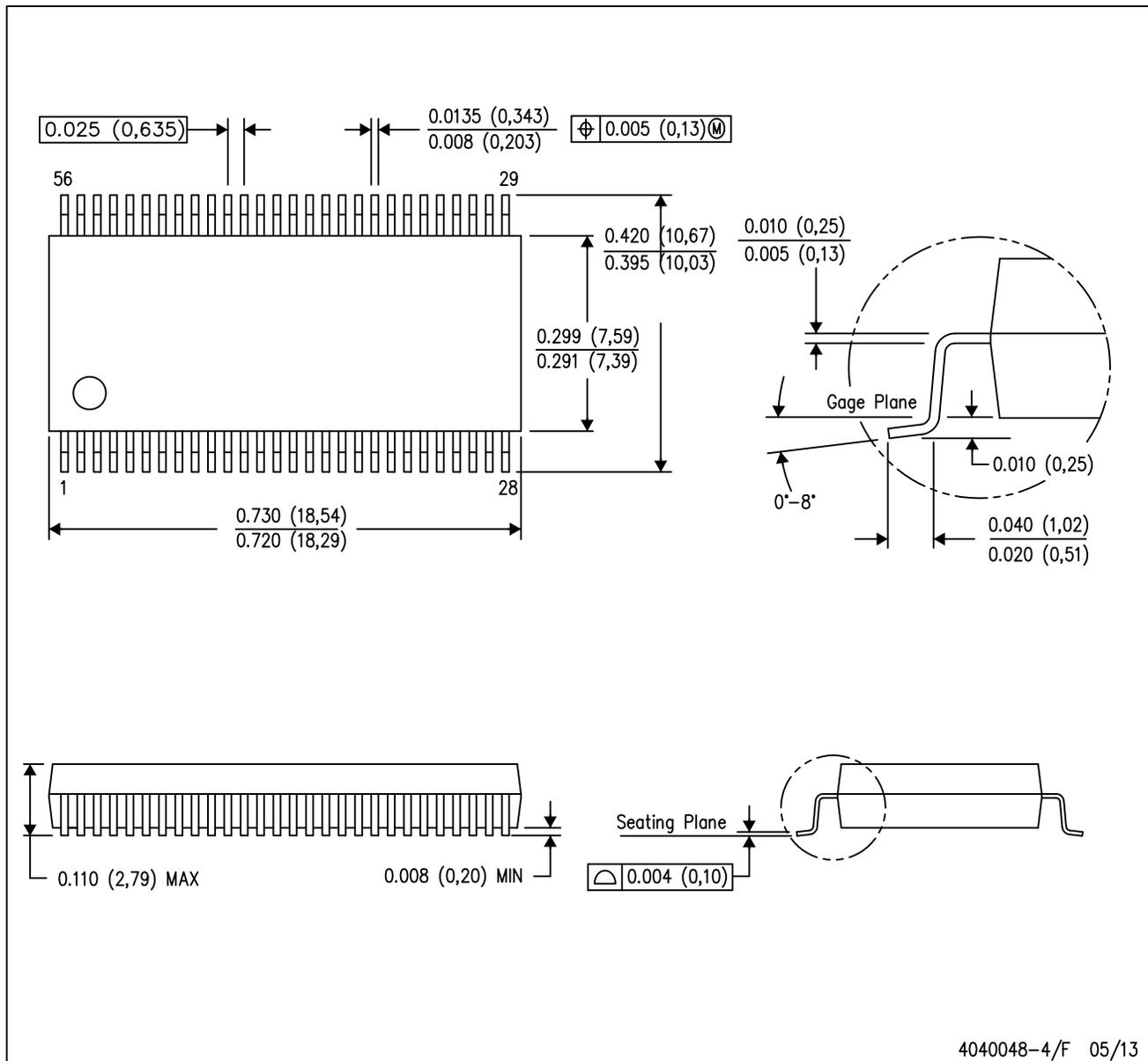
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16601DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABT16601DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

# MECHANICAL DATA

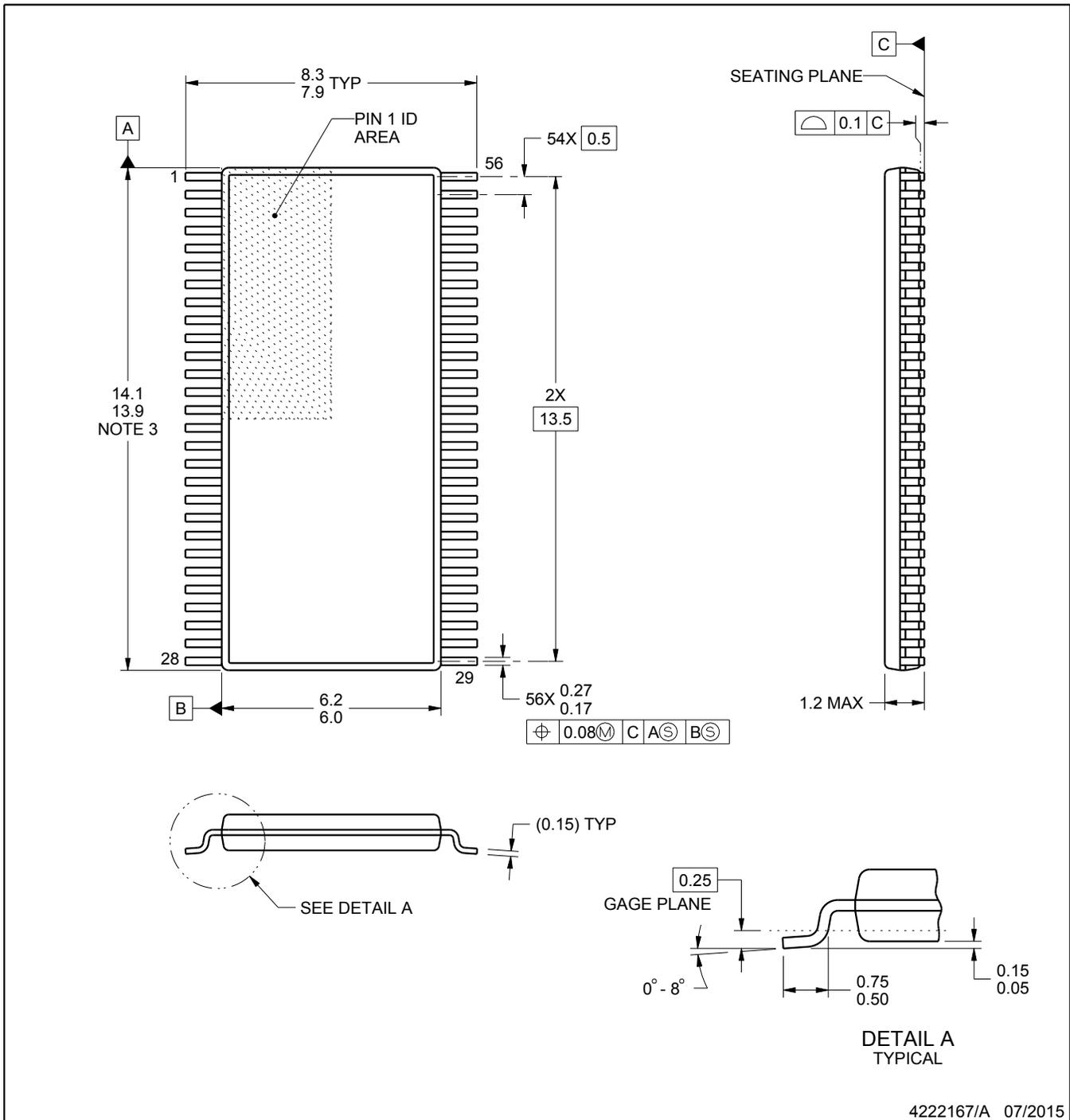
DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



NOTES:

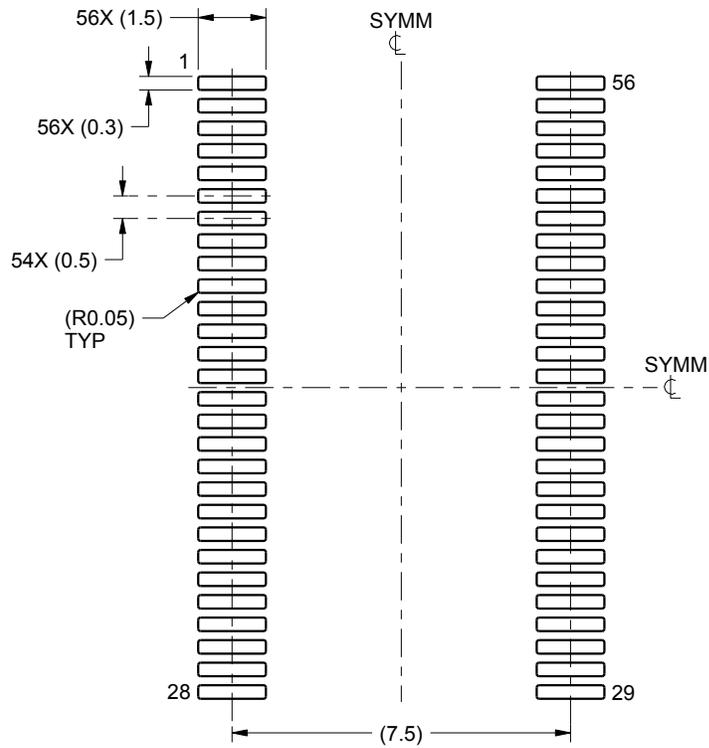
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

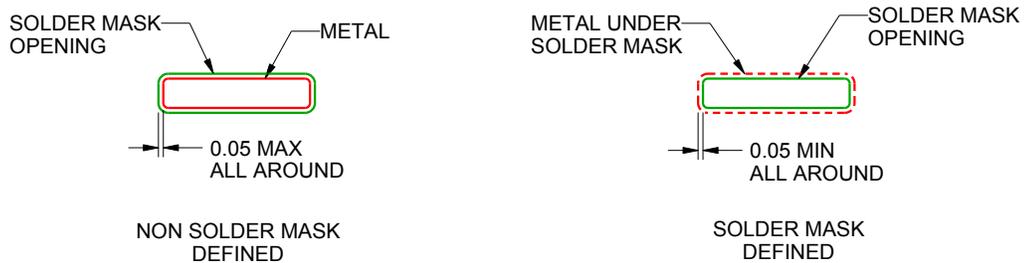
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

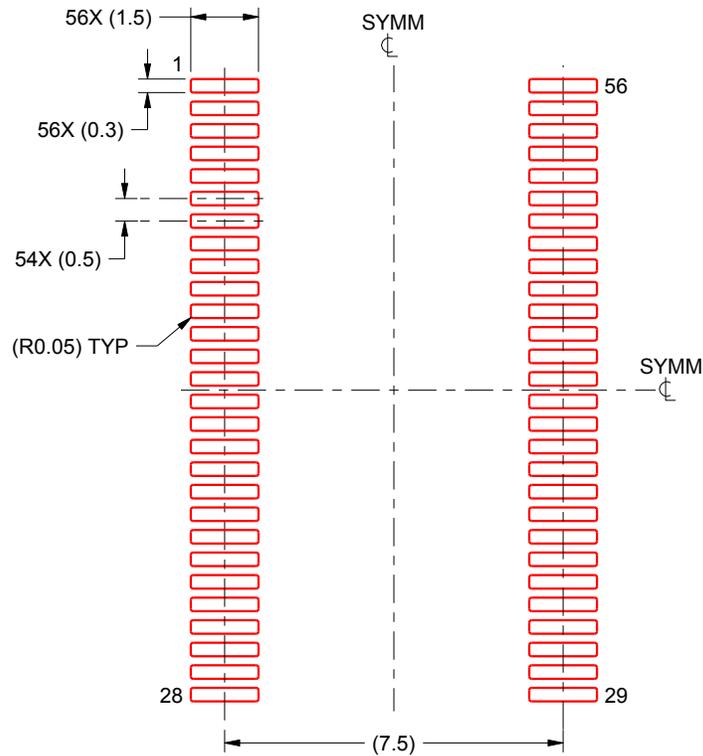
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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