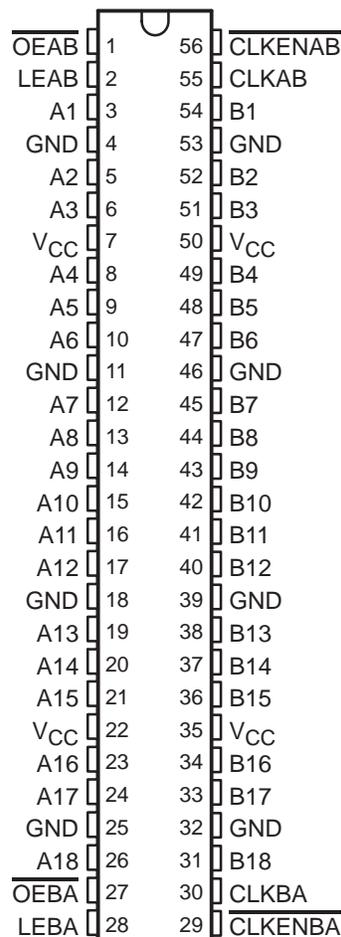


# SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS247G – AUGUST 1992 – REVISED JULY 1998

- **Members of the Texas Instruments Widebus™ Family**
- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **Typical V<sub>OLP</sub> (Output Ground Bounce) < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT162601 . . . WD PACKAGE  
SN74ABT162601 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ( $\overline{CLKENAB}$  and  $\overline{CLKENBA}$ ) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If  $\overline{LEAB}$  is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output-enable  $\overline{OEAB}$  is active-low. When  $\overline{OEAB}$  is low, the outputs are active. When  $\overline{OEAB}$  is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses  $\overline{OEBA}$ , LEBA, CLKBA, and  $\overline{CLKENBA}$ .

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

When V<sub>CC</sub> is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54ABT162601, SN74ABT162601**  
**18-BIT UNIVERSAL BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**description (continued)**

The SN54ABT162601 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .  
 The SN74ABT162601 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE†**

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	$B_0^{\ddagger}$
H	L	L	X	X	$B_0^{\ddagger}$
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	$B_0^{\ddagger}$
L	L	L	H	X	$B_0^{\S}$

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established

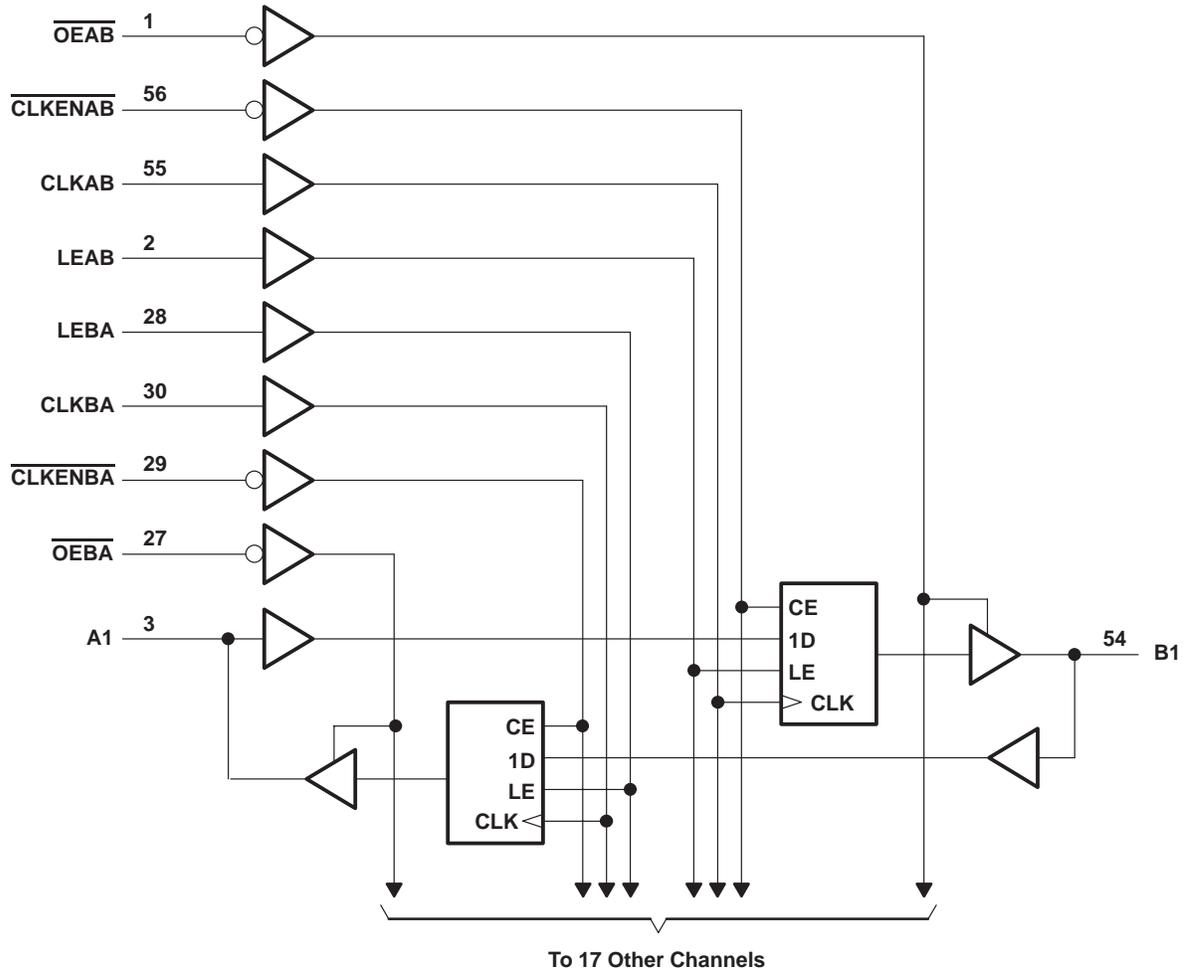
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low



**SN54ABT162601, SN74ABT162601**  
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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT162601 (A port) .....	96 mA
SN74ABT162601 (A port) .....	128 mA
B port .....	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	81°C/W
DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.



**SN54ABT162601, SN74ABT162601**  
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**recommended operating conditions (see Note 3)**

		SN54ABT162601		SN74ABT162601		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	A port		-24		mA
		B port		-12		
$I_{OL}$	Low-level output current	A port		48		mA
		B port		12		
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu$ s/V
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}$ C

NOTE 3: All unused inputs of the devices must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT162601		SN74ABT162601		UNIT	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA	-1.2			-1.2		-1.2		V	
V <sub>OH</sub>	A port	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5		2.5		V	
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		3			
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA	2			2					
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA	2*					2			
	B port	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA	3.35			3.3		3.35			
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -1 mA	3.85			3.8		3.85			
V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		3.1			3		3.1				
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA	2.6					2.6				
V <sub>OL</sub>	A port	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA	0.55			0.55				V	
			V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA	0.55*					0.55		
	B port	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA	0.8			0.8		0.8			
V <sub>hys</sub>			100							mV	
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	±1			±1		±1		μA	
	A or B ports	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	±20			±20		±20			
I <sub>OZPU</sub>		V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$	±50			±50**		±50		μA	
I <sub>OZPD</sub>		V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$	±50			±50**		±50		μA	
I <sub>OZH</sub> ‡		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V	10			10		10		μA	
I <sub>OZL</sub> ‡		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V	-10			-10		-10		μA	
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V	±100*					±100		μA	
I <sub>CEX</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V, Outputs high	50			50		50		μA	
I <sub>O</sub> §	A port	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA	
	B port		-25	-55	-100	-25	-100	-25	-100		
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, Outputs high	3			3		3		mA	
			V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, Outputs low	36			36		36		
			V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND, Outputs disabled	3			3		3		
ΔI <sub>CC</sub> ¶		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	50			50		50		μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V	3							pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V	9							pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



**SN54ABT162601, SN74ABT162601**  
**18-BIT UNIVERSAL BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(see Figure 1)

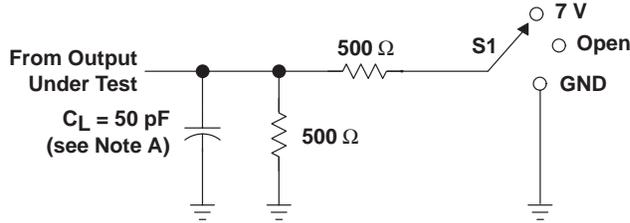
		SN54ABT162601		SN74ABT162601		UNIT
		MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency	0	150	0	150	MHz
$t_w$	Pulse duration	LEAB or LEBA high		2.5		ns
		CLKAB or CLKBA high or low		3.3		
$t_{su}$	Setup time	A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$		4.8		ns
		A before LEAB $\downarrow$ or B before LEBA $\downarrow$	CLK high	2.5		
			CLK low	1.2		
		CLKEN before CLK $\uparrow$		2.7		
$t_h$	Hold time	A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$		0.5		ns
		A after LEAB $\downarrow$ or B after LEBA $\downarrow$		2		
		CLKEN after CLK $\uparrow$		0.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT162601		SN74ABT162601		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			150			150		150		MHz
$t_{PLH}$	A	B	1.5	2.8	4	1.5	5.1	1.5	4.8	ns
$t_{PHL}$			2	3.7	5.2	2	6.1	2	5.7	
$t_{PLH}$	B	A	1	2.5	3.6	1	4.5	1	4	ns
$t_{PHL}$			2	3.3	4.5	2	5.1	2	4.9	
$t_{PLH}$	LEBA	A	2	3.3	4.5	2	5.6	2	5	ns
$t_{PHL}$			2	3.6	4.7	2	5.4	2	5	
$t_{PLH}$	LEAB	B	2	3.4	4.8	2	6.1	2	5.6	ns
$t_{PHL}$			2	3.8	5.2	2	6.4	2	5.9	
$t_{PLH}$	CLKBA	A	1.5	3.1	4.7	1.5	5.4	1.5	5.3	ns
$t_{PHL}$			1.5	3.1	4.3	1.5	5.2	1.5	5	
$t_{PLH}$	CLKAB	B	1.5	3.3	4.7	1.5	6	1.5	5.5	ns
$t_{PHL}$			1.5	3.5	4.8	1.5	5.8	1.5	5.3	
$t_{PZH}$	$\overline{OEBA}$	A	2	3.5	4.6	2	5.5	2	5.1	ns
$t_{PZL}$			2	3.7	4.7	2	5.8	2	5.4	
$t_{PZH}$	$\overline{OEAB}$	B	2	3.8	5.3	1.5	6.6	2	6.1	ns
$t_{PZL}$			2	3.6	5.1	2	6.2	2	5.7	
$t_{PHZ}$	$\overline{OEBA}$	A	2	3.6	5.4	1.4	6.6	2	6.2	ns
$t_{PLZ}$			1.5	3.2	4.7	1.5	5.8	1.5	5.4	
$t_{PHZ}$	$\overline{OEAB}$	B	2	3.4	4.8	1.4	5.6	2	5.4	ns
$t_{PLZ}$			1.5	3.2	4.5	1.5	5.7	1.5	5.2	

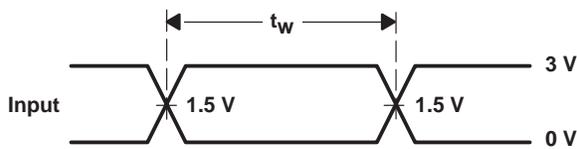


PARAMETER MEASUREMENT INFORMATION

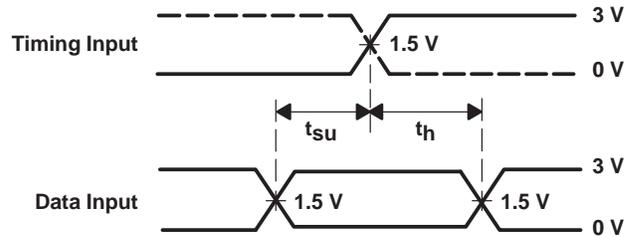


LOAD CIRCUIT

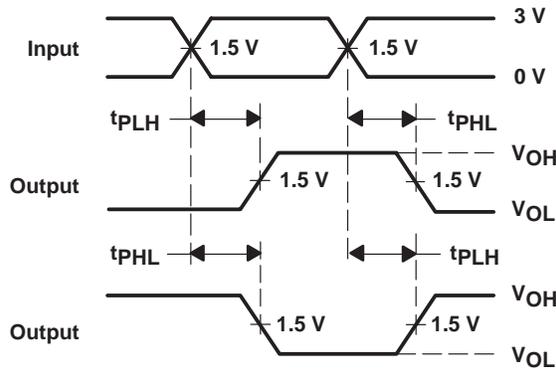
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



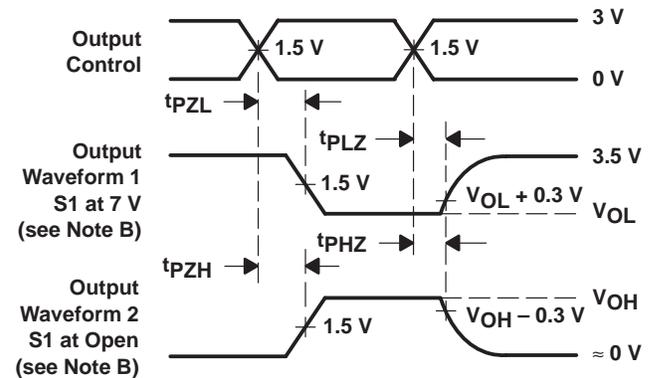
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74ABT162601DGGR</a>	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162601
SN74ABT162601DGGR.B	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162601
<a href="#">SN74ABT162601DLR</a>	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162601
SN74ABT162601DLR.B	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162601

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT162601DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ABT162601DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

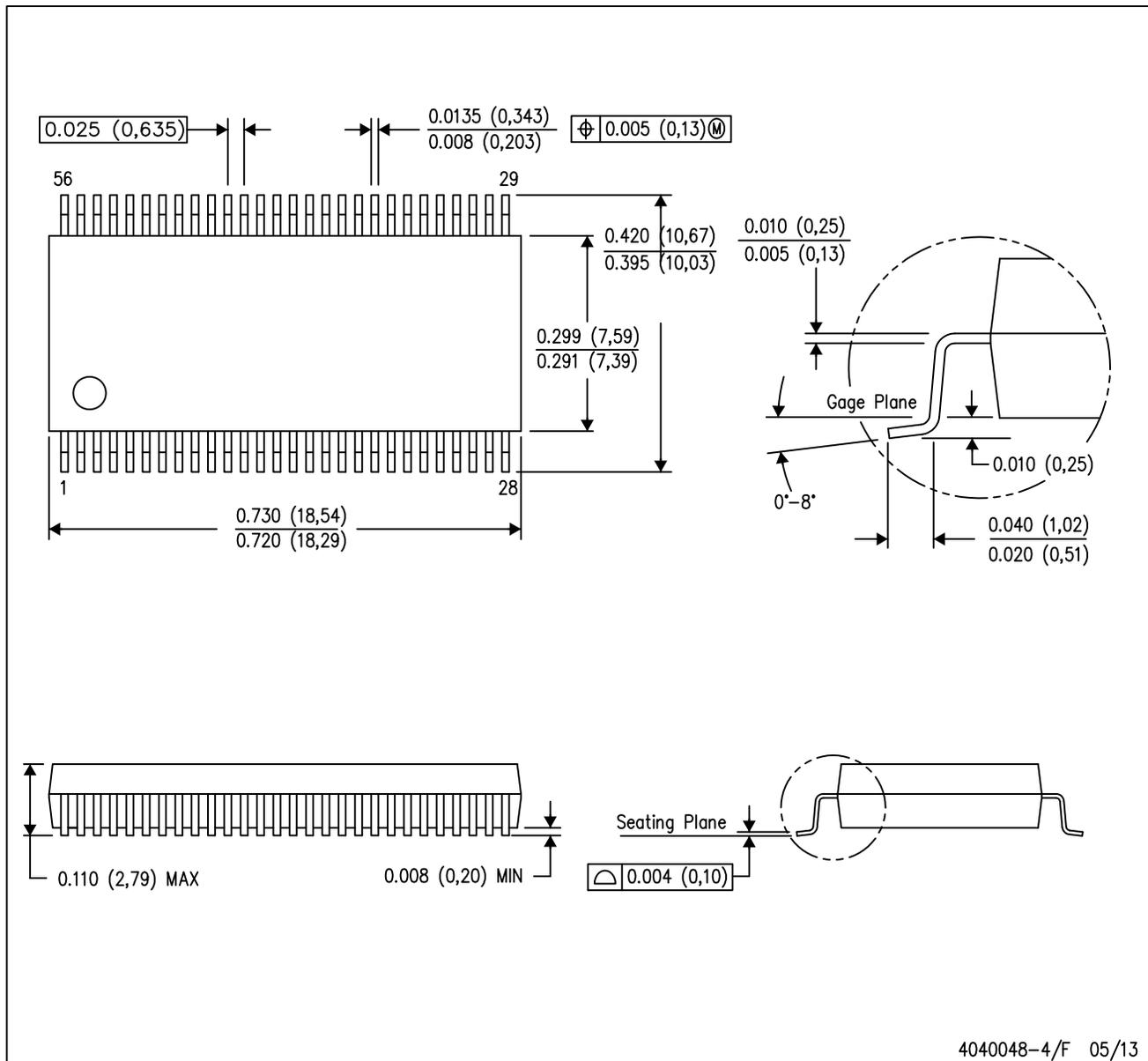

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT162601DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ABT162601DLR	SSOP	DL	56	1000	356.0	356.0	53.0

# MECHANICAL DATA

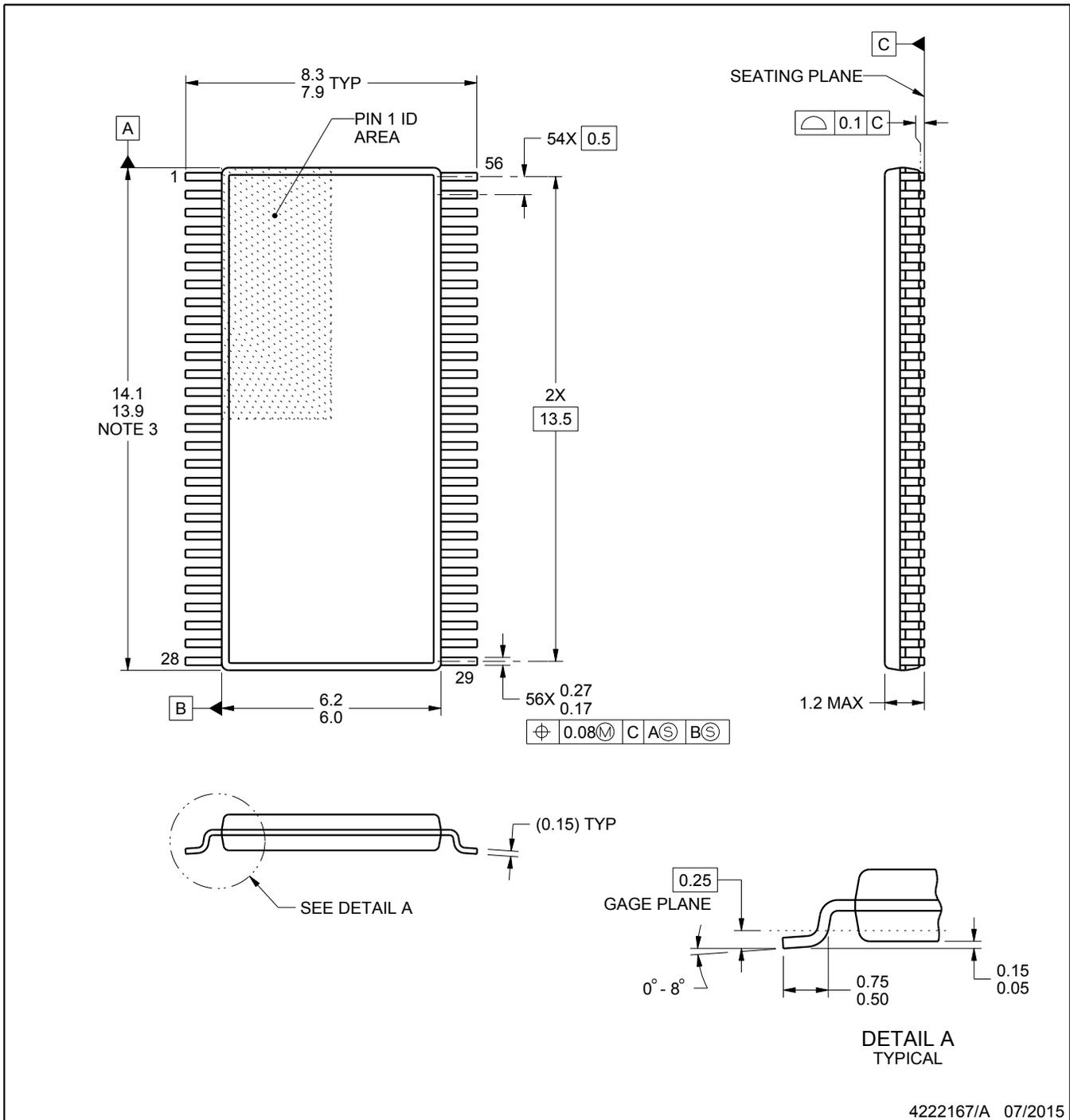
DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



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NOTES:

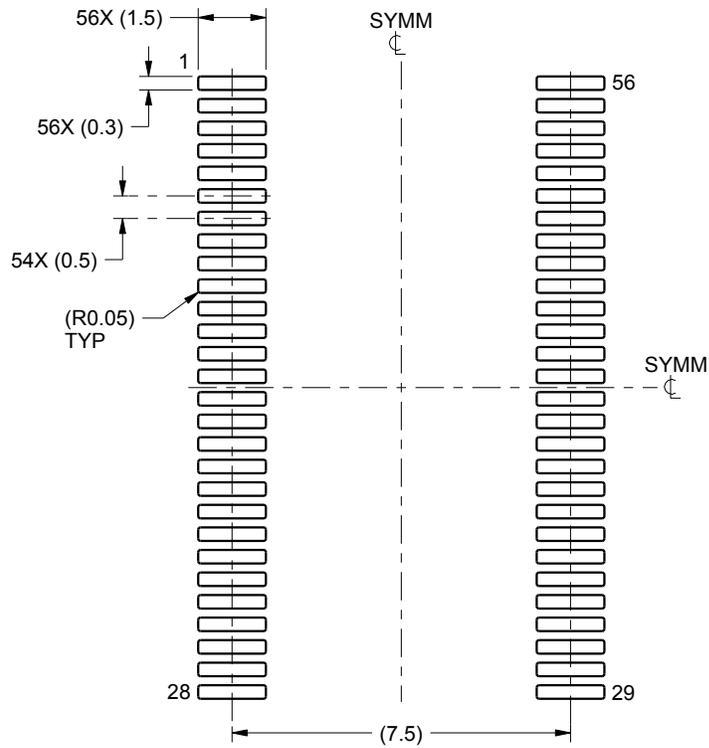
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

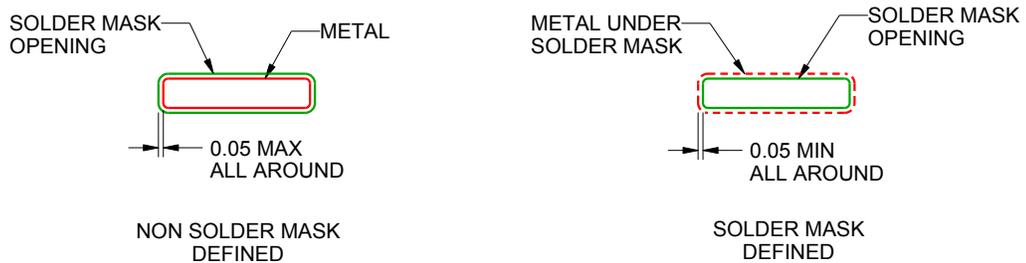
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

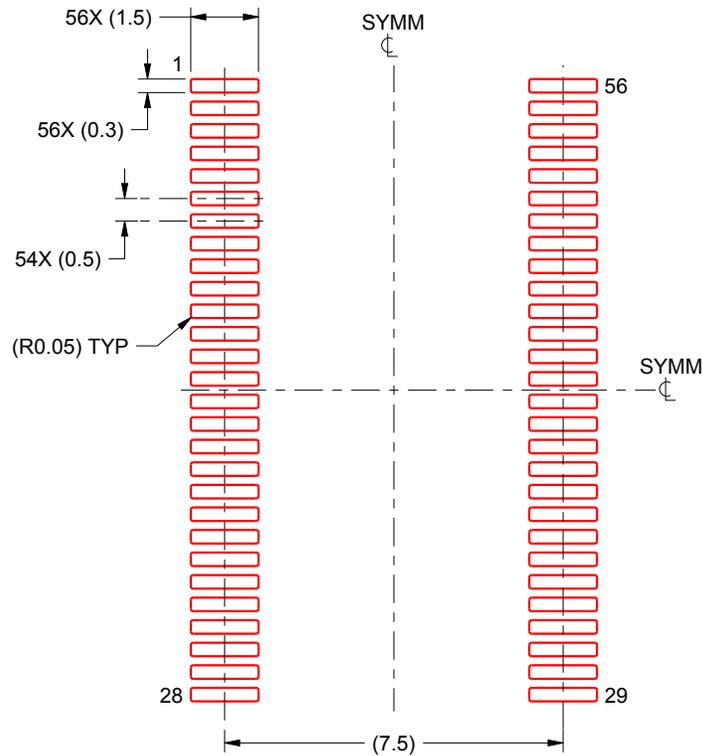
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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