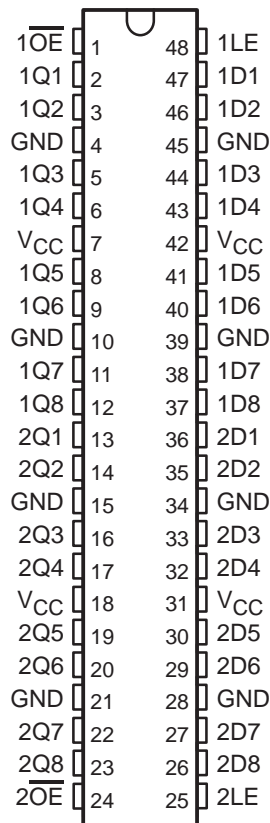


# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS160C – DECEMBER 1992 – REVISED MAY 1997

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$**
- **High-Impedance State During Power Up and Power Down**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16373A . . . WD PACKAGE  
SN74ABT16373A . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16373A are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16373A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16373A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus and EPIC-II B are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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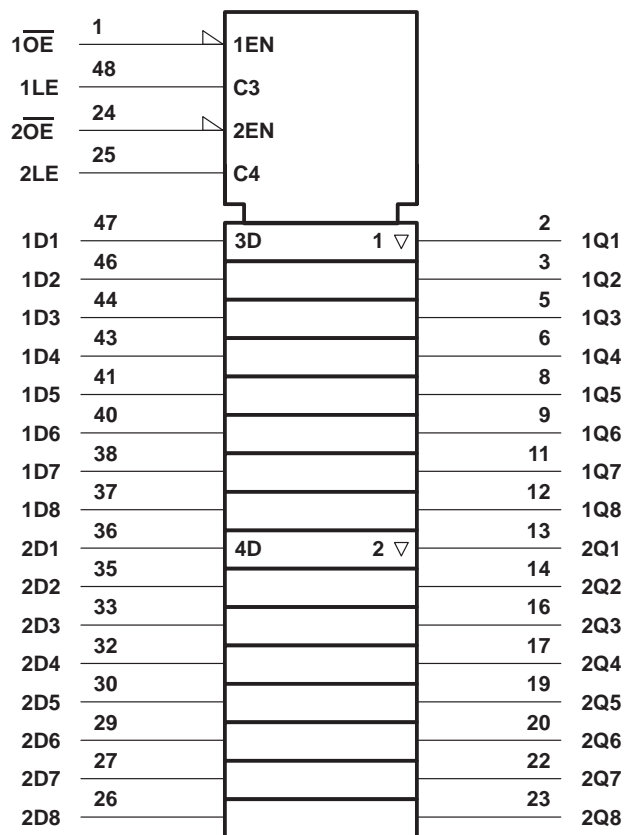
# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each 8-bit section)

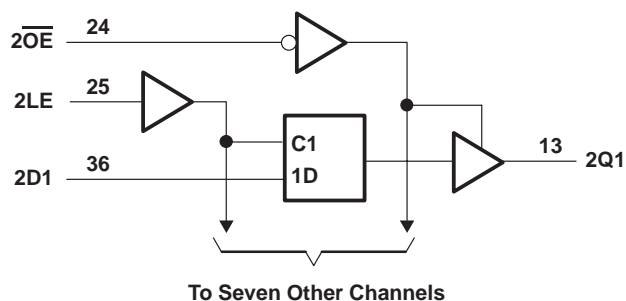
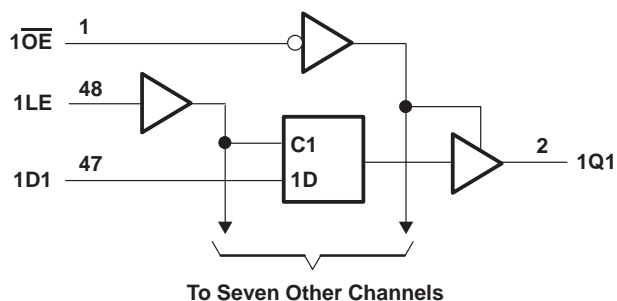
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16373A .....	96 mA
SN74ABT16373A .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	89°C/W
DL package .....	94°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

		SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
						Outputs enabled
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



# SN54ABT16373A, SN74ABT16373A

## 16-BIT TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$			2.5		2.5		2.5	V
	$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$			3		3		3	
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$			2		2		
$I_{OH} = -32\text{ mA}$				2*				2	
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$				0.55		0.55	V
		$I_{OL} = 64\text{ mA}$				0.55*		0.55	
$V_{hys}$				100					mV
$I_I$	$V_{CC} = 0\text{ to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
$I_{OZPU}^\ddagger$	$V_{CC} = 0\text{ to }2.1\text{ V}$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$		$\pm 50$		$\pm 50$	$\mu\text{A}$
$I_{OZPD}^\ddagger$	$V_{CC} = 2.1\text{ V to }0$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$		$\pm 50$		$\pm 50$	$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 2.7\text{ V}$ , $\overline{OE} \geq 2\text{ V}$			10		10		10	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 0.5\text{ V}$ , $\overline{OE} \geq 2\text{ V}$			-10		-10		-10	$\mu\text{A}$
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O \leq 4.5\text{ V}$			$\pm 100$				$\pm 100$	$\mu\text{A}$
$I_{CEX}$	Outputs high $V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$			50		50		50	$\mu\text{A}$
$I_{O}^\S$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-180	-50	-180	mA
$I_{CC}$	Outputs high			2		2		2	mA
	Outputs low	$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ ,		85		85		85	
	Outputs disabled	$V_I = V_{CC}\text{ or GND}$		2		2		2	
$\Delta I_{CC}^\parallel$	$V_{CC} = 5.5\text{ V}$ , One input at $3.4\text{ V}$ , Other inputs at $V_{CC}$ or GND			1.5		1.5		1.5	mA
$C_i$	$V_I = 2.5\text{ V or }0.5\text{ V}$			3.5					pF
$C_o$	$V_O = 2.5\text{ V or }0.5\text{ V}$			9.5					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}^\#$		SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	3.3		3.3		3.3		ns
$t_{su}$	Setup time, data before LE↓	1.5		2.4		1.5		ns
$t_h$	Hold time, data after LE↓	1		2.2		1		ns

# These values apply only to the SN74ABT16373A.



**SN54ABT16373A, SN74ABT16373A**  
**16-BIT TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16373A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
$t_{PLH}$	D	Q	1.4	3.7	5.3	1.4	6.5	ns
$t_{PHL}$			2	4	5.4	2	6.5	
$t_{PLH}$	LE	Q	1.7	4.1	5.7	1.7	7	ns
$t_{PHL}$			2.3	4.3	5.6	2.3	6.3	
$t_{PZH}$	$\overline{OE}$	Q	1.1	3.4	5	1.1	6.4	ns
$t_{PZL}$			1.5	3.5	4.9	1.5	5.8	
$t_{PHZ}$	$\overline{OE}$	Q	2.4	5.1	7.1	2.4	8.3	ns
$t_{PLZ}$			1.6	4.4	6.3	1.6	8	

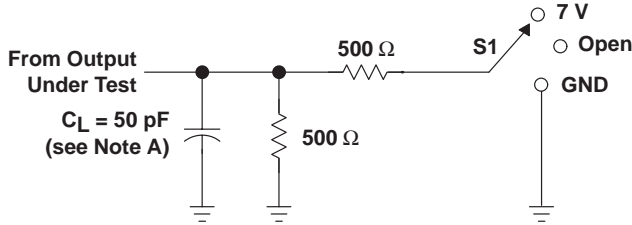
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16373A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
$t_{PLH}$	D	Q	1.4	3.7	5.3	1.4	6.3	ns
$t_{PHL}$			2	4	5.4	2	6.2	
$t_{PLH}$	LE	Q	1.7	4.1	5.7	1.7	6.7	ns
$t_{PHL}$			2.3	4.3	5.6	2.3	6.1	
$t_{PZH}$	$\overline{OE}$	Q	1.1	3.4	5	1.1	6.1	ns
$t_{PZL}$			1.5	3.5	4.9	1.5	5.6	
$t_{PHZ}$	$\overline{OE}$	Q	2.4	5.1	7.1	2.4	8.1	ns
$t_{PLZ}$			1.6	4.4	5.8	1.6	6.5	

# SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION

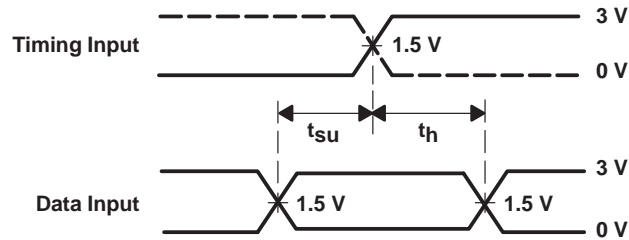


LOAD CIRCUIT

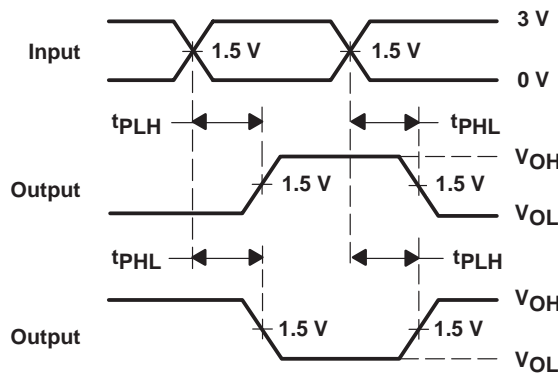
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



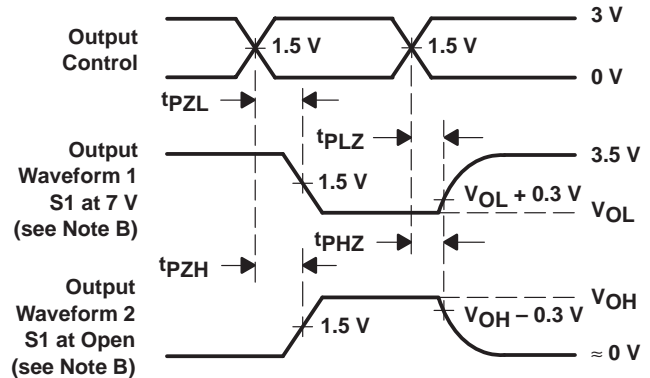
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9320001QXA</a>	Active	Production	CFP (WD)   48	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9320001QX A SNJ54ABT16373A WD
74ABT16373ADGGRE4	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
74ABT16373ADGGRG4	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
<a href="#">SN74ABT16373ADGGR</a>	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADGGR.B	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
<a href="#">SN74ABT16373ADL</a>	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADL.B	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADLG4.B	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
<a href="#">SN74ABT16373ADLR</a>	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADLR.B	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
SN74ABT16373ADLRG4	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16373A
<a href="#">SNJ54ABT16373AWD</a>	Active	Production	CFP (WD)   48	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9320001QX A SNJ54ABT16373A WD

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ABT16373A, SN74ABT16373A :**

- Catalog : [SN74ABT16373A](#)
- Enhanced Product : [SN74ABT16373A-EP](#), [SN74ABT16373A-EP](#)
- Military : [SN54ABT16373A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16373ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABT16373ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16373ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABT16373ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16373ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ABT16373ADL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ABT16373ADLG4.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

# MECHANICAL DATA

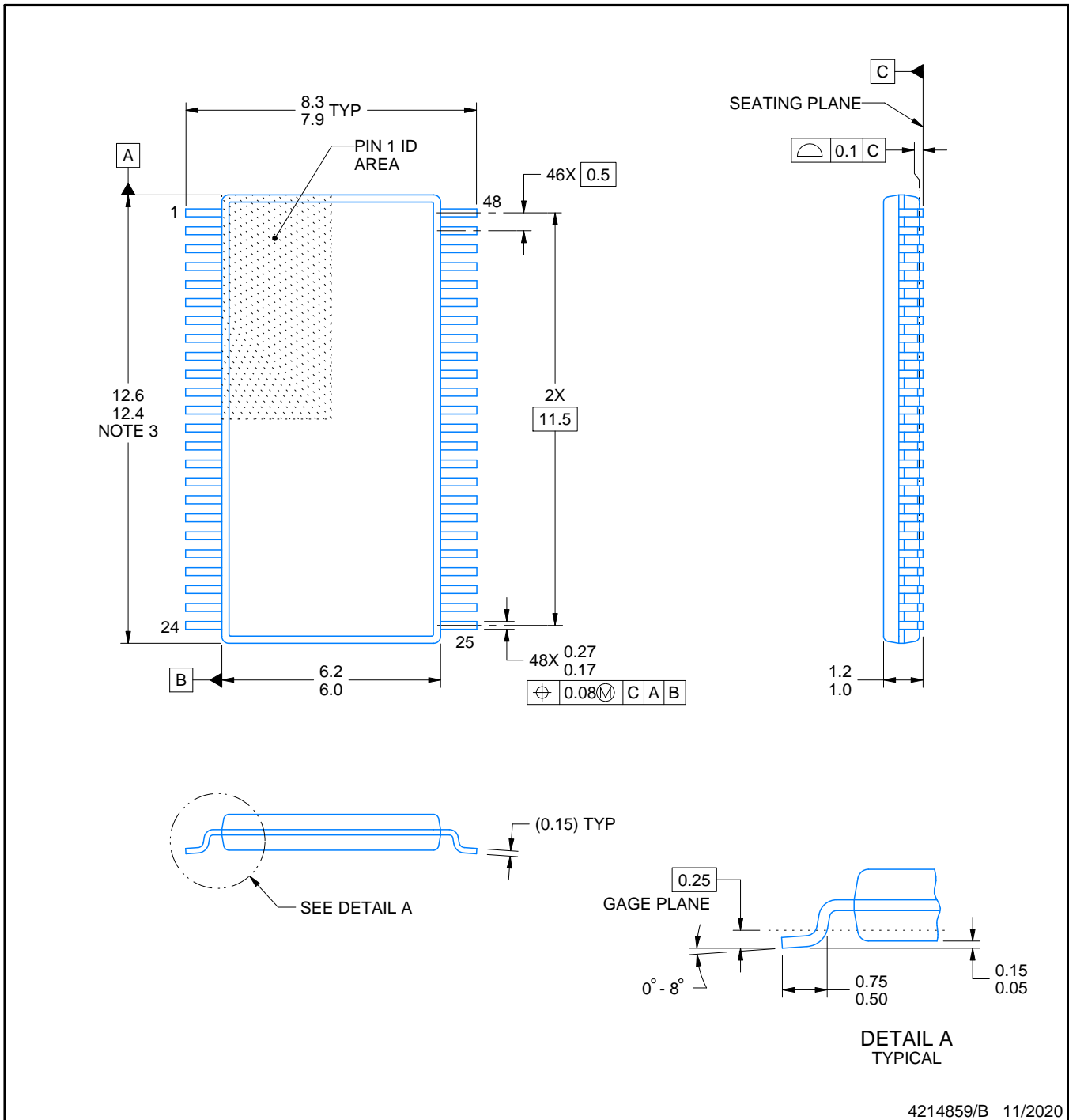
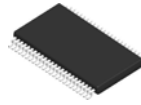
DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



4214859/B 11/2020

NOTES:

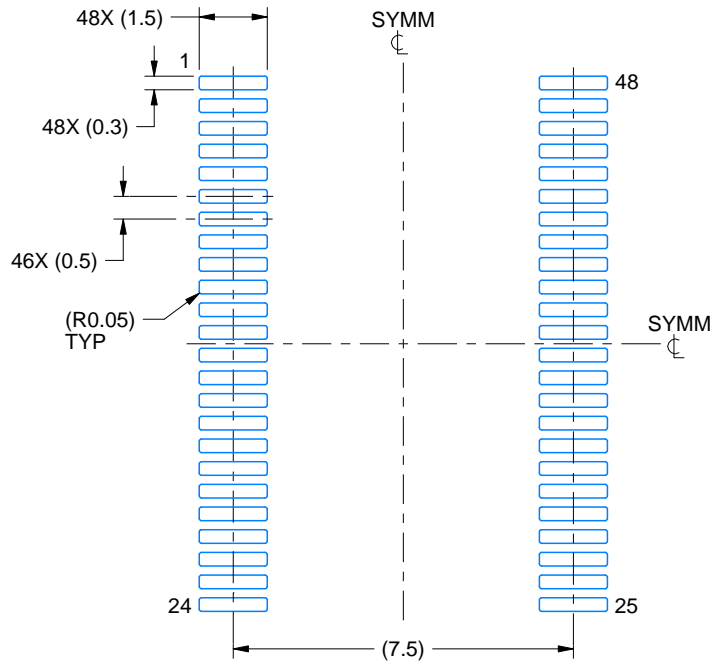
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

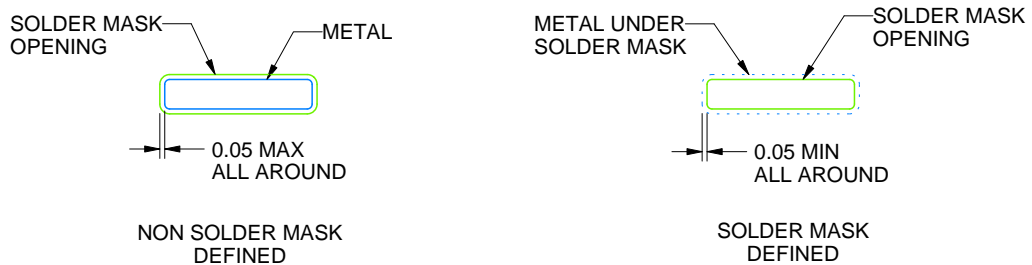
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

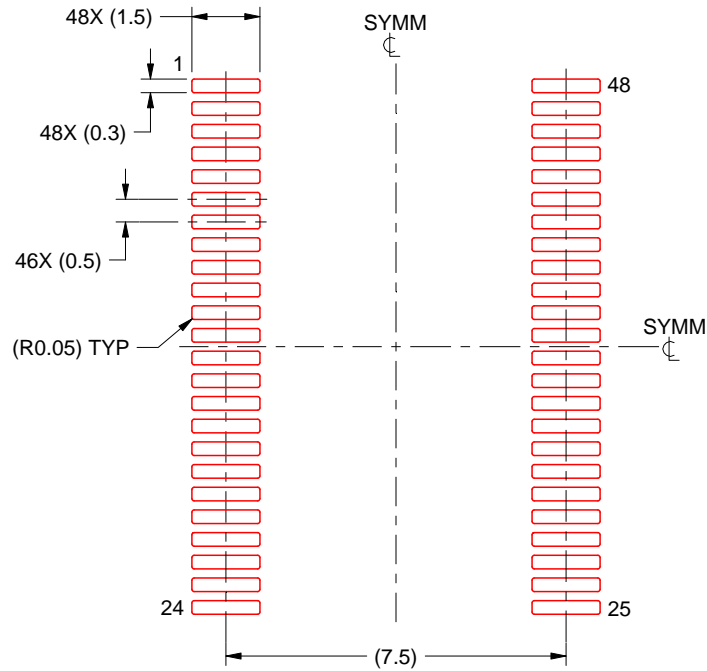
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



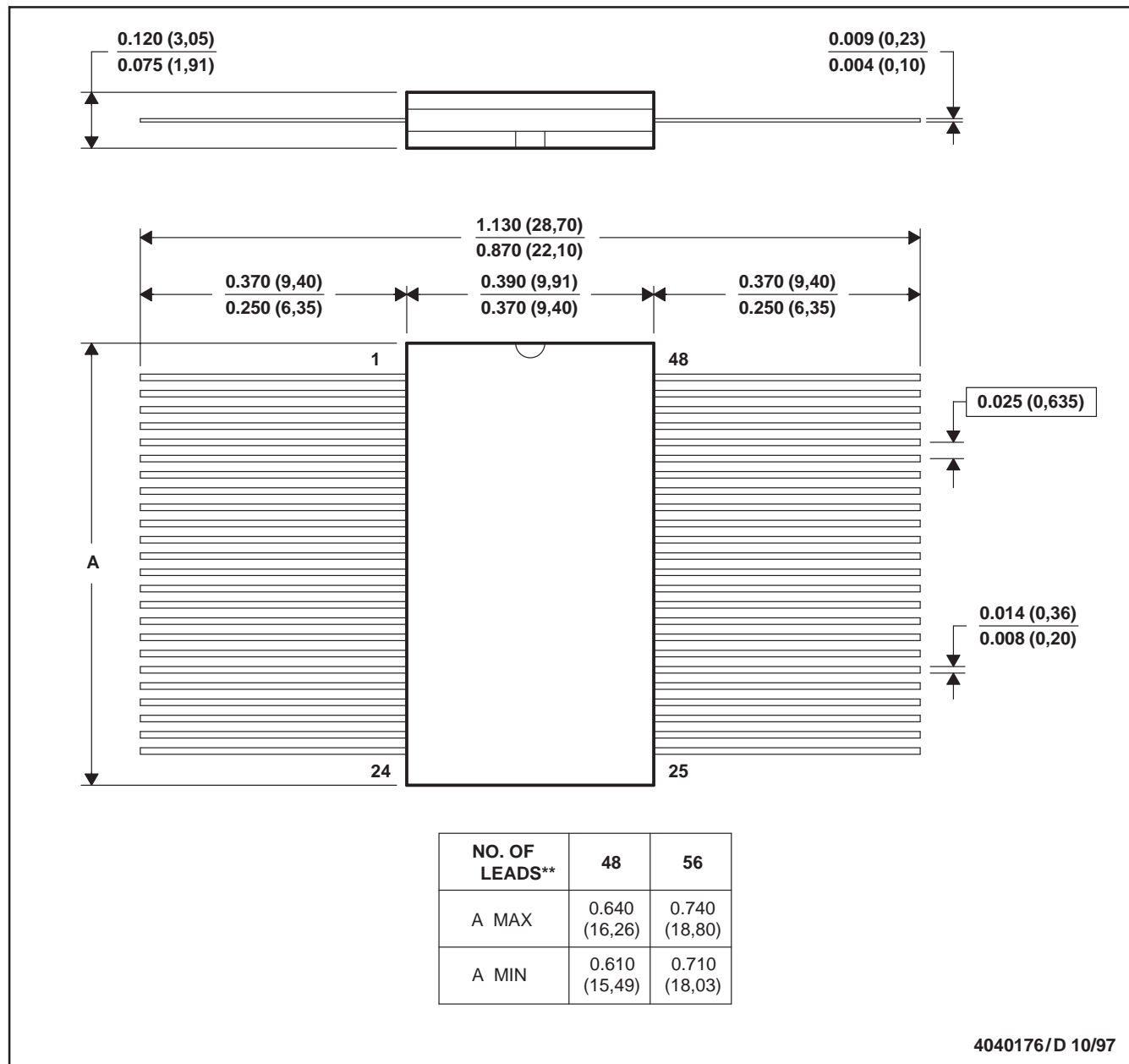
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

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