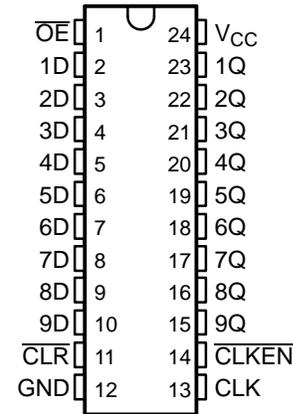


## FEATURES

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 7.9 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

This 9-bit bus-interface flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC823A is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

With the clock-enable ( $\overline{\text{CLKEN}}$ ) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high disables the clock buffer, latching the outputs. This device has noninverting data (D) inputs. Taking the clear ( $\overline{\text{CLR}}$ ) input low causes the nine Q outputs to go low, independently of the clock.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube of 25	SN74LVC823ADW	LVC823A
		Reel of 2000	SN74LVC823ADWR	
	SOP – NS	Reel of 2000	SN74LVC823ANSR	LVC823A
	SSOP – DB	Reel of 2000	SN74LVC823ADBR	LC823A
	TSSOP – PW	Tube of 60	SN74LVC823APW	LC823A
		Reel of 2000	SN74LVC823APWR	
		Reel of 250	SN74LVC823APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC823ADGVR	LC823A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**SN74LVC823A**  
**9-BIT BUS-INTERFACE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCAS305I—MARCH 1993—REVISED FEBRUARY 2005

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or the high-impedance state.  $\overline{OE}$  does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

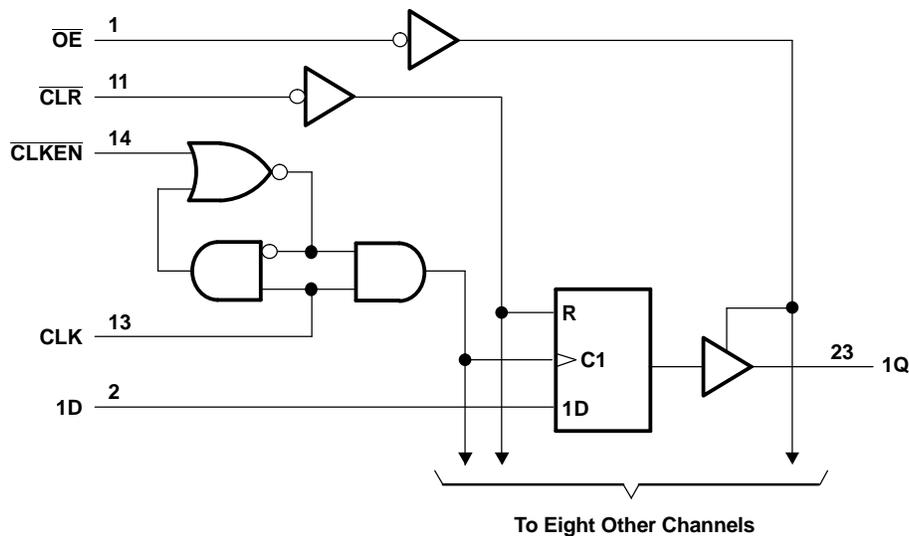
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**FUNCTION TABLE**  
**(EACH FLIP-FLOP)**

INPUTS					OUTPUT Q
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DB package	63	°C/W
		DGV package	86	
		DW package	46	
		NS package	65	
		PW package	88	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		0.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	
$V_I$	Input voltage	0	5.5	V	
$V_O$	Output voltage	High or low state	0	$V_{CC}$	V
		3-state	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 1.65\text{ V}$		-4	mA
		$V_{CC} = 2.3\text{ V}$		-8	
		$V_{CC} = 2.7\text{ V}$		-12	
		$V_{CC} = 3\text{ V}$		-24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
		$V_{CC} = 2.3\text{ V}$		8	
		$V_{CC} = 2.7\text{ V}$		12	
		$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C	

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LVC823A

## 9-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS305I—MARCH 1993—REVISED FEBRUARY 2005

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V
		I <sub>OH</sub> = -4 mA	1.65 V	1.2			
		I <sub>OH</sub> = -8 mA	2.3 V	1.7			
		I <sub>OH</sub> = -12 mA	2.7 V	2.2			
			3 V	2.4			
	I <sub>OH</sub> = -24 mA	3 V	2.2				
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		I <sub>OL</sub> = 8 mA	2.3 V			0.7	
		I <sub>OL</sub> = 12 mA	2.7 V			0.4	
		I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>		V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μA
I <sub>OZ</sub>		V <sub>O</sub> = 0 to 5.5 V	3.6 V			±10	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	I <sub>O</sub> = 0		10	μA
		3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>				10	
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			5	pF
	Data inputs					4	
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			7	pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This applies in the disabled state only.

### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	(1)		(1)		150		150		MHz
t <sub>w</sub>	Pulse duration	CLR low		(1)		3.3		3.3		ns
		CLK high or low		(1)		3.3		3.3		
t <sub>su</sub>	Setup time	CLR inactive before CLK↑		(1)		1		1		ns
		Data before CLK↑		(1)		1.3		1.3		
		CLKEN low before CLK↑		(1)		1.8		1.8		
t <sub>h</sub>	Hold time	Data after CLK↑		(1)		2		2		ns
		CLKEN low after CLK↑		(1)		1.3		1.3		

(1) This information was not available at the time of publication.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			(1)	(1)	(1)	(1)	150		150		MHz
$t_{pd}$	CLK	Q	(1)	(1)	(1)	(1)	8.9		1.4	8	ns
	$\overline{\text{CLR}}$		(1)	(1)	(1)	(1)	8.8	2.5	7.9		
$t_{en}$	$\overline{\text{OE}}$	Q	(1)	(1)	(1)	(1)	8.3		1.6	7.2	ns
$t_{dis}$	$\overline{\text{OE}}$	Q	(1)	(1)	(1)	(1)	7.1		1.1	6	ns
$t_{sk(o)}$									1		ns

(1) This information was not available at the time of publication.

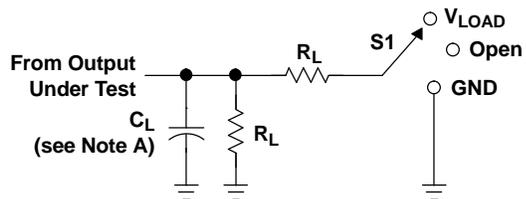
## Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance per flip-flop	Outputs enabled	(1)	(1)	59	pF
		Outputs disabled	(1)	(1)	46	

(1) This information was not available at the time of publication.

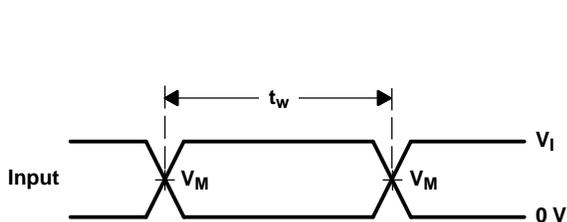
PARAMETER MEASUREMENT INFORMATION



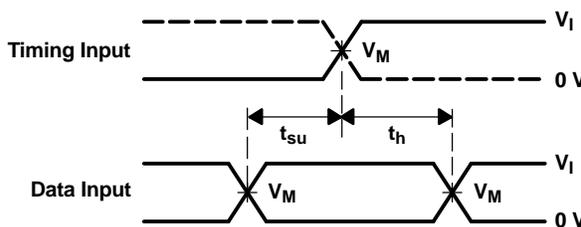
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

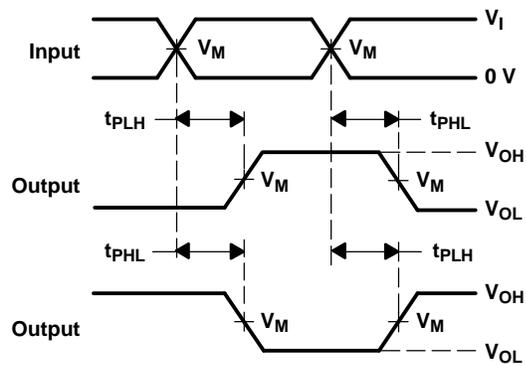
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



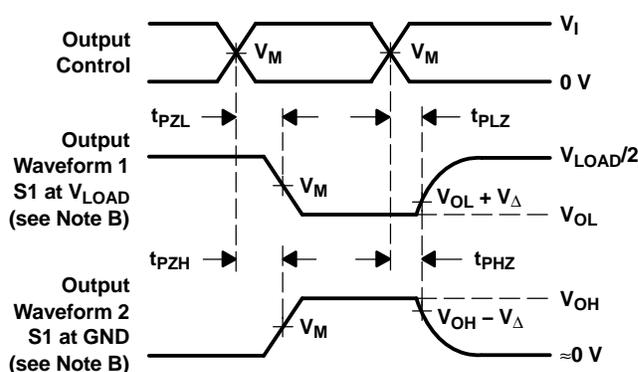
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LVC823ADBR</a>	Active	Production	SSOP (DB)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
SN74LVC823ADBR.B	Active	Production	SSOP (DB)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
<a href="#">SN74LVC823ADGVR</a>	Active	Production	TVSOP (DGV)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
SN74LVC823ADGVR.B	Active	Production	TVSOP (DGV)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
<a href="#">SN74LVC823ADW</a>	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC823A
SN74LVC823ADW.B	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC823A
<a href="#">SN74LVC823APW</a>	Active	Production	TSSOP (PW)   24	60   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
SN74LVC823APW.B	Active	Production	TSSOP (PW)   24	60   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
<a href="#">SN74LVC823APWR</a>	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
SN74LVC823APWR.B	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
SN74LVC823APWRG4	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
SN74LVC823APWRG4.B	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
<a href="#">SN74LVC823APWT</a>	Active	Production	TSSOP (PW)   24	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A
SN74LVC823APWT.B	Active	Production	TSSOP (PW)   24	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC823A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

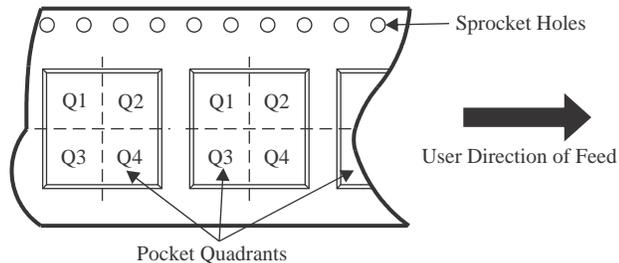
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC823ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC823ADGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC823APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC823APWRG4	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC823APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC823ADBR	SSOP	DB	24	2000	356.0	356.0	35.0
SN74LVC823ADGVR	TVSOP	DGV	24	2000	356.0	356.0	35.0
SN74LVC823APWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVC823APWRG4	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVC823APWT	TSSOP	PW	24	250	356.0	356.0	35.0

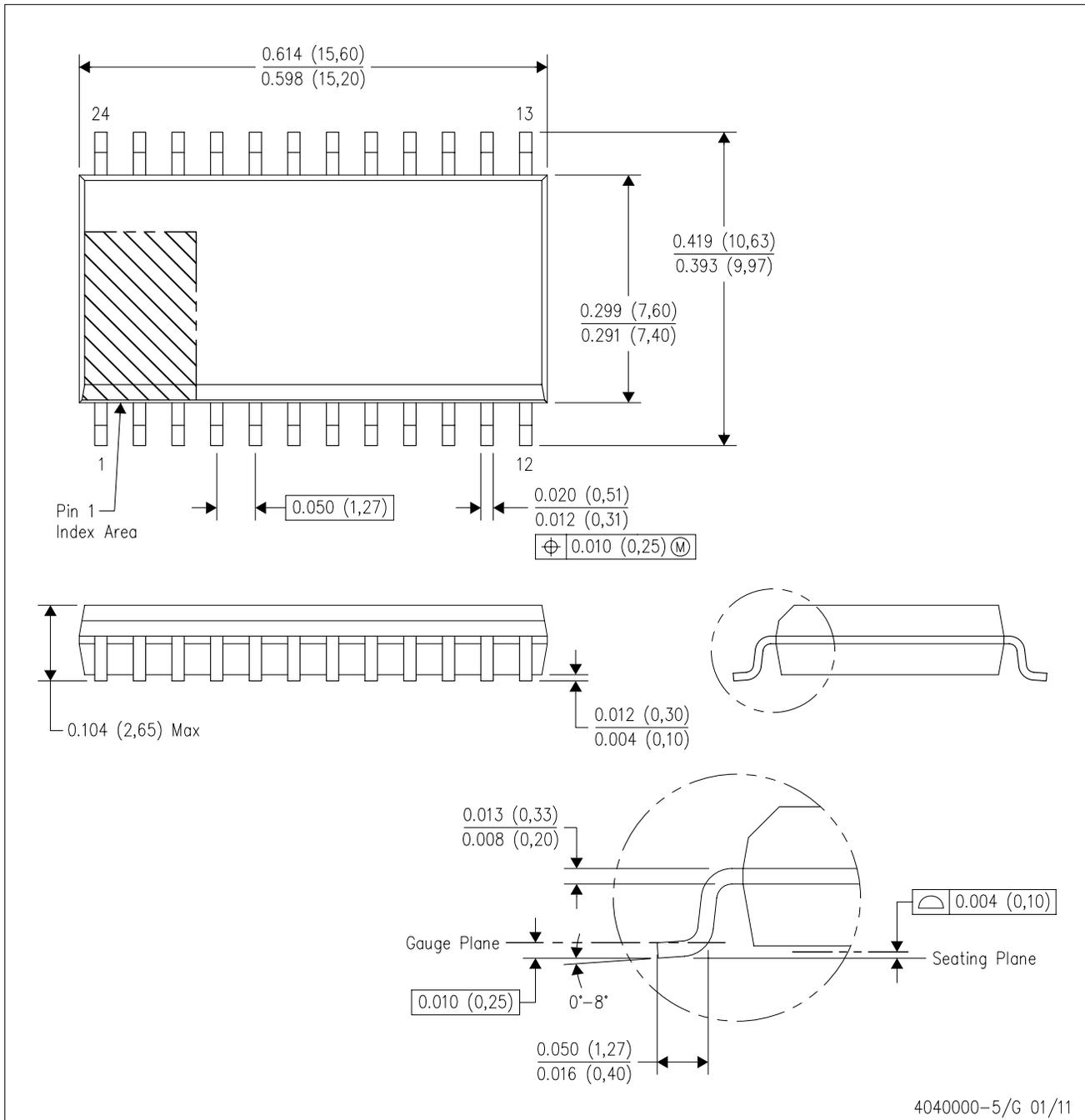
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVC823ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC823ADW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC823APW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC823APW.B	PW	TSSOP	24	60	530	10.2	3600	3.5

DW (R-PDSO-G24)

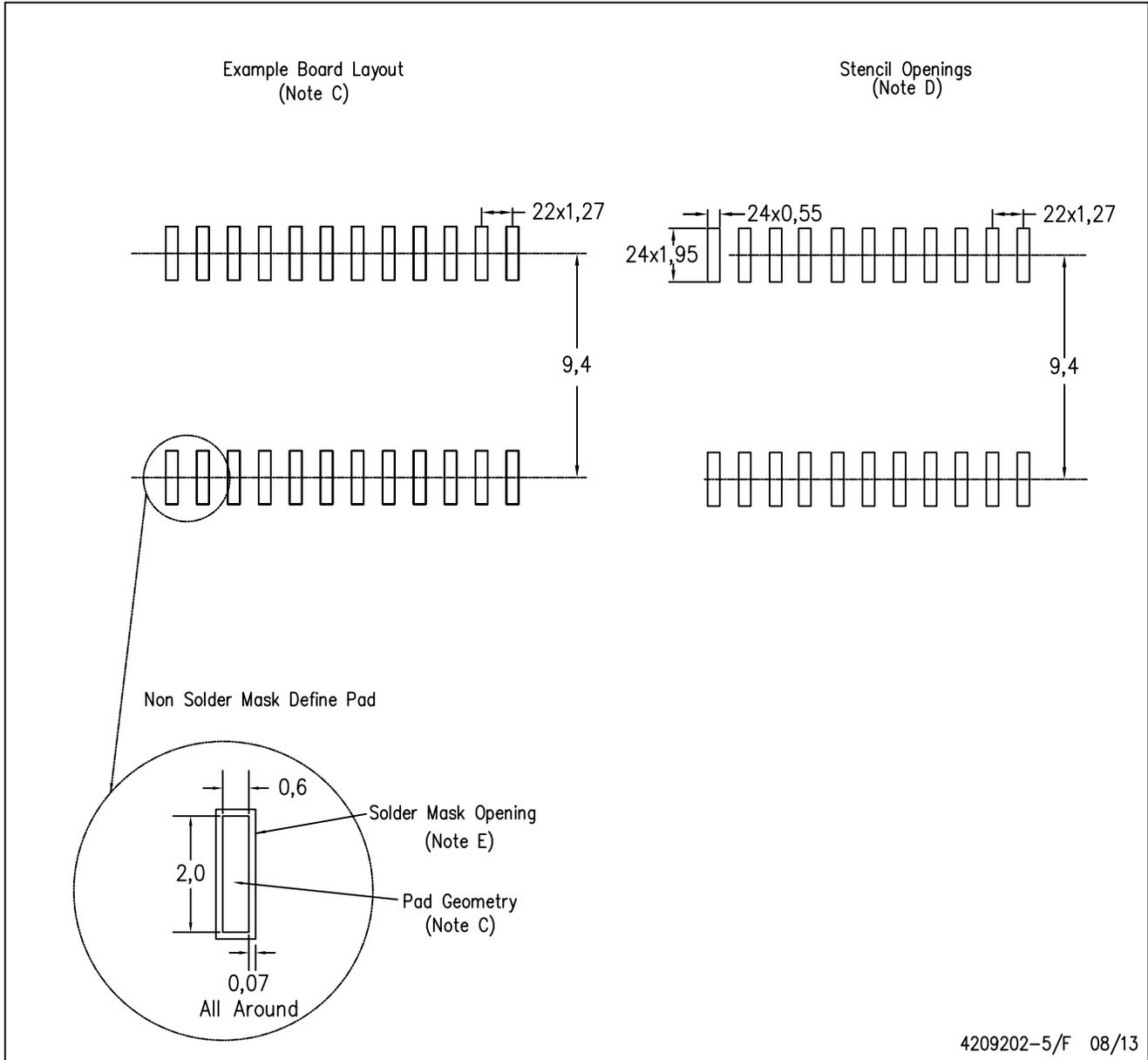
PLASTIC SMALL OUTLINE



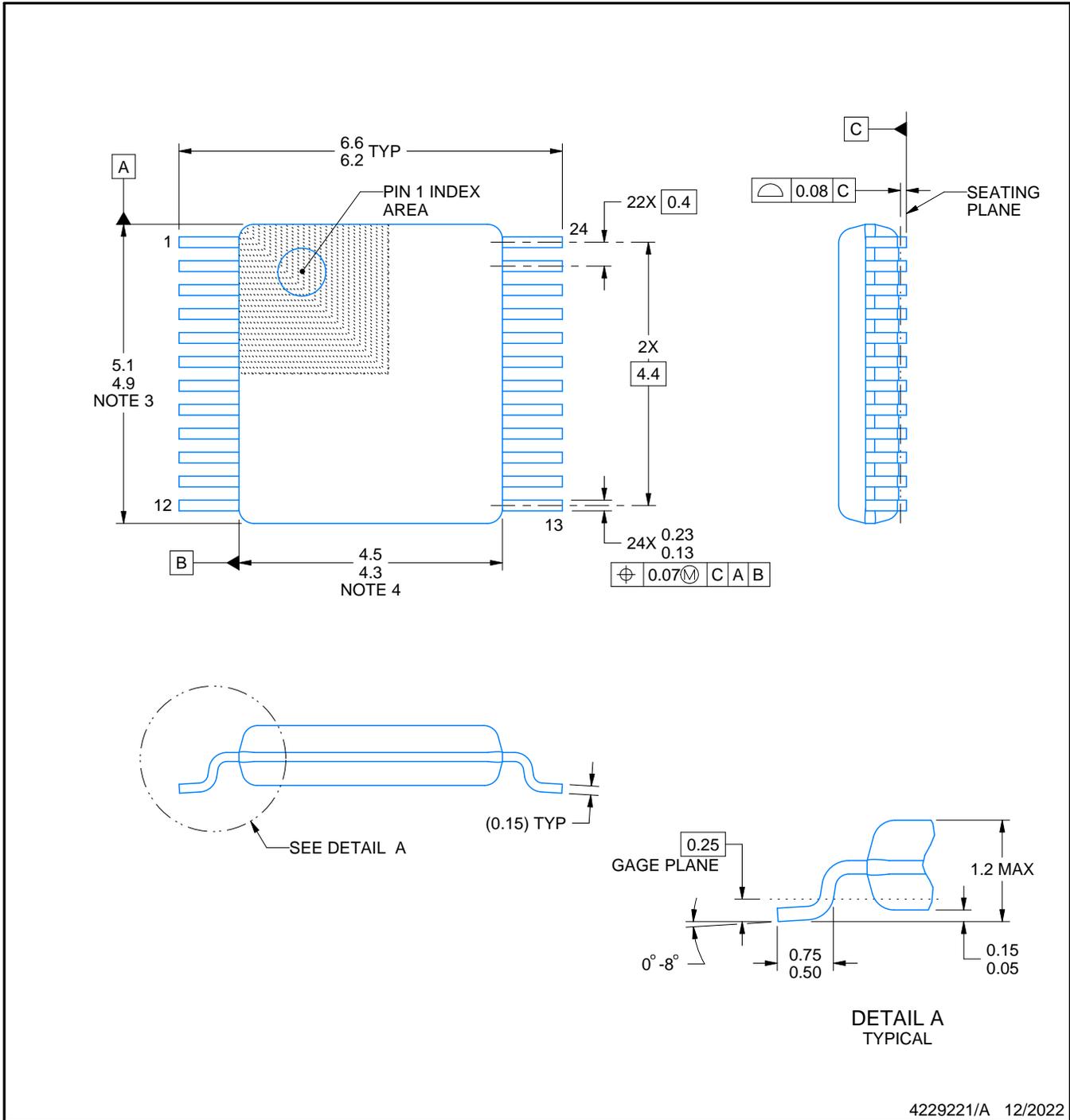
- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4229221/A 12/2022

NOTES:

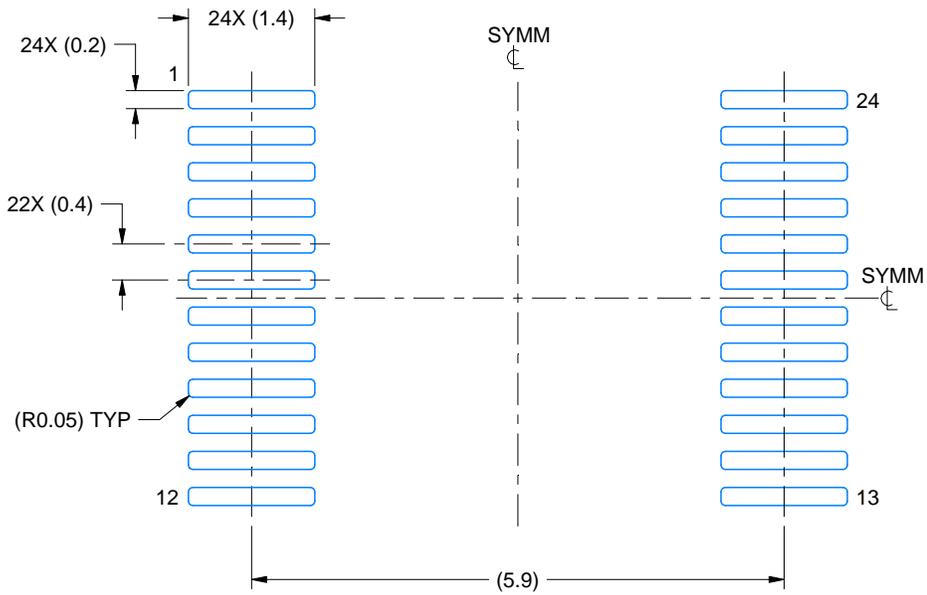
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

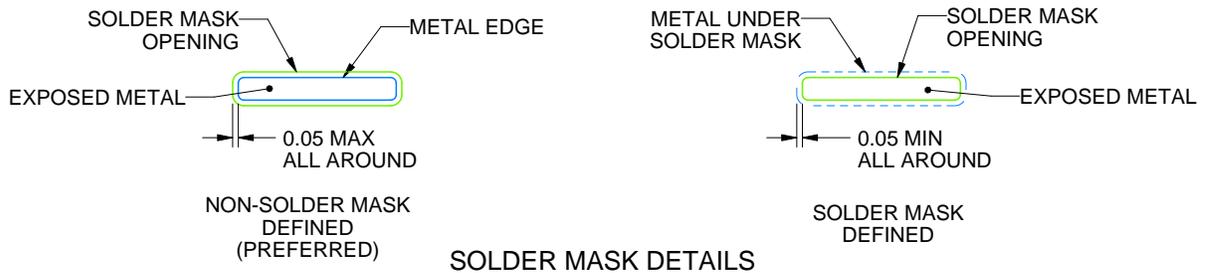
DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 12X



SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

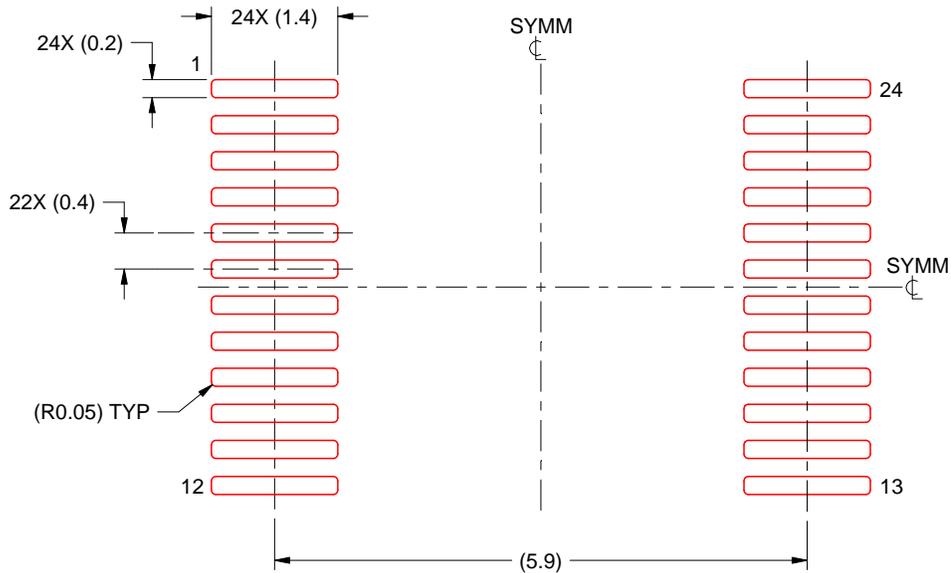
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 12X

4229221/A 12/2022

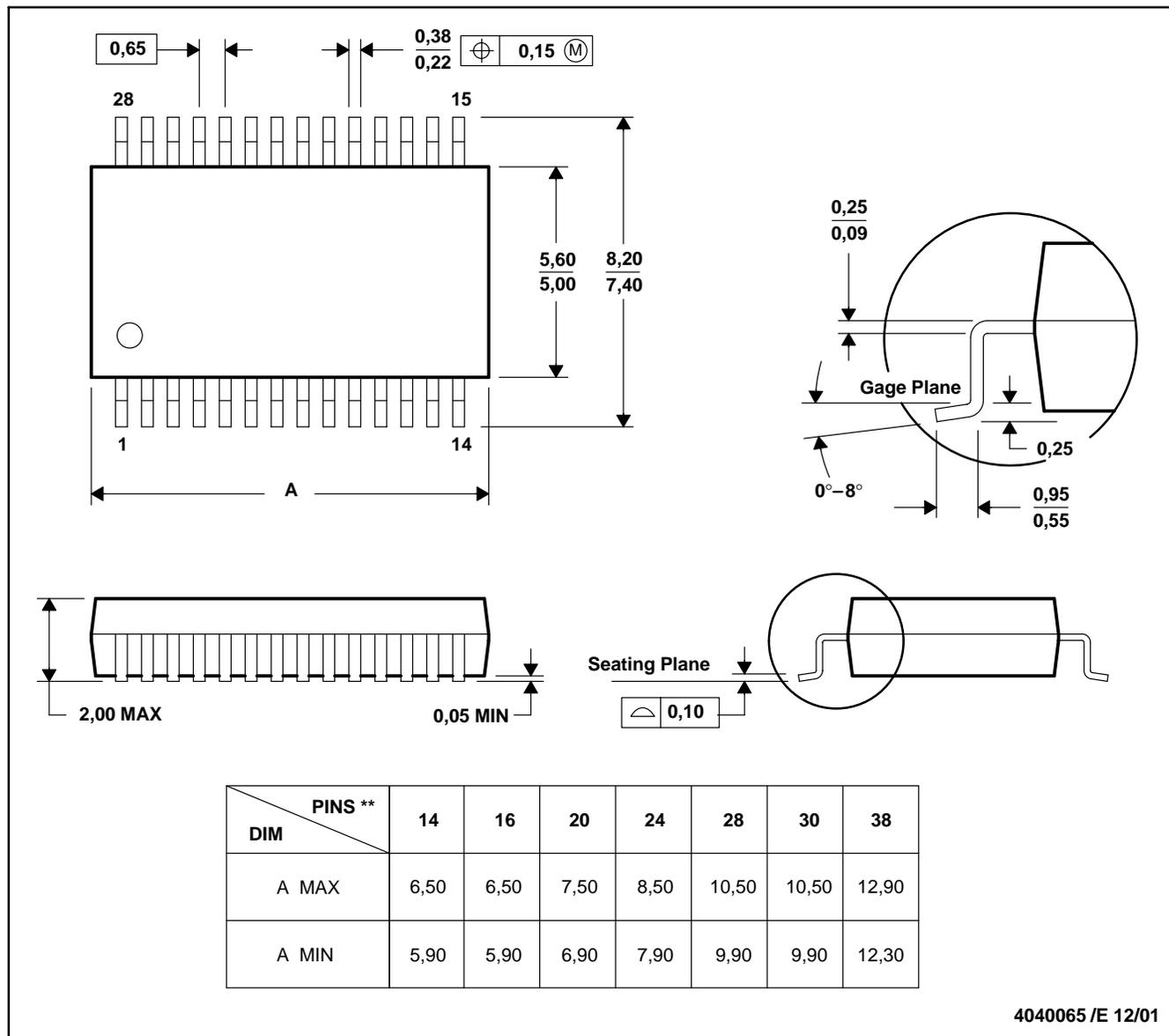
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



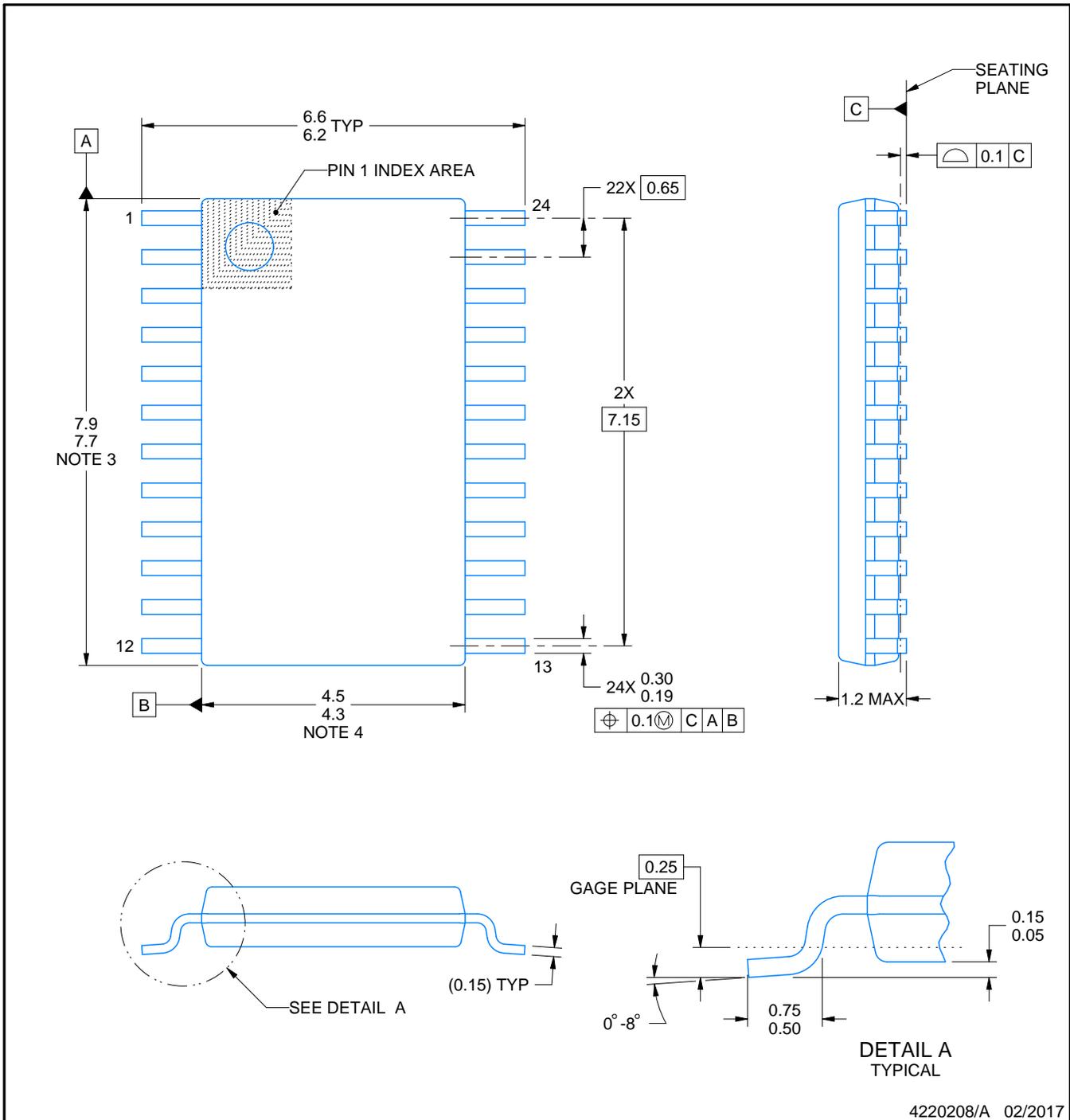
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW0024A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

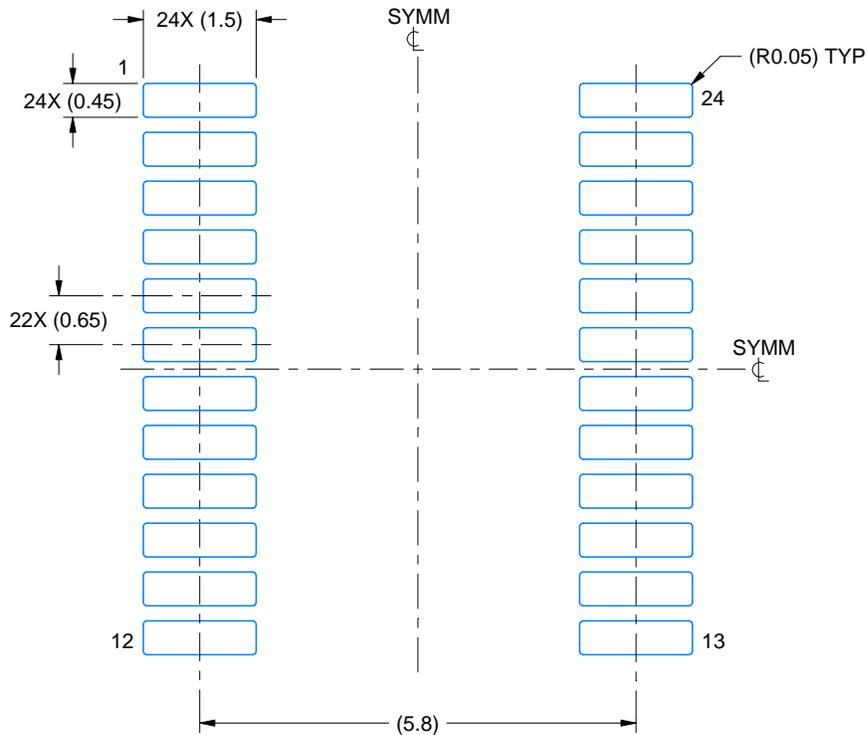
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

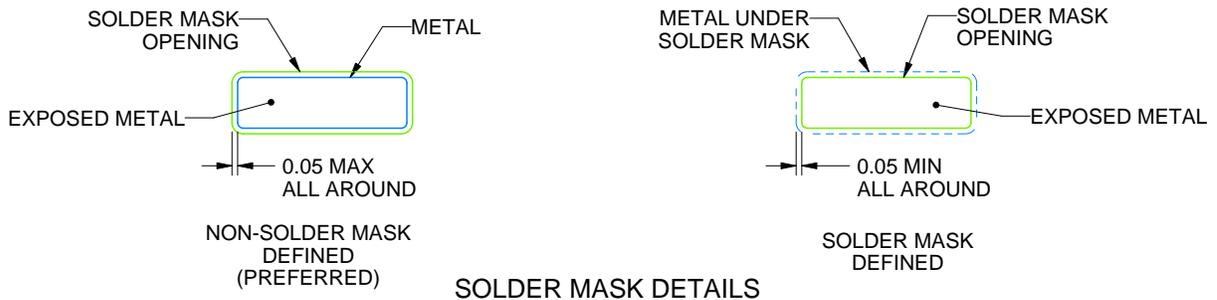
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

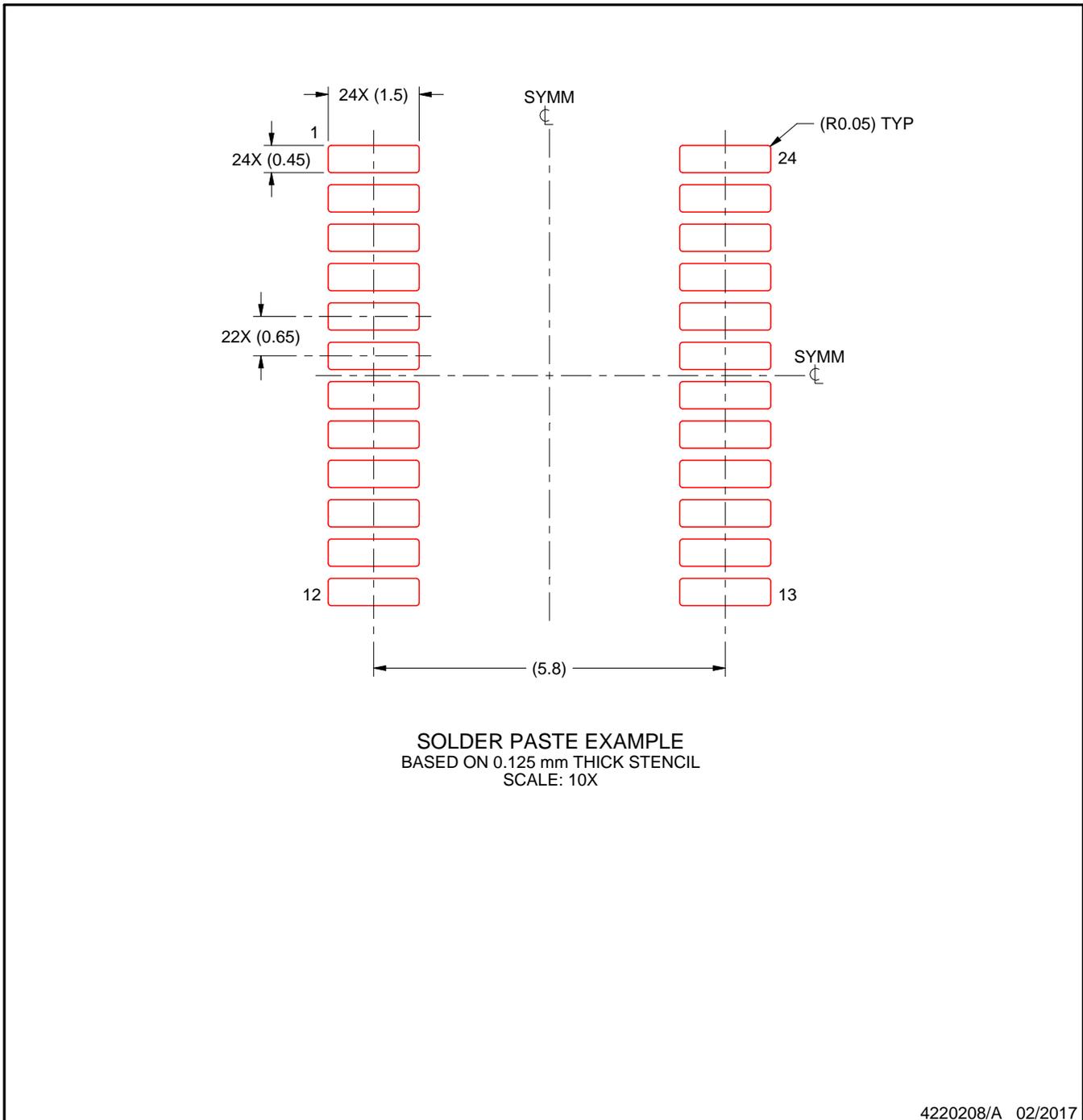
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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