TEXAS INSTRUMENTS

SN74HCS574-Q1
SCLS860A – NOVEMBER 2021 – REVISED FEBRUARY 2022

SN74HCS574-Q1 Automotive Octal D-Type Flip-Flops with Schmitt-Trigger Inputs, 3-State Outputs, and Flow-Through Pinout

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: −40°C to +125°C, T_A
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classifcation Level C6
- Available in wettable flank QFN (WRKS) package
- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{CC} of 100 nA
  - Typical input leakage current of ±100 nA
- ±7.8-mA output drive at 6 V

2 Applications

- Parallel data synchronization
- Parallel data storage
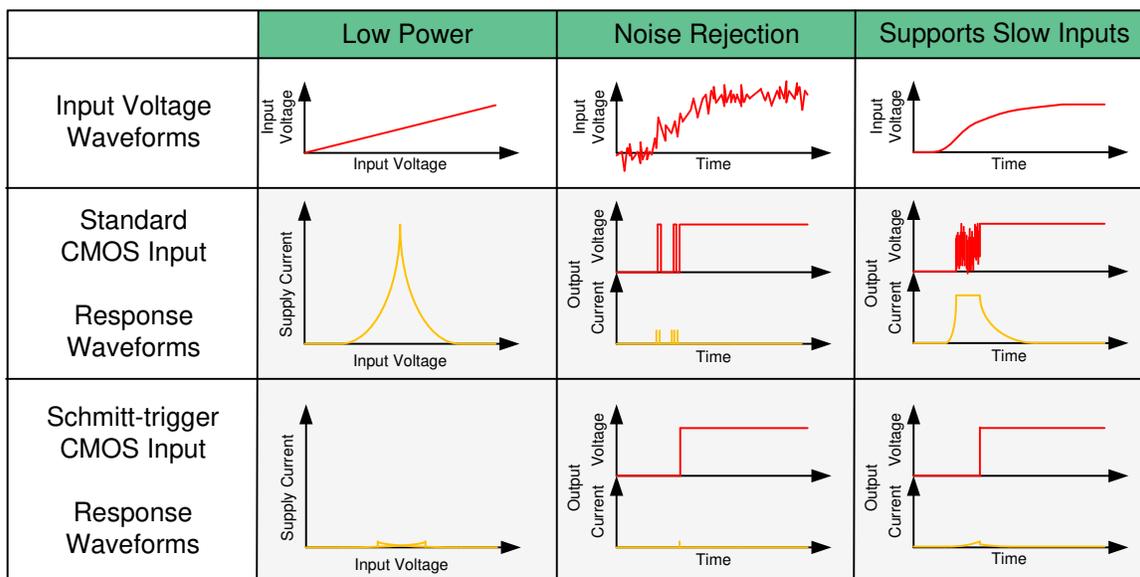- Shift register
- Pattern generators

3 Description

The SN74HCS574-Q1 contains eight D-type flip-flops. All inputs include Schmitt-trigger architecture. All channels share a rising edge triggered clock (CLK) input and active low output enable ($\overline{OE}$) input. This device has a flow-through pinout which allows for easier bus routing.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
SN74HCS574PW-Q1	TSSOP (20)	6.50 mm × 4.40 mm
SN74HCS574WRKS-Q1	VQFN (20)	4.50 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

	Low Power	Noise Rejection	Supports Slow Inputs
Input Voltage Waveforms			
Standard CMOS Input Response Waveforms			
Schmitt-trigger CMOS Input Response Waveforms			

Benefits of Schmitt-trigger inputs

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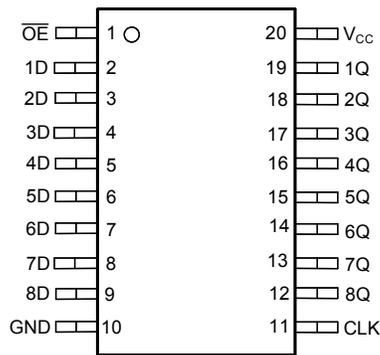
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

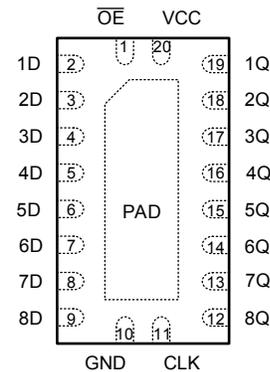| Changes from Revision * (November 2021) to Revision A (February 2022)	Page
• Changed data sheet from Advanced Information to Production Data.. 1	

5 Pin Configuration and Functions

**PW Package
20-Pin TSSOP
Top View**

**WRKS package
20-Pin VQFN
Top View**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OE	1	Input	Output enable for all channels, active low
1D	2	Input	Input for channel 1
2D	3	Input	Input for channel 2
3D	4	Input	Input for channel 3
4D	5	Input	Input for channel 4
5D	6	Input	Input for channel 5
6D	7	Input	Input for channel 6
7D	8	Input	Input for channel 7
8D	9	Input	Input for channel 8
GND	10	—	Ground
CLK	11	Input	Clock input for all channels, rising edge triggered
8Q	12	Output	Output for channel 8
7Q	13	Output	Output for channel 7
6Q	14	Output	Output for channel 6
5Q	15	Output	Output for channel 5
4Q	16	Output	Output for channel 4
3Q	17	Output	Output for channel 3
2Q	18	Output	Output for channel 2
1Q	19	Output	Output for channel 1
V$_{CC}$	20	—	Postive supply
Thermal Pad[1]		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1)   WRKS package only.

Product Folder Links: *SN74HCS574-Q1*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
I_{IK}	Input clamp current[2]	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output clamp current[2]	V_O < -0.5 V or V_O > $V_{CC +}$ 0.5 V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
I_{CC}	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1500	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_A	Ambient temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74HCS574-Q1		UNIT
		PW (TSSOP)	WRKS (VQFN)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	83.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	82.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	57.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	14.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	56.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	40.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1	V
				4.5 V	0.9		2.2	
				6 V	1.2		3	
ΔV_T	Hysteresis (V_{T+} - V_{T-})			2 V	0.2		1	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.3	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, I_O = 0		6 V		0.1	2	µA
C_i	Input capacitance			2 V to 6 V			5	pF

6.6 Timing Characteristics

over operating free-air temperature range (unless otherwise noted), C_L = 50 pF

PARAMETER		CONDITION	V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock Frequency		2 V		49	MHz
			4.5 V		120	
			6 V		135	
t_w	Pulse duration	CLK high or low	2 V	12		ns
			4.5 V	6		
			6 V	6		
t_{su}	Setup time	Data before CLK↑	2 V	18		ns
			4.5 V	6		
			6 V	6		
t_h	Hold time, data after CLK↑		2 V	0		ns
			4.5 V	0		
			6 V	0		

6.7 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*. C_L = 50 pF.

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
f_{max}	Max switching frequency			2 V	49			MHz
				4.5 V	120			
				6 V	135			

Product Folder Links: *SN74HCS574-Q1*

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*. C_L = 50 pF.

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Propogation delay	CLK	Any Q	2 V		26	40	ns
				4.5 V		12.2	14	
				6 V		10.3	11	
t_{en}	Enable time	$\overline{OE}$	Any Q	2 V		22.16	28.8	ns
				4.5 V		10.94	14.2	
				6 V		9.23	12.0	
t_{dis}	Disable time	$\overline{OE}$	Any Q	2 V		11.08	14.4	ns
				4.5 V		7.65	9.9	
				6 V		7.01	9.1	
t_t	Transition-time		Any Q	2 V		14.6	19.4	ns
				4.5 V		7.7	9.6	
				6 V		7.4	10.4	

6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load		20		pF

6.9 Typical Characteristics

$T_A = 25°C$
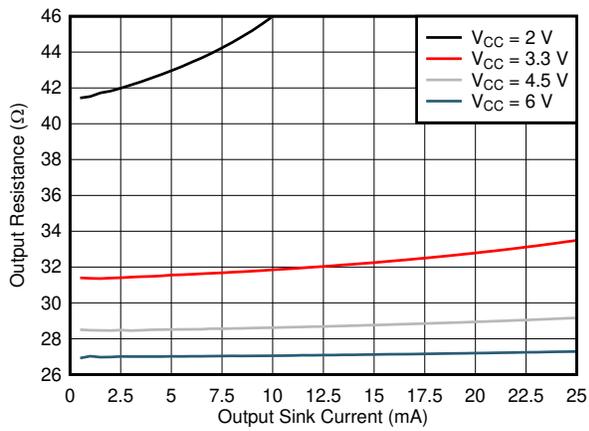
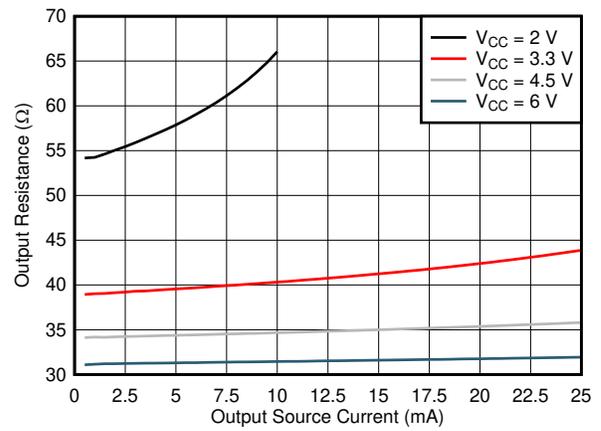**Figure 6-1. Output Driver Resistance in LOW State**

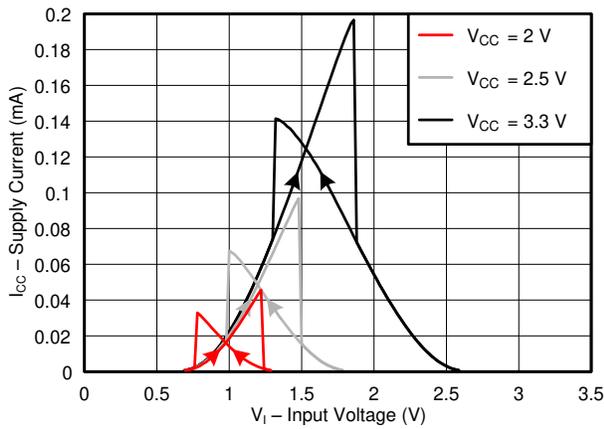**Figure 6-2. Output Driver Resistance in HIGH State**

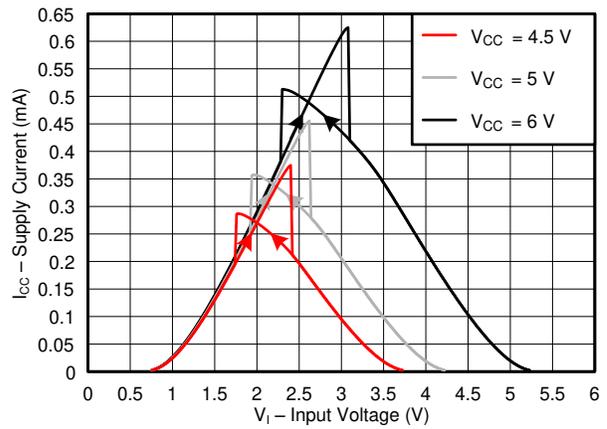**Figure 6-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3-V Supply**

Figure 6-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6-V Supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.
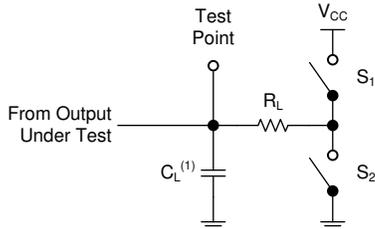
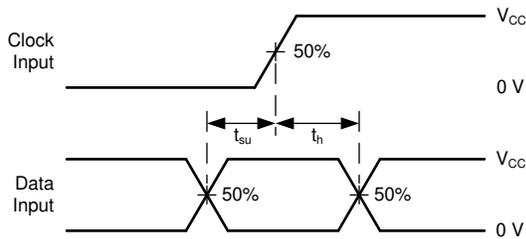(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit for 3-State Outputs
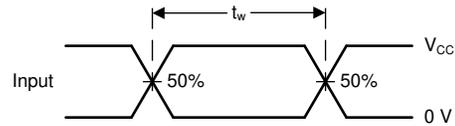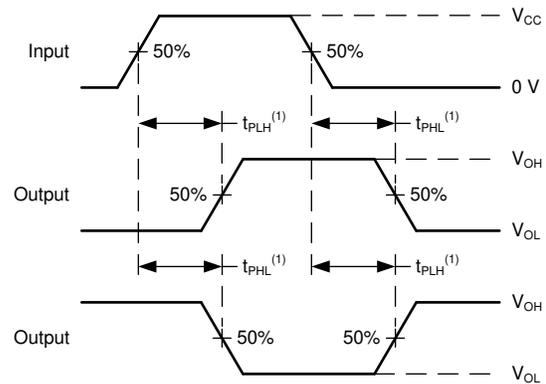

Figure 7-2. Voltage Waveforms, Pulse Duration

Figure 7-3. Voltage Waveforms, Setup and Hold Times

(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 7-4. Voltage Waveforms Propagation Delays
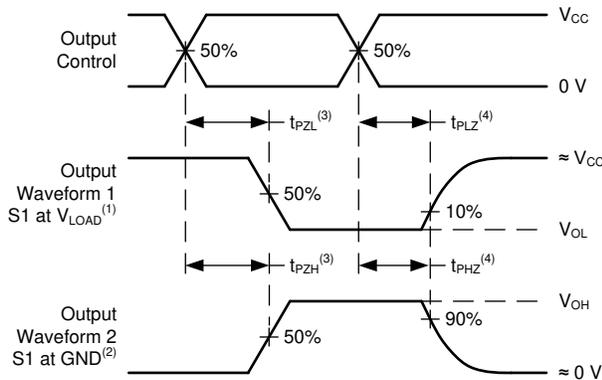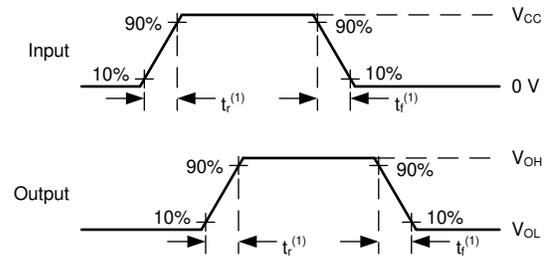

Figure 7-5. Voltage Waveforms Propagation Delays

(1) The greater between t_r and t_f is the same as t_t.

Figure 7-6. Voltage Waveforms, Input and Output Transition Times

Product Folder Links: *SN74HCS574-Q1*

8 Detailed Description

8.1 Overview

The SN74HCS574-Q1 contains eight D-type flip-flops. All inputs include Schmitt-trigger architecture. All channels share a clock (CLK) and output enable ($\overline{OE}$) input.

Data is stored in the flip-flop on the rising edge of the clock.

The output state of all channels is unknown at startup until valid data is clocked into the flip-flops.

When the outputs are enabled ($\overline{OE}$ is low), the outputs are actively driving low or high.

When the outputs are disabled ($\overline{OE}$ is high), the outputs are set into the high-impedance state.

The active low output enable ($\overline{OE}$) does not have any impact on the stored state in the flip-flops.

8.2 Functional Block Diagram
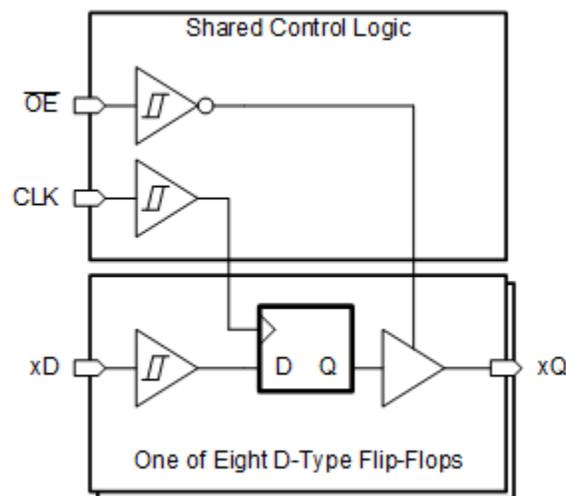
8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-State outputs. The three states that these outputs can be in are driving high, driving low, and high impedance. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10 kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the

Absolute Maximum Ratings table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Electrical Placement of Clamping Diodes for Each Input and Output.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
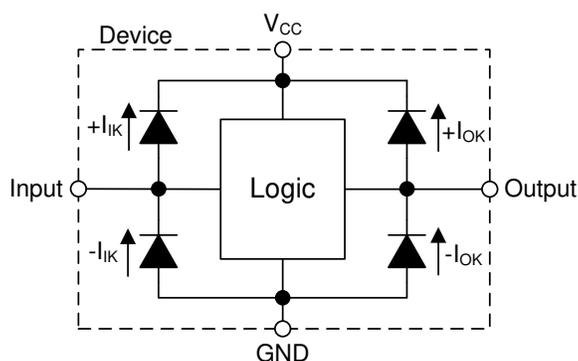

Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.
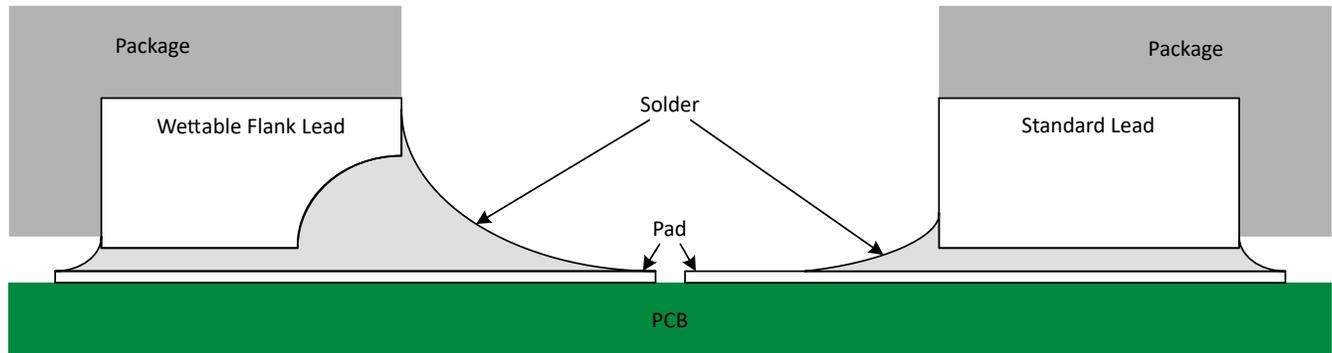

Figure 8-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering which makes QFN packages easier to inspect with automatic optical inspection (AOI). A wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet as shown in Figure 8-2. Please see the mechanical drawing for additional details.

8.4 Device Functional Modes

Table 8-1. Function Table

INPUTS[1]			OUTPUT[2]
$\overline{\text{OE}}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L, H, ↓	X	Q_0 [3]
H	X	X	Z

(1)   L = input low, H = input high, ↑ = input transitioning from low to high, ↓ = input transitioning from high to low, X = don't care
(2)   L = output low, H = output high, Q_0 = previous state, Z = high impedance
(3)   At startup, Q_0 is unknown

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, the SN74HCS574-Q1 is used to control an 8-bit data bus.

All outputs change with the rising edge of the CLK input, which can be used to synchronize signals.

The outputs can set to the high-impedance state using the $\overline{OE}$ to allow other devices to transmit on the data bus.
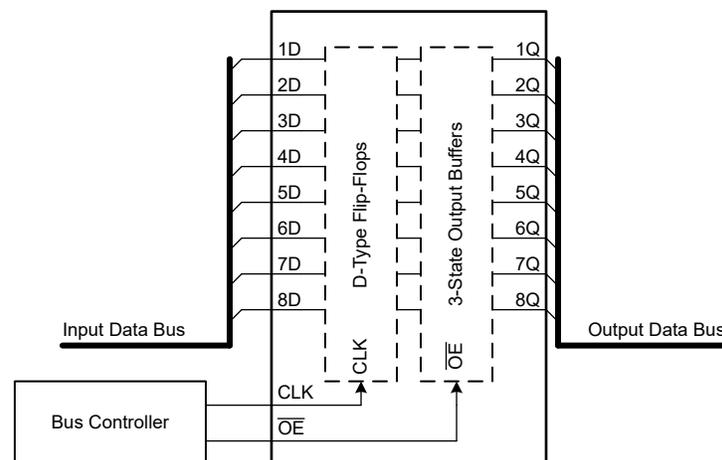
9.2 Typical Application

Figure 9-1.

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS574-Q1 plus the maximum static supply current, I_{CC}, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS574-Q1 plus the maximum supply current, I_{CC}, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS574-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HCS574-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the high state,

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Product Folder Links: *SN74HCS574-Q1*

the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS574-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS574-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.

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2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS574-Q1 to the receiving device(s).

3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.

4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.
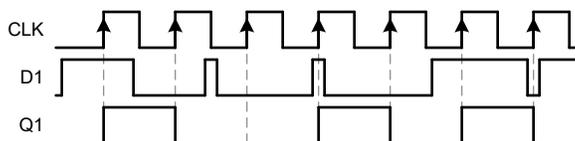
9.2.3 Application Curves

Figure 9-2. Example timing diagram for one channel

Product Folder Links: *SN74HCS574-Q1*

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.
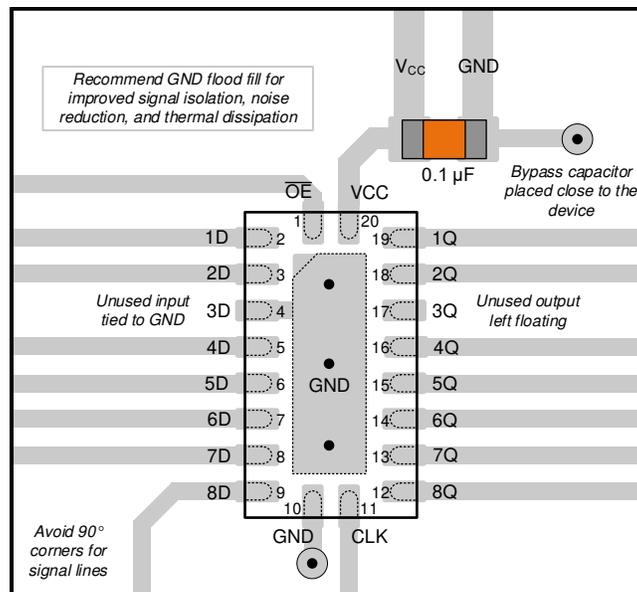
11.2 Layout Example

Figure 11-1. Example layout for the SN74HCS574-Q1 in the WRKS Package

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

* Texas Instruments, *HCMOS Design Considerations* application report (SCLA007)
* Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report (SDYA009)
* Texas Instruments, *Designing With Logic* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS574QPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS574Q
SN74HCS574QPWRQ1.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS574Q
SN74HCS574QWRKSRQ1	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS574Q
SN74HCS574QWRKSRQ1.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS574Q

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74HCS574-Q1 :

● Catalog : SN74HCS574

NOTE: Qualified Version Definitions:

　● Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS574QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCS574QWRKSRQ1	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS574QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCS574QWRKSRQ1	VQFN	RKS	20	3000	210.0	185.0	35.0

RKS 20

2.5 x 4.5, 0.5 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
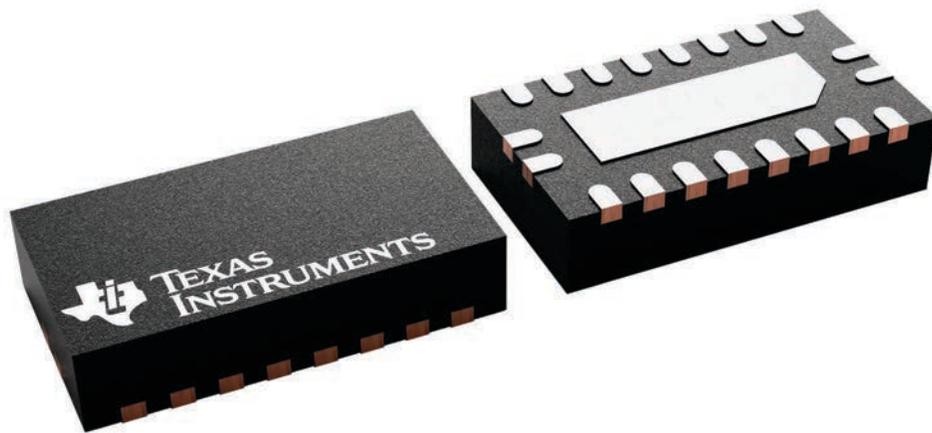
4226872/A
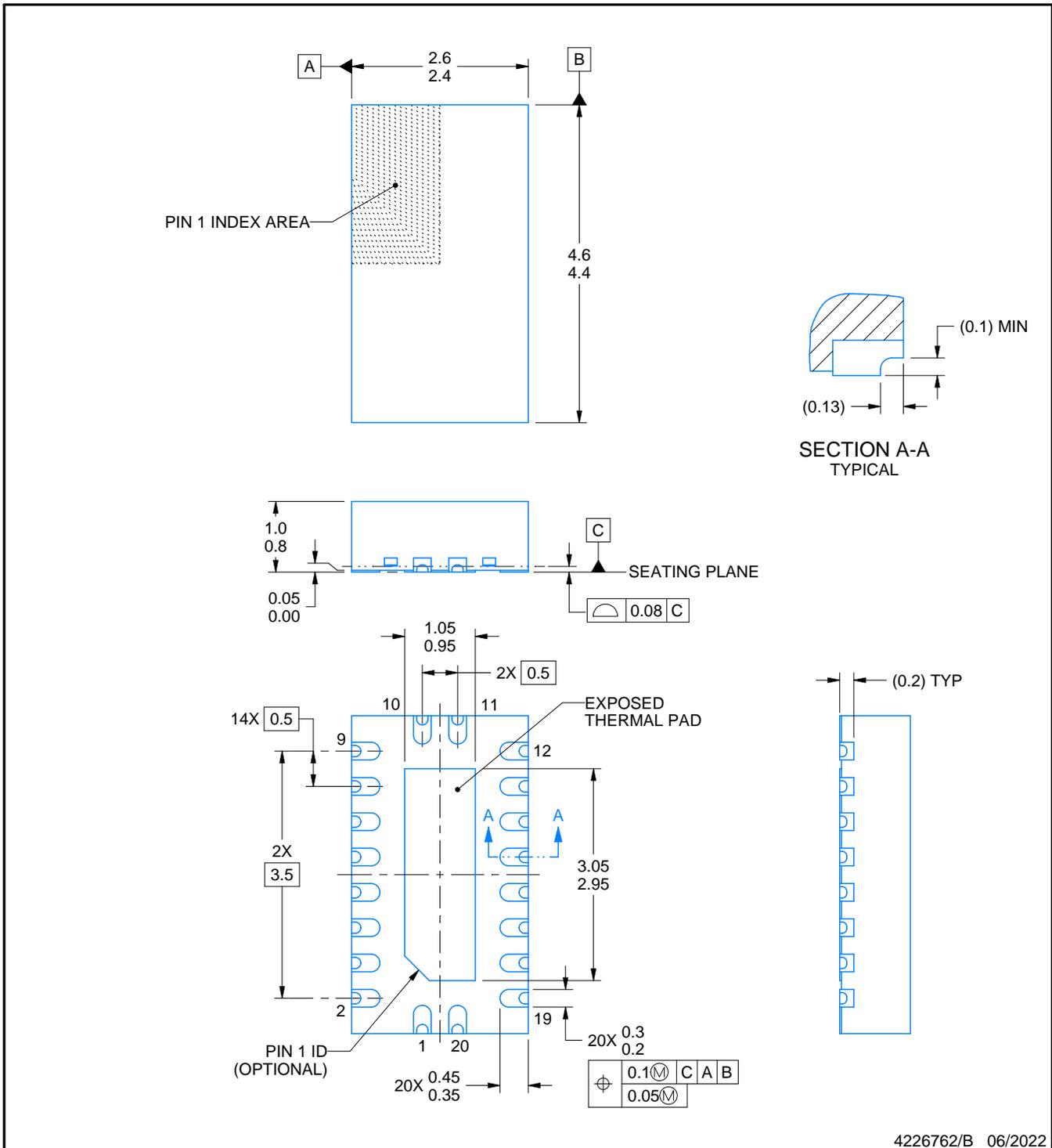
PIN 1 INDEX AREA

A ← 2.6 / 2.4 → B

4.6 / 4.4

(0.1) MIN

(0.13)

SECTION A-A
TYPICAL

1.0 / 0.8

0.05 / 0.00

C

SEATING PLANE

⌒ 0.08 C

1.05 / 0.95

2X 0.5

(0.2) TYP

10   11

14X 0.5

9   12

EXPOSED
THERMAL PAD

A   A

2X 3.5

3.05 / 2.95

2

19

PIN 1 ID
(OPTIONAL)

1   20

20X 0.3 / 0.2

20X 0.45 / 0.35

⌖ 0.1 Ⓜ C A B
0.05 Ⓜ

4226762/B   06/2022
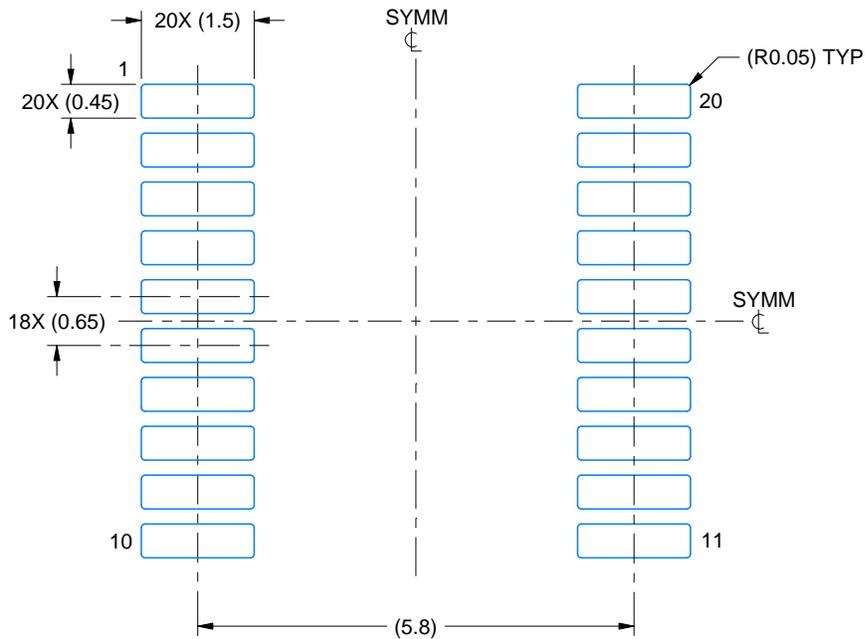
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

(1)

2X (0.5)

1 20

20X (0.6)

2

20X (0.25)

19

(1.25)

(3)

SYMM
℄

2X (3.5)

(4.3)

16X (0.5)

(R0.05) TYP

(∅ 0.2) VIA
TYP

9

12

10 11

SYMM
℄

(2.3)

LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
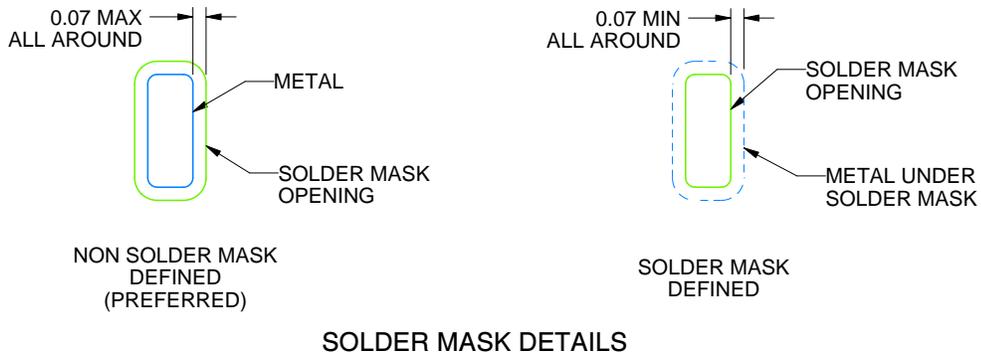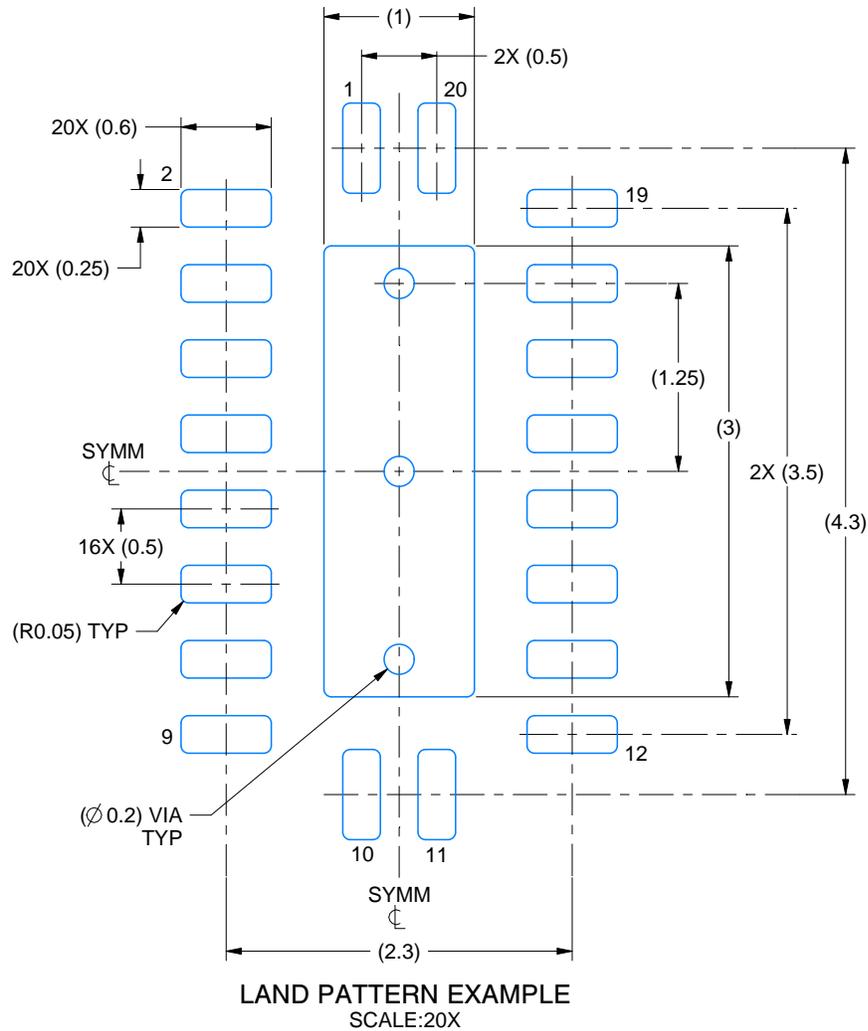
4226762/B   06/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

2X (0.95)

2X (0.5)

1

20

20X (0.6)

2

20X (0.25)

19

16X (0.5)

2X (1.31)

SYMM

2X (3.5)   (4.3)

(0.76)

METAL
TYP

9

12

(R0.05) TYP

10   11

SYMM

(2.3)
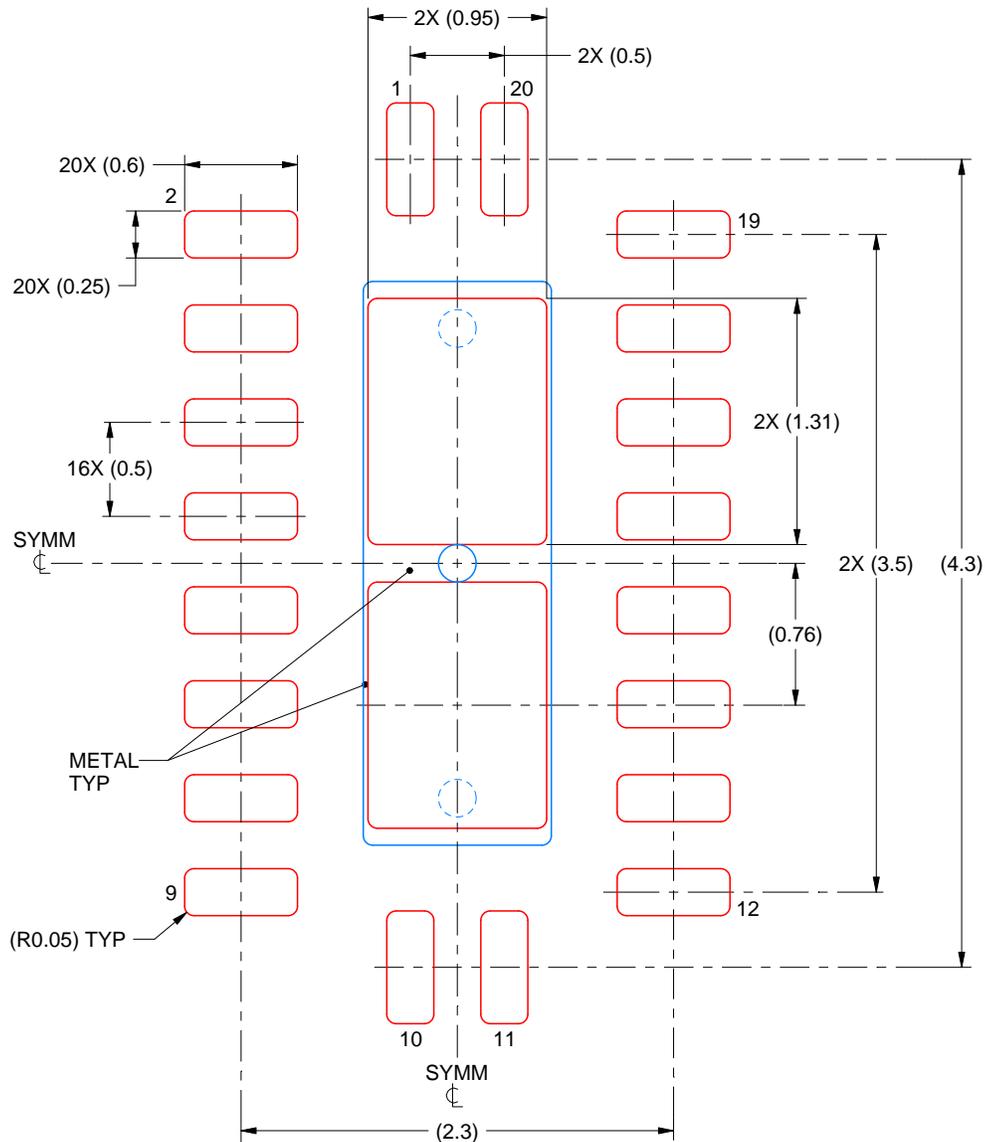
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226762/B   06/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

6.6
6.2 TYP

A

PIN 1 INDEX AREA

18X 0.65

1

20

6.6
6.4
NOTE 3

2X

5.85

10

11

B

4.5
4.3
NOTE 4

20X 0.30
0.19

⊕ 0.1 Ⓜ C A B

C ── SEATING PLANE

◯ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL

4220206/A   02/2017
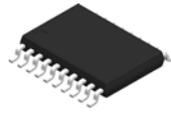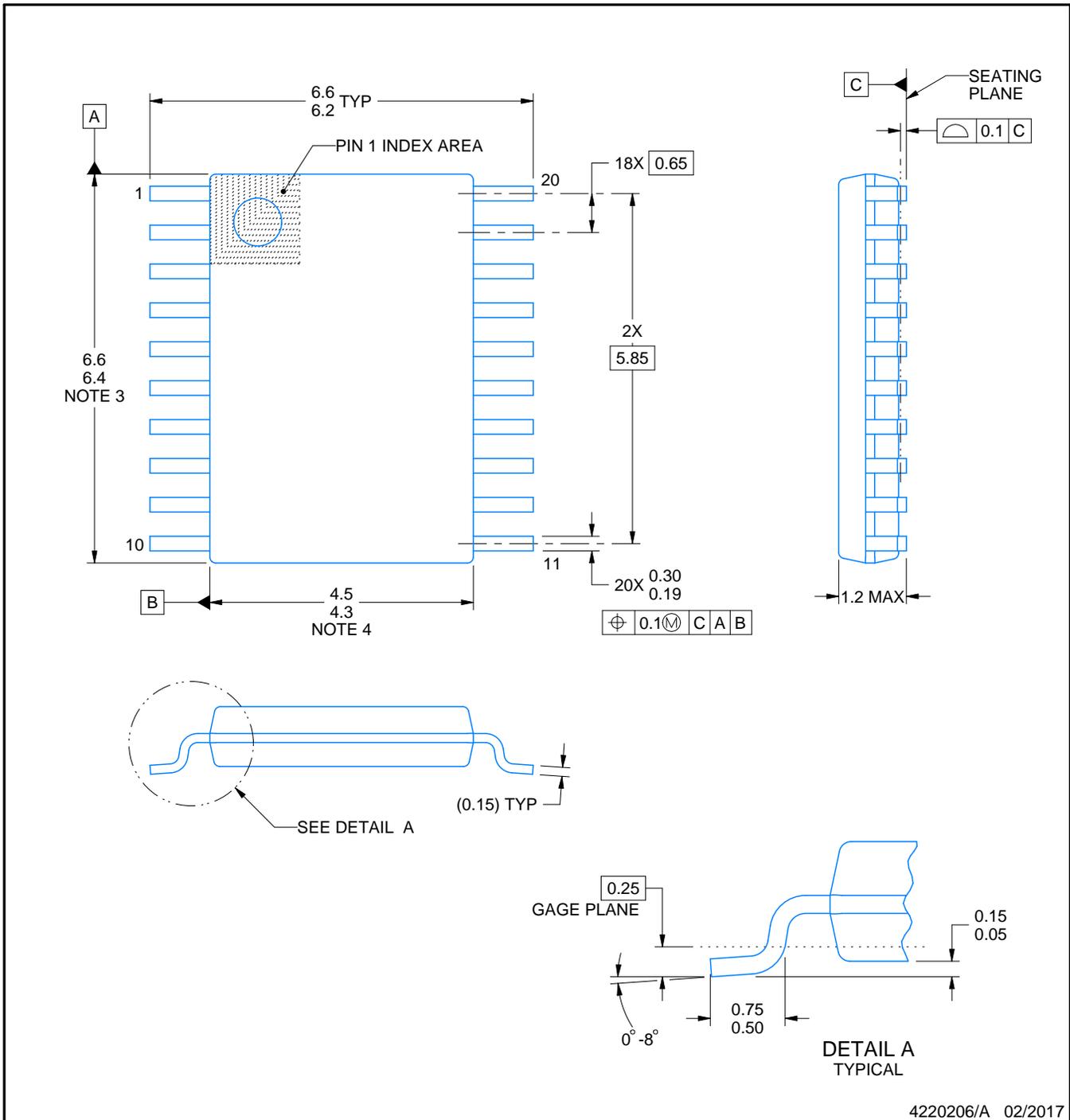
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK OPENING
METAL
EXPOSED METAL
0.05 MAX ALL AROUND

METAL UNDER SOLDER MASK
SOLDER MASK OPENING
EXPOSED METAL
0.05 MIN ALL AROUND
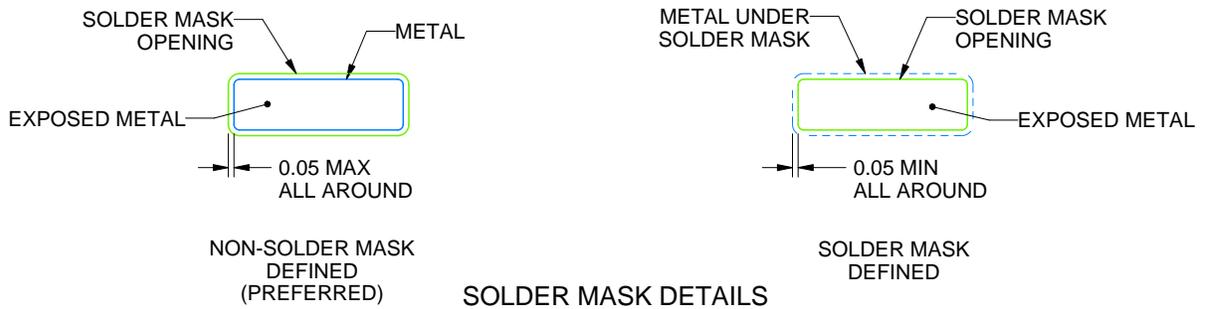
4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)
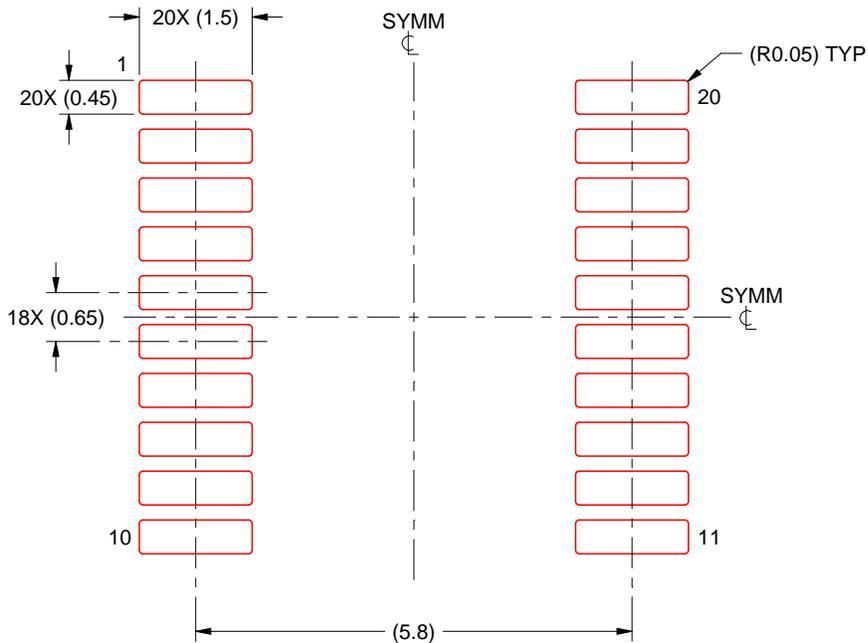
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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