

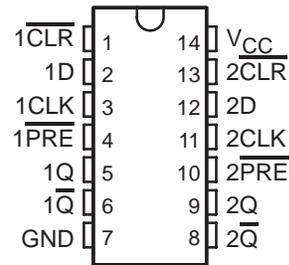
SN74AHCT74Q-Q1

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SGDS008B – MAY 1998 – REVISED APRIL 2008

- Qualified for Automotive Applications
- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

D OR PW PACKAGE
(TOP VIEW)



description

The SN74AHCT74Q is a dual positive-edge-triggered D-type flip-flop.

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

ORDERING INFORMATION†

| T _A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| –40°C to 125°C | SOIC – D | Tape and reel | SN74AHCT74QDRQ1 | AHCT74Q |
| | TSSOP – PW | Tape and reel | SN74AHCT74QPWRQ1 | HB74Q |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|-------------------------|-------------------------|-----|---|----------------|-------------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | D | Q | $\overline{\text{Q}}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H§ | H§ |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q ₀ | $\overline{\text{Q}}_0$ |

§ This configuration is unstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



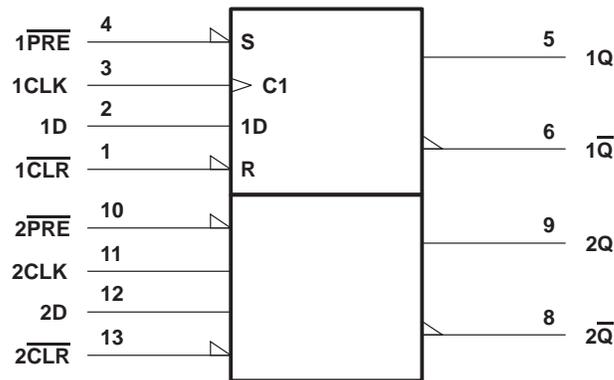
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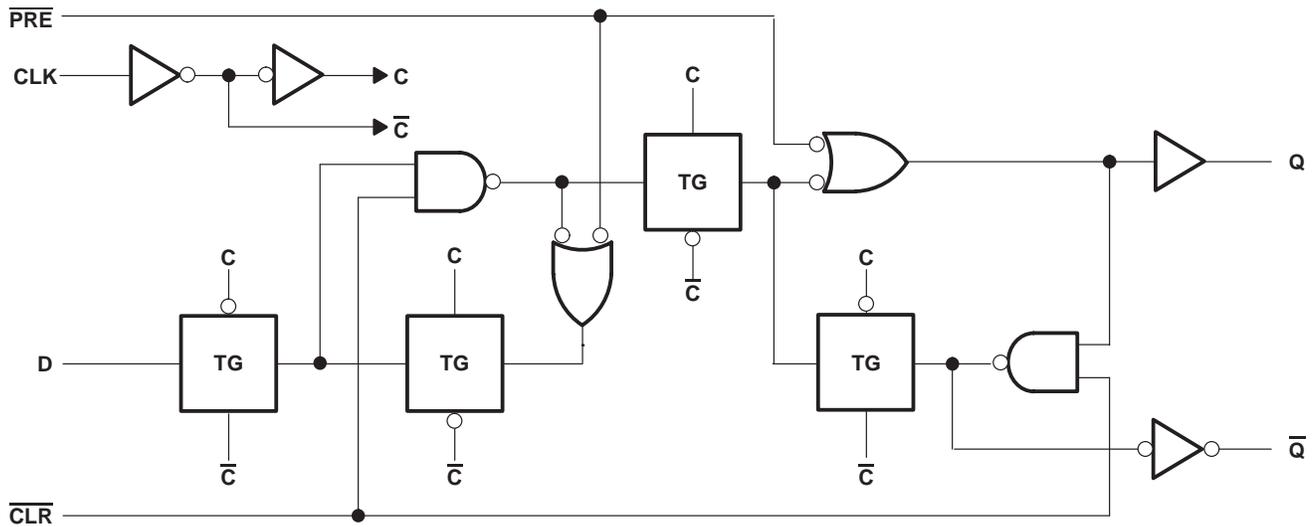
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



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DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | MIN | MAX | UNIT |
|--|-----|----------|------|
| V_{CC} Supply voltage | 4.5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | V |
| V_I Input voltage | 0 | 5.5 | V |
| V_O Output voltage | 0 | V_{CC} | V |
| I_{OH} High-level output current | | -8 | mA |
| I_{OL} Low-level output current | | 8 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | 20 | ns/V |
| T_A Operating free-air temperature | -40 | 125 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|--------------------------|---|--------------|--------------------------|-----|-----------|---------|---------------|------|
| | | | MIN | TYP | MAX | | | |
| V_{OH} | $I_{OH} = -50 \mu\text{A}$ | 4.5 V | 4.4 | 4.5 | | 4.4 | V | |
| | $I_{OH} = -8 \text{ mA}$ | | 3.94 | | | 3.8 | | |
| V_{OL} | $I_{OL} = 50 \mu\text{A}$ | 4.5 V | | | 0.1 | 0.1 | V | |
| | $I_{OL} = 8 \text{ mA}$ | | | | | 0.36 | | 0.44 |
| I_I | $V_I = 5.5 \text{ V}$ or GND | 0 V to 5.5 V | | | ± 0.1 | ± 1 | μA | |
| I_{CC} | $V_I = V_{CC}$ or GND, $I_O = 0$ | 5.5 V | | | 2 | 20 | μA | |
| ΔI_{CC}^\ddagger | One input at 3.4 V, Other inputs at V_{CC} or GND | 5.5 V | | | 1.35 | 1.5 | mA | |
| C_i | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | pF | |

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC} .



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DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER | | T _A = 25°C | | MIN | MAX | UNIT |
|-----------------|----------------------------|-----------------------|-----|-----|-----|------|
| | | MIN | MAX | | | |
| t _w | Pulse duration | PRE or CLR low | 5 | 5 | | ns |
| | | CLK | 5 | 5 | | |
| t _{su} | Setup time before CLK↑ | Data | 5 | 5 | | ns |
| | | PRE or CLR inactive | 3.5 | 3.5 | | |
| t _h | Hold time, data after CLK↑ | | 0 | 0 | | ns |

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | MIN | MAX | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|------|-----|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| f _{max} | | | C _L = 15 pF | 100 | 160 | | 80 | | MHz |
| | | | C _L = 50 pF | 80 | 140 | | 65 | | |
| t _{PLH} | PRE or CLR | Q or Q̄ | C _L = 15 pF | 7.6 | 10.4 | | 1 | 12 | ns |
| t _{PHL} | | | | 7.6 | 10.4 | | 1 | 12 | |
| t _{PLH} | CLK | Q or Q̄ | C _L = 15 pF | 5.8 | 7.8 | | 1 | 9 | ns |
| t _{PHL} | | | | 5.8 | 7.8 | | 1 | 9 | |
| t _{PLH} | PRE or CLR | Q or Q̄ | C _L = 50 pF | 8.1 | 11.4 | | 1 | 13 | ns |
| t _{PHL} | | | | 8.1 | 11.4 | | 1 | 13 | |
| t _{PLH} | CLK | Q or Q̄ | C _L = 50 pF | 6.3 | 8.8 | | 1 | 10 | ns |
| t _{PHL} | | | | 6.3 | 8.8 | | 1 | 10 | |

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

| PARAMETER | | MIN | MAX | UNIT |
|--------------------|---|-----|------|------|
| V _{OL(P)} | Quiet output, maximum dynamic V _{OL} | | 0.8 | V |
| V _{OL(V)} | Quiet output, minimum dynamic V _{OL} | | -0.8 | V |
| V _{OH(V)} | Quiet output, minimum dynamic V _{OH} | 4 | | V |
| V _{IH(D)} | High-level dynamic input voltage | 2 | | V |
| V _{IL(D)} | Low-level dynamic input voltage | | 0.8 | V |

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

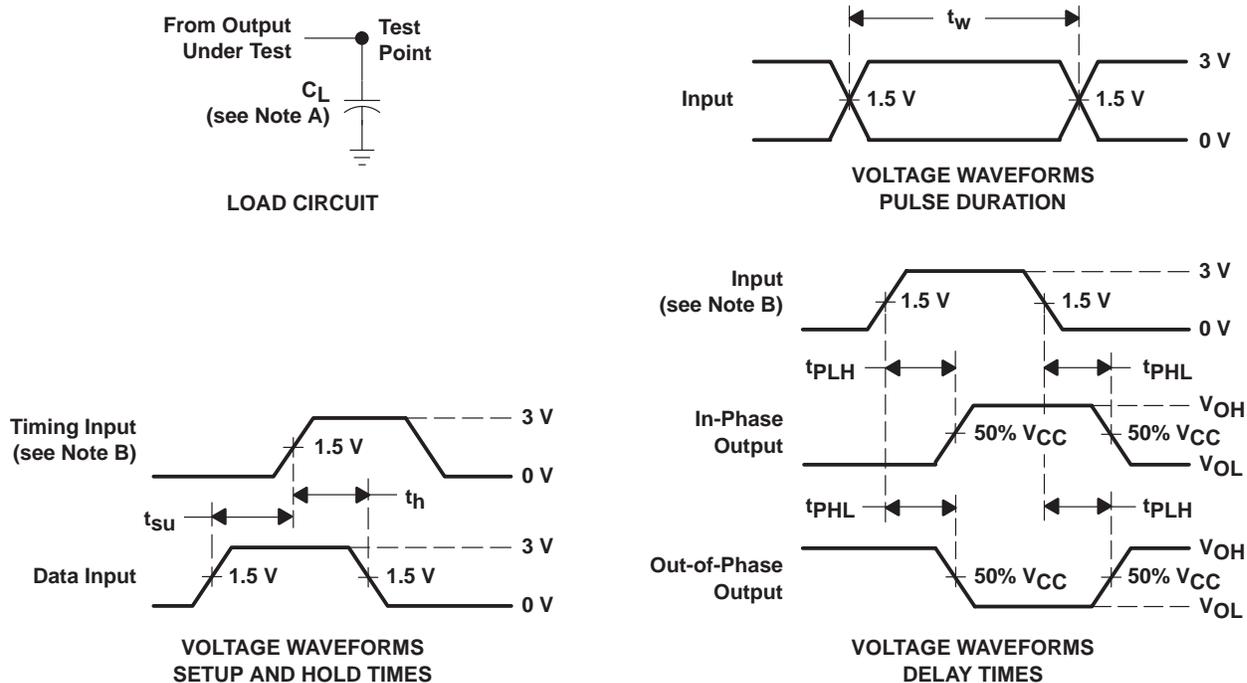
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------------|-------------------------------|--------------------|-----|------|
| C _{pd} | Power dissipation capacitance | No load, f = 1 MHz | 32 | pF |



SN74AHCT74Q-Q1 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74AHCT74QDRG4Q1 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT74Q |
| SN74AHCT74QDRG4Q1.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT74Q |
| SN74AHCT74QDRQ1 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT74Q |
| SN74AHCT74QDRQ1.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT74Q |
| SN74AHCT74QPWRG4Q1 | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB74Q |
| SN74AHCT74QPWRG4Q1.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB74Q |
| SN74AHCT74QPWRQ1 | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | HB74Q |
| SN74AHCT74QPWRQ1.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | HB74Q |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

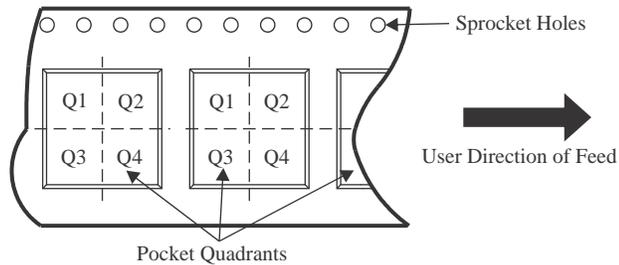
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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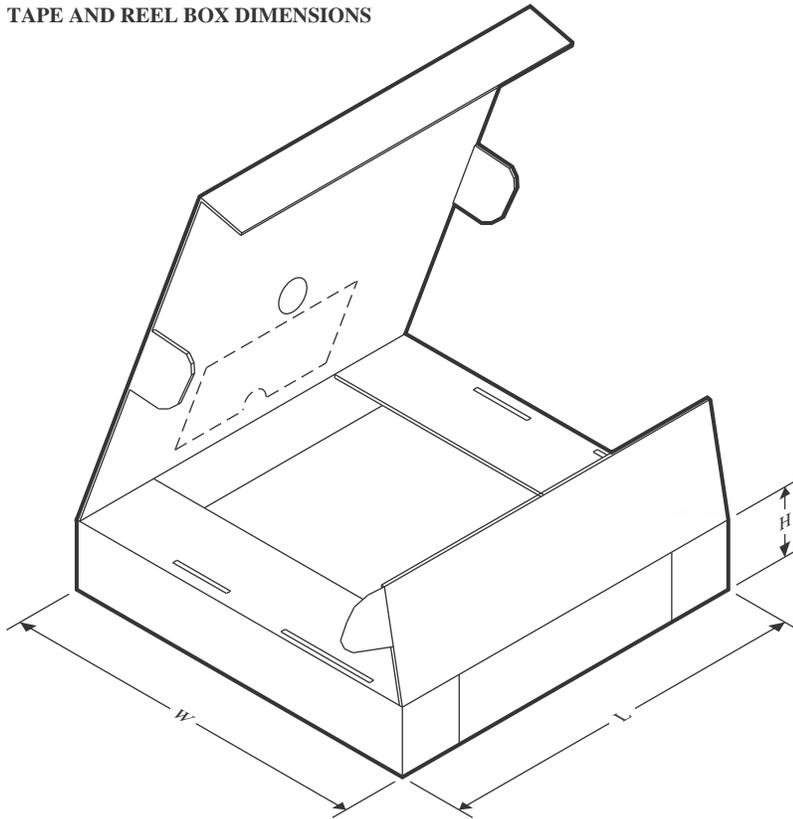
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHCT74QPWRG4Q1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT74QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHCT74QPWRG4Q1 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT74QPWRQ1 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

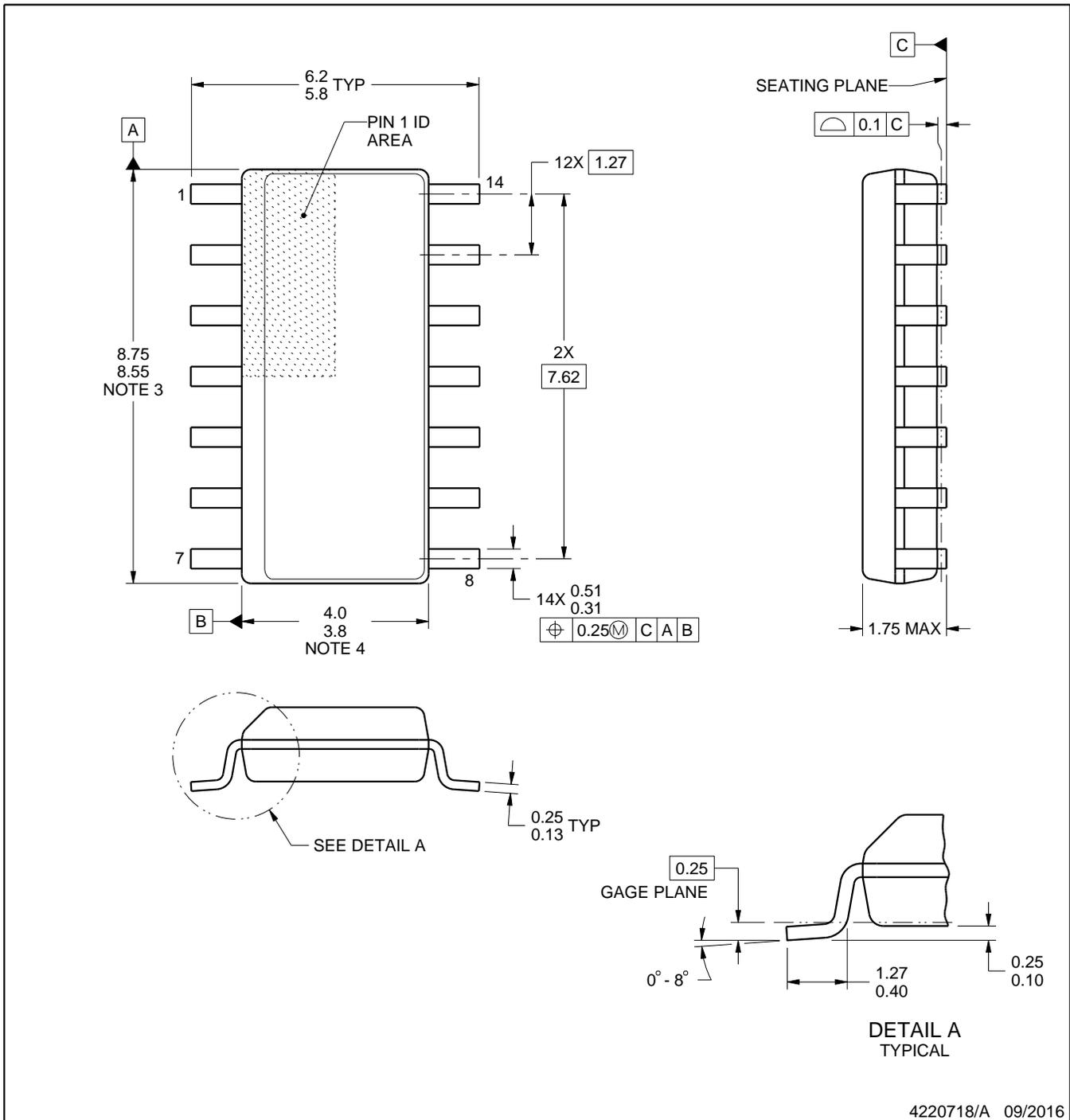
D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

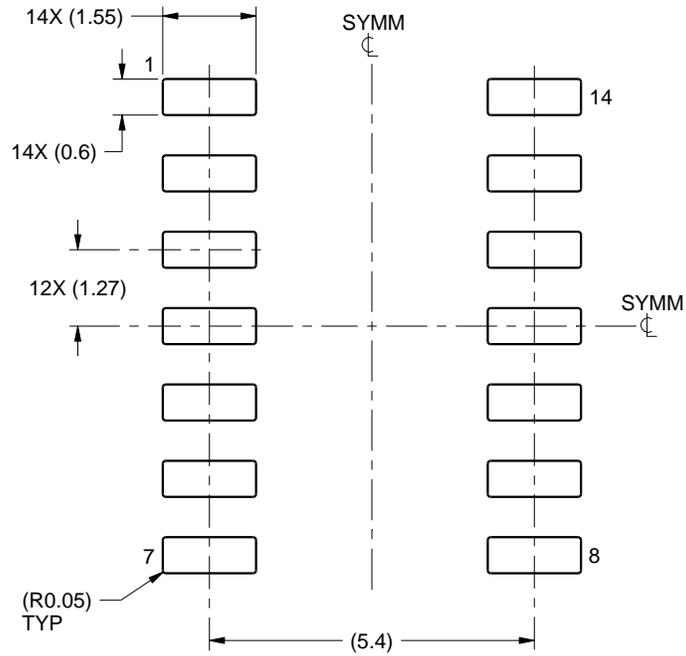
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

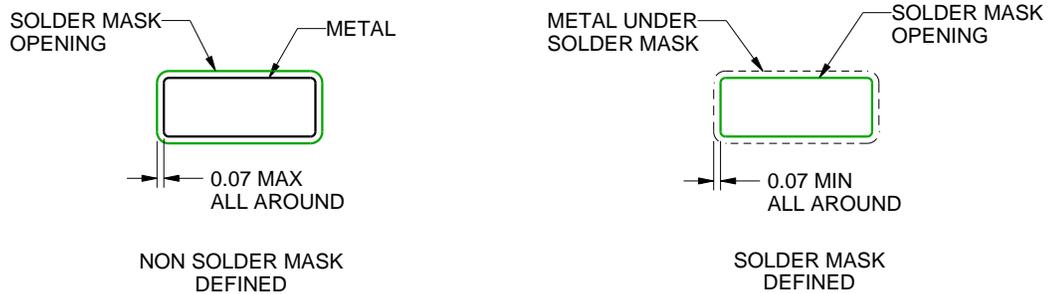
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

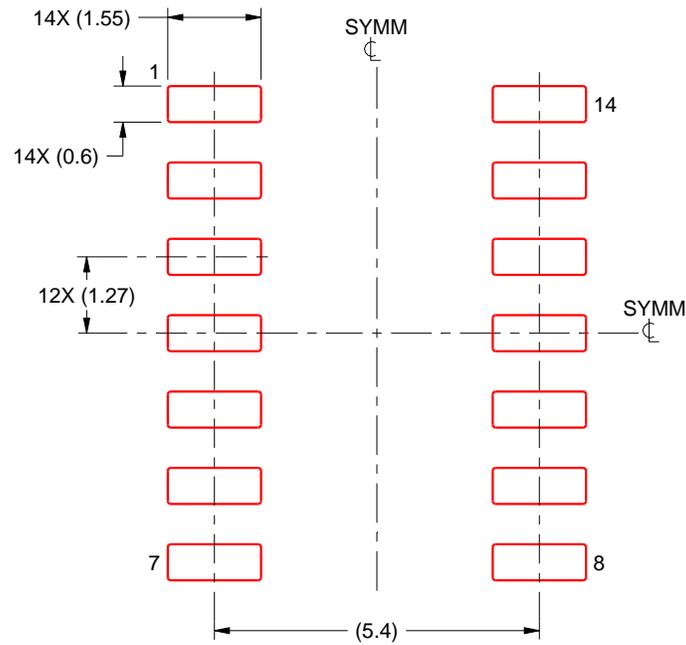
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

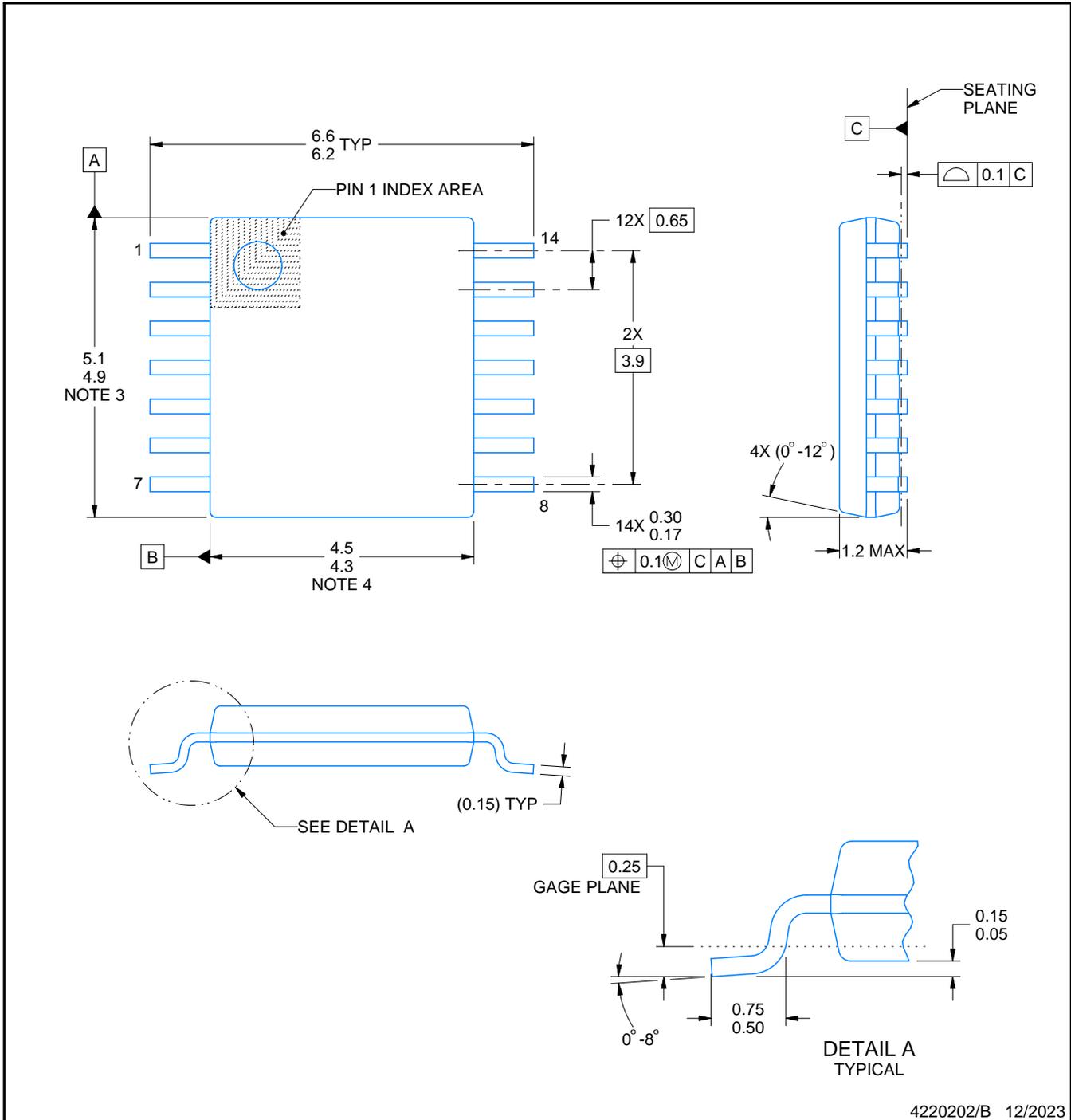
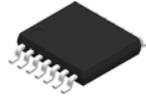


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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NOTES:

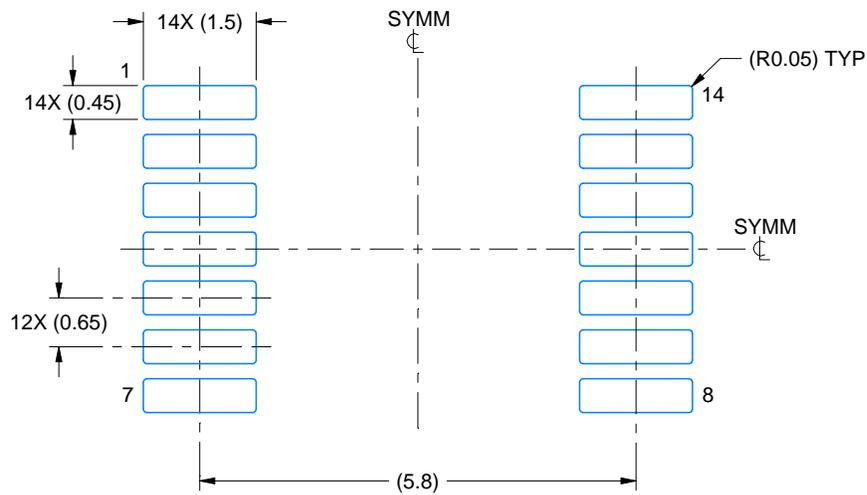
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

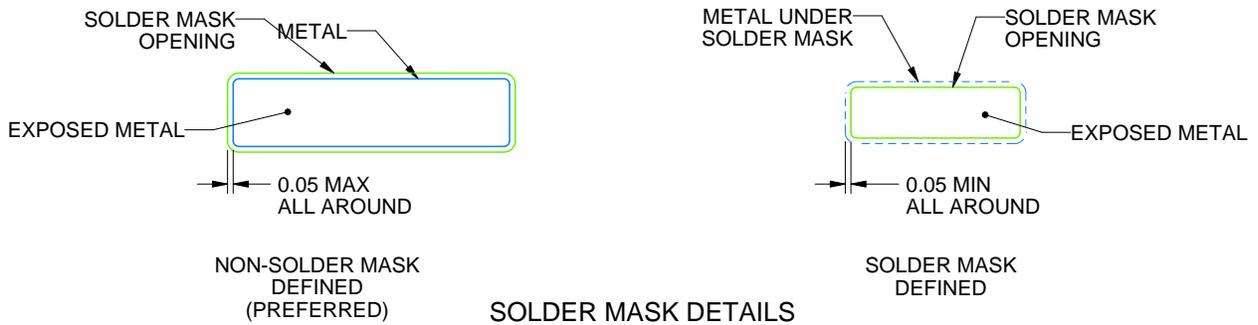
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

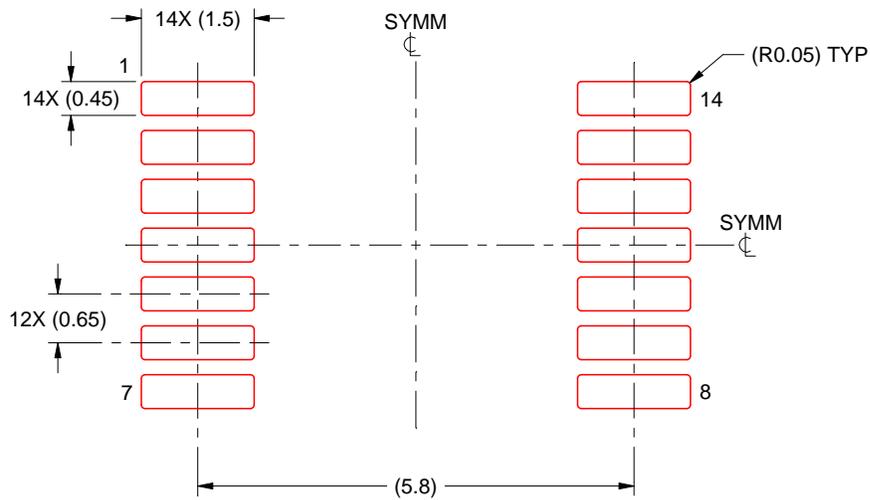
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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